

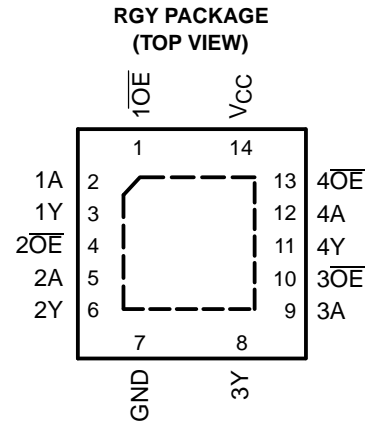


**THE DATASHEET OF  
SN74AUC125RGYRG4**



## FEATURES

- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 2.1 ns at 1.8 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1500-V Charged-Device Model (C101)



## DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 0.8-V to 2.7-V  $V_{CC}$  operation, but is designed specifically for 1.6-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC125 contains four independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AUC125RGYR	MS125

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

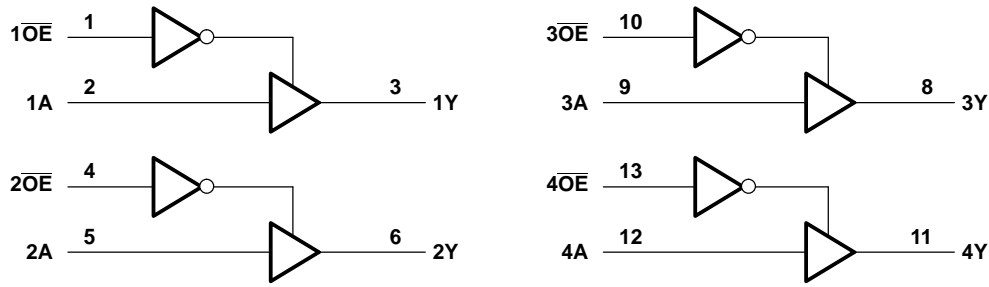


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**SN74AUC125**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**

SCES508A–NOVEMBER 2003–REVISED MARCH 2005

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Output voltage range <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_O$	Continuous output current			±20 mA
	Continuous current through $V_{CC}$ or GND			±100 mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>			47 °C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-5.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	0.8	2.7	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8\text{ V}$	$V_{CC}$	V	
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V	
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
$V_I$	Input voltage	0	3.6	V	
$V_O$	Output voltage	Active state	0	$V_{CC}$	V
		3-state	0	3.6	
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$	–0.7	mA	
		$V_{CC} = 1.1\text{ V}$	–3		
		$V_{CC} = 1.4\text{ V}$	–5		
		$V_{CC} = 1.65\text{ V}$	–8		
		$V_{CC} = 2.3\text{ V}$	–9		
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7	mA	
		$V_{CC} = 1.1\text{ V}$	3		
		$V_{CC} = 1.4\text{ V}$	5		
		$V_{CC} = 1.65\text{ V}$	8		
		$V_{CC} = 2.3\text{ V}$	9		
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V	
$T_A$	Operating free-air temperature	–40	85	°C	

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74AUC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCES508A–NOVEMBER 2003–REVISED MARCH 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -0.7 mA	0.8 V	0.55			
	I <sub>OH</sub> = -3 mA	1.1 V	0.8			
	I <sub>OH</sub> = -5 mA	1.4 V	1			
	I <sub>OH</sub> = -8 mA	1.65 V	1.2			
	I <sub>OH</sub> = -9 mA	2.3 V	1.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V	0.2			V
	I <sub>OL</sub> = 0.7 mA	0.8 V	0.25			
	I <sub>OL</sub> = 3 mA	1.1 V	0.3			
	I <sub>OL</sub> = 5 mA	1.4 V	0.4			
	I <sub>OL</sub> = 8 mA	1.65 V	0.45			
	I <sub>OL</sub> = 9 mA	2.3 V	0.6			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V	±5			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0	±10			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	2.7 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V	10			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V	2.5			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V	5			pF

(1) All typical values are at T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V		V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
t <sub>pd</sub>	A	Y	5.8	0.7	3.7	0.6	2.6	0.5	1	2.1	0.5	1.3	ns	
t <sub>en</sub>	$\overline{OE}$	Y	7.5	0.9	4.1	0.7	2.9	0.6	1	2.2	0.6	1.4	ns	
t <sub>dis</sub>	$\overline{OE}$	Y	6.4	1.6	5.1	1.5	3.6	1.4	2.4	3.5	1	2.6	ns	

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF (unless otherwise noted) (see Figure 1)

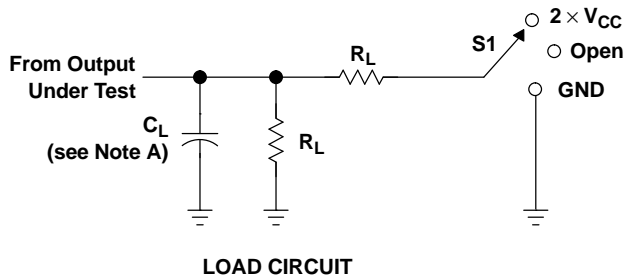
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.5	1.8	2.6	0.5	2.1	ns
t <sub>en</sub>	$\overline{OE}$	Y	0.6	1.6	2.8	0.6	2.3	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1.2	2.4	3.4	0.8	2.3	ns

### Operating Characteristics

$T_A = 25^\circ\text{C}$

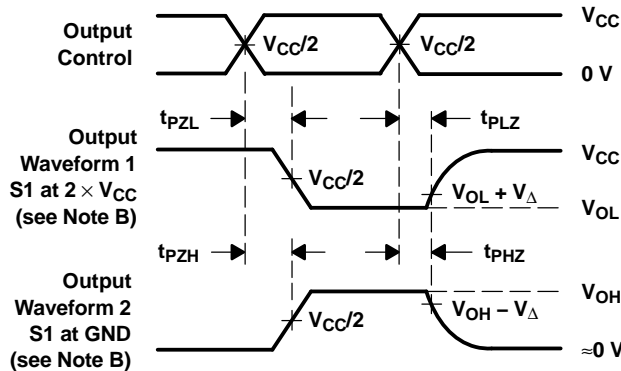
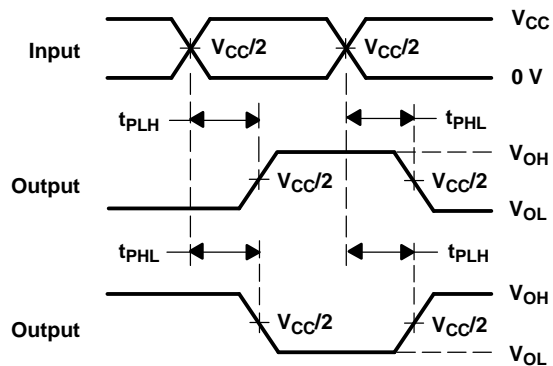
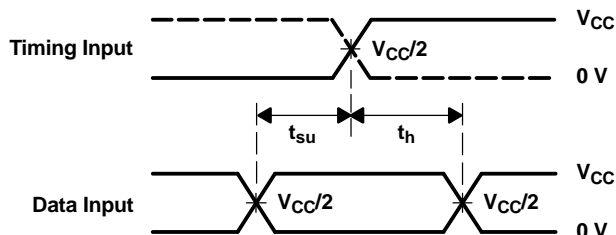
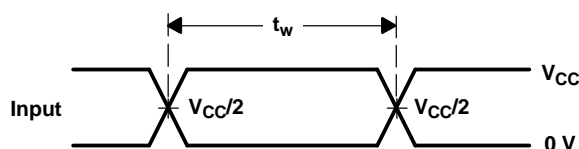
PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	Outputs enabled f = 10 MHz	15	15	15	16	17	pF
	Outputs disabled		2	2	2	3	4	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUC125RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MS125	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

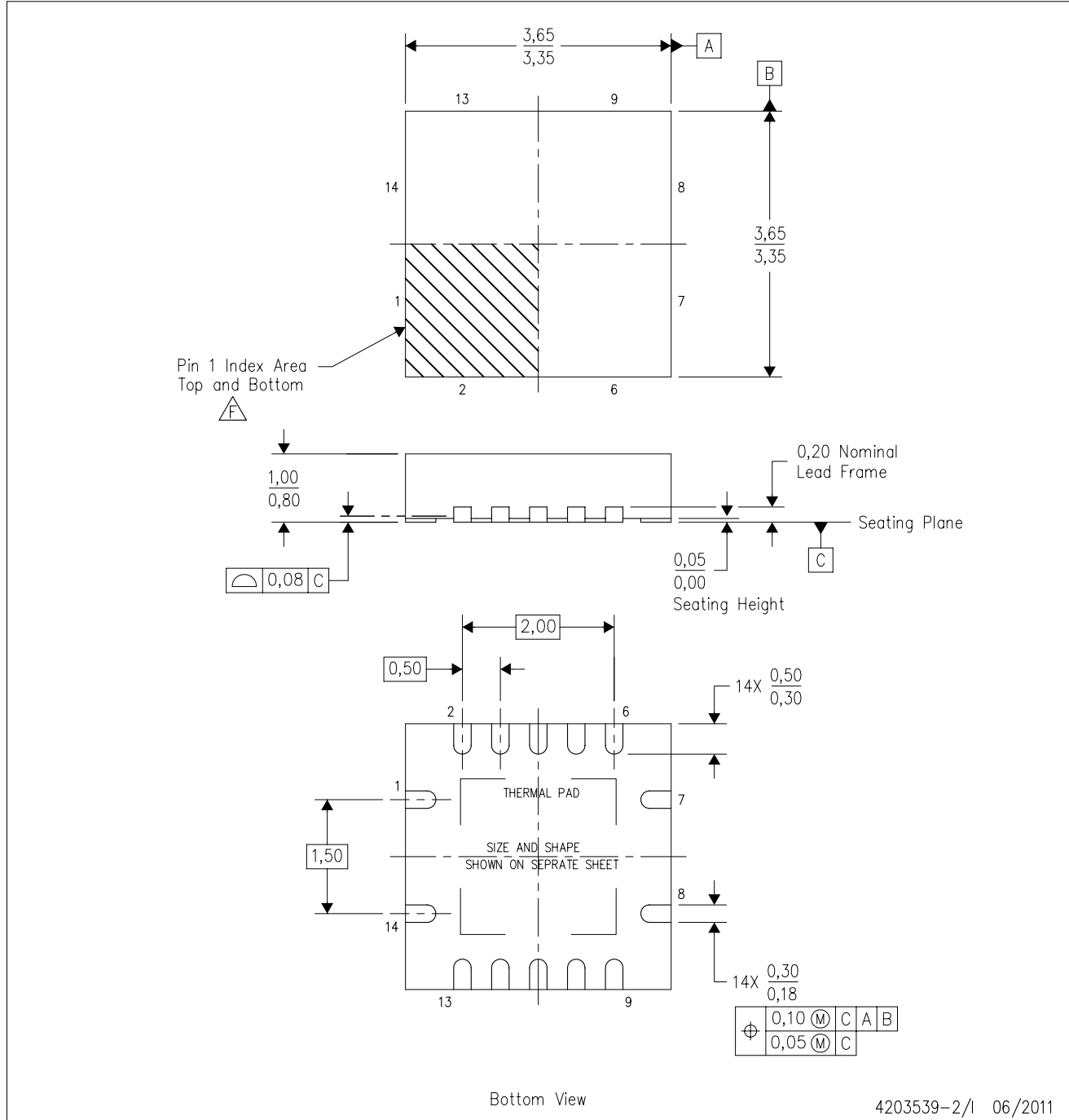
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC125RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

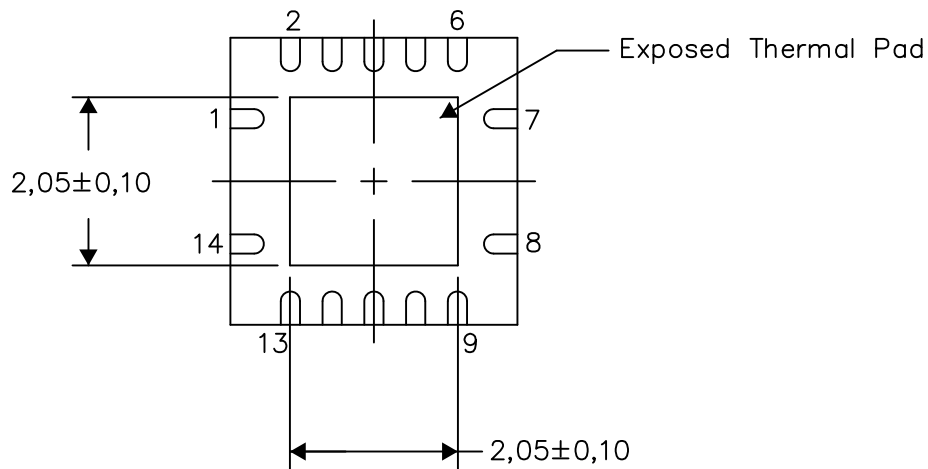
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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