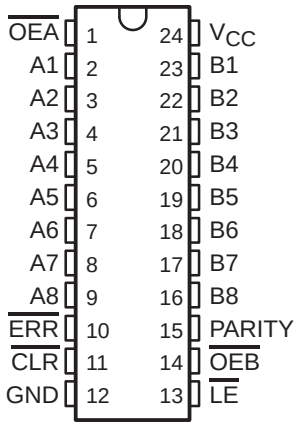
THE DATASHEET OF

SN74ALS29854DWRG4

- **Functionally Similar to AMD's AM29854**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Outputs**
- **Latch for Storing the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74ALS29854 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$, $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector $\overline{ERR}$ flag. $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{LE}$) and clear ($\overline{CLR}$) control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

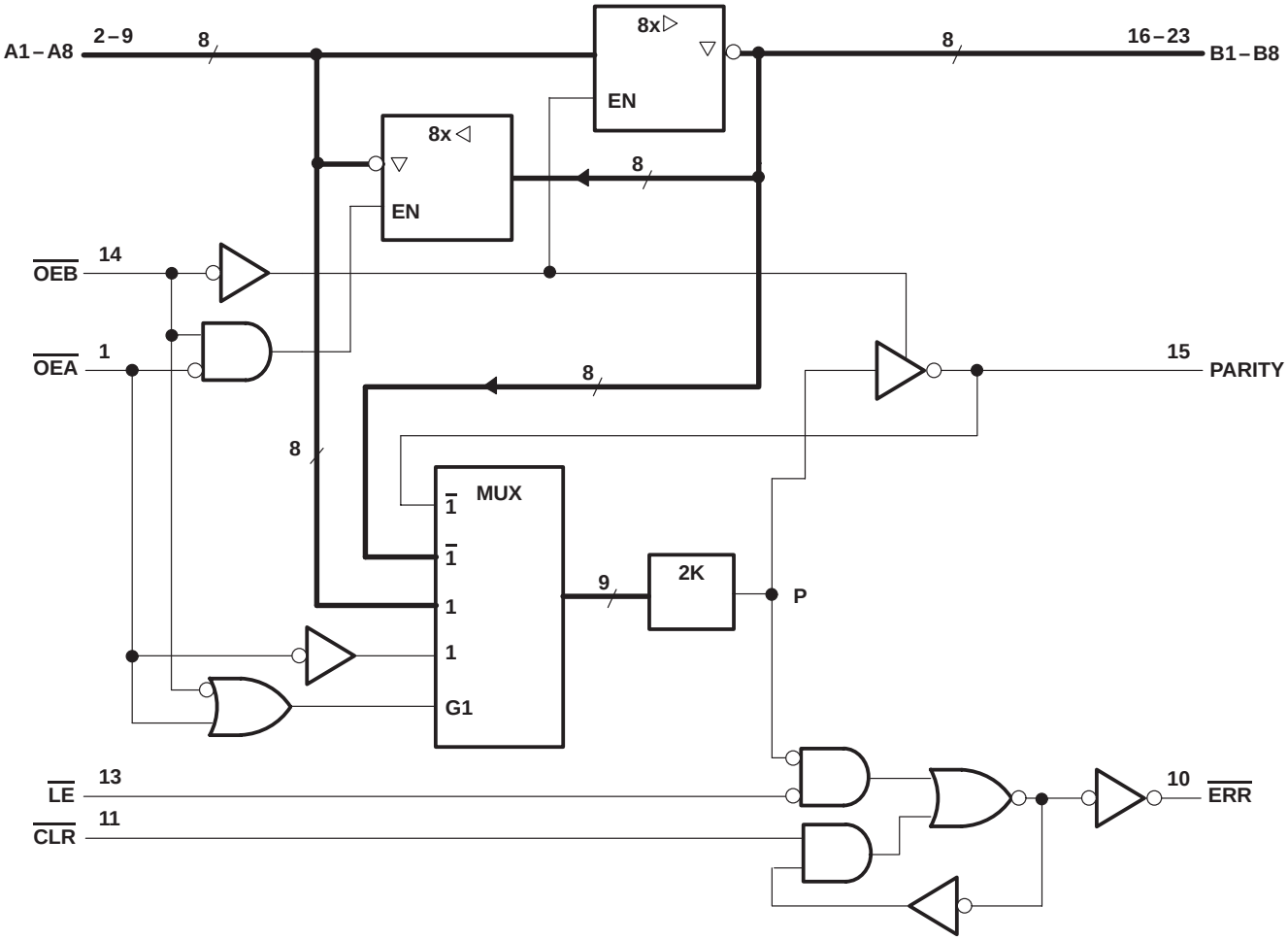
The SN74ALS29854 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

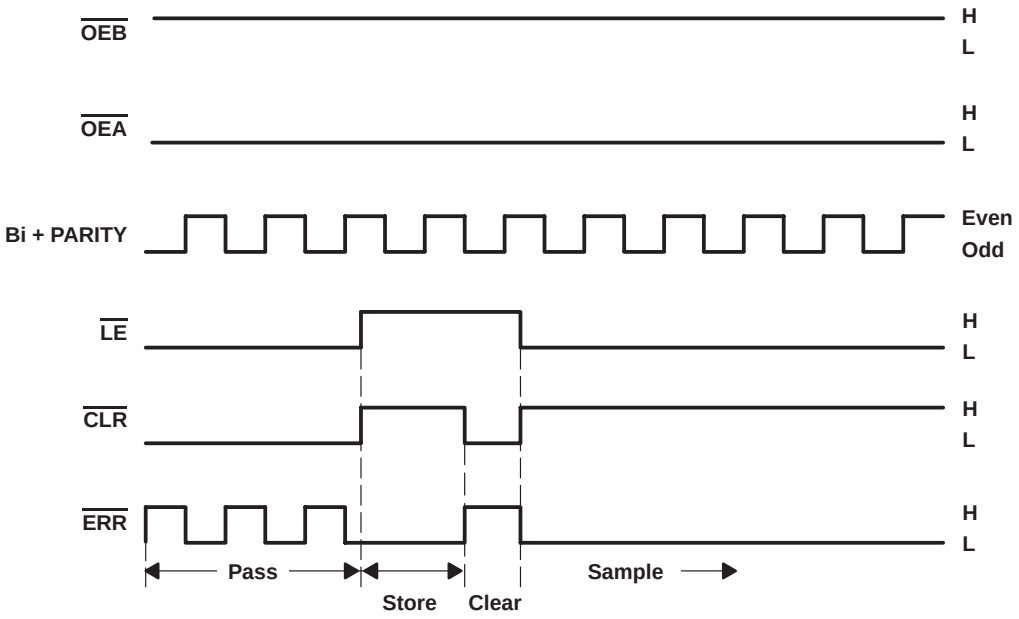
INPUTS						OUTPUT AND I/O				OPERATION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai $\sum$ of Hs	Bi† $\sum$ of Ls	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	X	L	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$, when enabled, shows inverted parity of the A bus.

logic diagram (positive logic)



error-flag waveforms



ERROR-FLAG FUNCTIONS

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT P	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L H	X	L H	Pass
L	H	L X H	X L H	L L H	Sample
H	L	X	X	H	Clear
H	H	X	L H	L H	Store

† $\overline{ERR}_{n-1}$ represents the state of $\overline{ERR}$ before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled I/O port . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$				5.5	V
I_{OH}	High-level output current				–24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{LE}$ high	10			ns
		$\overline{LE}$ low	10			
		$\overline{CLR}$ low	10			
t_{su}	Setup time before $\overline{LE}\downarrow$	Bi and PARITY	10			ns
		$\overline{CLR}$ high	15			
t_h	Hold time, Bi and PARITY after $\overline{LE}\downarrow$		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	All I/Os except $\overline{ERR}$	V_{CC} = 4.75 V	I_{OH} = –15 mA	2.4			V
			I_{OH} = –24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.75 V,	V_{OH} = 5.5 V			0.1	mA
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}‡	Data	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.2	mA
	Control					–0.75	
I_O§		V_{CC} = 5.25 V,	V_O = 0	–75		–250	mA
I_{CC}		V_{CC} = 5.25 V,	All outputs open		70	100	mA

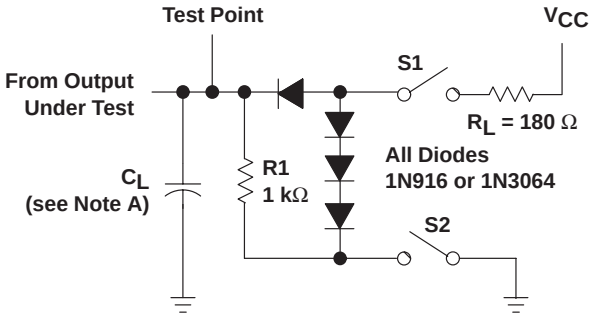
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4.75 V to 5.25 V, T_A = MIN to MAX†		UNIT
				MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 50 pF		8	ns
t_{PHL}					8	
t_{PLH}	A or B	B or A	C_L = 300 pF		13	ns
t_{PHL}					13	
t_{PLH}	A	PARITY	C_L = 50 pF		15	ns
t_{PHL}					18	
t_{PLH}	A	PARITY	C_L = 300 pF		22	ns
t_{PHL}					22	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		17	ns
t_{PZL}					17	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 300 pF		23	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 5 pF		8	ns
t_{PLZ}					8	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	C_L = 50 pF		15	ns
t_{PLZ}					8	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	C_L = 50 pF		12	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	C_L = 50 pF		12	ns
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 50 pF		17	ns
t_{PHL}					19	
t_{PLH}	$\overline{OEA}$	PARITY	C_L = 300 pF		22	ns
t_{PHL}					25	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	C_L = 50 pF		20	ns
t_{PHL}					20	

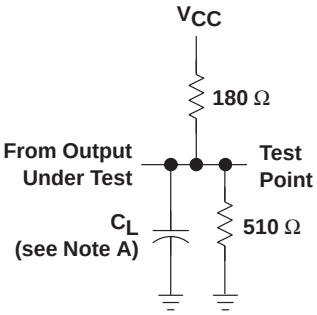
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



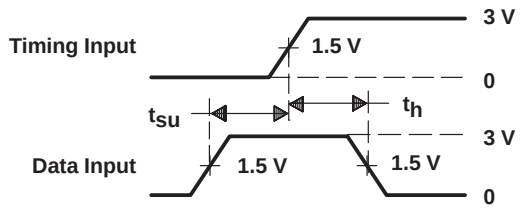
SWITCH POSITION TABLE

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

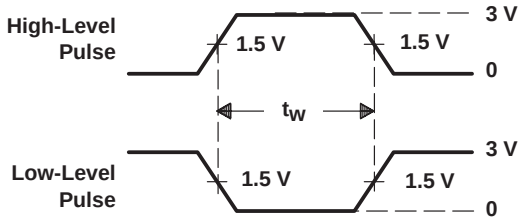


LOAD CIRCUIT 1
ALL OUTPUTS EXCEPT FOR ERROR FLAG

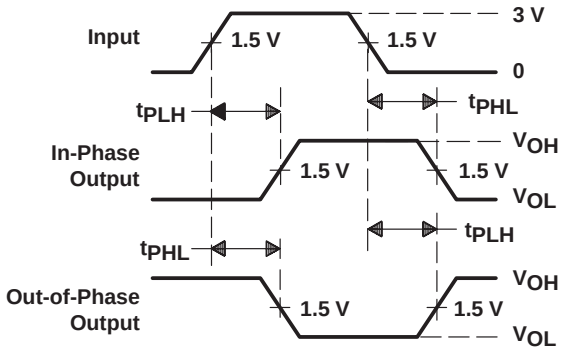
LOAD CIRCUIT 2
ERROR-FLAG OUTPUT



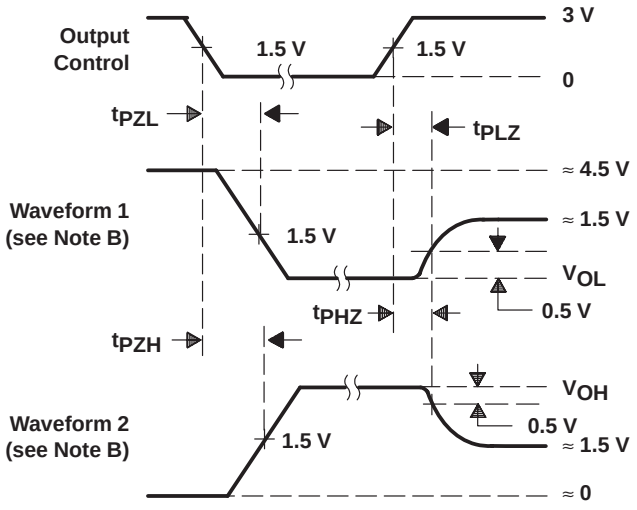
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74ALS29854DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29854NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS29854NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74ALS29854NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

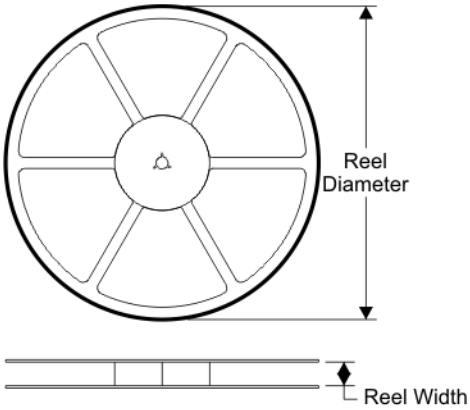
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

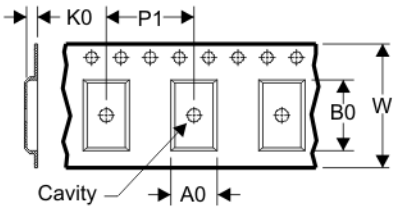
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

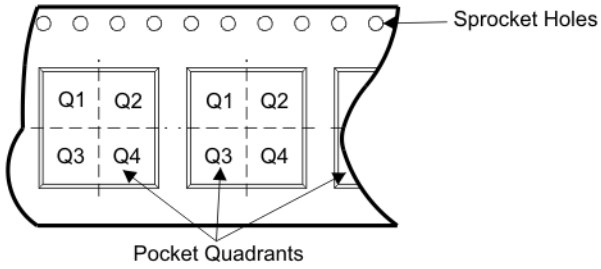


TAPE DIMENSIONS



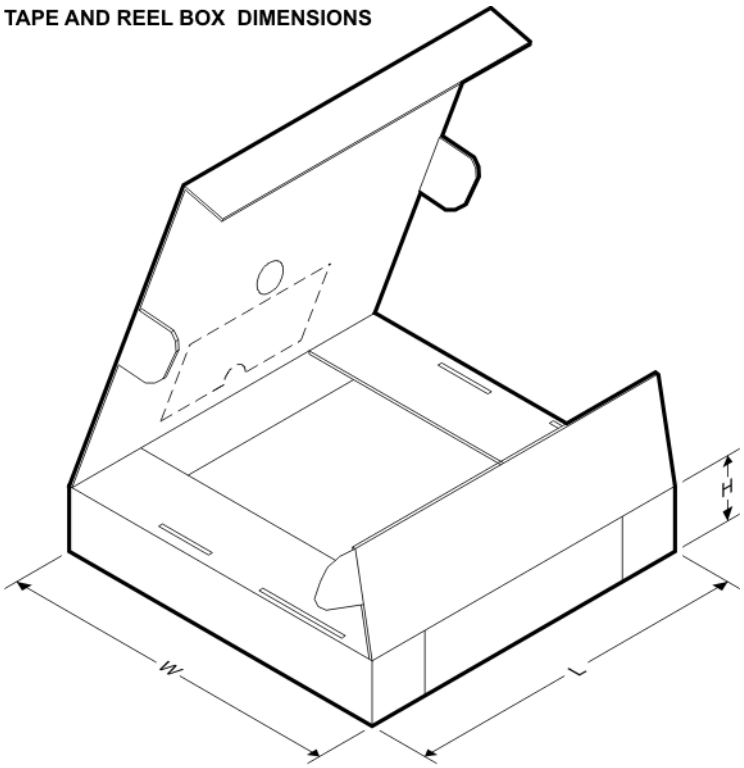
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS29854DWR	DW	24	SITE 60	330	24	10.75	15.7	2.7	12	24	Q1

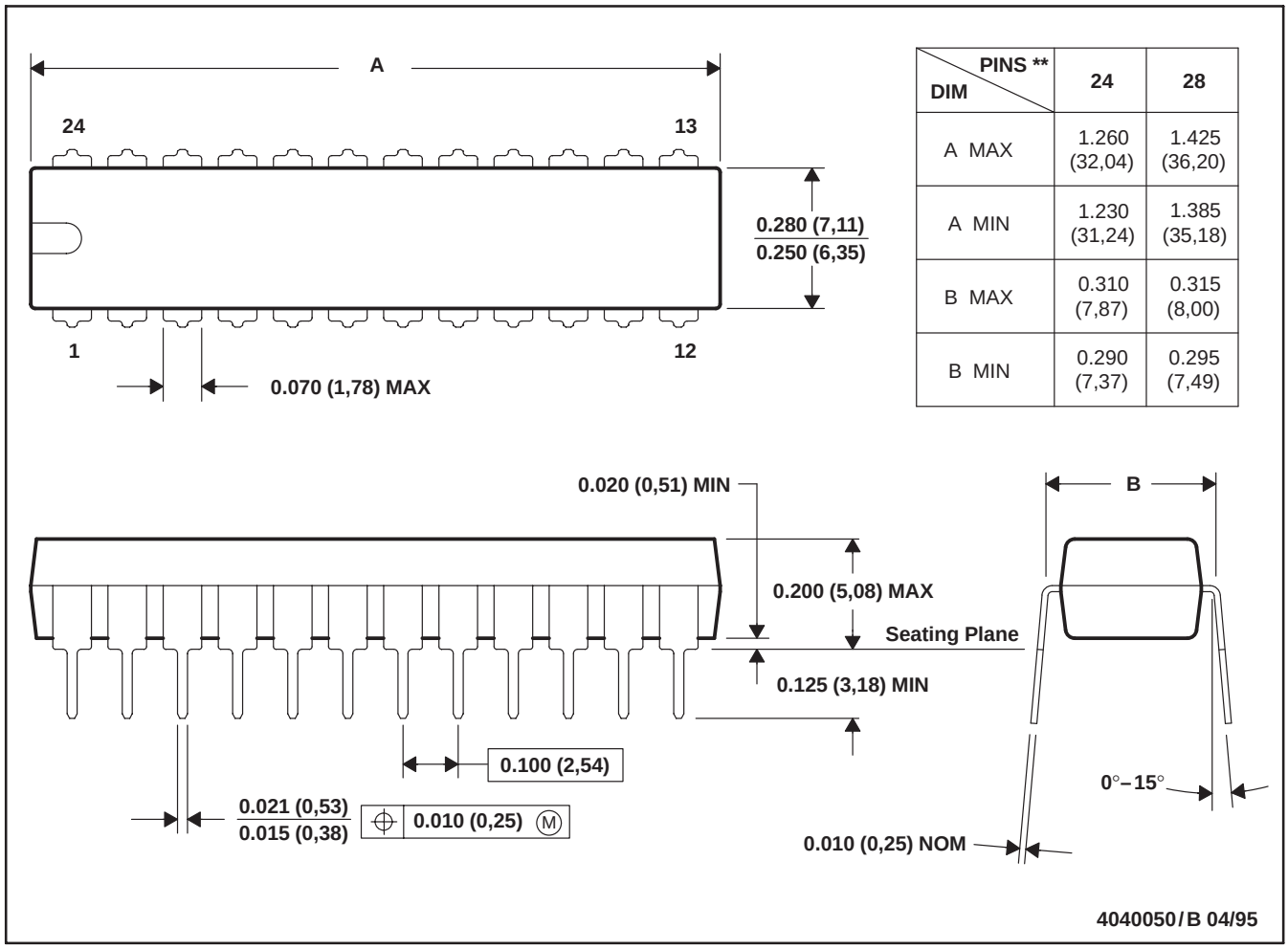
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALS29854DWR	DW	24	SITE 60	346.0	346.0	41.0

NT (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

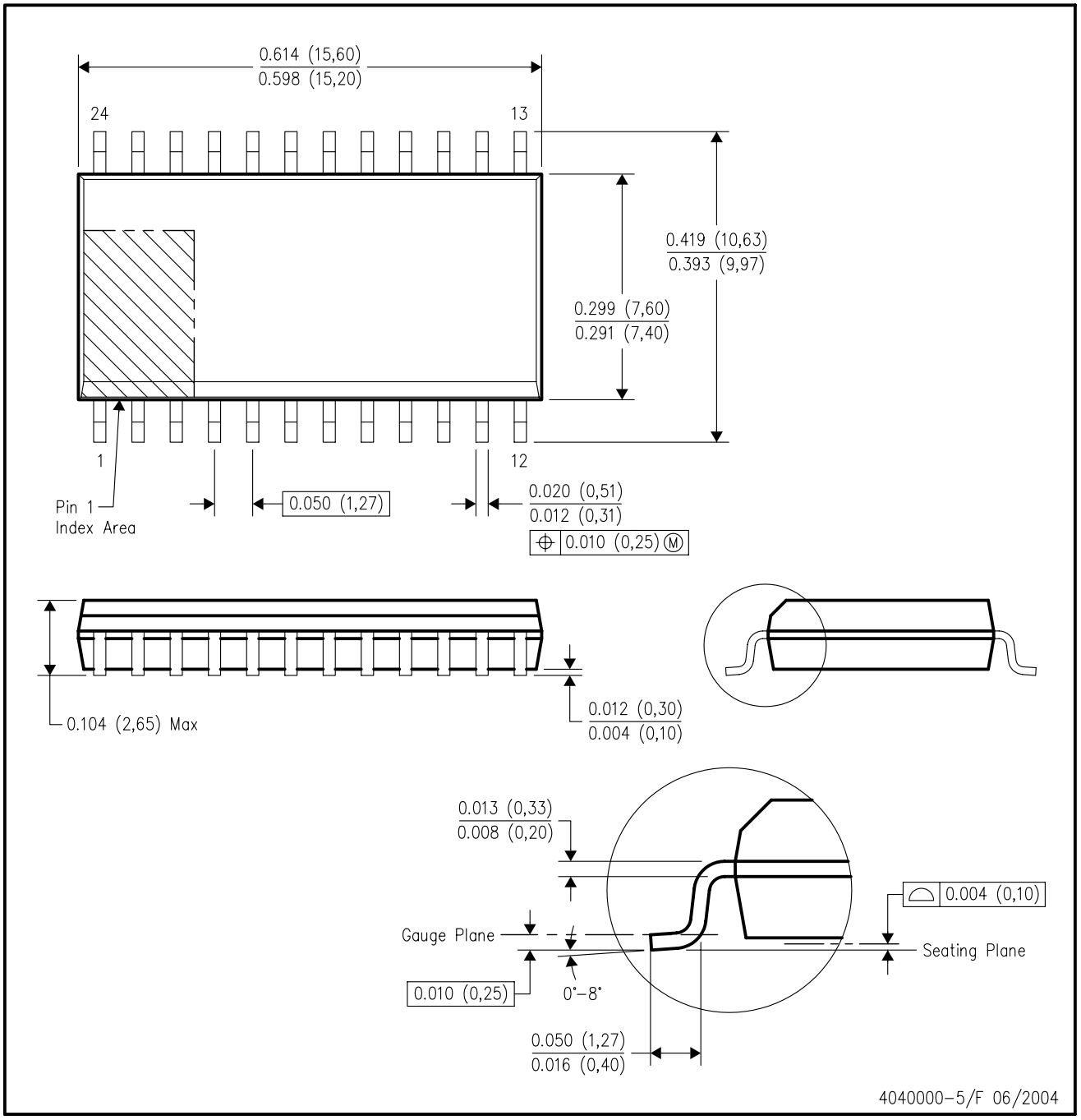
24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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