



**THE DATASHEET OF
SN74ABT16853DLG4**



SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5 V, T_A = 25^\circ C$**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}, 64\text{-mA } I_{OL}$)**
- **Parity-Error Flag With Parity Generator/Checker**
- **Latch for Storage of the Parity-Error Flag**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

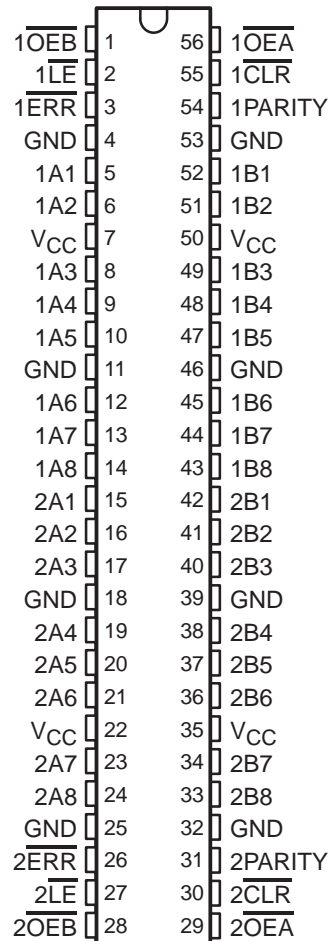
description

The 'ABT16853 dual 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus, with its corresponding parity bit, the open-collector parity-error (\overline{ERR}) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OE_A}$ and $\overline{OE_B}$) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT16853 provide true data at the outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the \overline{ERR} flag. The parity-error output can be passed, sampled, stored, or cleared from the latch using the latch-enable (\overline{LE}) and clear (\overline{CLR}) control inputs. When both $\overline{OE_A}$ and $\overline{OE_B}$ are low, data is transferred from the A bus to the B bus, and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16853 . . . WD PACKAGE
SN74ABT16853 . . . DGG OR DL PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB and Widebus are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

description (continued)

The SN54ABT16853 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16853 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	LE	AI Σ OF H	BI [†] Σ OF H	A	B	PARITY	$\overline{\text{ERR}}^{\ddagger}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H	H	X	X	Z	Z	Z	NC	Isolation [§] (parity check)
		L	H	X					H	
		X	L	L Odd H Even					H	
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

[†] Summation of high-level inputs includes PARITY along with Bi inputs.

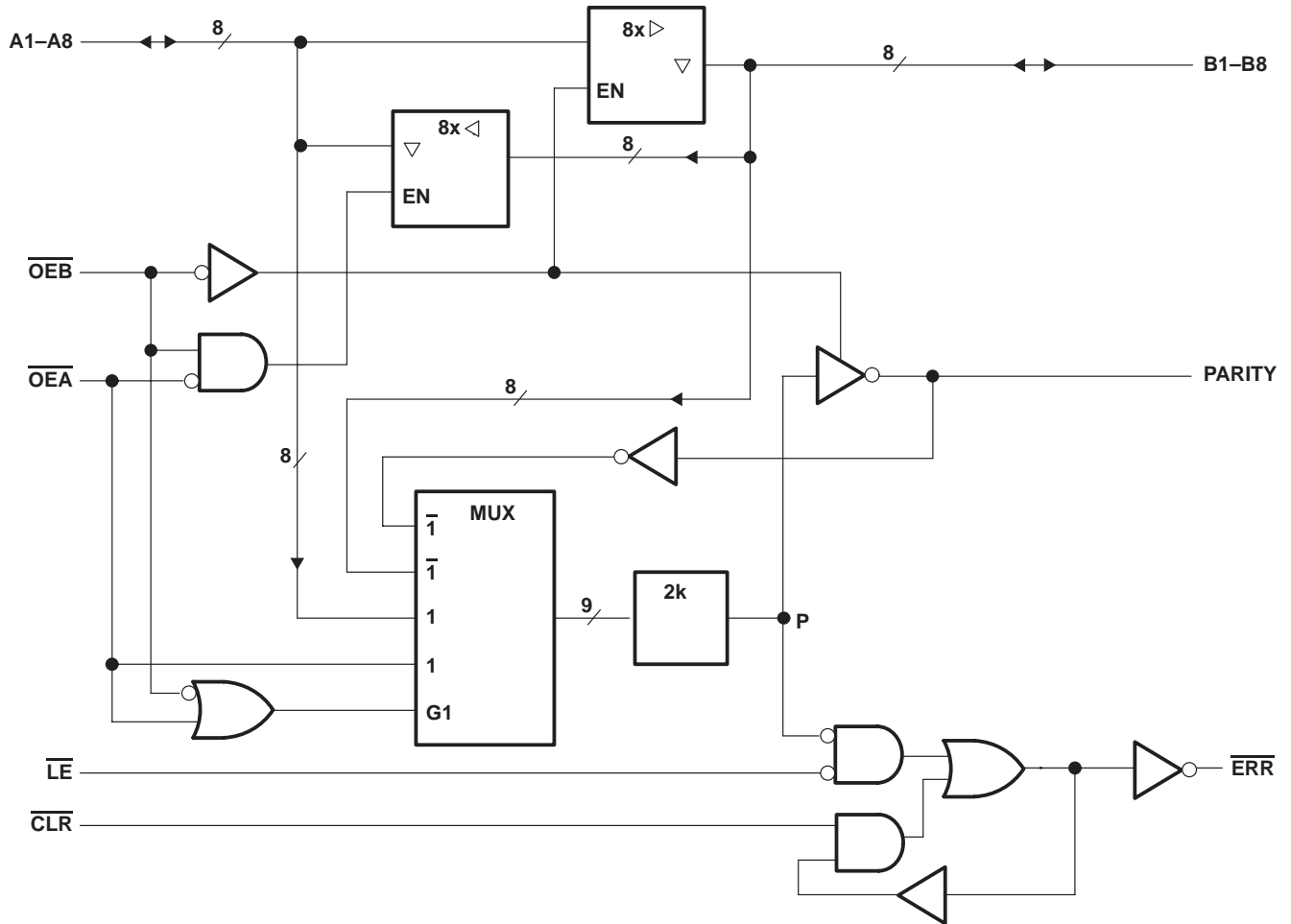
[‡] Output states shown assume $\overline{\text{ERR}}$ was previously high.

[§] In this mode, $\overline{\text{ERR}}$ (when clocked) shows inverted parity of the A bus.

SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

logic diagram (each transceiver) (positive logic)



ERROR-FLAG FUNCTION TABLE

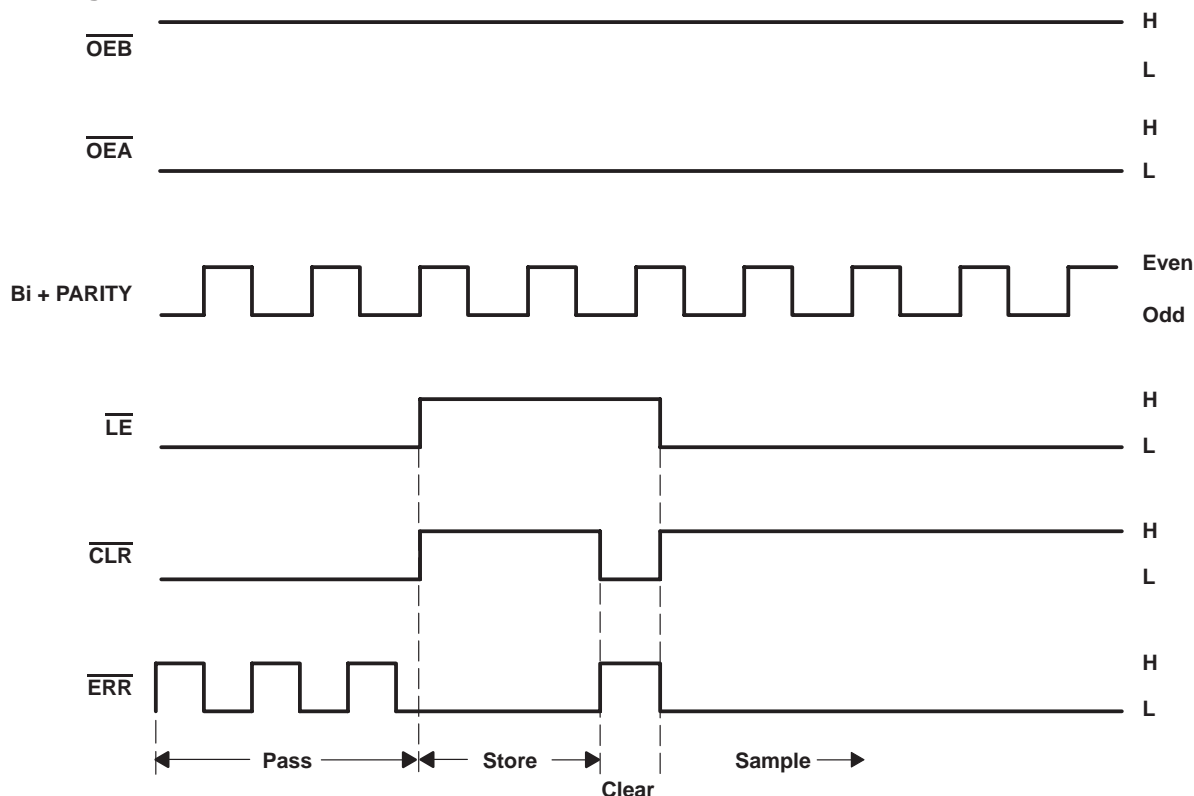
INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT ERR	FUNCTION
CLR	LE	POINT P	ERR _{n-1} †		
L	L	L	X	L	Pass
		H	X	H	
H	L	L	X	L	Sample
		H	H	H	
L	H	X	X	H	Clear
H	H	L	L	L	Store
		H	H	H	

† State of ERR before changes at CLR, LE, or point P

SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

error-flag waveforms



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16853	96 mA
SN74ABT16853	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

recommended operating conditions (see Note 3)

		SN54ABT16853		SN74ABT16853		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _{OH}	High-level output voltage		ERR		5.5	V
I _{OH}	High-level output current		Except ERR		-24	mA
I _{OL}	Low-level output current				48	mA
Δt/Δv	Input transition rise or fall rate		Outputs enabled		10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16853		SN74ABT16853		UNIT	
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	All outputs except ERR	V _{CC} = 4.5 V,	I _{OH} = -3 mA	2.5	3		2.5				V	
		V _{CC} = 5 V,	I _{OH} = -3 mA	3	3.4		3		3			
		V _{CC} = 4.5 V	I _{OH} = -24 mA				2					
			I _{OH} = -32 mA	2*	2.7				2			
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 24 mA		0.25	0.55				0.55	V	
			I _{OL} = 64 mA		0.3	0.55*				0.55		
V _{hys}					100						mV	
I _{OH}	ERR	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			20		20		20	μA	
I _{off}		V _{CC} = 0,	V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	Outputs high	V _{CC} = 5.5 V,	V _O = 5.5 V			50		50		50	μA	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND				±1		±1		±1	μA	
	A or B ports					±100		±100		±100		
I _{IL}	A or B ports	V _{CC} = 0,	V _I = GND			-50		-50		-50	μA	
I _{O‡}		V _{CC} = 5.5 V,	V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA	
I _{OZH} §		V _{CC} = 5.5 V,	V _O = 2.7 V			50		50		50	μA	
I _{OZL} §		V _{CC} = 5.5 V,	V _O = 0.5 V			-50		-50		-50	μA	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1.5	2		2		2	mA	
			Outputs low		32	40		40		40		
			Outputs disabled		1	2		2		2		
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				50		50		50	μA	
C _i	Control inputs	V _I = 2.5 V or 0.5 V				3					pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V				9					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT16853, SN74ABT16853 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

SCBS153B – OCTOBER 1992 – REVISED JANUARY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C		SN54ABT16853		SN74ABT16853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	\overline{LE} high or low	8.5		8.5		8.5		ns
		\overline{CLR} low	4		4		4		
t _{su}	Setup time	A, B, and PARITY before $\overline{LE}\downarrow$	10		10		10		ns
		\overline{CLR} before $\overline{LE}\downarrow$	0		0		0		
t _h	Hold time	A, B, and PARITY after $\overline{LE}\downarrow$	0		0		0		ns
		\overline{CLR} after $\overline{LE}\downarrow$	0		0		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

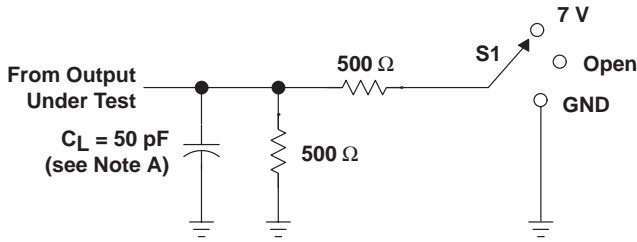
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT16853		SN74ABT16853		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t _{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t _{PLH}	A or \overline{OE}	PARITY	2	4.6	5.9	2	7.3	2	7.1	ns
t _{PHL}			2	4.8	6.2	2	7.6	2	7.2	
t _{PLH}	\overline{CLR}	\overline{ERR}	2	3.7	5.1	2	5.9	2	5.7	ns
t _{PZH}	\overline{OE}	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t _{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t _{PHZ}	\overline{OE}	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t _{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t _{PZH}	\overline{OE}	PARITY	2	3.6	5	2	5.8	2	5.7	ns
t _{PZL}			2.5	4.4	5.8	2.5	6.7	2.5	6.5	
t _{PHZ}	\overline{OE}	PARITY	1.5	3.2	4	1.5	4.8	1.5	4.7	ns
t _{PLZ}			1.5	2.9	3.7	1.5	4.2	1.5	4.1	
t _{PLH}	\overline{LE}	\overline{ERR}	2	3.5	4.2	2	5	2	4.8	ns
t _{PHL}			2	3.4	4.4	2	5.2	2	4.9	
t _{PLH}	A, B, or PARITY	\overline{ERR}	2	4.5	6.3	2	7.5	2	7.2	ns
t _{PHL}			2	4.8	6.3	2	7.7	2	7.4	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

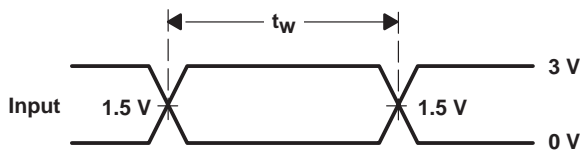
PARAMETER MEASUREMENT INFORMATION



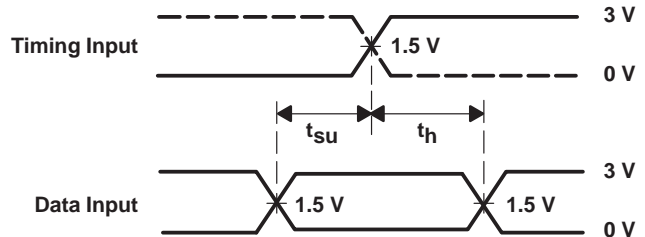
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

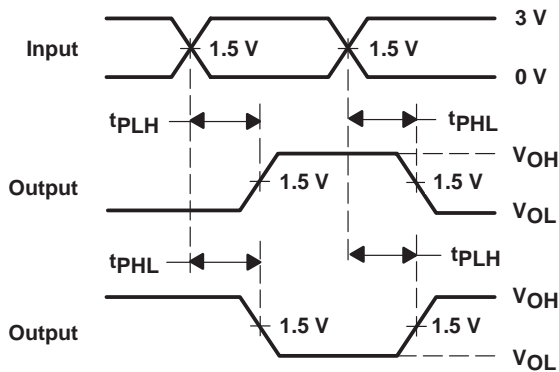
$\overline{\text{ERR}}$	S1
t_{PHL} (see Note E)	7 V
t_{PLH} (see Note F)	7 V



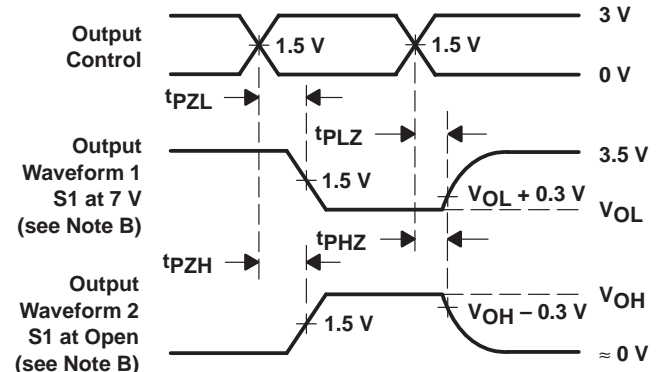
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PHL} is measured at 1.5 V.
 F. t_{PLH} is measured at $V_{OL} + 0.3 \text{ V}$.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74ABT16853DLG4 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management