



**THE DATASHEET OF
LTC2053CDD#PBF**



Precision, Rail-to-Rail, Zero-Drift, Resistor-Programmable Instrumentation Amplifier

FEATURES

- 116dB CMRR Independent of Gain
- Maximum Offset Voltage: 10 μ V
- Maximum Offset Voltage Drift: 50nV/ $^{\circ}$ C
- Rail-to-Rail Input
- Rail-to-Rail Output
- 2-Resistor Programmable Gain
- Supply Operation: 2.7V to \pm 5.5V
- Typical Noise: 2.5 μ V_{p-p} (0.01Hz to 10Hz)
- Typical Supply Current: 750 μ A
- LTC2053-SYNC Allows Synchronization to External Clock
- Available in MS8 and 3mm \times 3mm \times 0.8mm DFN Packages

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC[®]2053 is a high precision instrumentation amplifier. The CMRR is typically 116dB with a single or dual 5V supply and is independent of gain. The input offset voltage is guaranteed below 10 μ V with a temperature drift of less than 50nV/ $^{\circ}$ C. The LTC2053 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

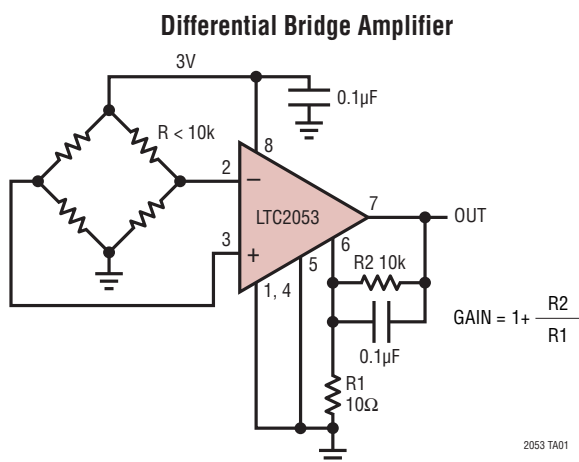
The LTC2053 uses charge balanced sampled data techniques to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier.

The differential inputs operate from rail-to-rail and the single-ended output swings from rail-to-rail. The LTC2053 can be used in single-supply applications, as low as 2.7V. It can also be used with dual \pm 5.5V supplies. The LTC2053 requires no external clock, while the LTC2053-SYNC has a CLK pin to synchronize to an external clock.

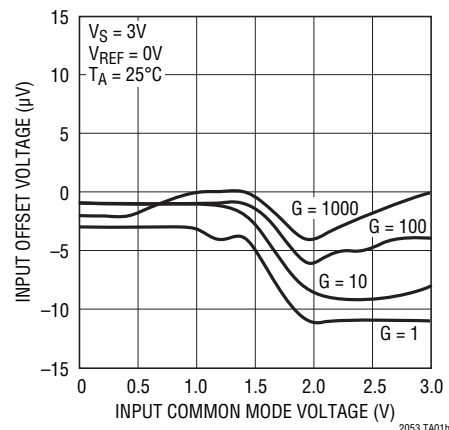
The LTC2053 is available in an MS8 surface mount package. For space limited applications, the LTC2053 is available in a 3mm \times 3mm \times 0.8mm dual fine pitch leadless package (DFN).

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TYPICAL APPLICATION



Typical Input Referred Offset vs Input Common Mode Voltage ($V_S = 3V$)



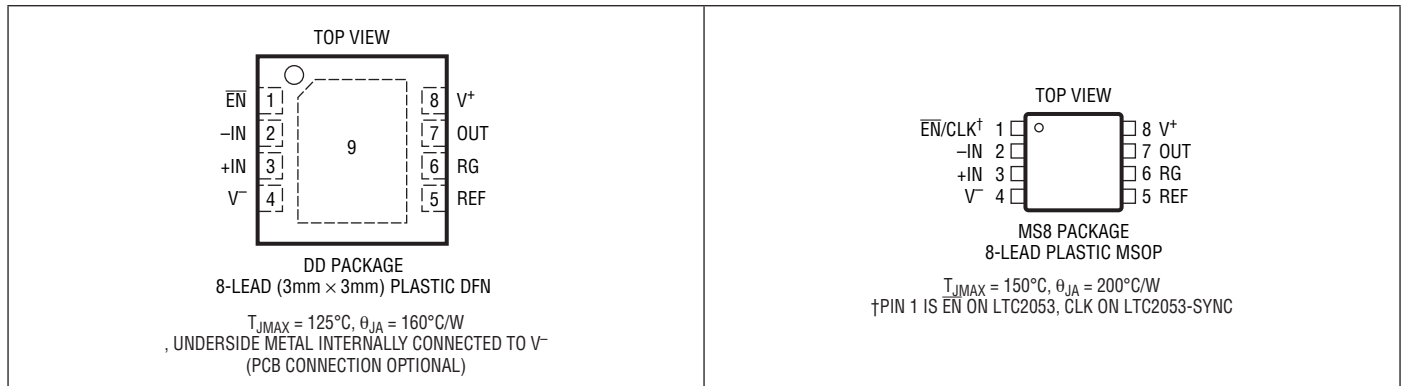
2053syncfd

LTC2053/LTC2053-SYNC

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....	11V	Storage Temperature Range	
Input Current.....	$\pm 10\text{mA}$	MS8 Package.....	-65°C to 150°C
$ V_{-IN} - V_{REF} $	5.5V	DD Package.....	-65°C to 125°C
$ V_{+IN} - V_{REF} $	5.5V	Lead Temperature (Soldering, 10 sec).....	300°C
Output Short-Circuit Duration.....	Indefinite		
Operating Temperature Range			
LTC2053C, LTC2053C-SYNC.....	0°C to 70°C		
LTC2053I, LTC2053I-SYNC.....	-40°C to 85°C		
LTC2053H.....	-40°C to 125°C		

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2053CDD#PBF	LTC2053CDD#TRPBF	LAEQ	8-Lead (3mm x 3mm) Plastic DFN	0°C to 70°C
LTC2053IDD#PBF	LTC2053IDD#TRPBF	LAEQ	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 85°C
LTC2053HDD#PBF	LTC2053HDD#TRPBF	LAEQ	8-Lead (3mm x 3mm) Plastic DFN	-40°C to 125°C
LTC2053CMS8#PBF	LTC2053CMS8#TRPBF	LTVT	8-Lead Plastic MSOP	0°C to 70°C
LTC2053IMS8#PBF	LTC2053IMS8#TRPBF	LTJY	8-Lead Plastic MSOP	-40°C to 85°C
LTC2053HMS8#PBF	LTC2053HMS8#TRPBF	LTAFB	8-Lead Plastic MSOP	-40°C to 125°C
LTC2053CMS8-SYNC#PBF	LTC2053CMS8-SYNC#TRPBF	LTBNP	8-Lead Plastic MSOP	0°C to 70°C
LTC2053IMS8-SYNC#PBF	LTC2053IMS8-SYNC#TRPBF	LTBNP	8-Lead Plastic MSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $\text{REF} = 200\text{mV}$. Output voltage swing is referenced to V^- . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$, LTC2053	●		3	12	ppm
	$A_V = 1$, LTC2053-SYNC	●		3	15	ppm
Input Offset Voltage (Note 2)	$V_{\text{CM}} = 200\text{mV}$			-5	± 10	μV
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to 85°C	●			± 50	$\text{nV}/^\circ\text{C}$
	$T_A = 85^\circ\text{C}$ to 125°C	●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		4	10	nA
Average Input Offset Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		1	3	nA
Input Noise Voltage	DC to 10Hz			2.5		$\mu\text{V}_{\text{P-P}}$
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 3V , LTC2053C, LTC2053C-SYNC	●	100	113		dB
	$A_V = 1$, $V_{\text{CM}} = 0.1\text{V}$ to 2.9V , LTC2053I, LTC2053I-SYNC	●	100	113		dB
	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 3V , LTC2053I, LTC2053I-SYNC	●		95	113	dB
	$A_V = 1$, $V_{\text{CM}} = 0.1\text{V}$ to 2.9V , LTC2053H	●		100		dB
	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 3V , LTC2053H	●		85		dB
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V}$ to 6V	●	110	116		dB
Output Voltage Swing High	$R_L = 2\text{k}$ to V^-	●	2.85	2.94		V
	$R_L = 10\text{k}$ to V^-	●	2.95	2.98		V
Output Voltage Swing Low		●			20	mV
Supply Current	No Load	●		0.75	1	mA
Supply Current, Shutdown	$V_{\text{EN}} \geq 2.5\text{V}$, LTC2053 Only				10	μA
$\overline{\text{EN}}/\text{CLK}$ Pin Input Low Voltage, V_{IL}					0.5	V
$\overline{\text{EN}}/\text{CLK}$ Pin Input High Voltage, V_{IH}			2.5			V
$\overline{\text{EN}}/\text{CLK}$ Pin Input Current	$V_{\text{EN}}/\text{CLK} = V^-$			-0.5	-10	μA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		$\text{V}/\mu\text{s}$
Internal Sampling Frequency				3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $\text{REF} = 200\text{mV}$. Output voltage swing is referenced to V^- . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$	●		3	10	ppm
Input Offset Voltage (Note 2)	$V_{\text{CM}} = 200\text{mV}$			-5	± 10	μV
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C}$ to 85°C	●			± 50	$\text{nV}/^\circ\text{C}$
	$T_A = 85^\circ\text{C}$ to 125°C	●		-1	-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		4	10	nA
Average Input Offset Current (Note 3)	$V_{\text{CM}} = 1.2\text{V}$	●		1	3	nA
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 5V , LTC2053C	●	105	116		dB
	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 5V , LTC2053C-SYNC	●	100	116		dB
	$A_V = 1$, $V_{\text{CM}} = 0.1\text{V}$ to 4.9V , LTC2053I	●	105	116		dB
	$A_V = 1$, $V_{\text{CM}} = 0.1\text{V}$ to 4.9V , LTC2053I-SYNC	●	100	116		dB
	$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 5V , LTC2053I, LTC2053I-SYNC	●		95	116	dB
	$A_V = 1$, $V_{\text{CM}} = 0.1\text{V}$ to 4.9V , LTC2053H	●		100		dB
$A_V = 1$, $V_{\text{CM}} = 0\text{V}$ to 5V , LTC2053H	●		85		dB	
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V}$ to 6V	●	110	116		dB

LTC2053/LTC2053-SYNC

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $\text{REF} = 200\text{mV}$. Output voltage swing is referenced to V^- . All other specifications reference the OUT pin to the REF pin.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing High	$R_L = 2\text{k to } V^-$ $R_L = 10\text{k to } V^-$	●	4.85	4.94		V
		●	4.95	4.98		V
Output Voltage Swing Low		●			20	mV
Supply Current	No Load	●		0.85	1.1	mA
Supply Current, Shutdown	$V_{\text{EN}} \geq 4.5\text{V}$, LTC2053 Only				10	μA
$\overline{\text{EN}}/\text{CLK}$ Pin Input Low Voltage, V_{IL}					0.5	V
$\overline{\text{EN}}/\text{CLK}$ Pin Input High Voltage, V_{IH}			4.5			V
$\overline{\text{EN}}/\text{CLK}$ Pin Input Current	$V_{\text{EN}}/\text{CLK} = V^-$			-1	-10	μA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/ μs
Internal Sampling Frequency				3		kHz

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $\text{REF} = 0\text{V}$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	$A_V = 1$	●		0.001	0.01	%
Gain Nonlinearity	$A_V = 1$	●		3	10	ppm
Input Offset Voltage (Note 2)	$V_{\text{CM}} = 0\text{V}$			10	± 20	μV
Average Input Offset Drift (Note 2)	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$ $T_A = 85^\circ\text{C to } 125^\circ\text{C}$	●			± 50	nV/ $^\circ\text{C}$
		●			-2.5	$\mu\text{V}/^\circ\text{C}$
Average Input Bias Current (Note 3)	$V_{\text{CM}} = 1\text{V}$	●		4	10	nA
Average Input Offset Current (Note 3)	$V_{\text{CM}} = 1\text{V}$	●		1	3	nA
Common Mode Rejection Ratio (Notes 4, 5)	$A_V = 1$, $V_{\text{CM}} = -5\text{V to } 5\text{V}$, LTC2053C	●	105	118		dB
	$A_V = 1$, $V_{\text{CM}} = -5\text{V to } 5\text{V}$, LTC2053C-SYNC	●	100	118		dB
	$A_V = 1$, $V_{\text{CM}} = -4.9\text{V to } 4.9\text{V}$, LTC2053I	●	105	118		dB
	$A_V = 1$, $V_{\text{CM}} = -4.9\text{V to } 4.9\text{V}$, LTC2053I-SYNC	●	100	118		dB
	$A_V = 1$, $V_{\text{CM}} = -5\text{V to } 5\text{V}$, LTC2053I, LTC2053I-SYNC	●	95	118		dB
	$A_V = 1$, $V_{\text{CM}} = -4.9\text{V to } 4.9\text{V}$, LTC2053H	●	100			dB
	$A_V = 1$, $V_{\text{CM}} = -5\text{V to } 5\text{V}$, LTC2053H	●	90			dB
Power Supply Rejection Ratio (Note 6)	$V_S = 2.7\text{V to } 11\text{V}$	●	110	116		dB
Maximum Output Voltage Swing	$R_L = 2\text{k to GND}$, C- and I-Grades $R_L = 10\text{k to GND}$, All Grades $R_L = 2\text{k to GND}$, LTC2053H Only	●	± 4.5	± 4.8		V
		●	± 4.6	± 4.9		V
		●	± 4.4	± 4.8		V
Supply Current	No Load	●		0.95	1.3	mA
Supply Current, Shutdown	$V_{\text{EN}} \geq 4.5\text{V}$, LTC2053 Only				20	μA
$\overline{\text{EN}}$ Pin Input Low Voltage, V_{IL}					-4.5	V
CLK Pin Input Low Voltage, V_{IL}					0.5	V
$\overline{\text{EN}}/\text{CLK}$ Pin Input High Voltage, V_{IH}			4.5			V
$\overline{\text{EN}}/\text{CLK}$ Pin Input Current	$V_{\text{EN}}/\text{CLK} = V^-$			-3	-20	μA
Internal Op Amp Gain Bandwidth				200		kHz
Slew Rate				0.2		V/ μs
Internal Sampling Frequency				3		kHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 3: If the total source resistance is less than 10k, no DC errors result from the input bias currents or the mismatch of the input bias currents or the mismatch of the resistances connected to $-IN$ and $+IN$.

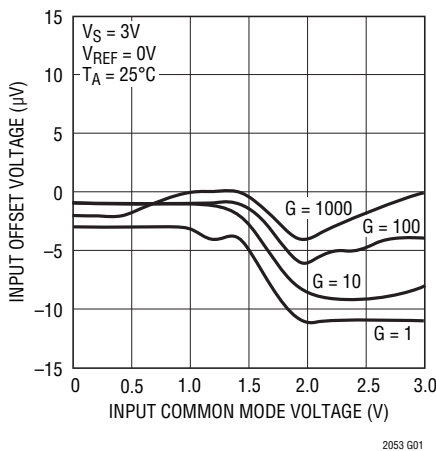
Note 4: The CMRR with a voltage gain, A_V , larger than 10 is 120dB (typ).

Note 5: At temperatures above 70°C, the common mode rejection ratio lowers when the common mode input voltage is within 100mV of the supply rails.

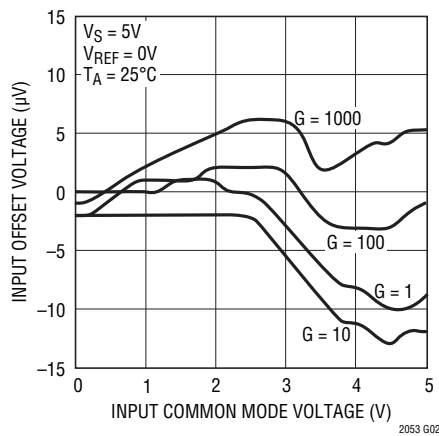
Note 6: The power supply rejection ratio (PSRR) measurement accuracy depends on the proximity of the power supply bypass capacitor to the device under test. Because of this, the PSRR is 100% tested to relaxed limits at final test. However, their values are guaranteed by design to meet the data sheet limits.

TYPICAL PERFORMANCE CHARACTERISTICS

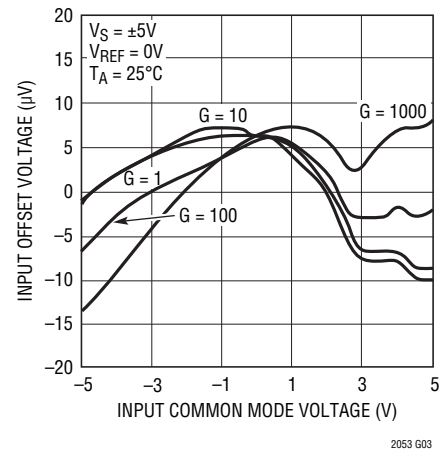
Input Offset Voltage vs Input Common Mode Voltage



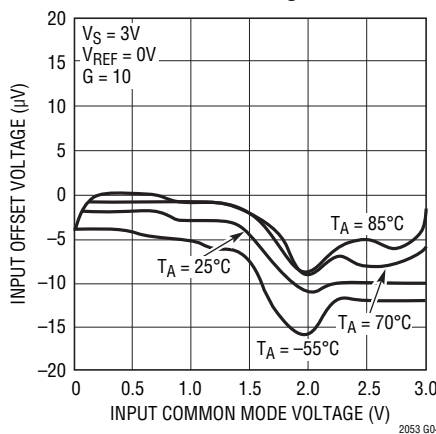
Input Offset Voltage vs Input Common Mode Voltage



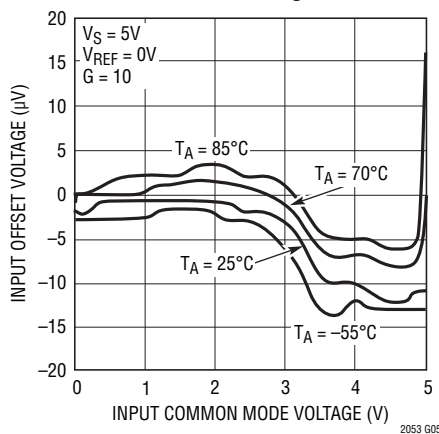
Input Offset Voltage vs Input Common Mode Voltage



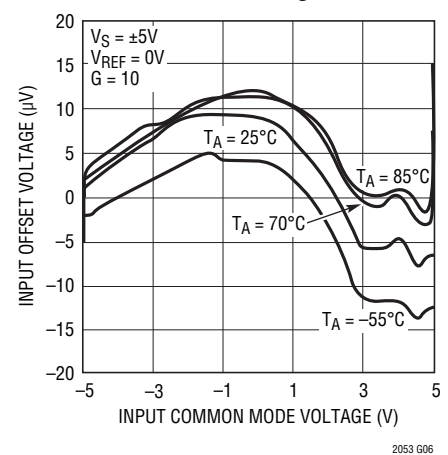
Input Offset Voltage vs Input Common Mode Voltage



Input Offset Voltage vs Input Common Mode Voltage

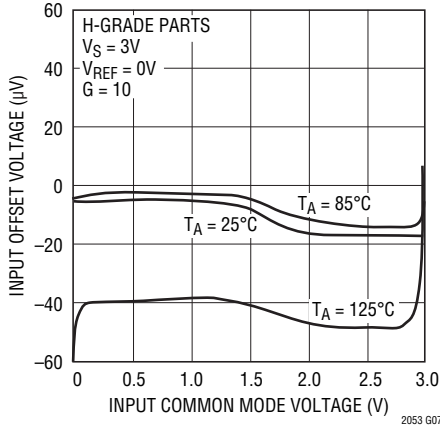


Input Offset Voltage vs Input Common Mode Voltage

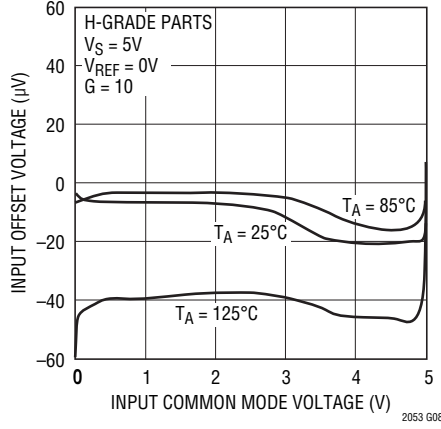


TYPICAL PERFORMANCE CHARACTERISTICS

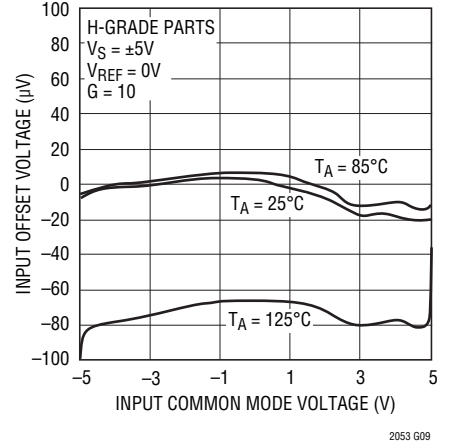
Input Offset Voltage vs Input Common Mode Voltage



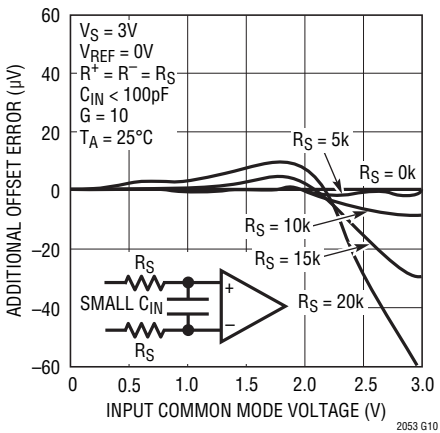
Input Offset Voltage vs Input Common Mode Voltage



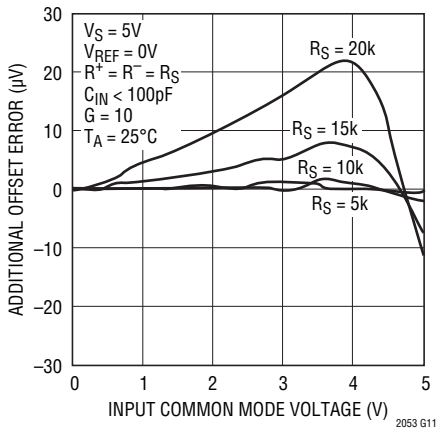
Input Offset Voltage vs Input Common Mode Voltage



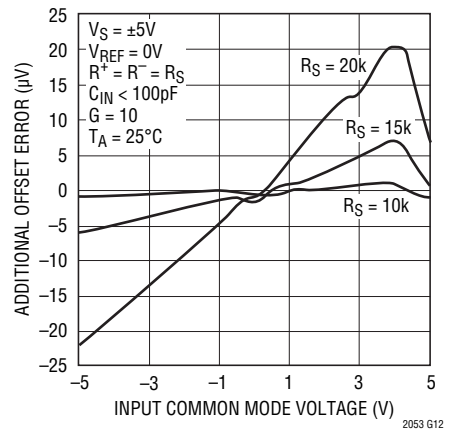
Error Due to Input R_S vs Input Common Mode ($C_{IN} < 100pF$)



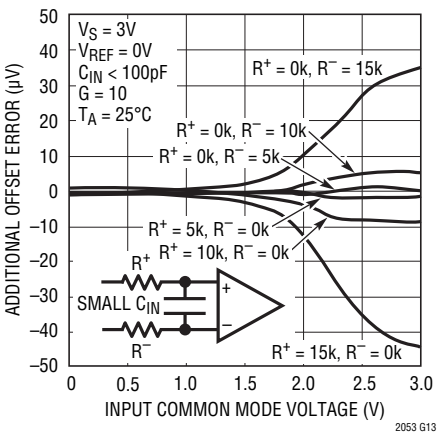
Error Due to Input R_S vs Input Common Mode ($C_{IN} < 100pF$)



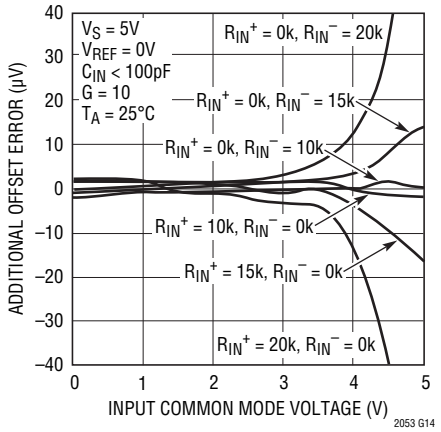
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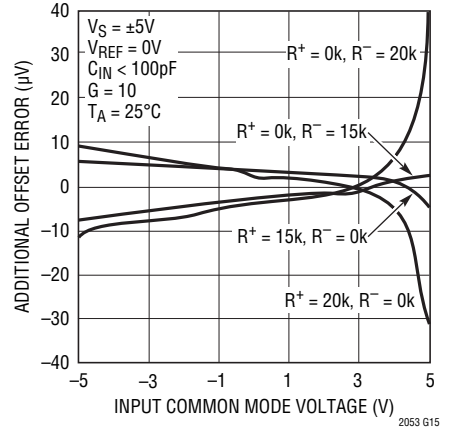
Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} < 100pF$)



Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} < 100pF$)

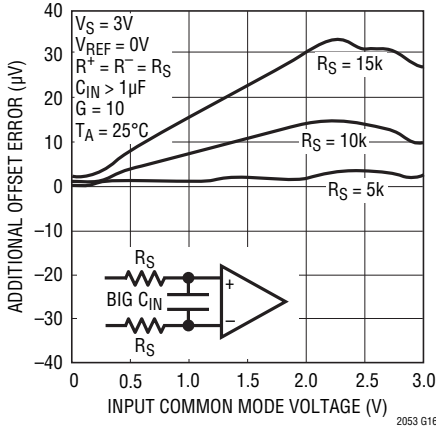


Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} < 100pF$)

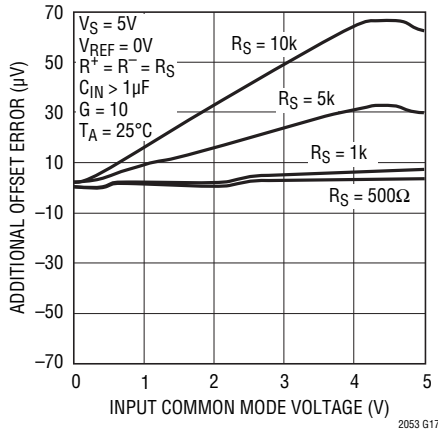


TYPICAL PERFORMANCE CHARACTERISTICS

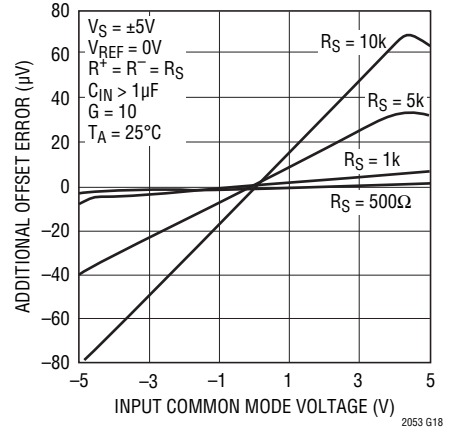
Error Due to Input R_S vs Input Common Mode ($C_{IN} > 1\mu F$)



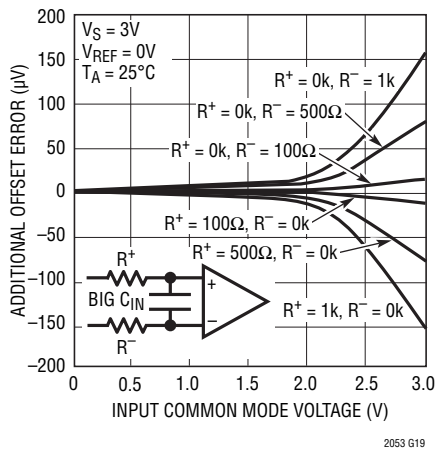
Error Due to Input R_S vs Input Common Mode ($C_{IN} > 1\mu F$)



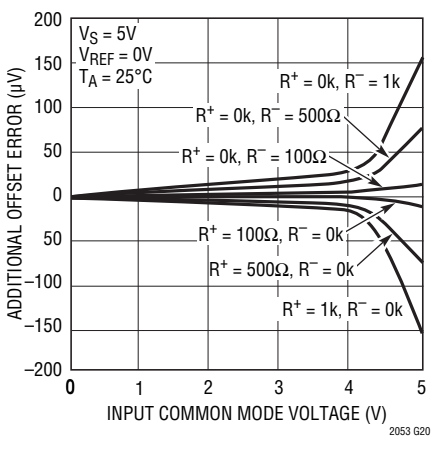
Error Due to Input R_S vs Input Common Mode ($C_{IN} > 1\mu F$)



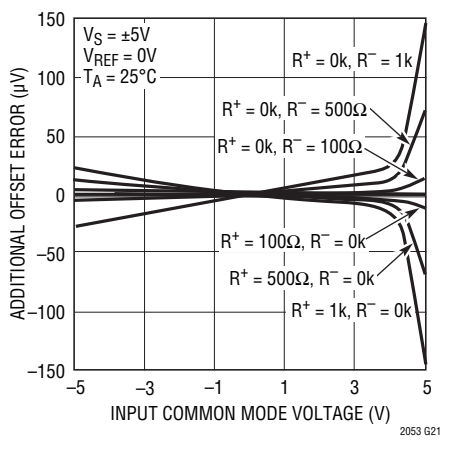
Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} > 1\mu F$)



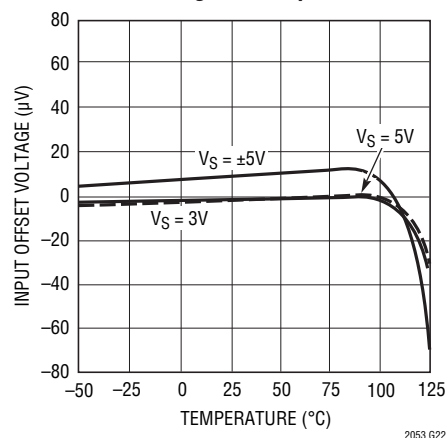
Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} > 1\mu F$)



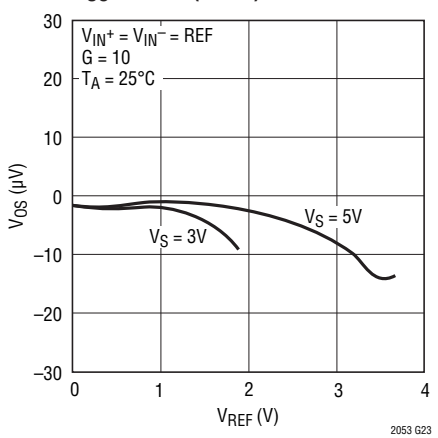
Error Due to Input R_S Mismatch vs Input Common Mode ($C_{IN} > 1\mu F$)



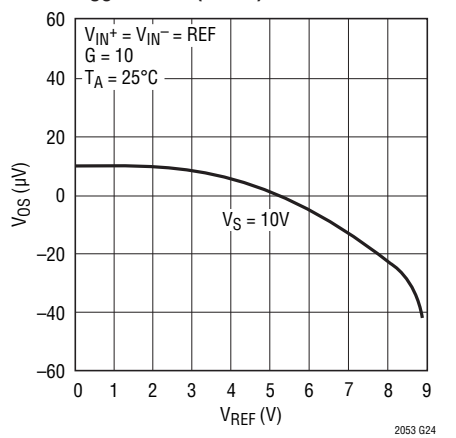
Offset Voltage vs Temperature



V_{OS} vs REF (Pin 5)

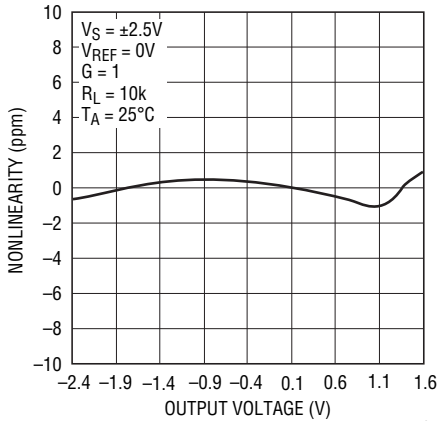


V_{OS} vs REF (Pin 5)

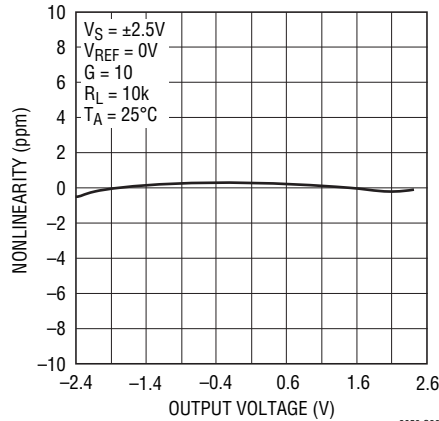


TYPICAL PERFORMANCE CHARACTERISTICS

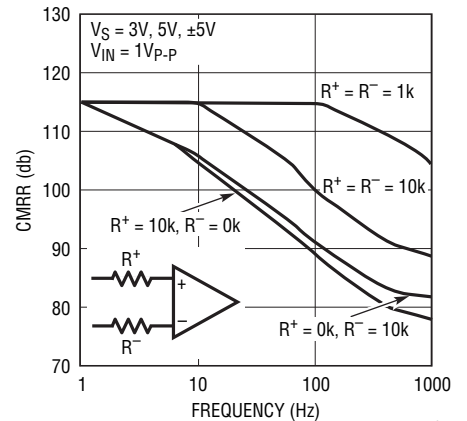
Gain Nonlinearity, G = 1



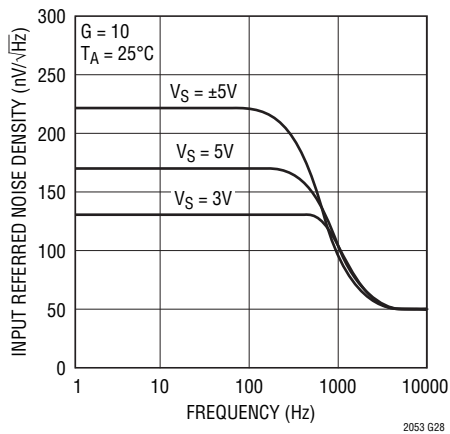
Gain Nonlinearity, G = 10



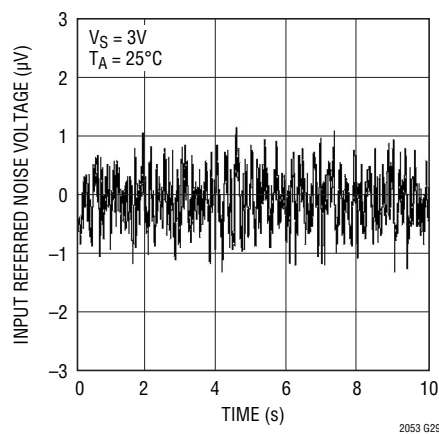
CMRR vs Frequency



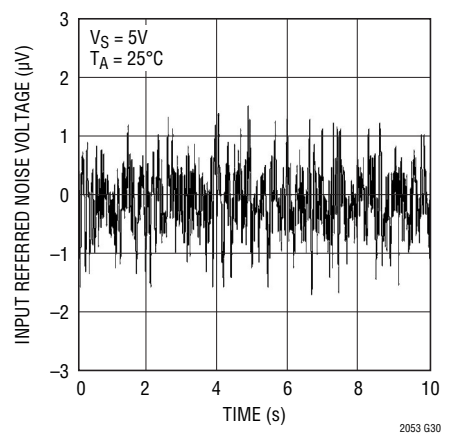
Input Voltage Noise Density vs Frequency



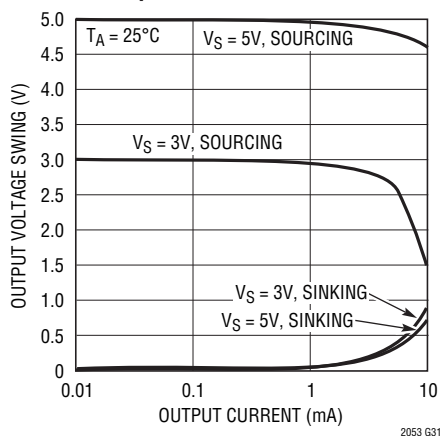
Input Referred Noise in 10Hz Bandwidth



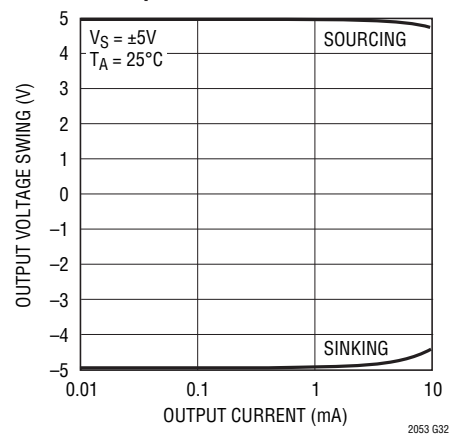
Input Referred Noise in 10Hz Bandwidth



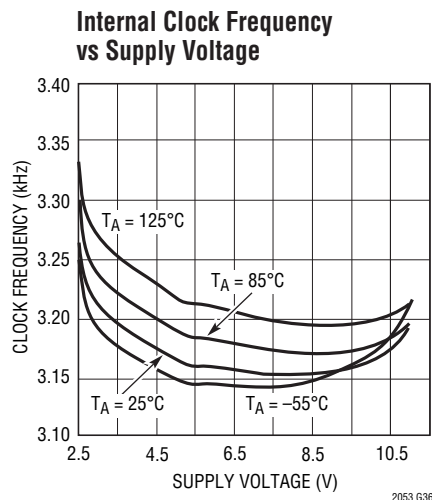
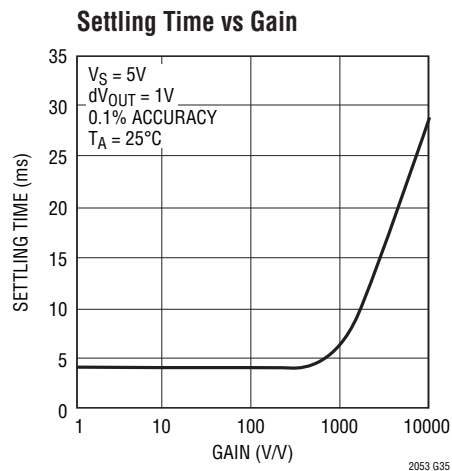
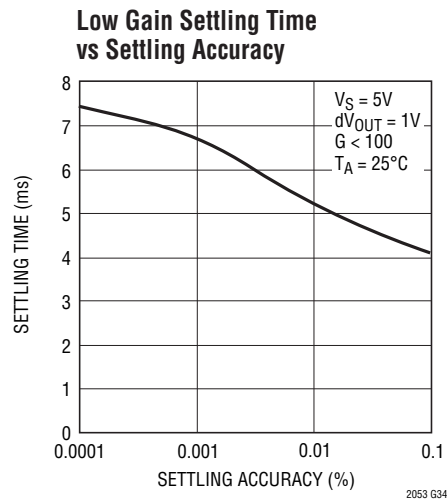
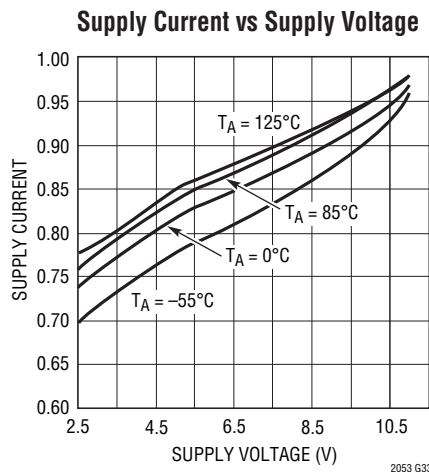
Output Voltage Swing vs Output Current



Output Voltage Swing vs Output Current



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

EN (Pin 1, LTC2053 Only): Active Low Enable Pin.

CLK (Pin 1, LTC2053-SYNC Only): Clock input for Synchronizing to External System Clock.

-IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

V⁻ (Pin 4): Negative Supply.

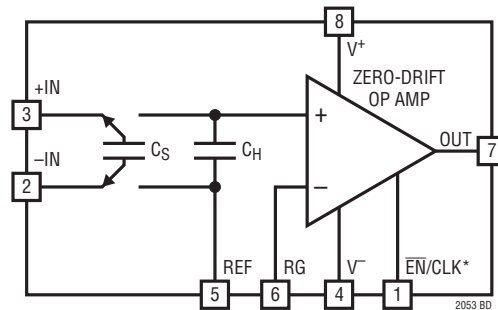
REF (Pin 5): Voltage Reference (V_{REF}) for Amplifier Output.

RG (Pin 6): Inverting Input of Internal Op Amp. See Figure 1.

OUT (Pin 7): Amplifier Output. See Figure 1.

V⁺ (Pin 8): Positive Supply.

BLOCK DIAGRAM



*NOTE: PIN 1 IS $\overline{\text{EN}}$ ON THE LTC2053 AND CLK ON THE LTC2053-SYNC

APPLICATIONS INFORMATION

Theory of Operation

The LTC2053 uses an internal capacitor (C_S) to sample a differential input signal riding on a DC common mode voltage (see the Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor (C_H) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

Input Voltage Range

The input common mode voltage range of the LTC2053 is rail-to-rail. However, the following equation limits the size of the differential input voltage:

$$V^- \leq (V_{+IN} - V_{-IN}) + V_{REF} \leq V^+ - 1.3$$

Where V_{+IN} and V_{-IN} are the voltages of the +IN and -IN pins, respectively, V_{REF} is the voltage at the REF pin and V^+ is the positive supply voltage.

For example, with a 3V single supply and a 0V to 100mV differential input voltage, V_{REF} must be between 0V and 1.6V.

± 5 Volt Operation

When using the LTC2053 with supplies over 5.5V, care must be taken to limit the maximum difference between any of the input pins (+IN or -IN) and the REF pin to 5.5V; if not, the device will be damaged. For example, if rail-to-rail input operation is desired when the supplies are at ± 5 V, the REF pin should be 0V, ± 0.5 V. As a second example, if V^+ is 10V and V^- and REF are at 0V, the inputs should not exceed 5.5V.

Settling Time

The sampling rate is 3kHz and the input sampling period during which C_S is charged to the input differential voltage V_{IN} is approximately 150 μ s. First assume that on each input sampling period, C_S is charged fully to V_{IN} . Since $C_S = C_H (= 1000\text{pF})$, a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 333 μ s(N). The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, the settling time is dominated by the switched capacitor front end for gains below 100 (see the Typical Performance Characteristics section).

APPLICATIONS INFORMATION

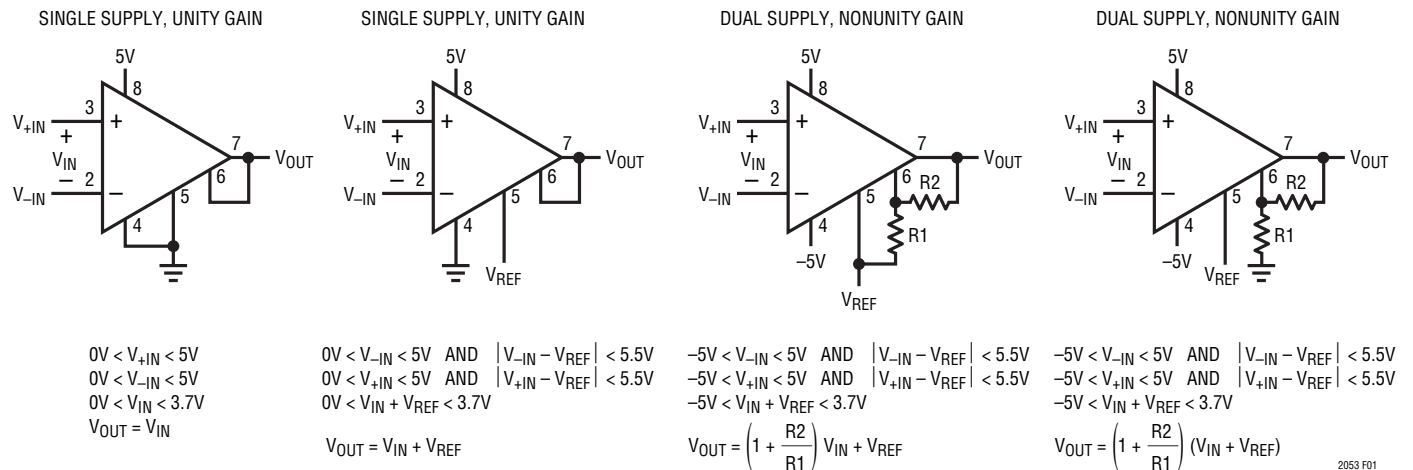


Figure 1

Input Current

Whenever the differential input V_{IN} changes, C_H must be charged up to the new input voltage via C_S . This results in an input charging current during each input sampling period. Eventually, C_H and C_S will reach V_{IN} and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on C_S every cycle even if V_{IN} is a DC voltage. For example, the parasitic bottom plate capacitor on C_S must be charged from the voltage on the REF pin to the voltage on the $-IN$ pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to $R_S C_S$. **If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between $-IN$ and $+IN$. With R_S less than 10k, no DC errors occur due to this input current.**

In the Typical Performance Characteristics section of this data sheet, there are curves showing the additional error from non-zero source resistance in the inputs. If there are no large capacitors across the inputs, the amplifier is less sensitive to source resistance and source resistance mismatch. When large capacitors are placed across the inputs, the input charging currents previously described result in larger DC errors, especially with source resistor mismatches.

Power Supply Bypassing

The LTC2053 uses a sampled data technique and, therefore, contains some clocked digital circuitry. It is, therefore, sensitive to supply bypassing. For single or dual supply operation, a 0.1 μ F ceramic capacitor must be connected between Pin 8 (V^+) and Pin 4 (V^-) with leads as short as possible.

Synchronizing to an External Clock (LTC2053-SYNC Only)

The LTC2053 has an internally generated sample clock that is typically 3kHz. **There is no need to provide the LTC2053 with a clock.** However, in some applications, it may be desirable for the user to control the sampling frequency more precisely to avoid undesirable aliasing. This can be done with the LTC2053-SYNC. This device uses Pin 1 as a clock input whereas the LTC2053 uses Pin 1 as an enable pin. If CLK (Pin 1) is left floating on the LTC2053-SYNC, the device will run on its internal oscillator, similar to the LTC2053. However, if not externally synchronizing to a system clock, it is recommended that the LTC2053 be used instead of the LTC2053-SYNC because the LTC2053-SYNC is sensitive to parasitic capacitance on the CLK pin when left floating. **Clocking the LTC2053-SYNC is accomplished by driving the CLK pin at 8 times the desired sample clock frequency. This completely disables the internal clock. For example, to achieve the nominal LTC2053 sample clock rate of 3kHz, a 24kHz external clock should be applied to the CLK pin of the**

2053syncfd

APPLICATIONS INFORMATION

LTC2053-SYNC. If a square wave is used to drive the CLK pin, a $5\mu\text{s}$ RC time constant should be placed in front of the CLK pin to maintain low offset voltage performance (see Figure 2). This avoids internal and external coupling of the high frequency components of the external clock at the instant the LTC2053-SYNC holds the sampled input.

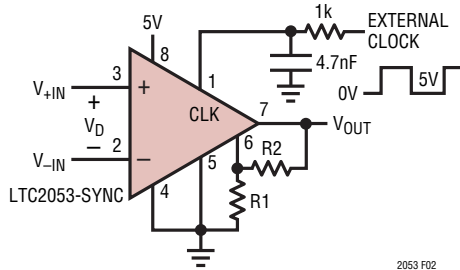


Figure 2. Driving the CLK Input of the LTC2053-SYNC

The LTC2053-SYNC is tested with a sample clock of 3kHz ($f_{\text{CLK}} = 24\text{kHz}$) to the same specifications as the LTC2053. In addition, the LTC2053-SYNC is tested at one-half and 2x this frequency to verify proper operation. The curves in the Typical Performance Characteristics section of this data sheet apply to the LTC2053-SYNC when driving it with a 24kHz clock at Pin 1 ($f_{\text{CLK}} = 24\text{kHz}$, 3kHz sample clock rate). Below are three curves that show the behavior of the LTC2053-SYNC as the clock frequency is varied. The offset is essentially unaffected over a 2:1 increase or decrease of the typical LTC2053 sample clock speed. The bias current is directly proportional to the clock speed. The noise is roughly proportional to the square root of the clock frequency. **For optimum noise and bias current performance, drive the LTC2053-SYNC with a nominal 24kHz external clock (3kHz sample clock).**

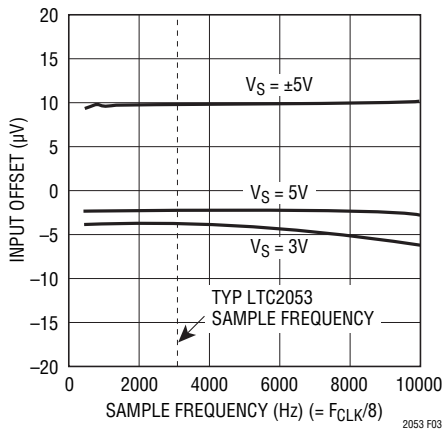


Figure 3. LTC2053-SYNC Input Offset vs Sample Frequency

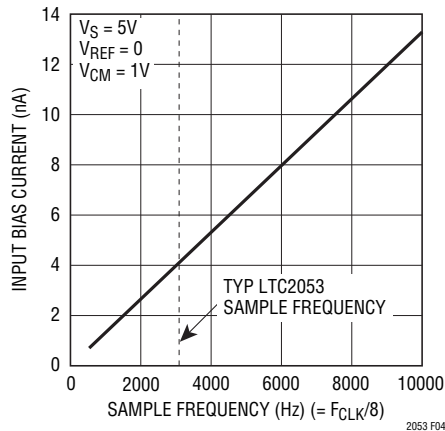


Figure 4. LTC2053-SYNC Average Input Bias Current vs Sample Frequency

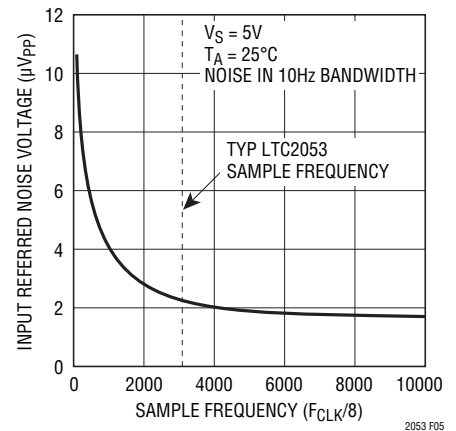
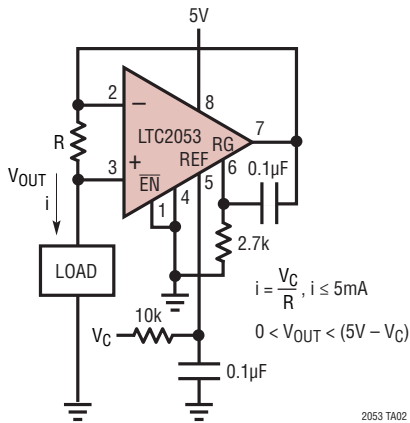


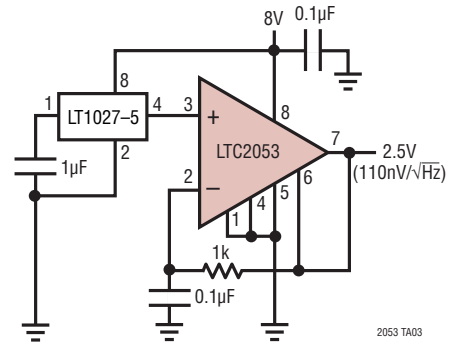
Figure 5. LTC2053-SYNC Input Referred Noise vs Sample Frequency

TYPICAL APPLICATIONS

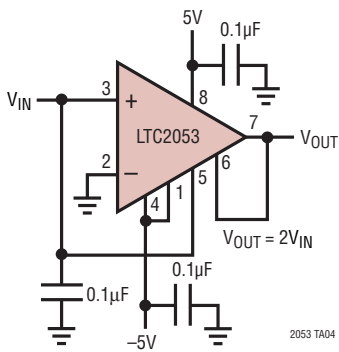
Precision Current Source



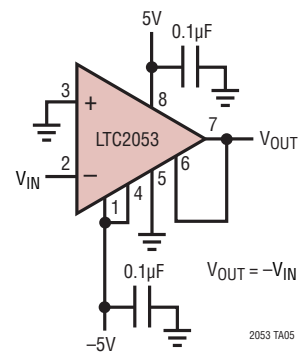
**Precision $\div 2$
(Low Noise 2.5V Reference)**



**Precision Doubler
(General Purpose)**

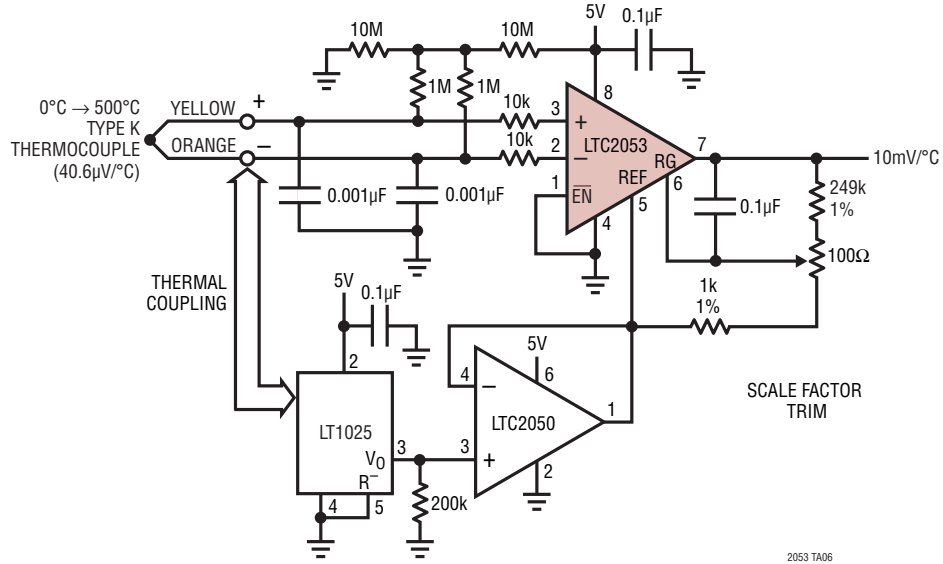


**Precision Inversion
(General Purpose)**

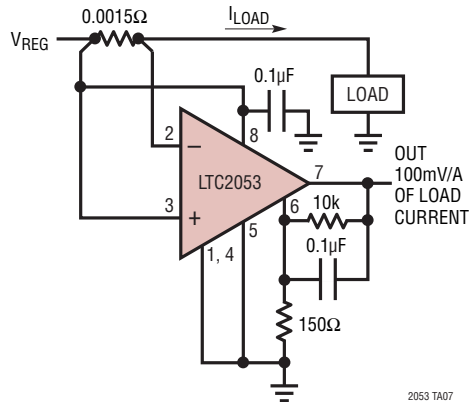


TYPICAL APPLICATIONS

Differential Thermocouple Amplifier



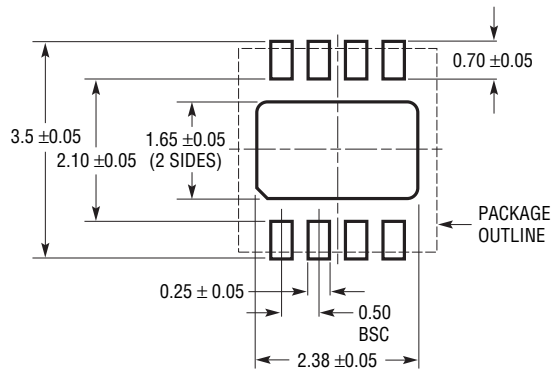
High Side Power Supply Current Sense



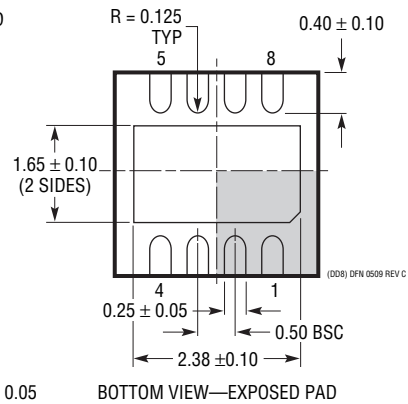
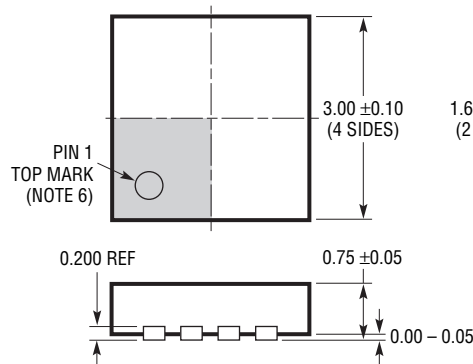
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2053#packaging> for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
 (Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:

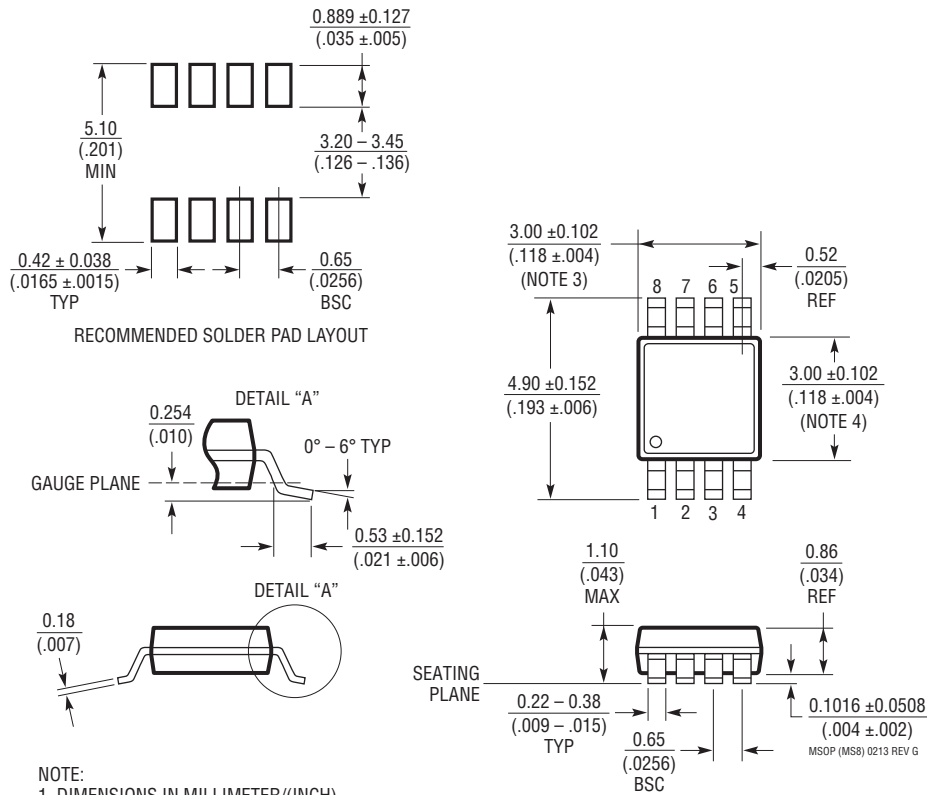
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2053#packaging> for the most recent package drawings.

MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:



1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	7/10	Corrected text in the Absolute Maximum Ratings section	2
		Updated Pin 6 and Pin 7 text in the Pin Functions section	9
		Replaced Figure 1	11
D	12/15	Corrected title for Figure 2	12

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