THE DATASHEET OF

SI32184-A-GMR

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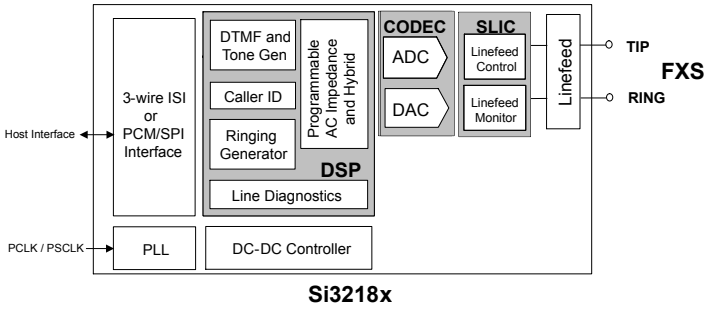
Si3218x Data Sheet

ProSLIC® Single-Channel FXS Solutions

The Si3218x devices are single-channel ProSLIC® products that implement a complete foreign exchange station (FXS) telephony interface solution in accordance with all relevant global specifications. The Si3218x ProSLIC ICs operate from a 3.3 V supply and interface to standard PCM/SPI or 3-wire ISI digital interfaces with 3.3 V or 1.8 V I/O. The Si3218x integrated dc-dc controller automatically generates the optimal battery voltages required for each linestate. Si3218x ICs are available with voltage rating of –106 V. The Si3218x device are available in a 5x6 mm 36-pin QFN package and a 6x6 mm 40-pin QFN Package.

Applications:

- VoIP Gateways and Routers
- xDSL IADs
- Optical Network Terminals/Units (ONT/U)
- Analog Terminal Adapters (ATA)
- Cable eMTA
- Wireless Fixed Terminals (WFT)
- Wireless Local Loop (WLL)
- WiMAX CPE



Functional Block Diagram

KEY FEATURES

- Complete FXS solution in a single 5x6 mm or 6x6 mm package
- Performs all BORSCHT functions
- Ideal for short to medium loops
- Global programmability
- Patented low-power ringing
- Simplified configuration and diagnostics
  - Supported by ProSLIC API
  - Audio diagnostics with loopback
  - Integrated test load
- Ultra low power consumption
- Wideband voice support
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- A-Law/μ-Law companding, linear PCM
- Flexible integrated tracking dc-dc controller supporting patent-pending low-cost capacitive boost configuration
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Pulse metering
- DTMF generation
- DTMF detection (Si32183/5)
- 3.3 V operation
- Support for 1.8 V I/O
- Maximum battery up to –106 V
- Pb-free/RoHS-compliant packaging
- Two digital interface options
  - 3-wire Integrated Serial Interface (ISI) or PCM/SPI interface

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1. Ordering Guide

Table 1.1. Si3218x Ordering Guide

P/N	Description	Package Type[2]	Max V_{BAT}	Temperature
Si32182-A-FM	Wideband FXS, ISI interface, parametric MLT	QFN36	–106 V	0 to 70 °C
Si32182-A-GM	Wideband FXS, ISI interface, parametric MLT	QFN36	–106 V	–40 to 85 °C
Si32183-A-FM	Wideband FXS, ISI interface, parametric MLT, DTMF detection	QFN36	–106 V	0 to 70 °C
Si32183-A-GM	Wideband FXS, ISI interface, parametric MLT, DTMF detection	QFN36	–106 V	–40 to 85 °C
Si32184-A-FM	Wideband FXS, PCM interface, parametric MLT	QFN40	–106 V	0 to 70 °C
Si32184-A-GM	Wideband FXS, PCM interface, parametric MLT	QFN40	–106 V	–40 to 85 °C
Si32185-A-FM	Wideband FXS, PCM interface, parametric MLT, DTMF detection	QFN40	–106 V	0 to 70 °C
Si32185-A-GM	Wideband FXS, PCM interface, parametric MLT, DTMF detection	QFN40	–106 V	–40 to 85 °C

Note:

1. Adding the suffix "R" to the part number (e.g. Si3218x-A-FMR) denotes tape and reel.
2. QFN - Quad-Flat No-leads.

Table 1.2. Ordering GuideSi3218x Evaluation Kits

Part Number	Description	V_{BAT} Max
Si32183ACB10SL0EVB	ISI Wideband FXS with DTMF detection low-cost capacitive boost dc-dc converter EVB	–100 V
Si32185ACB10SL0EVB	PCM interface, wideband FXS with DTMF detection low-cost capacitive boost dc-dc converter EVB	–100 V

2. Functional Description

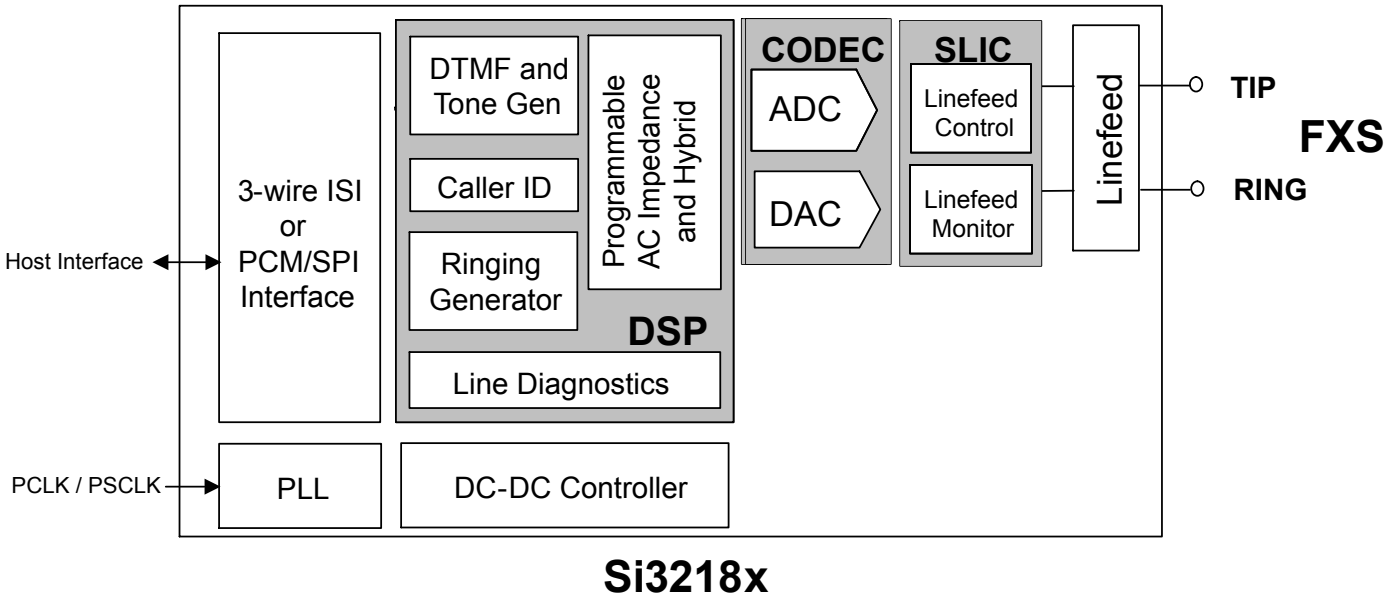


Figure 2.1. Si3218x Functional Block Diagram

The Si3218x series provides all SLIC, codec, DTMF detection, and signal generation functions needed for one complete analog telephone interface. The Si3218x performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop and self-test capabilities.

The Si3218x supports wideband audio (150 Hz–6.8 kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50 Hz–7 kHz). The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality.

The Si3218x series supports a standard PCM/SPI digital interface, or a 3-wire ISI digital interface.

The Si3218x incorporates a programmable dc-dc converter controller that reacts to line conditions to provide the optimal battery voltage required for each line-state. Si3218x ICs are available with voltage ratings of –106 V.

Programmable on-hook voltage, programmable off-hook loop current, reverse polarity operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC.

The Si3218x supports low power ringing with or without a programmable dc offset. The available voltage offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

3. Electrical Specifications

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, High Voltage Die	T_{JHV}	Continuous	—	—	Internally Limited	°C
Silicon Junction Temperature, Low Voltage Die	T_{JLV}	Continuous	—	—	125	°C
Supply Voltage	V_{DDD}		3.13	3.3	3.47	V
Battery Voltage[2]	V_{BAT}		–106	—	–15	V
IO Supply Voltage	V_{DDIO}		1.71	—	3.47	V

Note:

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Minimum and maximum battery voltage limits are dependent upon loop conditions and dc-dc converter configuration.

Table 3.2. Power Supply Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Reset	I_{DD}	V_T and V_R = Hi-Z , RSTB = 0	—	6.14	—	mA
	I_{VBAT}		—	0	—	mA
Supply Currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z	—	20.2	—	mA
	I_{VBAT}		—	0.19	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V,	—	11.06	—	mA
	I_{VBAT}	Automatic Power Save Mode Enabled	—	0.25	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V,	—	30.33	—	mA
	I_{VBAT}	Automatic Power Save Mode Disabled	—	1.51	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V	—	11.02	—	mA
	I_{VBAT}	V_R or V_T = Hi-Z, Automatic Power Save Mode Enabled	—	0.25	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V	—	29.59	—	mA
	I_{VBAT}	V_R or V_T = Hi-Z, Automatic Power Save Mode Disabled	—	0.86	—	mA
Supply Currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} = 48 V	—	43.79	—	mA
	I_{VBAT}		—	2.28	—	mA
Supply Currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 20 mA, R_{LOAD} = 200 Ω	—	44.56	—	mA
	I_{VBAT}		—	21.53	—	mA
Supply Currents: Ringing	I_{DD}	V_{TR} = 55 V_{RMS} + 0 V_{DC},	—	33.75	—	mA
	I_{VBAT}	low power ringing, sinusoidal, f = 20 Hz, R_{LOAD} = 5 REN = 1400 Ω	—	33.21	—	mA

Note:

1. All specifications are for a tracking low-cost capacitive boost dc-dc converter at 25 °C. VDDD = 3.3 V; VDC = 12 V.
2. I_{DD} includes I_{DDIO}.

Table 3.3. AC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Compression	2-Wire - PCM	See Figure 3.6 Overload Compression Performance on page 17.	—	—	
Single Frequency Distortion	2-Wire - PCM or PCM - 2-Wire: 200 Hz to 3.4 kHz	—	—	–40	dB
	PCM - 2-Wire - PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	–63	dB
Signal-to-(Noise + Distortion) Ratio[1]	200 Hz to 3.4 kHz transmit or receive path Active off-hook, and OHT, any Z_T	See Figure 3.5 Transmit and Receive Path SNDR on page 17.	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[1]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[1]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Frequency	0 dBm 0 [5]	See Figure 3.7 Receive Path Frequency Response on page 18 and Figure 3.8 Transmit Path Frequency Response on page 19.			
Group Delay vs. Frequency		See Figure 3.9 Transmit Group Delay Distortion on page 20 and Figure 3.10 Receive Group Delay Distortion on page 20.			
Gain Tracking[2]	1014 Hz sine wave, reference level –10 dBm, Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[3]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[3]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[4]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP

Parameter	Test Condition	Min	Typ	Max	Unit
PSRR from V_{DDD}, V_{DDIO} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	—	60	—	dB
	1 kHz to 3.4 kHz	—	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	—	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Note:

1. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
2. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DD} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
5. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 3.4. Linefeed Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy-Ground Start (TIP Open)	V_{OHTO}	$I_{RING} < I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance-Ground Start (TIP Open)	R_{ROTO}	$I_{RING} < I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance-Ground Start (TIP Open)	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80 mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 0 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude	$V_{RINGING}$	Open circuit, V_{BAT} = –106 V	–104	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	50 V_{RMS}, 0 V_{OFFSET}, 0–5 REN	—	1	—	%
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Loop Voltage Sense Accuracy		$V_{TIP} – V_{RING}$ = 48 V	—	2	4	%
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, Loop Current = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%

Table 3.5. Digital I/O Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	SCLK, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	0.7 x V_{DDIO}	—	V_{DDIO}	V
Low-Level Input Voltage	V_{IL}	SCLK, PSCLK, ISI_MOSI, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	—	—	0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, INTB: I_O = –4 mA	V_{DDIO} – 0.6	—	—	V
Low-Level Output Voltage	V_{OL}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, ISI_MISO, INTB: I_O = 4 mA	—	—	0.4	V
SPI_MOSI_THRU and RSTB Internal Pullup Current			33	42	65	µA
Input Leakage Current	I_L		—	—	10	µA

Table 3.6. Charge Pump Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (DCDRV, DCFF)	V_{CP}		2 x V_{DD} – 1	—	2 x V_{DD}	V
Output Current	I_{CP}		—	—	3[1]	mA

Note:
1. Peak drive current capability is >60 mA.

Table 3.7. Switching Characteristics — General Inputs

Parameter	Symbol	Min	Typ	Max	Unit
RSTB Pulse Width (PCM/SPI or ISI Interface)	t_{RST}	200	—	—	µs
RSTB High to First SPI Transfer start (PCM/SPI Interface) or First Register/RAM Access (ISI Interface)	t_{RCS}	5	—	—	ms

Note:
1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} - 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

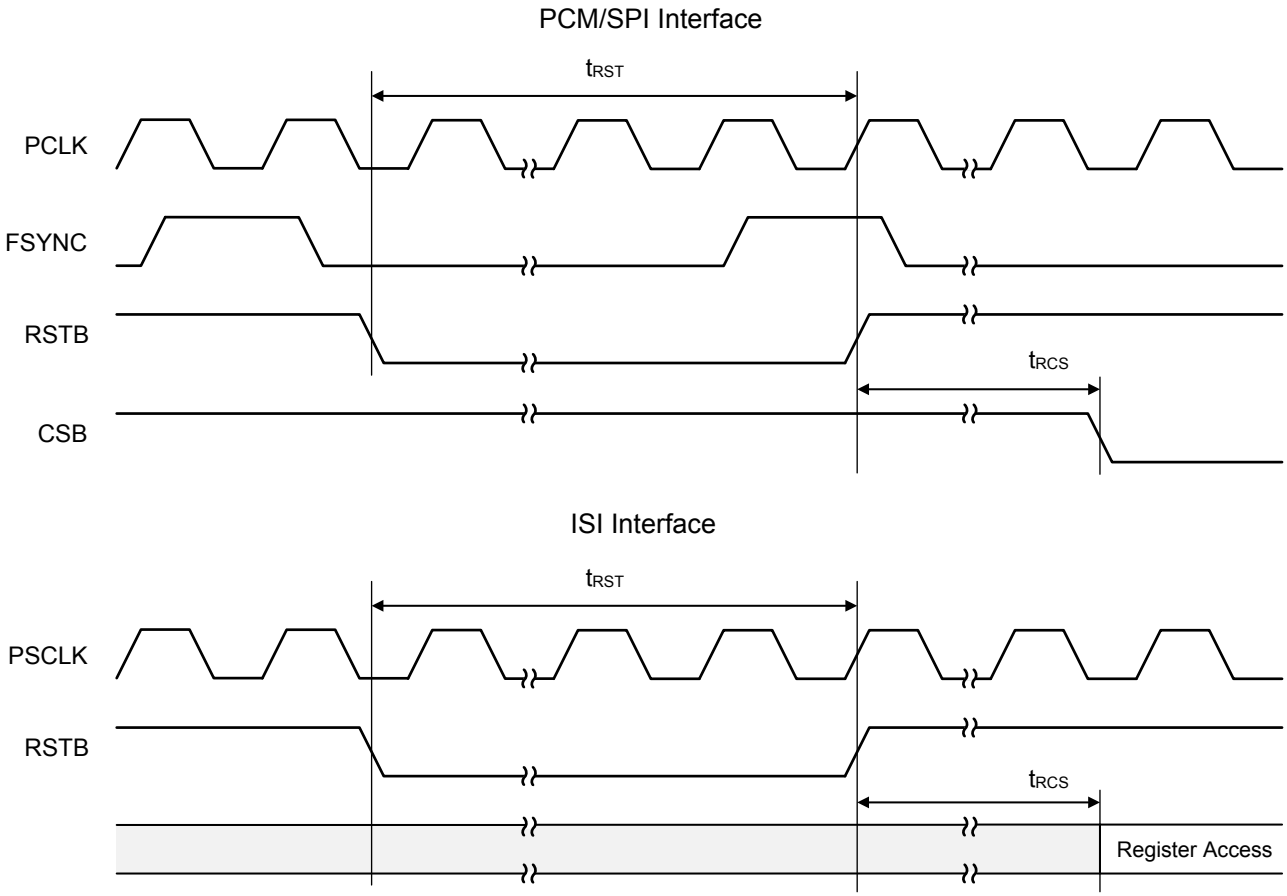


Figure 3.1. Si3218x Reset Timing Diagrams

Table 3.8. Switching Characteristics — SPI

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		83	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SPI_MISO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SPI_MISO Transition	t_{d2}		—	—	20	ns
Delay Time, CSB Rise to SPI_MISO Tri-state	t_{d3}		—	—	20	ns
Setup Time, CSB to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, CSB to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SPI_MOSI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SPI_MOSI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SPI_MOSI to SPI_MOSI_THRU Propagation Delay	t_{d4}		—	4	10	ns

Note:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDIO} – 0.4$ V, $V_{IL} = 0.4$ V.
2. Characteristics for outputs specified with $C_L = 20$ pF.

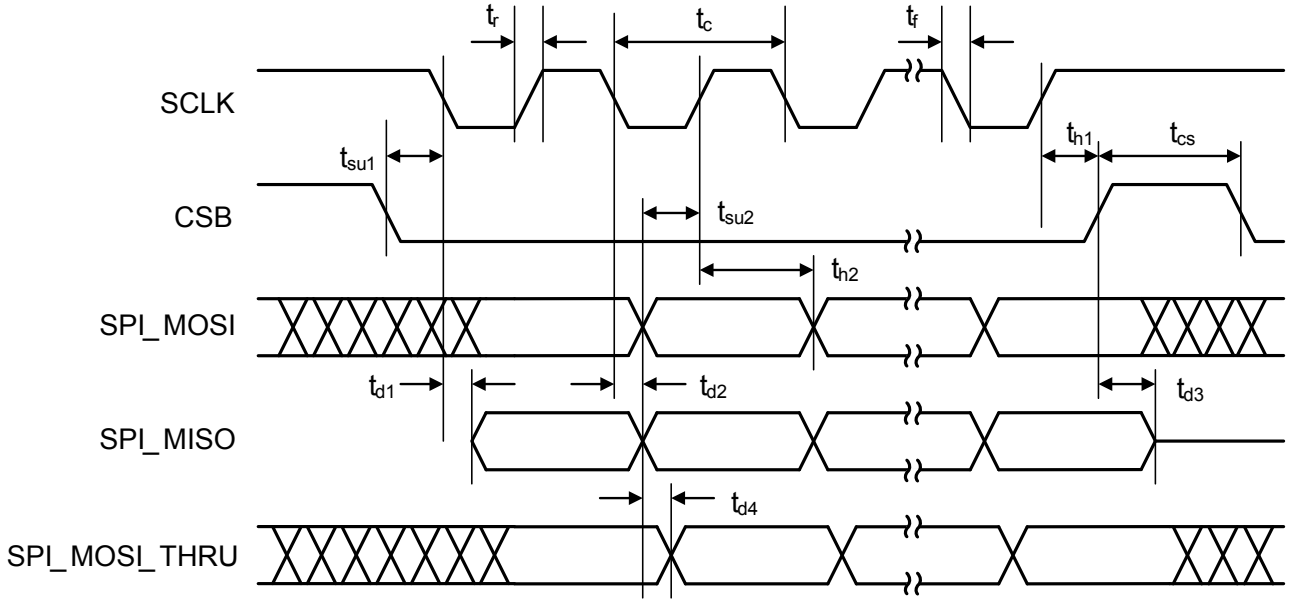


Figure 3.2. SPI Timing Diagram

Table 3.9. Switching Characteristics — PCM Highway Interface

Parameter	Symbol	Test Condition	Min[1]	Typ[1]	Max[1]	Unit
PCLK Period	t_p		122	—	1953	ns
PCLK Jitter Tolerance	$t_{jitter(FXS)}$		—	—	8	ns_{RMS}
Valid PCLK Inputs[2]			—	256	—	kHz
			—	512	—	kHz
			—	768	—	kHz
			—	1.024	—	MHz
			—	1.536	—	MHz
			—	1.544	—	MHz
			—	2.048	—	MHz
			—	4.096	—	MHz
				8.192		MHz
FSYNC Period[3]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance[4]	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to PCM_MISO Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to PCM_MISO Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to PCM_MISO Tristate[6]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, PCM_MOSI to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCM_MOSI to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs-t_p	

Note:

1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} – $V_{I/O}$ – 0.4 V, V_{IL} = 0.4 V.
2. A constant PCLK and FSYNC are required.
3. FSYNC source is assumed to be 8 kHz under all operating conditions.
4. FSYNC Jitter Tolerance relative to PCLK.
5. Characteristics for outputs specified with C_L = 20 pF.
6. Specification applies to PCLK fall to PCM_MISO tristate when that mode is selected.

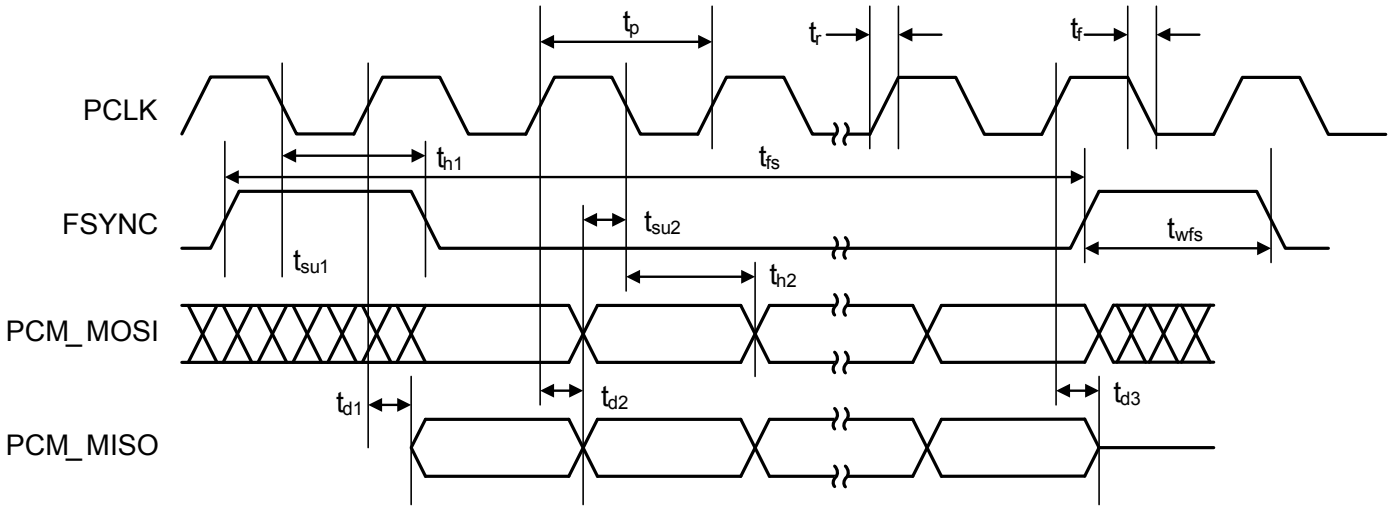


Figure 3.3. PCM Highway Interface Timing Diagram

Table 3.10. Switching Characteristics — ISI

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, ISI_MOSI to PSCLK Fall	t_{su}	7.5	—	—	ns
Hold Time, ISI_MOSI to PSCLK Fall	t_h	5	—	—	ns
Delay Time, PSCLK Rise to ISI_MISO	t_d	—	—	16	ns
PSCLK Period	t_p	—	40.69	—	ns
PSCLK Duty Cycle		40	50	60	%

Note:
1. Timing should be guaranteed by ISI-enabled host SoC.

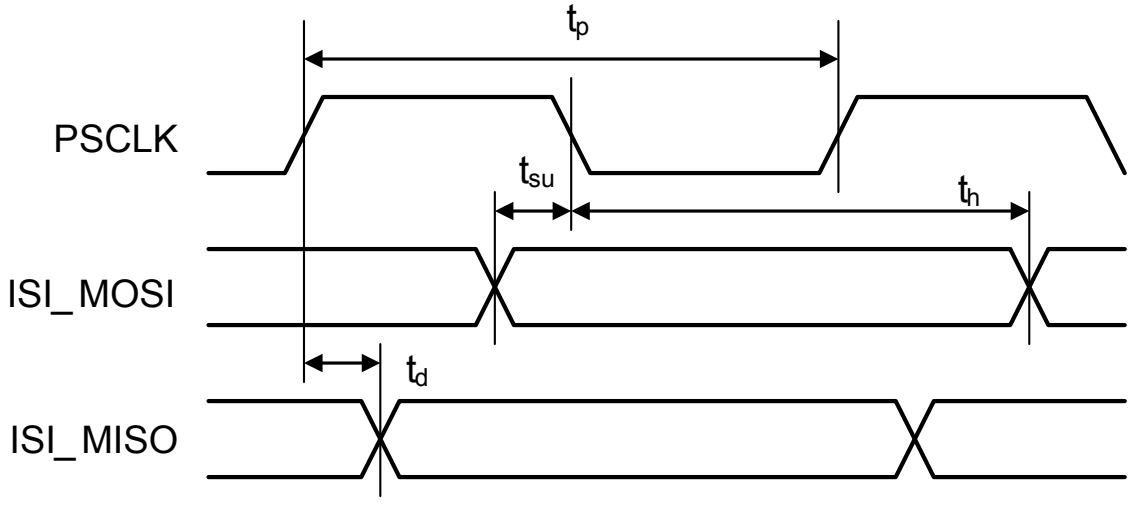


Figure 3.4. ISI Timing Diagram

Table 3.11. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
Thermal Resistance, Typical QFN-36[1]	θ_{JA}		26.8	°C/W
	θ_{JB}		11.4	°C/W
	θ_{JC}		17.5	°C/W
Thermal Resistance, Typical QFN-40 [1]	θ_{JA}		33.8	°C/W
	θ_{JB}		17.3	°C/W
	θ_{JC}		20.5	°C/W
Maximum Junction Temperature, (High Voltage Die)[3]	T_{JHV}	Continuous	Internally Limited	°C
Maximum Junction Temperature (Low Voltage Die)[2]	T_{JLV}		125	°C

Note:

1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are empirical measurements taken from EVBs.
2. Operation of the Si3218x above 125 °C junction temperature may degrade device reliability.
3. Si3218x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold is normally set to 145 °C; when in the ringing state the thermal shutdown is set to 200 °C.

Table 3.12. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{DDIO}	–0.5 to 4.0	V
Digital Input Voltage	V_{IND}	–0.3 to 3.6	V
Battery Supply Voltage	V_{BAT}	+0.4 to –112	V
Tip or Ring Voltage	V_{TIP}, V_{RING}	V_{BAT} – 0.4	V
TIP, RING Current	I_{TIP}, I_{RING}	±100	mA

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.

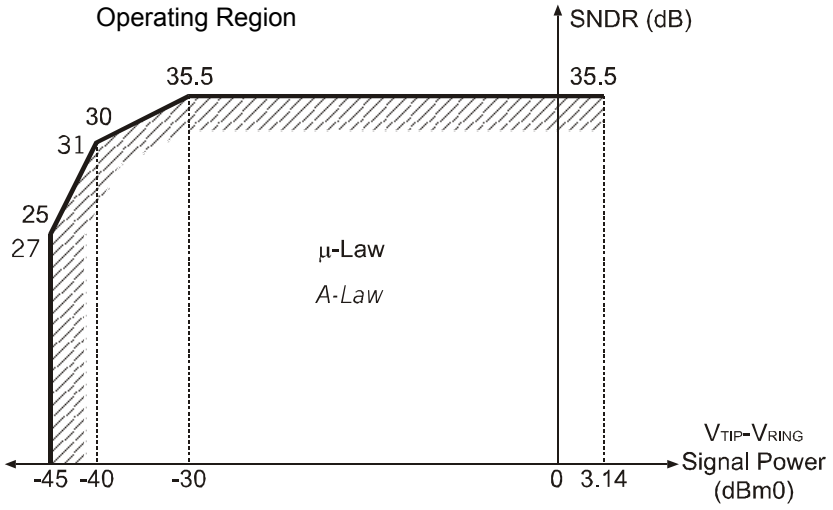


Figure 3.5. Transmit and Receive Path SNDR

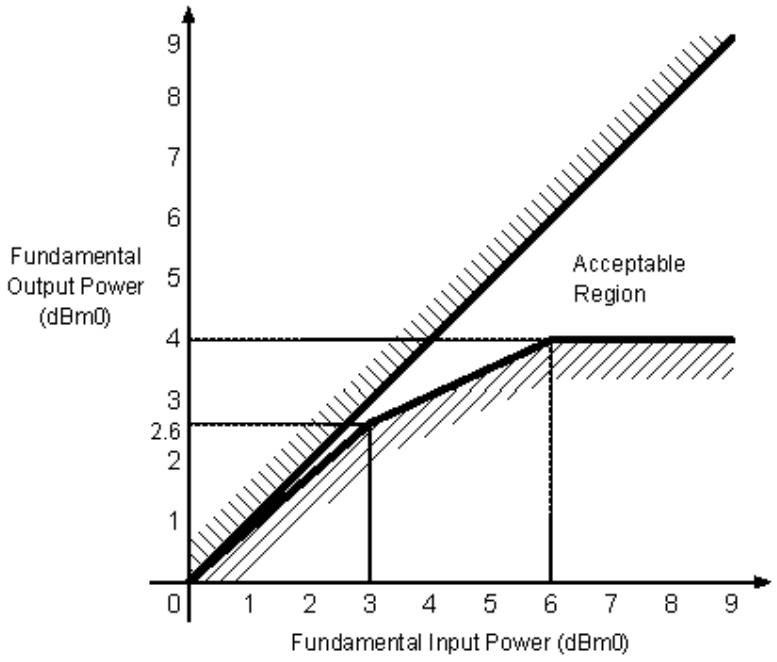


Figure 3.6. Overload Compression Performance

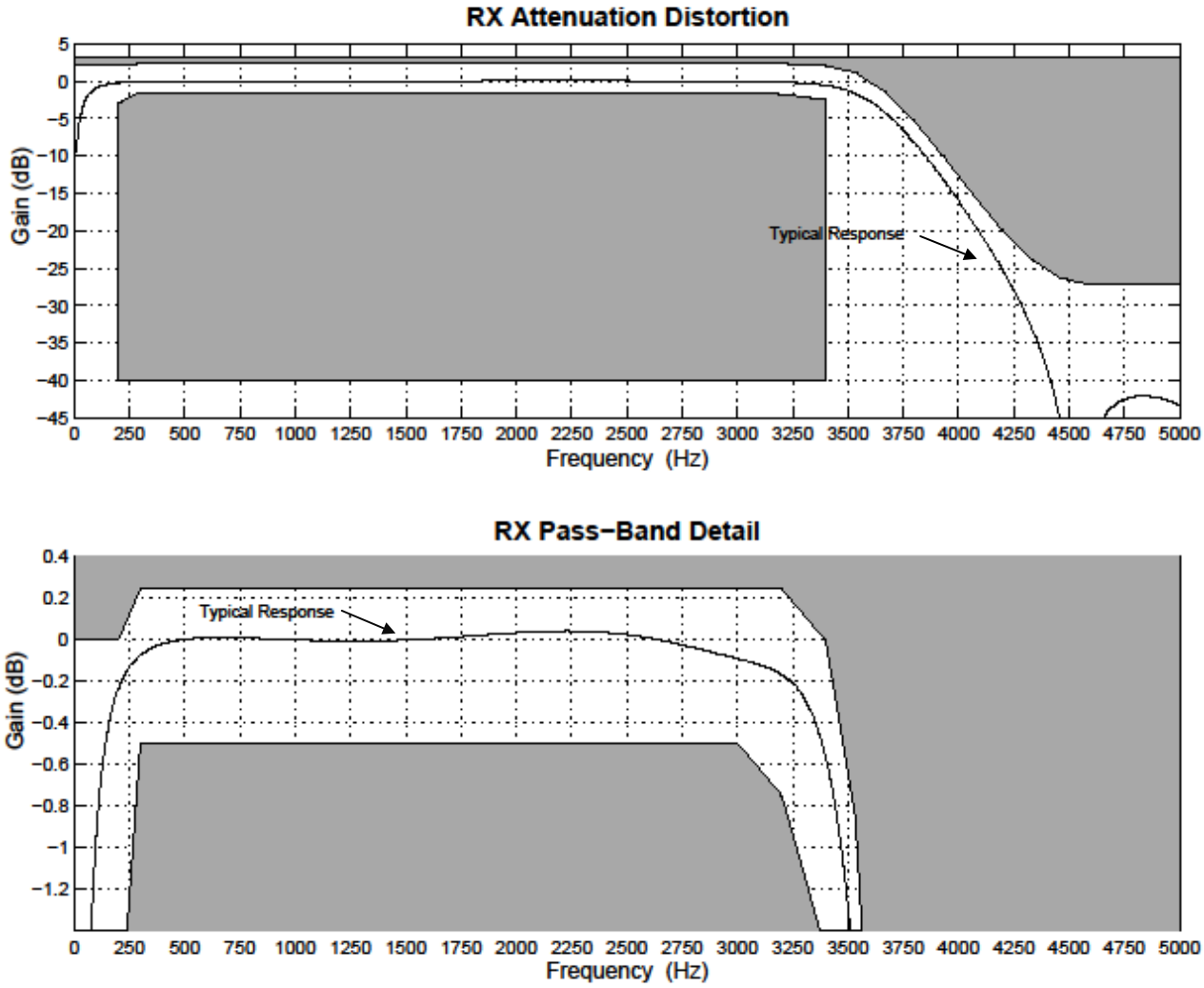


Figure 3.7. Receive Path Frequency Response

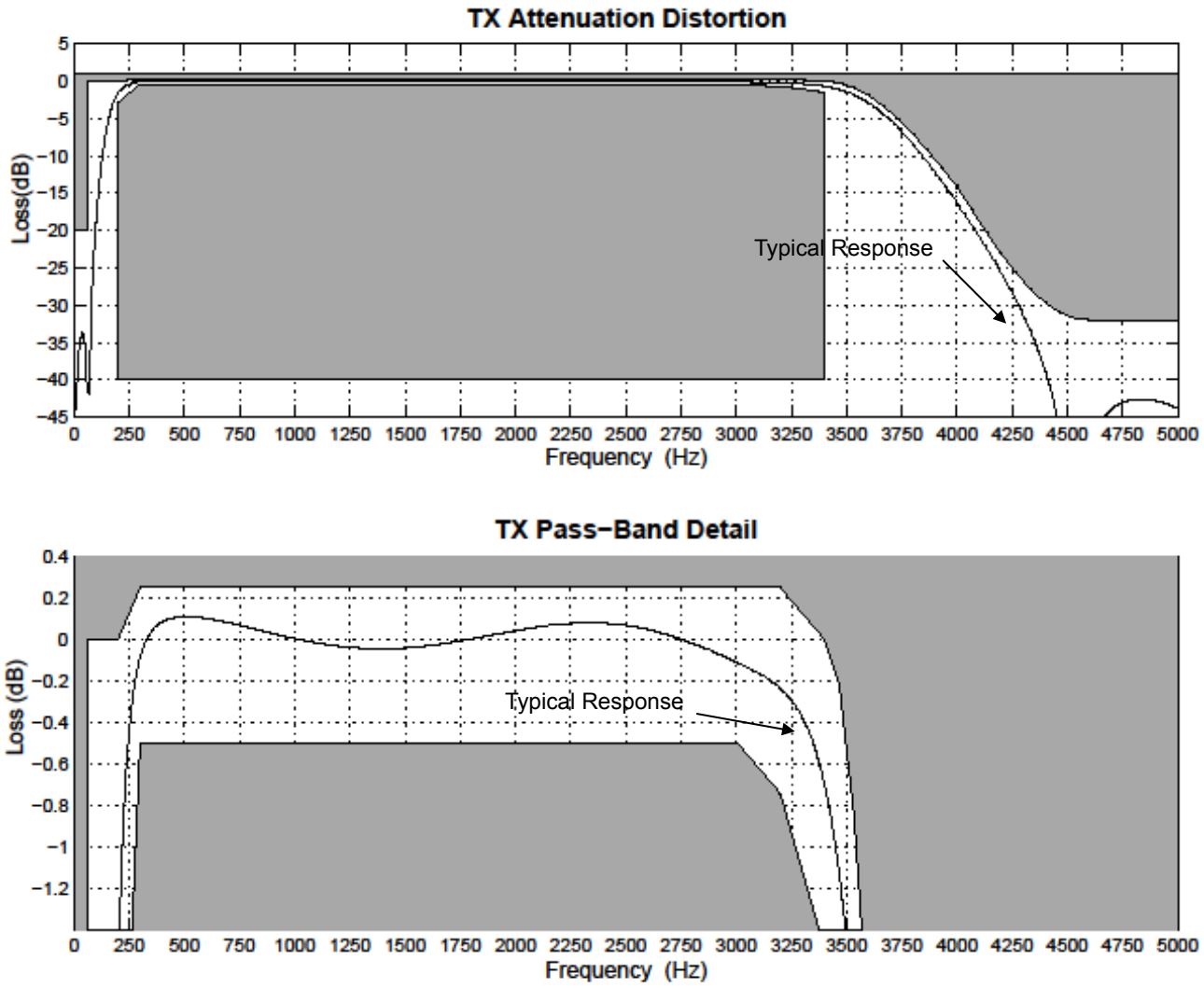


Figure 3.8. Transmit Path Frequency Response

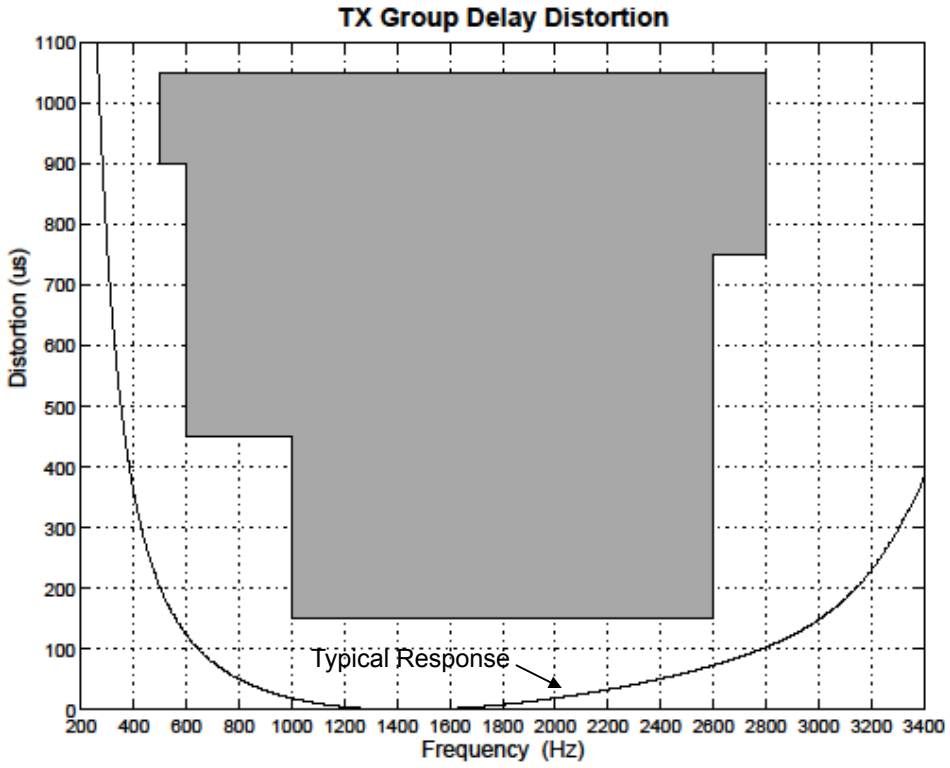


Figure 3.9. Transmit Group Delay Distortion

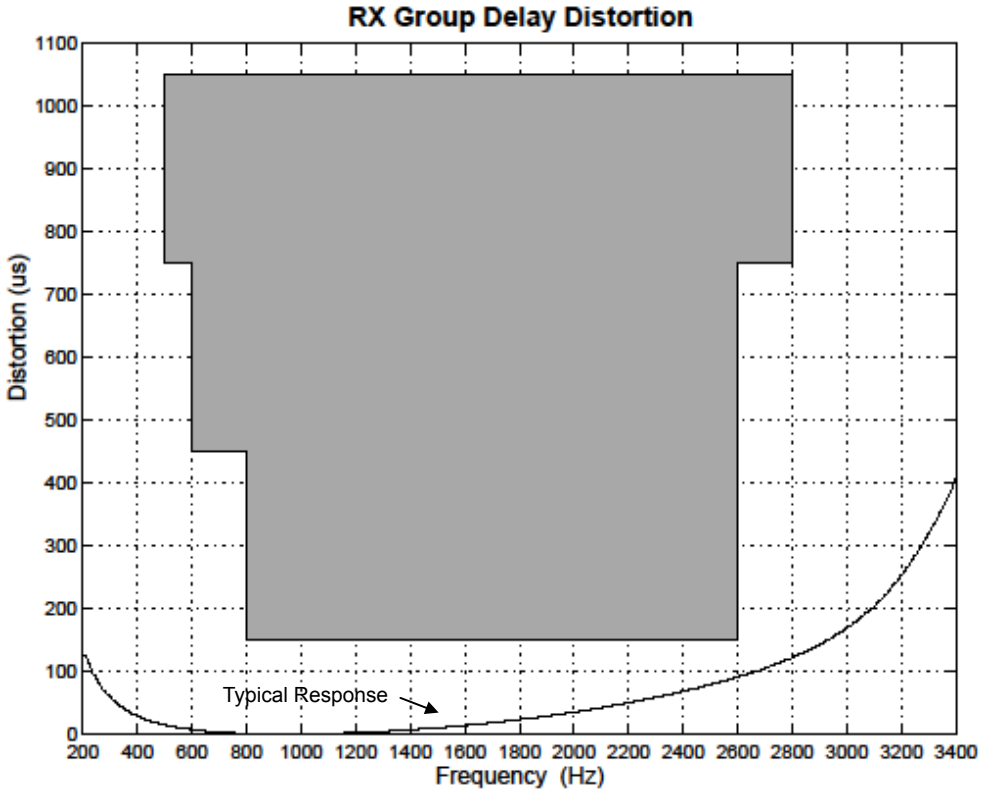


Figure 3.10. Receive Group Delay Distortion

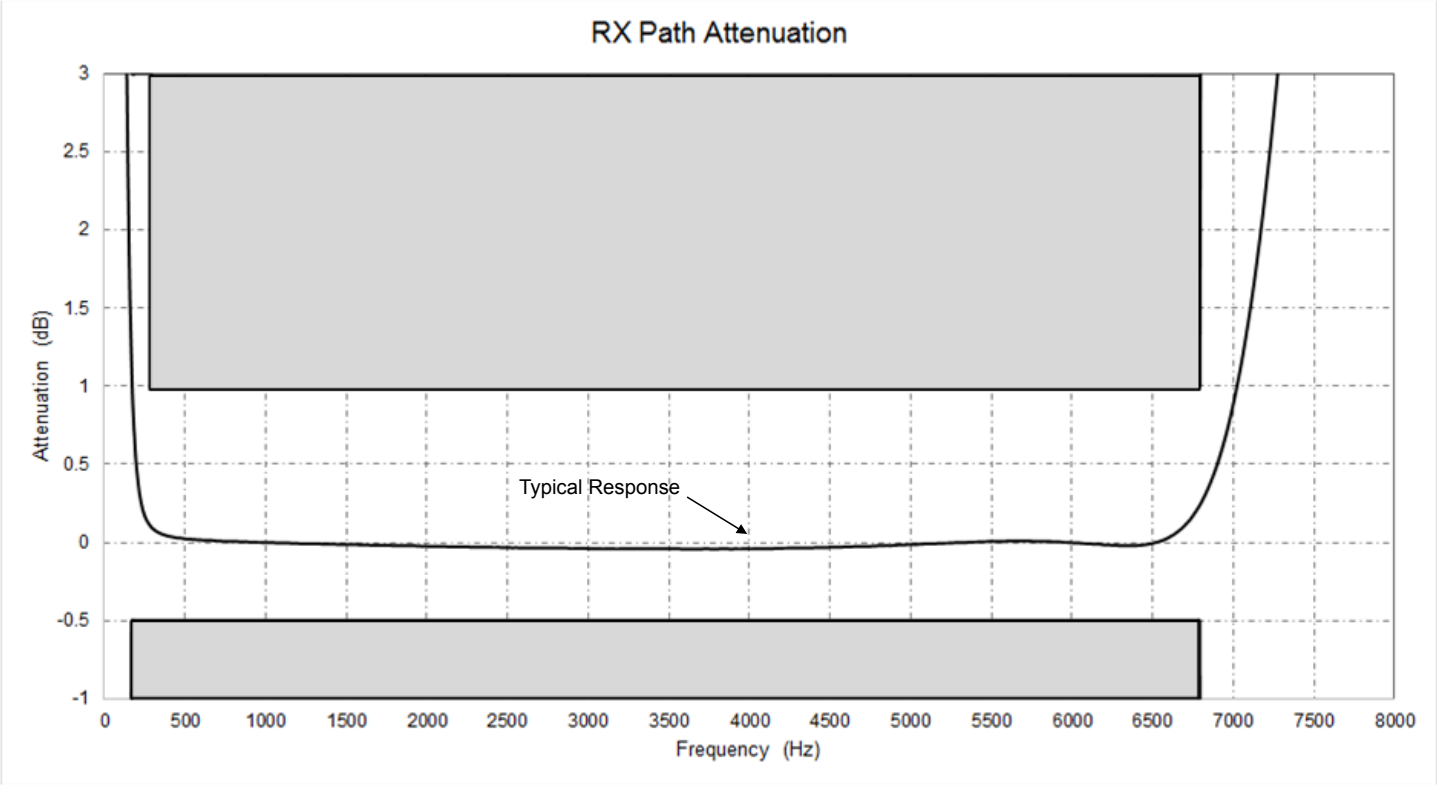


Figure 3.11. Receive Wideband Frequency Response

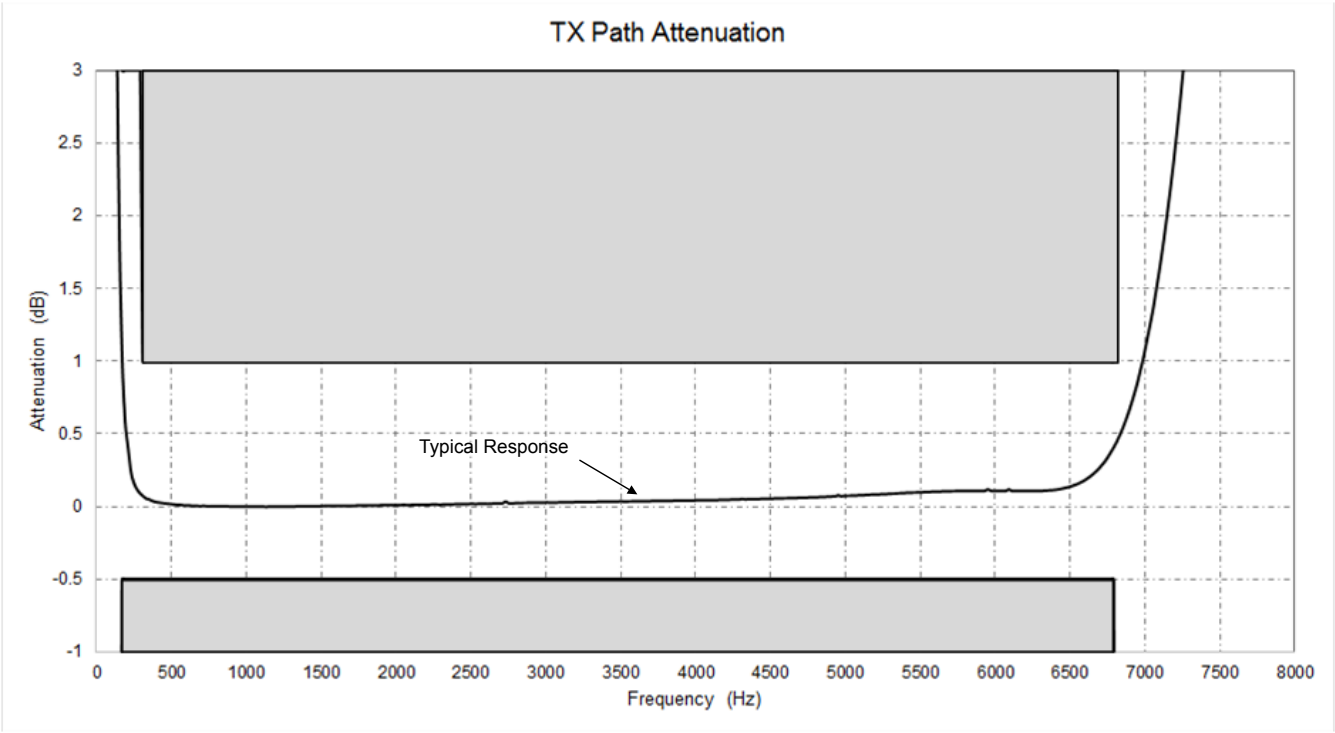


Figure 3.12. Transmit Wideband Frequency Response

4. FXS Features

4.1 DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in the figure below. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

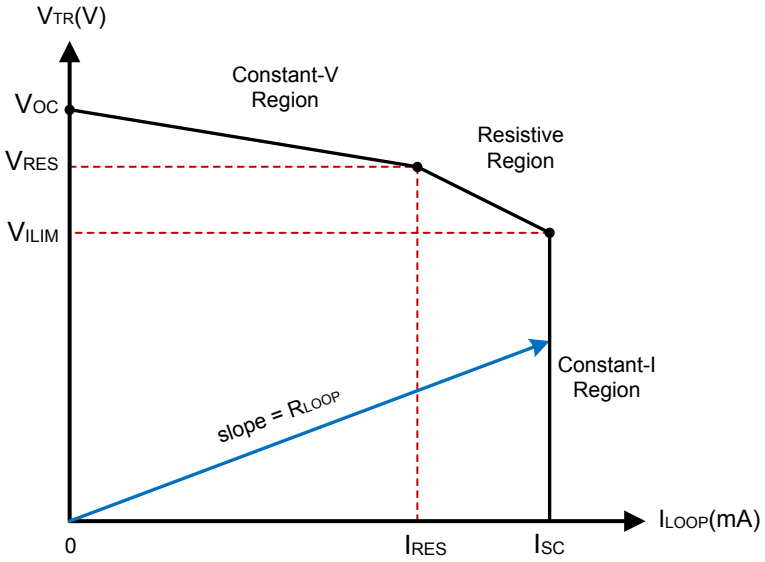


Figure 4.1. Dual ProSLIC DC Feed Characteristics

4.2 Linefeed Operation States

The linefeed interface includes eight different register-programmable operating states as listed in Table 4.1 Linefeed Operating States on page 23. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

4.3 Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip Monitor ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (VTIP–VRING), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

4.4 Power Monitoring and Power Fault Detection

The Si3218x line monitoring functions are used to continuously protect against excessive power conditions. The Si3218x contains an on-chip, analog sensing diode that provides real-time temperature data and turns off the device when a preset threshold is exceeded.

If the Si3218x detects a fault condition or overpower condition, it automatically sets that device to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended since it is used to protect the Si3218x HVIC under excessive power conditions.The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

4.5 Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold, TJmax, of 145 °C or 200 °C, the device has the ability to shut itself down to a low-power state without user intervention.

Table 4.1. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (≥400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (≥400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

4.6 Loop Closure Detection

The Si3218x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.7 Ground Key Detection

The Si3218x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.8 Ringing Generation

The Si3218x supports the patented Low-Power Ringing (LPR) method exclusively, which when used with a tracking battery scheme, maximizes the ringing power transfered to the load and reduces overall power consumption. Ringing is fully programmable including frequency, amplitude, dc offset, wave shape and crest factor. The Si3218x also supports automatic ring cadencing and ringtrip detection (AC and DC).

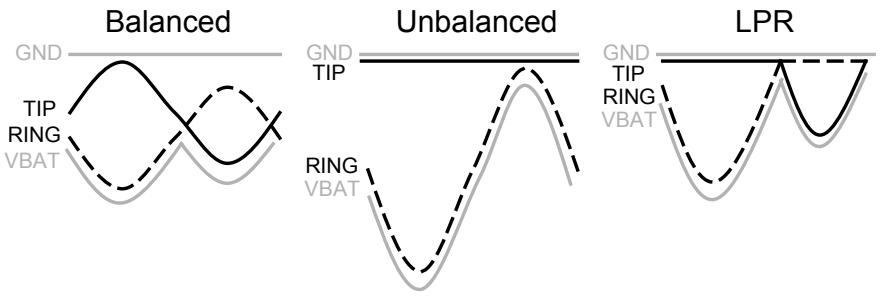


Figure 4.2. Ringing Mode

4.9 Polarity Reversal

The Si3218x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

4.10 Two-wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3218x to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

4.11 Transhybrid Balance Figure

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

4.12 Tone Generators

The Si3218x includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

4.13 DTMF Detection (Si32183/5)

In DTMF, two tones generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits.

4.14 Pulse Metering

The pulse metering system for the Si3218x is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 0.5 VRMS at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thuscreating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

4.15 DC-DC Controller

The Si3218x-C devices integrate a dc-dc controller to control an external tracking dc-dc converter which generates the high voltage supply (VBAT) to the SLIC. The tracking VBAT voltage generated from a single positive dc input is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms.

The dc-dc controller output DCDRV is driven by an internal charge pump which allows it to connect directly to the gate of the MOSFET switch of the dc-dc converter. This eliminates the need for the MOSFET predrive circuit that is typically required when other SLICs are used with a MOSFET with VTH greater than VDD. See Table 3.7 Switching Characteristics — General Inputs on page 11.

4.16 Wideband Audio

The Si3218x supports wideband audio (150 Hz–6.8 kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50 Hz–7 kHz). The wideband provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received at an effective 16 kHz rate by using multiple timeslots in a single 8 kHz frame.

4.17 Test Facilities

The Si3218x supports a rich set of metallic loop tests to diagnose external faults, as well as a set of inward self-tests to support diagnostics of the Si3218x-based voice port. Implementation of metallic loop tests required the ProSLIC® MLT API, while the inward self-tests are included in the standard ProSLIC® API.

Supported Metallic Loop Tests include:

Voltages	Measures AC and DC voltages from T-R, T-G and R-G.
Receiver Off-hook	Discriminates between resistive fault and off-hook terminating device.
REN	Measures Ringer Equivalence Number (REN).
REN Capacitance	Measures T-R capacitance of on-hook load.
Capacitance	Measures 3-Terminal Capacitance.
Resistance	Measures resistance from T-R, T-G or R-G.

Supported Inward Self-Tests include:

PCM Loopback	Configures Si3218x for 8 or 16-bit PCM loopback.
DC Feed	Verify DC Feed I/V and loop closure using integrated test load.
Ringing and Ringtrip	Verify ringing voltage (AC and DC). Optional ringtrip check to support system level signaling verification.
Battery	Verify VBAT.
Audio Gain	Measure gain of RX (host to line) and TX (line to host) paths without using an external load, test equipment, or requiring the host to provide audio samples.

In addition to these specific test suites, the user is free to implement a variety of general test facilities including:

Monitor ADC	Provides TIP/RING voltages (inside and outside overcurrent protection), TIP/RING currents and VBAT voltage.
Audio Diagnostic Filters	3 cascaded 2nd order Biquad filters with peak hold and averaging capabilities.
Loopback Modes	Digital and analog loopback modes to isolate portions of the audio path.
Tone Generators	The dual tone generators may be used as general purpose signal generators for test purposes.

5. System Interfaces

5.1 SPI Control Interface

The controller interface to the Si3218x is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CSB), serial data input (SPI_MOSI), and serial data output (SPI_MISO). In addition, the ProSLIC devices feature a serial data through output (SPI_MOSI_THRU) to support operation of up to 32 channels using a single chip select line. The FXS port occupies one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

5.2 PCM Interface and Companding

The PCM interface supported on select Si3218x devices is a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 4 to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 256 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Si3218x supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

5.3 Integrated Serial Interface

The ISI interface supported on select Si3218x devices is a three-wire proprietary interface which serializes SPI and PCM communications and interrupts, reducing the SoC interface from nine wires to three (PSCLK, ISI_MISO, ISI_MOSI). SPI communications and PCM data transfers are embedded in the serial data. The host side of the ISI is integrated onto selected SoCs from several vendors.

ISI is a point to point interface; therefore, it is not possible to daisy-chain more than one ISI ProSLIC device.

Both µ-255 Law (µ-Law) and A-law companding formats are supported in addition to 16-bit linear data mode with no companding.

5.4 Input/Output Voltage Selection

The digital host interface I/O (PCM/SPI or ISI) on the Si3218x may directly interface to 1.8 V to 3.3 V devices. The I/O voltage selection is made by supplying the VDDIO pin with the appropriate I/O supply voltage.

To avoid power supply sequencing issues, VDDIO should be connected to the same supply as VDD in 3.3 V interface designs. Other voltages between 1.8 V and 3.3 V can also be used for VDDIO (for example 2.5 V), but steps must be taken to ensure that the VDDIO supply comes up after the VDD supply if VDDIO is not connected to VDD or VDDREG.

6. Pin Descriptions

6.1 Pin Descriptions: 36 Pin QFN (Si32182/3)

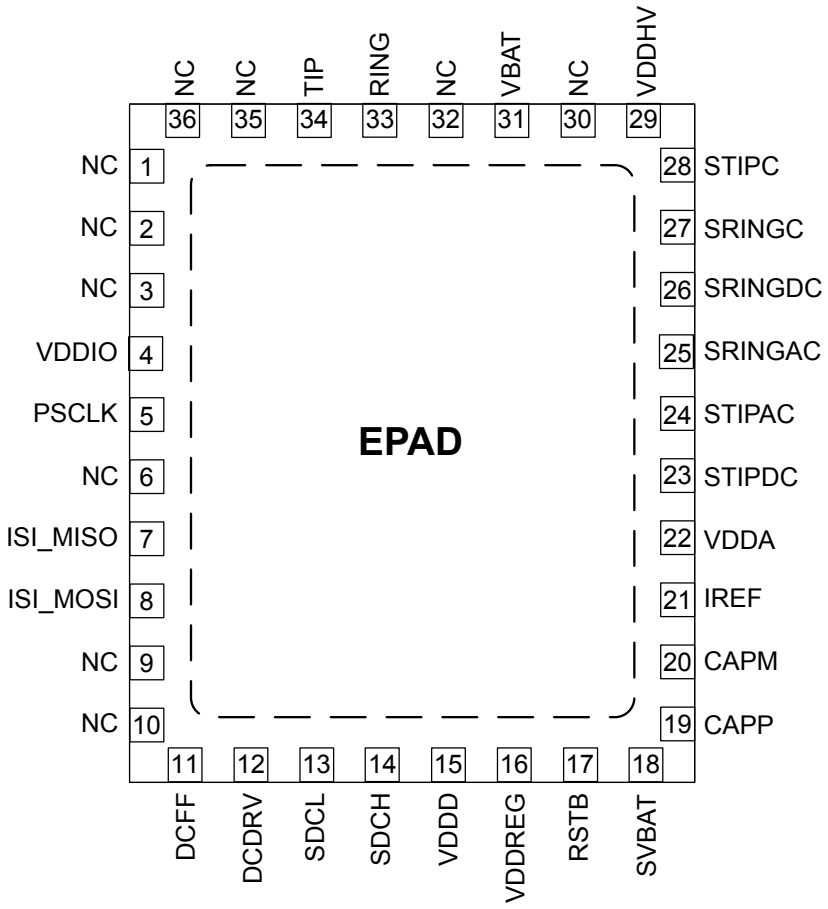


Table 6.1. Si32182/3 Pin Descriptions

Pin #	Pin Name	Description
1	NC	**No connection.** This pin should be left unconnected.
2	NC	**No connection.** This pin should be left unconnected.
3	NC	**No connection.** This pin should be left unconnected.
4	VDDIO	**Digital IO Supply Voltage.** 3.3 V or 1.8 V digital power supply for internal circuitry.
5	PSCLK	**ISI Bus Clock Input.** Clock input for ISI bus timing.

Pin #	Pin Name	Description
6	NC	**No connection.** This pin should be left unconnected.
7	ISI_MISO	**Transmit ISI Output.** ISI Master Input, Slave Output. Output data to ISI bus.
8	ISI_MOSI	**Transmit ISI Input.** ISI Master Output, Slave input. Input data from ISI bus.
9	NC	**No connection.** This pin should be left unconnected.
10	NC	**No connection.** This pin should be left unconnected.
11	DCFF	**DC-DC Charge Pump Output.**
12	DCDRV	**DC Drive.** DC-DC converter control signal output which drives external transistor.
13	SDCL	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
14	SDCH	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
15	VDDD	**IC Voltage Supply.** 3.3 V digital power supply for internal circuitry.
16	VDDREG	**Regulated Core Power Supply.**
17	RSTB	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
18	SVBAT	**VBAT Sense.** Input used to sense voltage on DC-DC converter output voltage lead.
19	CAPP	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
20	CAPM	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
21	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
22	VDDA	**Analog Supply Voltage.** Analog 3.3 V power supply for internal analog circuitry.
23	STIPDC	**TIP DC Sense.** Analog DC input used to sense voltage on TIP lead.

Pin #	Pin Name	Description
24	STIPAC	**TIP AC Sense.** Analog AC input used to sense voltage on TIP lead.
25	SRINGAC	**RING AC Sense.** Analog AC input used to sense voltage on RING lead.
26	SRINGDC	**RING DC Sense.** Analog DC input used to sense voltage on RING lead.
27	SRINGC	**RING Coarse Sense Input.** Voltage sensing outside protection circuit.
28	STIPC	**TIP Coarse Sense Input.** Voltage sensing outside protection circuit.
29	VDDHV	**Analog Supply Voltage.** Analog 3.3 V power supply for internal analog circuitry.
30	NC	**No connection.** This pin should be left unconnected.
31	VBAT	**Battery Voltage Supply.** Connect to battery supply from DC-DC converter.
32	NC	**No connection.** This pin should be left unconnected.
33	RING	**RING Terminal.** Connect to the RING lead of the subscriber loop.
34	TIP	**TIP Terminal.** Connect to the TIP lead of the subscriber loop.
35	NC	**No connection.** This pin should be left unconnected.
36	NC	**No connection.** This pin should be left unconnected.

6.2 Pin Descriptions: 40 Pin QFN (Si32184/5)

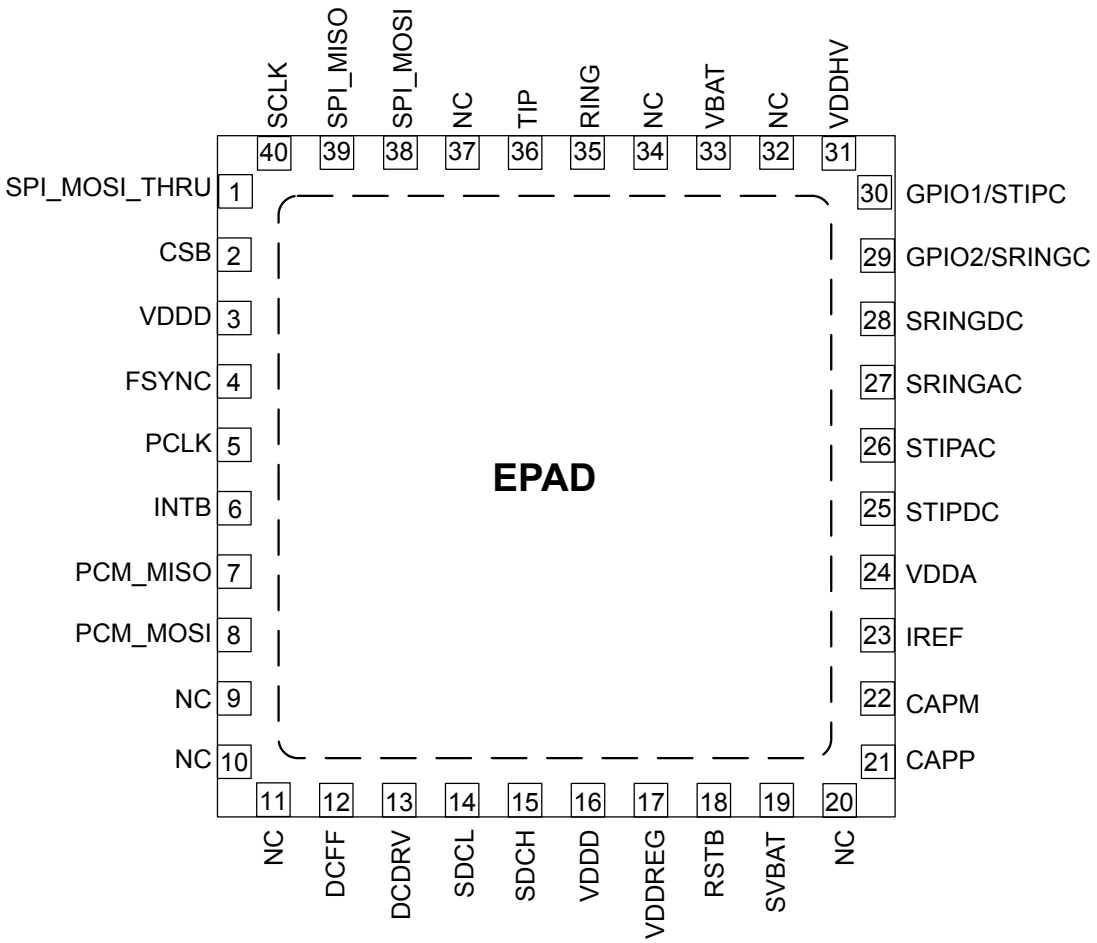


Table 6.2. Si32184/5 Pin Descriptions

Pin #	Pin Name	Description
1	SPI_MOSI_THRU	**SPI_MOSI Pass-Through.** Cascaded SPI_MOSI signal for daisy-chain mode.
2	CSB	**Chip Select Input.** Active low. When inactive, SCLK and SPI_MOSI are ignored and SPI_MISO is high impedance. When active, the serial port is operational.
3	VDDIO	**Digital IO Supply Voltage.** 3.3 V or 1.8 V digital power supply for internal circuitry.
4	FSYNC	**Frame Sync Clock Input.** 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
5	PCLK	**PCM Bus Clock Input.** Clock input for PCM bus timing.
6	INTB	**Interrupt Output.** Maskable interrupt output. Open drain output for wire-Ored operation.

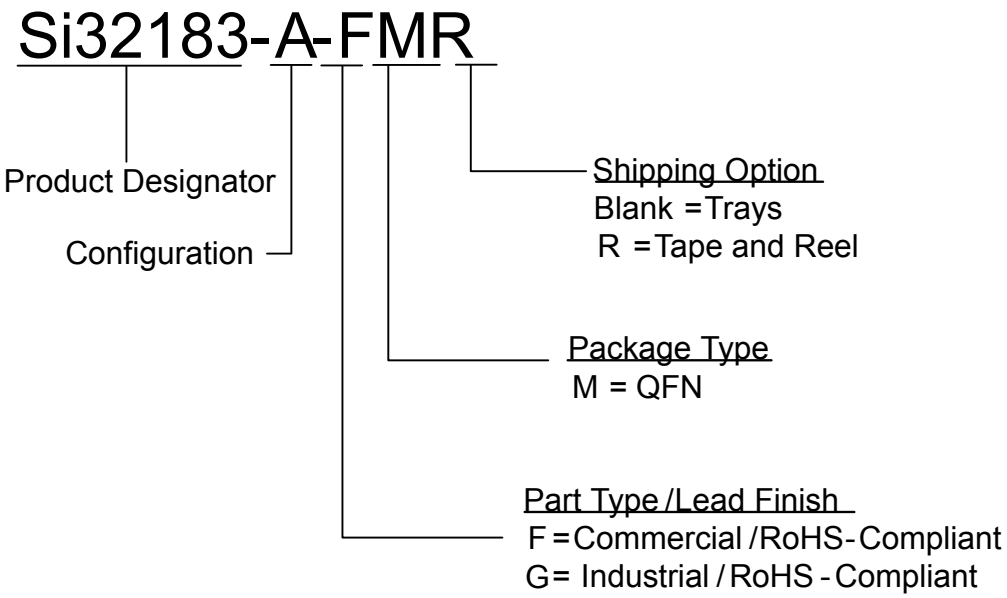
Pin #	Pin Name	Description
7	PCM_MISO	**Transmit PCM Output.** PCM Master Input, Slave Output. Output data to PCM bus.
8	PCM_MOSI	**Transmit PCM Input.** PCM Master Output, Slave input. Input data from PCM bus.
9	NC	**No Connection.** This pin should be left unconnected.
10	NC	**No connection.** This pin should be left unconnected.
11	NC	**No connection.** This pin should be left unconnected.
12	DCFF	**DC-DC Charge Pump Output.**
13	DCDRV	**DC Drive.** DC-DC converter control signal output which drives external transistor.
14	SDCL	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
15	SDCH	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
16	VDDD	**IC Voltage Supply.** 3.3 V digital power supply for internal circuitry.
17	VDDREG	**Regulated Core Power Supply.**
18	RSTB	**Reset Input** Active low input. Hardware reset used to place all control registers in the default state.
19	SVBAT	**VBAT Sense.** Input used to sense voltage on DC-DC converter output voltage lead.
20	NC	**No connection.** This pin should be left unconnected.
21	CAPP	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
22	CAPM	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
23	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
24	VDDA	**Analog Supply Voltage.** Analog 3.3 V power supply for internal analog circuitry.

Pin #	Pin Name	Description
25	STIPDC	**TIP DC Sense.** Analog DC input used to sense voltage on TIP lead..
26	STIPAC	**TIP AC Sense.** Analog AC input used to sense voltage on TIP lead..
27	SRINGAC	**RING AC Sense.** Analog AC input used to sense voltage on RING lead..
28	SRINGDC	**RING DC Sense.** Analog DC input used to sense voltage on RING lead..
29	SRINGC	**RING Coarse Sense Input.** Voltage sensing outside protection circuit.
30	STIPC	**TIP Coarse Sense Input.** Voltage sensing outside protection circuit.
31	VDDHV	**Analog Supply Voltage.** Analog 3.3 V power supply for internal analog circuitry.
32	NC	**No connection.** This pin should be left unconnected.
33	VBAT	**Battery Voltage Supply.** Connect to battery supply from DC-DC converter.
34	NC	**No connection.** This pin should be left unconnected.
35	RING	**RING Terminal.** Connect to the RING lead of the subscriber loop.
36	TIP	**TIP Terminal.** Connect to the TIP lead of the subscriber loop.
37	NC	**No connection.** This pin should be left unconnected.
38	SPI_MOSI	**Serial Port Data Input.** SPI Master Output, Slave Input. Input control data from Serial Peripheral Interface bus.
39	SPI_MISO	**Serial Port Data Output.** SPI Master Input, Slave Output. Output control data to Serial Peripheral Interface bus.
40	SCLK	**Serial Port Bit Clock Input.** Serial port clock input. Controls the serial data on SPI_MISO and latches the data on SPI_MOSI.

7. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



8. Package Outline

8.1 Package Outline: 36 Pin QFN

The figure below illustrates the package details for the Si3218x in a 36-pin QFN package. The table below lists the values for the dimensions shown in the illustration.

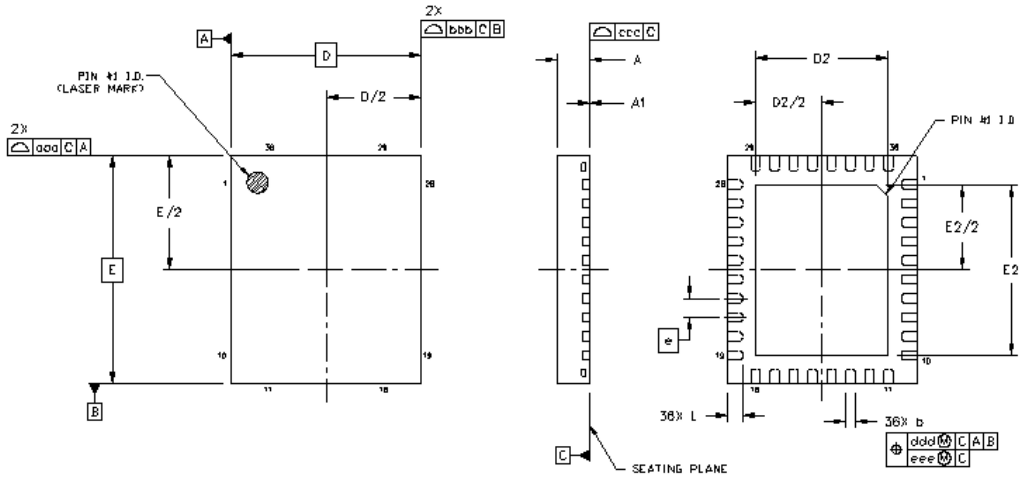


Figure 8.1. 36-Pin QFN Package

Table 8.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC.	
D2	3.40	3.50	3.60
e		0.50 BSC.	
E		6.00 BSC.	
E2	4.40	4.50	4.60
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 Package Outline: 40-Pin QFN

The figure below illustrates the package details for the Si3218x in a 40-pin QFN package. The table below lists the values for the dimensions shown in the illustration.

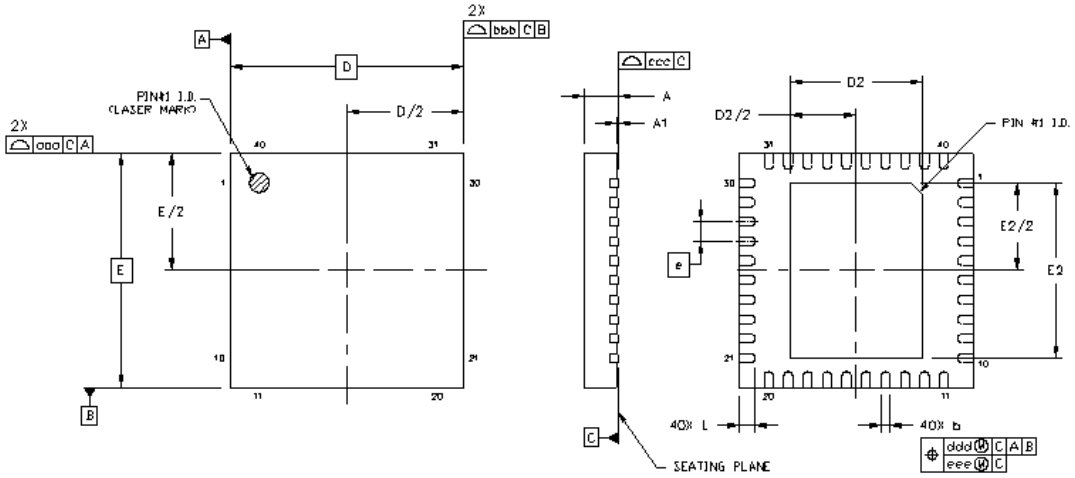


Figure 8.2. 40-Pin QFN Package

Table 8.2. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC.	
D2	3.30	3.40	3.50
e		0.50 BSC.	
E		6.00 BSC.	
E2	4.40	4.50	4.60
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

9. Land Pattern

9.1 Land Pattern: 36-Pin QFN

The figure below shows the recommended land pattern details for the 36-Pin QFN package. The table below lists the values for the dimensions shown in the illustration.

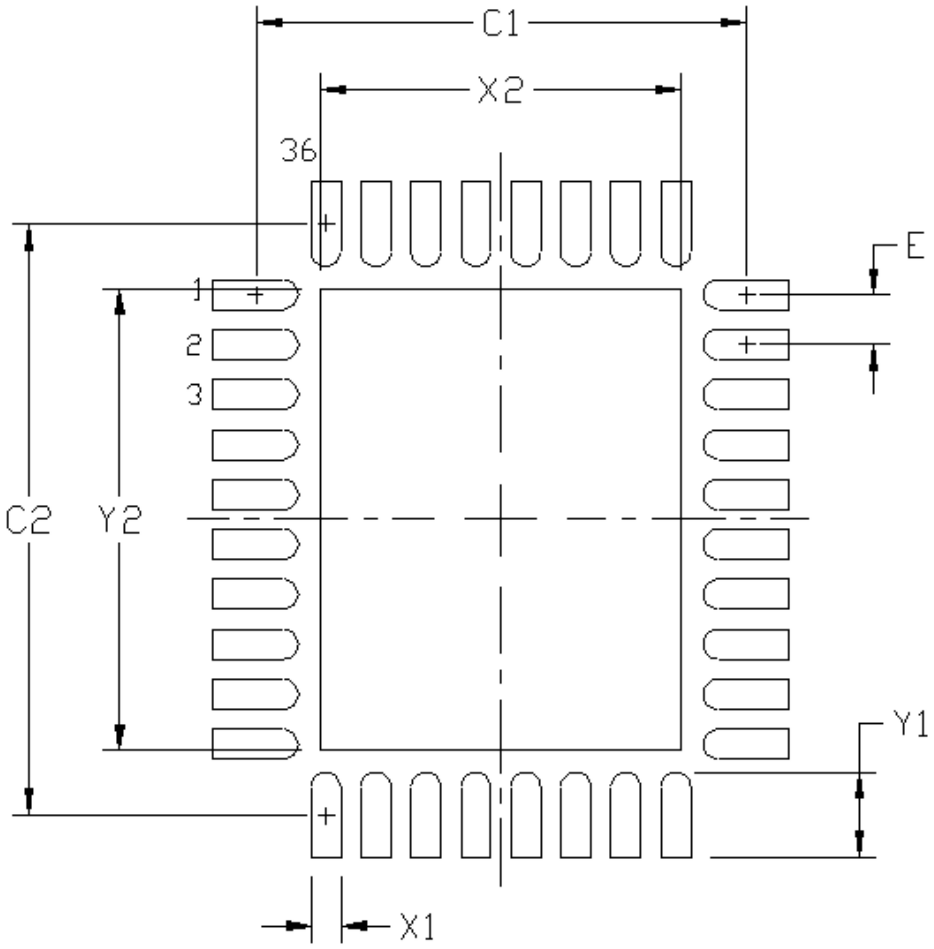


Figure 9.1. 36-Pin QFN Land Pattern

Table 9.1. PCB Land Pattern

Dimension	mm
C1	4.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	3.60
Y2	4.60

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 4x3 array of 0.85 mm square openings on 1.2 mm pitch should be used for the center ground pad to achieve a target solder coverage of ~50%.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. 2.The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

PCB Design

1. High-Tg PCB materials (Tg 170°standard industry practice).
2. A minimum of eight thermal vias are required in each center pad.
3. The recommended via diameter is 0.20-0.30 mm (8-12 mils).
4. Thermal vias placed in the center pads must have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (d 1.0mm).
5. Vias placed within the center pad areas must be either filled, or tented on the top side of the board, to prevent solder thieving from under the device.

9.2 Land Pattern 40-pin QFN

The figure below shows the recommended land pattern details for the 40-Pin QFN package. The table below lists the values for the dimensions shown in the illustration.

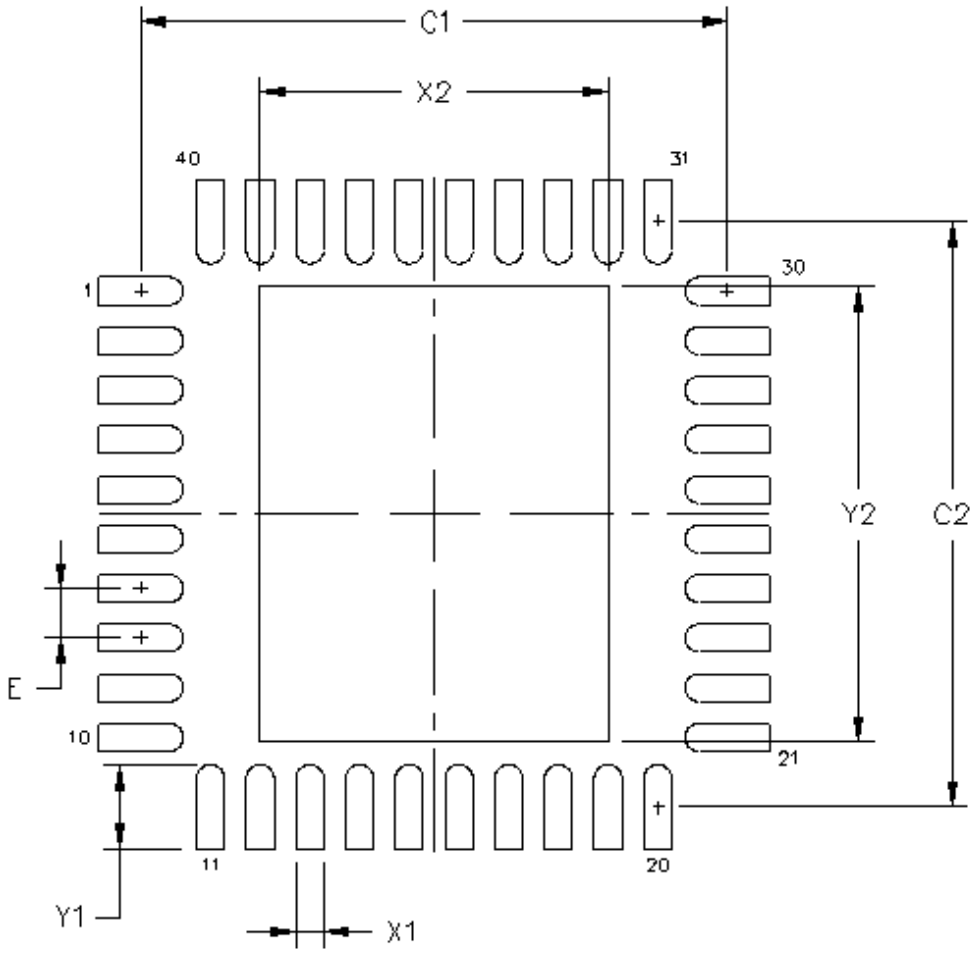


Figure 9.2. 40-Pin QFN Land Pattern

Table 9.2. PCB Land Pattern

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	3.50
Y2	4.60

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

PCB Design

1. High-Tg PCB materials (Tg 170°standard industry practice).
2. A minimum of eight thermal vias are required in each center pad.
3. The recommended via diameter is 0.20-0.30 mm (8-12 mils).
4. Thermal vias placed in the center pads must have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (d 1.0mm).
5. Vias placed within the center pad areas must be either filled, or tented on the top side of the board, to prevent solder thieving from under the device.

10. Top Marking

10.1 Top Marking 36-pin QFN

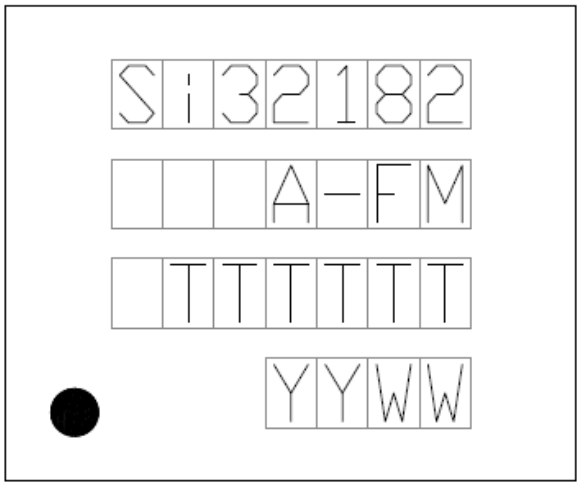


Figure 10.1. 36-Pin QFN Top Marking

Table 10.1. Top Marking Explanation

Line 1 Marking:	Device Root Part Number	e.g., Si32182
Line 2 Marking:	Device Part Number Suffix	Configuration, temperature rating, and package type
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code to track lot information.
Line 4 Marking:	YY = Year WW = Work Week Circle = 0.5 mm Diameter, Lower-Left-Justified	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. Pin 1 Identifier

10.2 Top Marking: 40-Pin QFN

Figure 10.2. 40-Pin QFN Top Marking

Table 10.2. Top Marking Explanation

Line 1 Marking:	Device Root Part Number	e.g., Si32184
Line 2 Marking:	Device Part Number Suffix	Configuration, temperature rating, and package type
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code to track lot information.
Line 4 Marking:	YY = Year WW = Work Week Circle = 0.5 mm Diameter, Lower-Left-Justified	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. Pin 1 Identifier

11. Document Revision History

Revision 0.4 to Revision 1.0

- Updated Si32184/5 pinout.
- Removed Si32180/1 references.
- Updated Longitudinal Performance specifications.
- Updated Absolute Maximum Ratings.
- Updated Top Marking.

Revision 0.3 to Revision 0.4

- Updated the features list on page 1.
- Updated the functional block diagram.
- Updated the Electrical Specifications section.
- Updated 4. FXS Features.

Revision 0.2 to Revision 0.3

- Added new 5x6 ISI and 6x6 PCM package options.

Revision 0.1 to Revision 0.2

- Updated power supply characteristics.
- Updated timing diagrams.
- Updated pin references and descriptions.
- Added package outline information.
- Added PCB land pattern information.
- Added top mark information.

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