THE DATASHEET OF

SIM3L156-C-GMR

www.win-source.net 0086-755-83957316

SiM3L1xx

High-Performance, Low-Power, 32-Bit Precision32™ MCU Family with up to 256 kB of Flash

32-bit ARM Cortex-M3 CPU

- 50 MHz maximum frequency
- Single-cycle multiplication, hardware division support
- Nested vectored interrupt control (NVIC) with 8 priority levels

Memory

- 32–256 kB flash, in-system programmable
- 8–32 kB SRAM with configurable low power retention

Clock Sources

- Internal oscillator with PLL: 23–50 MHz
- Low power internal oscillator: 20 MHz
- Low frequency internal oscillator (LFO): 16.4 kHz
- External real-time clock (RTC) crystal oscillator
- External oscillator: Crystal, RC, C, CMOS clock

Power Management

- Three adjustable low drop-out (LDO) regulators
- Power-on reset circuit and brownout detectors
- DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output)
- Multiple power modes supported for low power optimization

Low Power Features

- 75 nA typical current in Power Mode 8
- Low-current RTC (180 nA from LFO, 300 nA from crystal)
- 4 µs wakeup, register state retention and no reset required from lowest power mode
- 175 µA/MHz at 3.6 V executing from flash
- 140 µA/MHz at 3.6 V executing from SRAM
- Specialized on-chip charge pump reduces power consumption
- Process/Voltage/Temperature (PVT) Monitor

5 V Tolerant Flexible I/O

- Up to 62 contiguous 5 V tolerant GPIO with one priority cross-bar providing flexibility in pin assignments

Temperature Range: –40 to +85 °C

Supply Voltage: 1.8 to 3.8 V

Analog Peripherals

- 12-Bit Analog-to-Digital Converter: Up to 250 ksps 12-bit mode or 1 Msps 10-bit mode
- 10-Bit Current-mode Digital-to-Analog Converter
- 2 x Low-current comparators

Digital and Communication Peripherals

- 1 x USART with IrDA and ISO7816 Smartcard support
- 1 x UART that operates in low power mode
- 2 x SPIs, 1 x I2C, 16/32-bit CRC
- 128/192/256-bit Hardware AES Encryption
- Encoder/Decoder: Manchester and Three-out-of-Six
- Integrated LCD Controller: up to 160 segments (40x4), auto-contrast and low power operation

Timers/Counters

- 3 x 32-bit or 6 x 16-bit timers with capture/compare
- 16-bit, 6-channel counter with capture/compare/PWM and dead-time controller with differential outputs
- 16-bit low power timer/advanced capture counter operational in the lowest power mode
- 32-bit real time clock (RTC) with multiple alarms
- Watchdog timer
- Low power mode advanced capture counter (ACCTR)

Data Transfer Peripherals

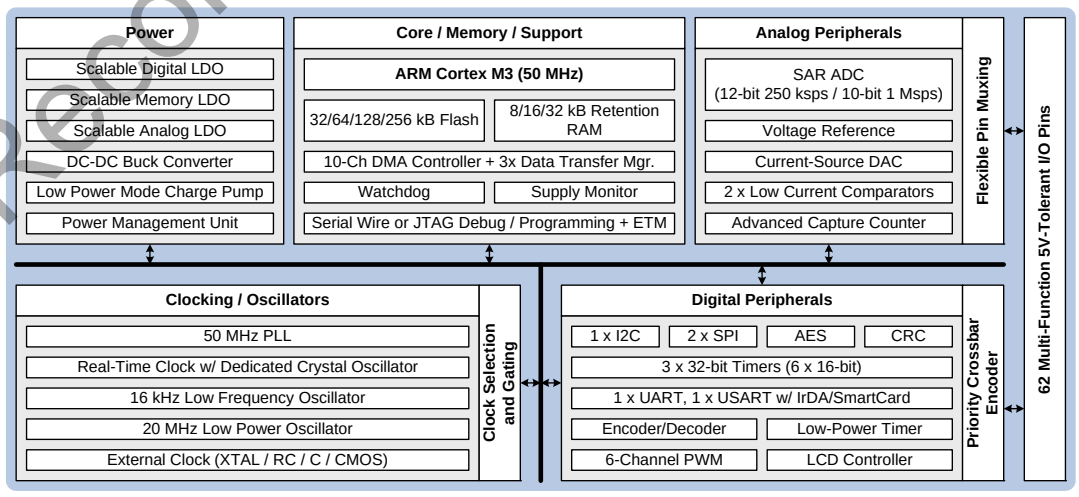
- 10-Channel DMA Controller
- 3 Channel Data Transfer Manager manages complex DMA transfers without core intervention

On-Chip Debugging

- Serial wire debug (SWD) with serial wire viewer (SWV) or JTAG (no boundary scan) allow debug and programming
- Cortex-M3 embedded trace macrocell (ETM)

Package Options

- QFN options: 40-pin (6 x 6 mm), 64-pin (9 x 9 mm)
- TQFP options: 64-pin (10 x 10 mm), 80-pin (12 x 12 mm)



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1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3L1xx devices.

1.1.1. SiM3L1xx Reference Manual

The Silicon Laboratories SiM3L1xx Reference Manual provides the detailed description for each peripheral on the SiM3L1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3L1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vectored Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

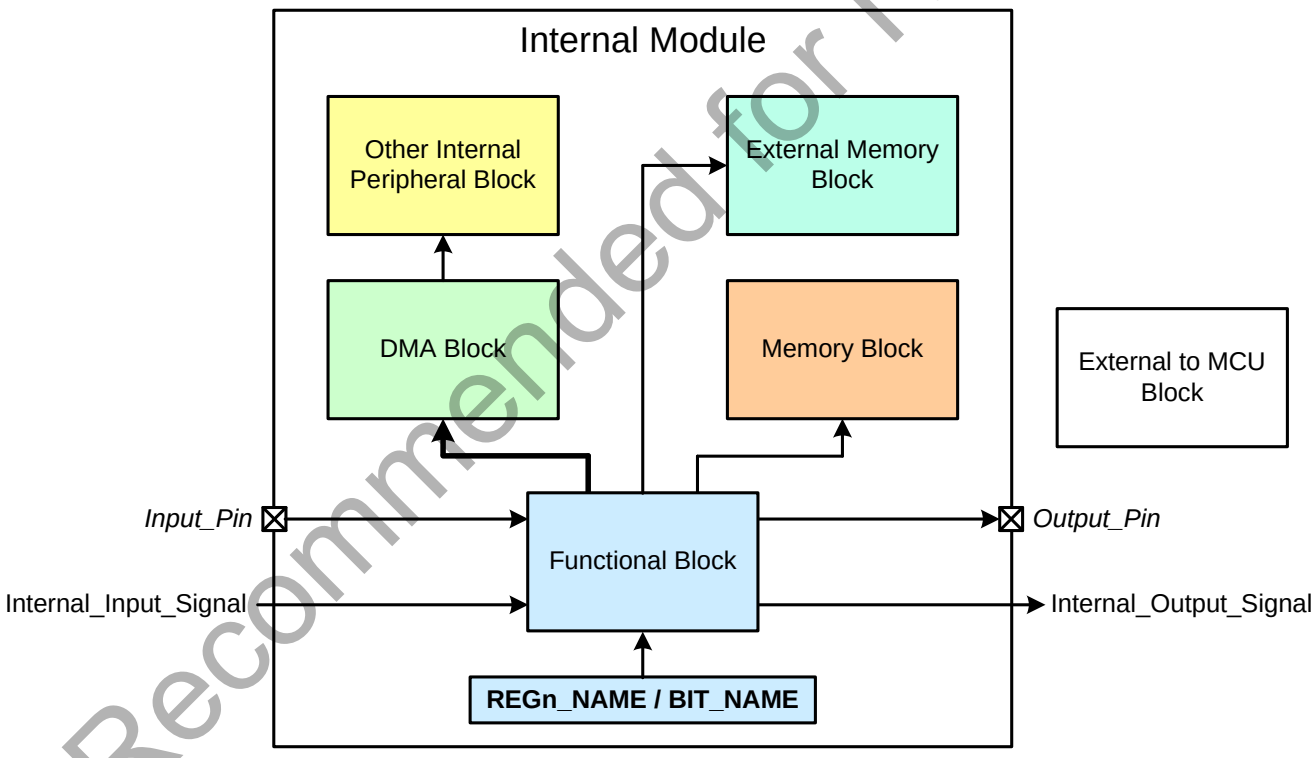

Figure 1.1. Block Diagram Conventions

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2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3L1xx devices.

2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is not used.

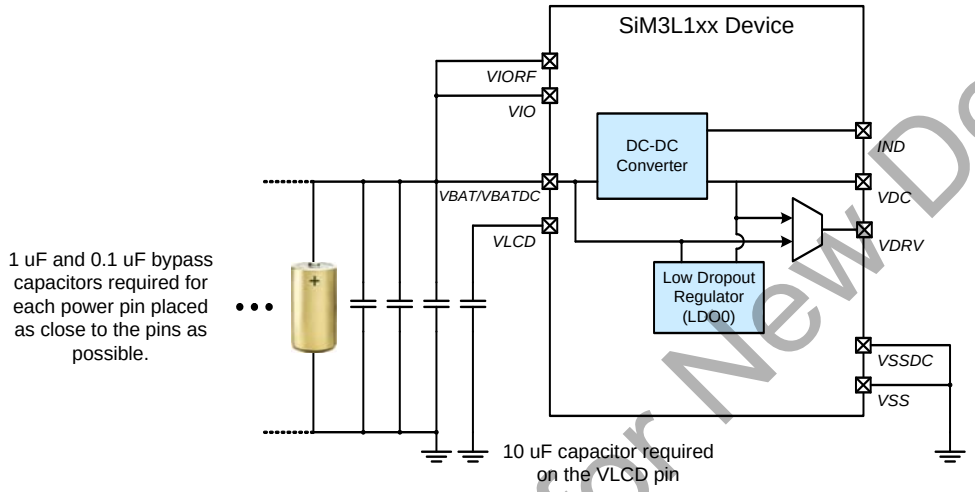

Figure 2.1. Connection Diagram with DC-DC Converter Unused

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the internal dc-dc buck converter is in use and I/O are powered directly from the battery.

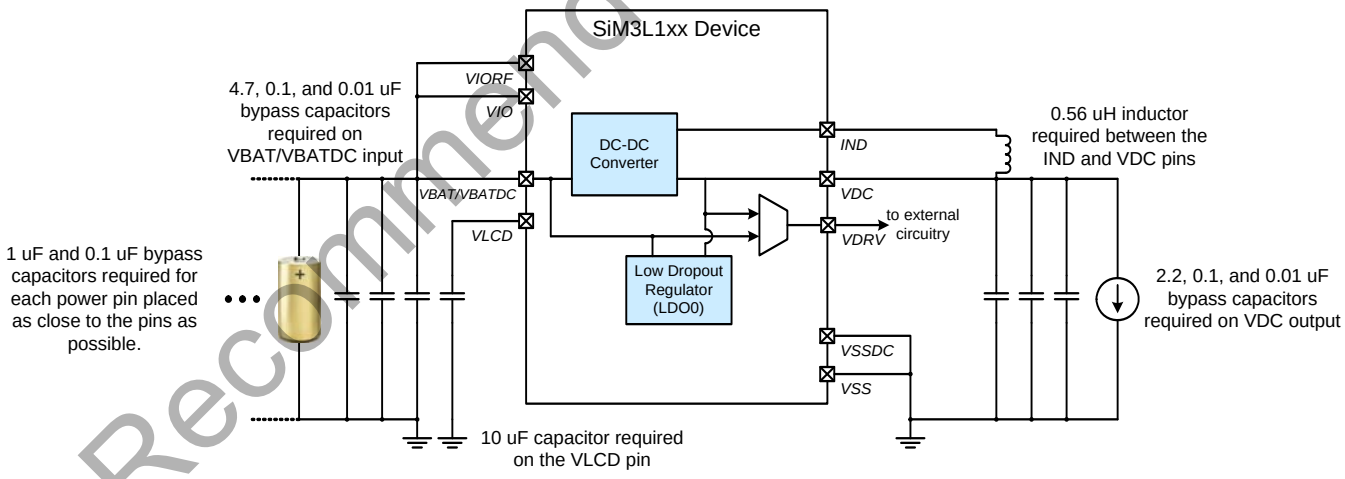

Figure 2.2. Connection Diagram with DC-DC Converter Used and I/O Powered from Battery

Figure 2.3 shows a typical connection diagram for the power pins of the SiM3L1xx devices when used with an external radio device like the Silicon Labs EZRadio® or EZRadioPRO® devices.

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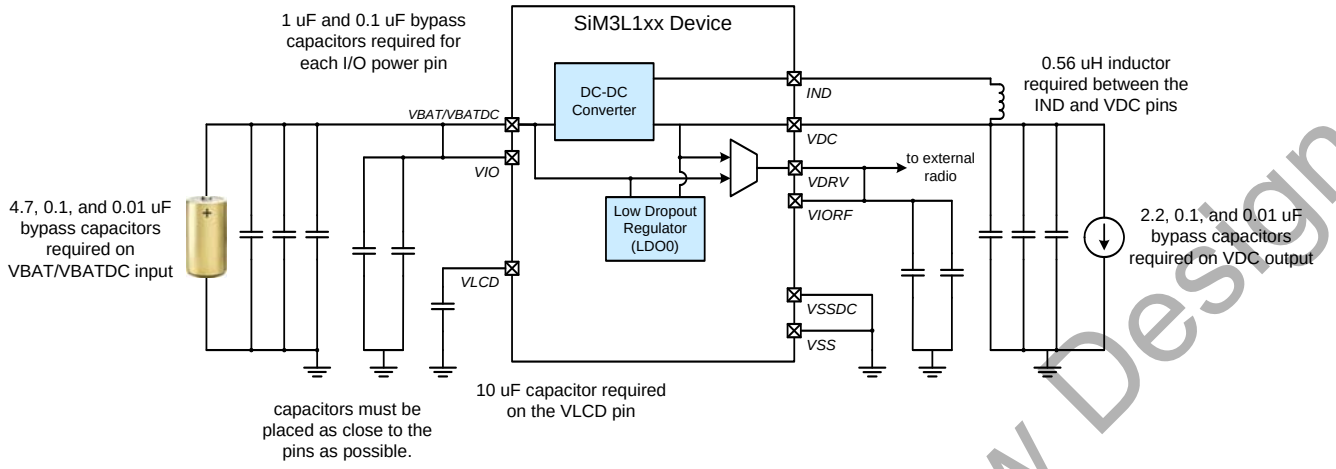

Figure 2.3. Connection Diagram with External Radio Device

Figure 2.4 shows a typical connection diagram for the power pins of the SiM3L1xx devices when the dc-dc buck converter is used and the I/O are powered separately.

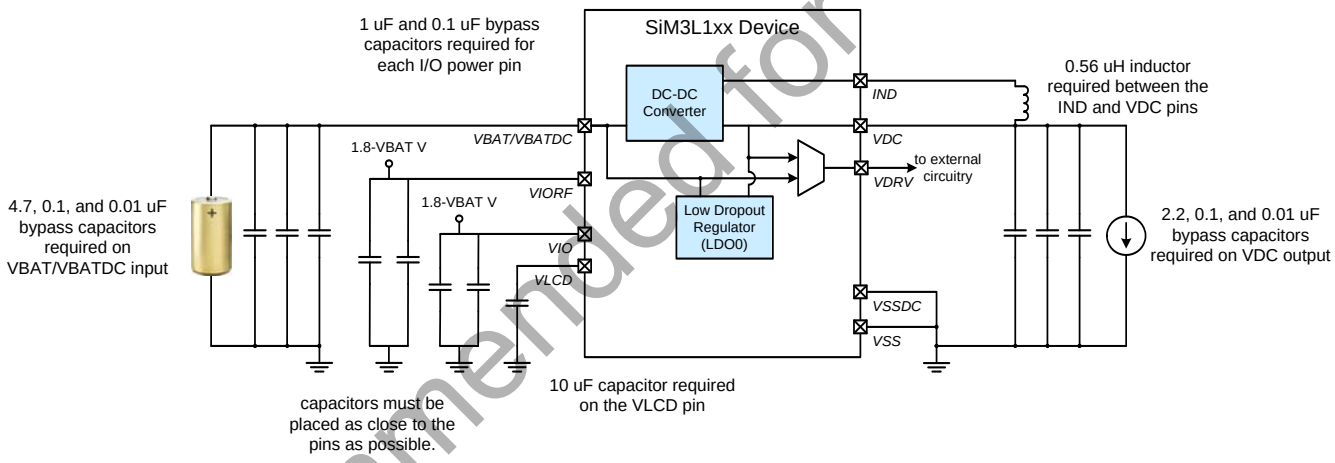

Figure 2.4. Connection Diagram with DC-DC Converter Used and I/O Powered Separately

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3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all Tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VBAT/VBATDC	V_{BAT}		1.8	—	3.8	V
Operating Supply Voltage on VDC	V_{DC}		1.25	—	3.8	V
Operating Supply Voltage on VDRV	V_{DRV}		1.25	—	3.8	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VIORF	V_{IORF}		1.8	—	V_{BAT}	V
Operation Supply Voltage on VLCD	V_{LCD}		1.8	—	3.8	V
System Clock Frequency (AHB)	f_{AHB}		0	—	50	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	+85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

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Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	17.5	18.9	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	6.7	7.2	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	1.15	1.4	mA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.3	14.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	5.4	5.9	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	980	1.2	µA
Normal Mode[1,2,3,4]—Full speed with code executing from flash, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	9.7	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	8.65	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	4.15	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	3.9	—	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	13.4	16.6	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	4.7	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	810	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	9.4	12.5	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	3.3	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	630	—	µA
Power Mode 1[1,2,3,4]—Full speed with code executing from RAM, LDOs powered by dc-dc at 1.9 V, peripheral clocks OFF	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.3 V	—	7.05	—	mA
		F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz V_{BAT} = 3.8 V	—	6.3	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.3 V	—	2.75	—	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz V_{BAT} = 3.8 V	—	2.6	—	mA
Power Mode 2[1,2,3,4,5]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	7.6	11.3	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	2.75	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	575	—	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2[1,2,3,4,5]—Core halted with only Port I/O clocks on (wake from pin).	I_{BAT}	F_{AHB} = 49 MHz, F_{APB} = 24.5 MHz	—	4	7.2	mA
		F_{AHB} = 20 MHz, F_{APB} = 10 MHz	—	1.47	—	mA
		F_{AHB} = 2.5 MHz, F_{APB} = 1.25 MHz	—	430	—	µA
Power Mode 3[1,2,6]—Fast-Wake Mode (PM3CLKEN = 1)	I_{BAT}	V_{BAT} = 3.8 V	—	320	530	µA
		V_{BAT} = 1.8 V	—	225	—	µA
Power Mode 4[1,2,4,6]—Slower clock speed with code executing from flash, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	385	640	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	330	—	µA
Power Mode 5[1,2,4,6]—Slower clock speed with code executing from RAM, peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	320	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	275	—	µA
Power Mode 6[1,2,4,6]—Core halted with peripheral clocks ON	I_{BAT}	F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 3.8 V	—	315	490	µA
		F_{AHB} = F_{APB} = 16 kHz, V_{BAT} = 1.8 V	—	270	—	µA
Power Mode 8[1,2]—Low Power Sleep, powered through VBAT, VIO, and VIORF at 2.4 V, 32kB of retention RAM	I_{BAT}	RTC Disabled, T_A = 25 °C	—	75	400	nA
		RTC w/ 16.4 kHz LFO, T_A = 25 °C	—	360	—	nA
		RTC w/ 32.768 kHz Crystal, T_A = 25 °C	—	670	—	nA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 8[1,2]—Low Power Sleep, powered by the low power mode charge pump, 32kB of retention RAM	I_{BAT}	RTC w/ 16.4 kHz LFO, V_{BAT} = 2.4 V, T_A = 25 °C	—	180	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 2.4 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, V_{BAT} = 3.8 V, T_A = 25 °C	—	245	—	nA
		RTC w/ 32.768 kHz Crystal, V_{BAT} = 3.8 V, T_A = 25 °C	—	390	—	nA
Unloaded V_{IO} and V_{IORF} Current[10]	I_{VIO}		—	2	—	nA
Power Mode 8 Peripheral Currents						
UART0	I_{UART0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	195	600	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	120	—	nA
LCD0[7], No segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	495	660	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	395	—	nA
LCD0[7], All (4 x 40) segments active	I_{LCD0}	V_{BAT} = 3.8 V, T_A = 25 °C	—	800	—	nA
		V_{BAT} = 2.4 V, T_A = 25 °C	—	580	—	nA
Advanced Capture Counter (ACCTR0), LC Single-Ended Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.11	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.44	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	1.45	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	1.82	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	2.15	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	2.54	—	nA/Hz

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Advanced Capture Counter (ACCTR0), LC Dual or Quadrature Mode, Relative to Sampling Frequency[9]	I_{ACCTR}	V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 01	—	1.39	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 01	—	1.89	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 10	—	2.08	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 10	—	2.59	—	nA/Hz
		V_{BAT} = 2.4 V, T_A = 25 °C, CPMD = 11	—	3.47	—	nA/Hz
		V_{BAT} = 3.8 V, T_A = 25 °C, CPMD = 11	—	4.03	—	nA/Hz
Analog Peripheral Supply Currents						
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 49 MHz	—	1.4	1.6	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	25	—	µA
		Operating at 2.5 MHz	—	25	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz	—	190	310	nA
External Oscillator (EXTOSC0)	I_{EXTOSC}	FREQCN = 111	—	3.8	4.5	mA
		FREQCN = 110	—	840	960	µA
		FREQCN = 101	—	185	230	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	13	µA
		FREQCN = 001	—	5	7	µA
		FREQCN = 000	—	3	5	µA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Not Recommended for New Designs

Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SARADC0	I_{SARADC}	Sampling at 1 Msps, Internal VREF used	—	1.2	1.6	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	540	µA
Temperature Sensor	I_{TSENSE}		—	75	110	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	—	µA
		Normal Power Mode	—	160	—	µA
VREF0	I_{REFP}		—	80	—	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	2	µA
		CMPMD = 10	—	3	8	µA
		CMPMD = 01	—	10	16	µA
		CMPMD = 00	—	25	42	µA
IDAC0[8]	I_{IDAC}		—	70	100	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	10	22	µA
Flash Current on VBAT						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:

1. Currents are additive. For example, where I_{BAT} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes all peripherals that cannot have clocks gated in the Clock Control module.
3. Includes LDO and PLL0OSC (>20 MHz) or LPOSC0 (≤20 MHz) supply current.
4. Internal Digital and Memory LDOs scaled to optimal output voltage.
5. Flash AHB clock turned off.
6. Running from internal LFO, Includes LFO supply current.
7. LCD0 current does not include switching currents for external load.
8. IDAC output current not included.
9. Does not include LC tank circuit.
10. Does not include digital drive current or pullup current for active port I/O. Unloaded I_{VIO} is included in all I_{BAT} PM8 production test measurements.

Not Recommended for New Designs

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 or 6 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time (using LFO as clock source)	t_{PM3FW}		—	425	—	µs
Power Mode 8 Wake Time	t_{PM8}		—	3.8	—	µs

Notes:
1. Wake times are specified as the time from the wake source to the execution phase of the first instruction following WFI. This includes latency to recognize the wake event and fetch the first instruction (assuming wait states = 0).

Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{BAT} High Supply Monitor Threshold (VBATHITHEN = 1)	V_{VBATMH}	Early Warning	—	2.20	—	V
		Reset	1.95	2.05	2.1	V
V_{BAT} Low Supply Monitor Threshold (VBATHITHEN = 0)	V_{VBATML}	Early Warning	—	1.85	—	V
		Reset	1.70	1.75	1.77	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{BAT}	—	1.4	—	V
		Falling Voltage on V_{BAT}	0.8	1	1.3	V
V_{BAT} Ramp Time	t_{RMP}	Time to $V_{BAT} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{BAT} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.5	1.5	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	2.5	10	kHz
V_{BAT} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

Not Recommended for New Designs

Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC-DC Buck Converter						
Input Voltage Range	V_{DCIN}		1.8	—	3.8	V
Input Supply to Output Voltage Differential (for regulation)	V_{DCREG}		0.45	—	—	V
Output Voltage Range	V_{DCOUT}		1.25	—	3.8	V
Output Voltage Accuracy	V_{DCACC}		—	±25	—	mV
Output Current	I_{DCOUT}		—	—	90	mA
Inductor Value[1]	L_{DC}		0.47	0.56	0.68	µH
Inductor Current Rating	I_{LDC}	I_{load} < 50 mA	450	—	—	mA
		I_{load} > 50 mA	550	—	—	mA
Output Capacitor Value	C_{DCOUT}		1	2.2	10	µF
Input Capacitor Value[2]	C_{DCIN}		—	4.7	—	µF
Load Regulation	R_{load}		—	0.03	—	mV/mA
Maximum DC Load Current During Startup	I_{DCMAX}		—	—	5	mA
Switching Clock Frequency	F_{DCCLK}		1.9	2.9	3.8	MHz
Local Oscillator Frequency	F_{DCOSC}		2.4	2.9	3.4	MHz
LDO Regulators						
Input Voltage Range[3]	V_{LDOIN}	Sourced from VBAT	1.8	—	3.8	V
		Sourced from VDC	1.9	—	3.8	V
Output Voltage Range[4]	V_{LDO}		0.8	—	1.9	V
LDO Output Voltage Accuracy	V_{LDOACC}		—	±25	—	mV
Output Settings in PM8 (All LDOs)	V_{LDO}	1.8 V ≤ V_{BAT} ≤ 2.9 V		1.5		V
		1.95 V ≤ V_{BAT} ≤ 3.5 V		1.8		V
		2.0 V ≤ V_{BAT} ≤ 3.8 V		1.9		V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Not Recommended for New Designs

Table 3.5. On-Chip Regulators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Memory LDO Output Setting[5]	V_{LDOMEM}	During Programming	1.8	—	1.9	V
		During Normal Operation	1.5	—	1.9	V
Digital LDO Output Setting	V_{LDODIG}	$F_{AHB} \leq 20$ MHz	1.0	—	1.9	V
		$F_{AHB} > 20$ MHz	1.2	—	1.9	V
Analog LDO Output Setting During Normal Operation[6]	V_{LDOANA}			1.8		V

Notes:

1. See reference manual for recommended inductors.
2. Recommended: X7R or X5R ceramic capacitors with low ESR. Example: Murata GRM21BR71C225K with ESR < 10 mΩ (@ frequency > 1 MHz).
3. Input voltage specification accounts for the internal LDO dropout voltage under the maximum load condition to ensure that the LDO output voltage will remain at a valid level as long as V_{LDOIN} is at or above the specified minimum.
4. The memory LDO output should always be set equal to or lower than the output of the analog LDO. When lowering both LDOs (for example to go into PM8 under low supply conditions), first adjust the memory LDO and then the analog LDO. When raising the output of both LDOs, adjust the analog LDO before adjusting the memory LDO.
5. Output range represents the programmable output range, and does not reflect the minimum voltage under all conditions. Dropout when the input supply is close to the output setting is normal, and accounted for.
6. Analog peripheral specifications assume a 1.8 V output on the analog LDO.

Not Recommended for New Designs

Table 3.6. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During sequential write operations, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Not Recommended for New Designs

Table 3.7. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency (Free-running output mode, RANGE = 2)	$f_{PLL0OSC}$	Full Temperature and Supply Range	48.3	49	49.7	MHz
Power Supply Sensitivity (Free-running output mode, RANGE = 2)	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 49 MHz	—	300	—	ppm/V
Temperature Sensitivity (Free-running output mode, RANGE = 2)	$TS_{PLL0OSC}$	V_{BAT} = 3.3 V, Fout = 49 MHz	—	50	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	50	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 50 MHz M=39, N=99, LOCKTH = 0		2.75	—	µs
		f_{REF} = 2.5 MHz, $f_{PLL0OSC}$ = 50 MHz M=19, N=399, LOCKTH = 0	—	9.45	—	µs
		f_{REF} = 32.768 kHz, $f_{PLL0OSC}$ = 50 MHz M=0, N=1524, LOCKTH = 0	—	92	—	µs
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{BAT} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{BAT} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{BAT} = 3.3 V	—	0.2	—	%/°C

Not Recommended for New Designs

Table 3.7. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC External Input CMOS Clock Frequency	$f_{RTCEXTCLK}$		0	—	40	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

Table 3.8. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency	f_{CMOS}		0*	—	50	MHz
External Crystal Frequency	f_{XTAL}		0.01	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
Low Power Mode Charge Pump Supply Range (input from V_{BAT})	V_{BAT}		2.4	—	3.8	V
***Note:** Minimum of 10 kHz when debugging.						

Not Recommended for New Designs

Table 3.9. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VBAT)	V_{ADC}	High Speed Mode	2.2	—	3.8	V
		Low Power Mode	1.8	—	3.8	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{BAT}	V
Input Voltage Range*	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF = 2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF = 2.4 V	–1	0	1	LSB

Not Recommended for New Designs

Table 3.9. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Temperature Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error	E_M		–0.07	–0.02	0.02	%
Dynamic Performance (10 kHz Sine Wave Input 1dB below full scale, Max throughput)						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB
***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.						

Not Recommended for New Designs

Table 3.10. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{BAT} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range, T_A = 25 °C	1.98	2.046	2.1	mA
		1 mA Range, T_A = 25 °C	0.99	1.023	1.05	mA
		0.5 mA Range, T_A = 25 °C	491	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VBAT Power Supply Rejection Ratio		2 mA Range	—	–220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

Not Recommended for New Designs

Table 3.11. ACCTR (Advanced Capture Counter)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Response Time, CMPMD = 11 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
LC Comparator Response Time, CMPMD = 00 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
LC Comparator Positive Hysteresis Mode 0 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
LC Comparator Negative Hysteresis Mode 0 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
LC Comparator Positive Hysteresis Mode 1 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
LC Comparator Negative Hysteresis Mode 1 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
LC Comparator Positive Hysteresis Mode 2 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
LC Comparator Negative Hysteresis Mode 2 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

Not Recommended for New Designs

Table 3.11. ACCTR (Advanced Capture Counter) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LC Comparator Positive Hysteresis Mode 3 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
LC Comparator Negative Hysteresis Mode 3 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
LC Comparator Input Range (ACCTR0_LCIN pin)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
LC Comparator Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
LC Comparator Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
LC Comparator Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
LC Comparator Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Offset Error	DAC_{EOFF}		–1	—	1	LSB
Reference DAC Full Scale Output	DAC_{FS}	Low Range	—	V_{IO}/8	—	V
		High Range	—	V_{IO}	—	V
Reference DAC Step Size	DAC_{LSB}	Low Range (48 steps)	—	V_{IO}/384	—	V
		High Range (64 steps)	—	V_{IO}/64	—	V
LC Oscillator Period	T_{LCOSC}		—	25	—	ns
LC Bias Output Impedance	R_{LCBIAS}	10 µA Load	—	1	—	kΩ
LC Bias Drive Strength	I_{LCBIAS}		—	—	2	mA
Pull-Up Resistor Tolerance	R_{TOL}	PUVAL[4:2] = 0 to 6	-15	—	15	%
		PUVAL[4:2] = 7	-10	—	10	%

Not Recommended for New Designs

Table 3.12. Voltage Reference Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	1.6	1.65	1.7	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
Internal Precision Reference						
Valid Supply Range	V_{BAT}	VREF2X = 0	1.8	—	3.8	V
		VREF2X = 1	2.7	—	3.8	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.17	1.2	1.23	V
		25 °C ambient, VREF2X = 1	2.35	2.4	2.45	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	35	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

Table 3.13. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.77	—	mV/°C
Slope Error*	E_M		—	±25	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs

***Note:** Absolute input pin voltage is limited by the lower of the supply at VBAT and VIO.

Not Recommended for New Designs

Table 3.14. Comparator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CMPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CMPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	0.37	—	mV
		CMPHYP = 01	—	7.9	—	mV
		CMPHYP = 10	—	16.7	—	mV
		CMPHYP = 11	—	32.8	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	0.37	—	mV
		CMPHYN = 01	—	–7.9	—	mV
		CMPHYN = 10	—	–16.1	—	mV
		CMPHYN = 11	—	–32.7	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.47	—	mV
		CMPHYP = 01	—	5.85	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24.4	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.47	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12.1	—	mV
		CMPHYN = 11	—	–24.6	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.66	—	mV
		CMPHYP = 01	—	4.55	—	mV
		CMPHYP = 10	—	9.3	—	mV
		CMPHYP = 11	—	19	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

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Table 3.14. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.37	—	mV
		CMPHYP = 01	—	3.8	—	mV
		CMPHYP = 10	—	7.8	—	mV
		CMPHYP = 11	—	15.6	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.37	—	mV
		CMPHYN = 01	—	–3.9	—	mV
		CMPHYN = 10	—	–7.9	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{BAT} + 0.25	V
Input Pin Capacitance	C_{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

Table 3.15. LCD0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Charge Pump Output Voltage Error	V_{CPERR}		—	±50	—	mV
LCD Clock Frequency	F_{LCD}		16	—	33	kHz

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Table 3.16. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (PB0, PB1, PB3, or PB4)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IO} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IO} – 0.1	—	—	V
Output High Voltage (PB2)	V_{OH}	Low Drive, I_{OH} = –1 mA	V_{IORF} – 0.7	—	—	V
		Low Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
		High Drive, I_{OH} = –3 mA	V_{IORF} – 0.7	—	—	V
		High Drive, I_{OH} = –10 µA	V_{IORF} – 0.1	—	—	V
Output Low Voltage (any Port I/O pin or $\overline{\text{RESET}}$[1])	V_{OL}	Low Drive, I_{OL} = 1.4 mA	—	—	0.6	V
		Low Drive, I_{OL} = 10 µA	—	—	0.1	V
		High Drive, I_{OL} = 8.5 mA	—	—	0.6	V
		High Drive, I_{OL} = 10 µA	—	—	0.1	V
Input High Voltage (PB0, PB1, PB3, PB4 or $\overline{\text{RESET}}$)	V_{IH}		V_{IO} – 0.6	—	—	V
Input High Voltage (PB2)	V_{IH}		V_{IORF} – 0.6	—	—	V
Input Low Voltage any Port I/O pin or $\overline{\text{RESET}}$)	V_{IL}		—	—	0.6	V
Weak Pull-Up Current[2] (per pin)	I_{PU}	V_{IO} or V_{IORF} = 1.8	-6	-3.5	-2	µA
		V_{IO} or V_{IORF} = 3.8	-32	-20	-10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	$0 \le V_{IN} \le V_{IO}$ or V_{IORF}	-1	—	1	µA

Notes:
1. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.
2. On the SiM3L1x6 and SiM3L1x4 devices, the SWV pin will have double the weak pull-up current specified whenever the device is held in reset.

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3.2. Thermal Conditions

Table 3.17. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with the exposed pad soldered to a topside PCB pad.						

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3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.18 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.18. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VBAT/VBATDC	V_{BAT}		V_{SS}–0.3	4.2	V
Voltage on VDC	V_{DC}		V_{SSDC}–0.3	4.2	V
Voltage on VDRV	V_{DRV}		V_{SS}–0.3	4.2	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIORF	V_{IORF}		V_{SS}–0.3	4.2	V
Voltage on VLCD	V_{LCD}		V_{SS}–0.3	4.2	V
Voltage on I/O (PB0, PB1, PB3, PB4) or $\overline{\text{RESET}}$[1]	V_{IN}	$V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
Voltage on PB2 I/O Pins[1]	V_{IN}	$V_{IORF} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$V_{IORF} < 3.3$ V	V_{SS}–0.3	V_{IORF}+2.5	V
Total Current Sunk into Supply Pins	I_{SUPP}	VBAT/VBATDC, VIO, VIORF, VDRV, VDC, VLCD	—	400	mA
Total Current Sourced out of Ground Pins[2]	I_{VSS}	V_{SS}, V_{SSDC}	400	—	mA
Current Sourced or Sunk by any I/O Pin	I_{PIO}	All I/O and $\overline{\text{RESET}}$	–100	100	mA
Power Dissipation at T_A = 85 °C	P_D	TQFP-80 Packages	—	500	mW
		QFN-64 Packages	—	800	mW
		TQFP-64 Packages	—	650	mW
		QFN-40 Packages	—	650	mW

Notes:
1. Exceeding the minimum V_{IO} voltage may cause current to flow through adjacent device pins.
2. VSS and VSSDC provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

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4. Precision32™ SiM3L1xx System Overview

The SiM3L1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 50 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB flash; in-system programmable, 8–32 kB SRAM configurable to retention mode in 4 kB blocks. Blocks configured to retention mode preserve state in the low power PM8 mode.
- **Power:**
  - Three adjustable low drop-out (LDO) regulators.
  - DC-DC buck converter allows dynamic voltage scaling for maximum efficiency (250 mW output).
  - Power-on reset circuit and brownout detectors.
  - Power Management Unit (PMU).
  - Specialized charge pump reduces power consumption in low power modes.
  - Process/Voltage/Temperature (PVT) Monitor.
  - Register state retention in lowest power mode.
- **I/O:** Up to 62 contiguous 5 V tolerant I/O pins and one flexible peripheral crossbar.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–50 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock.
- **Integrated LCD Controller (4x40).**
- **Data Peripherals:**
  - 10-Channel DMA Controller.
  - 3 x Data Transfer Managers.
  - 128/192/256-bit Hardware AES Encryption.
  - CRC with programmable 16-bit polynomial, one 32-bit polynomial, and bus snooping capability.
  - Encoder / Decoder.
- **Timers/Counters:**
  - 3 x 32-bit Timers.
  - 1 x Enhanced Programmable Counter Array (EPCA).
  - Real Time Clock (RTC0).
  - Low Power Timer.
  - Watchdog Timer.
  - Low Power Mode Advanced Capture Counter (ACCTR).
- **Communications Peripherals:**
  - 1 x USART with IrDA and ISO7816 SmartCard support.
  - 1 x UART that operates in low power mode (PM8).
  - 2 x SPIs.
  - 1 x I2C.
- **Analog:**
  - 1 x 12-Bit Analog-to-Digital Converter (SARADC).
  - 1 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 2 x Low-Current Comparators (CMP).
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillators, the SiM3L1xx devices are truly stand-alone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all

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peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.8 V operation over the industrial temperature range (–40 to +85 °C). The SiM3L1xx devices are available in 40-pin or 64-pin QFN and 64-pin or 80-pin TQFP packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

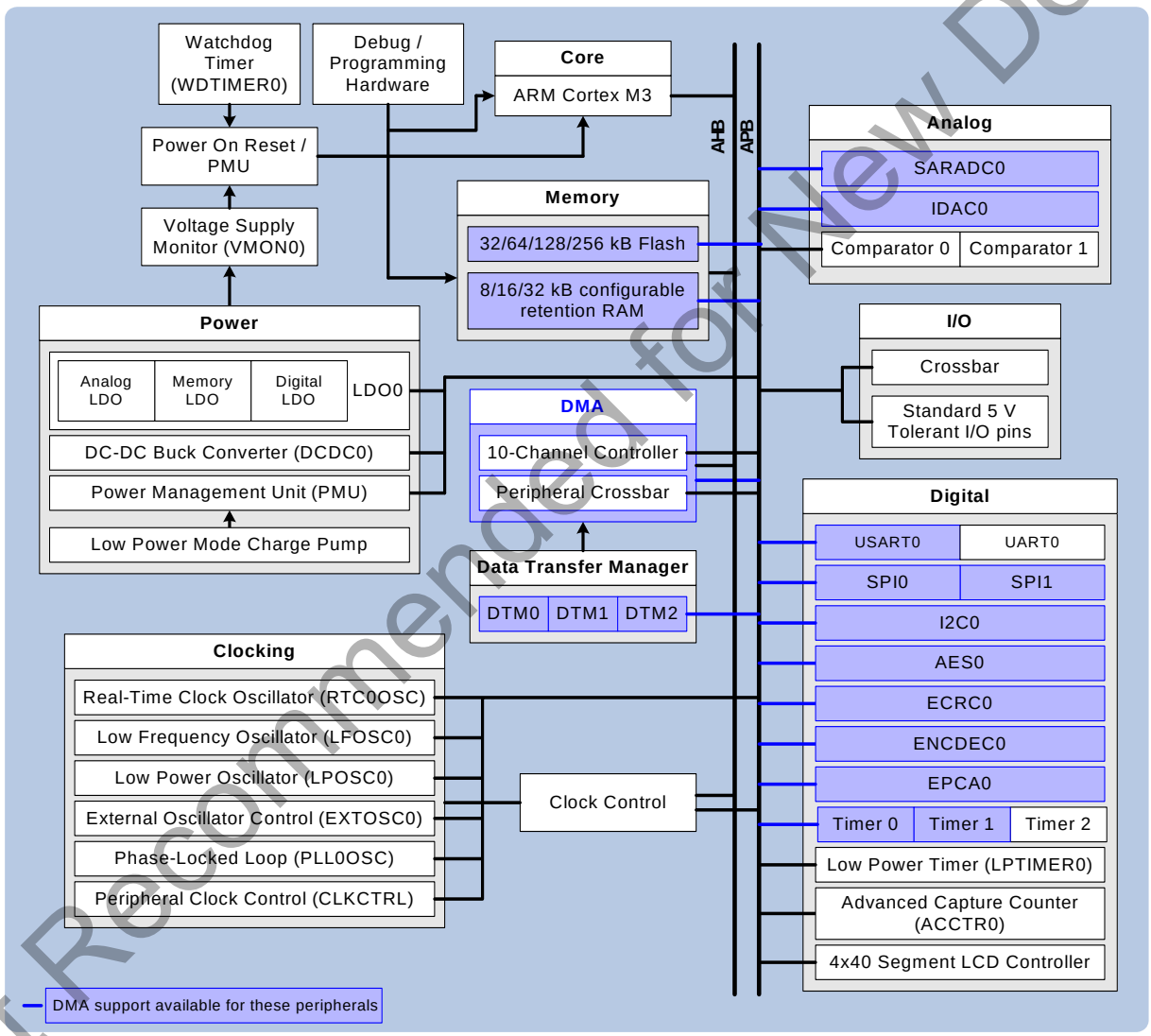

Figure 4.1. Precision32™ SiM3L1xx Family Block Diagram

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4.1. Power

The SiM3L1xx devices include a dc-dc buck converter that can take an input from 1.8–3.8 V and create an output from 1.25–3.8 V. In addition, SiM3L1xx devices include three low dropout regulators as part of the LDO0 module: one LDO powers the analog subsystems, one LDO powers the flash and SRAM memory at 1.8 V, and one LDO powers the digital and core circuitry. Each of these regulators can be independently powered from the dc-dc converter or directly from the battery voltage, and their outputs are adjustable to conserve system power. SiM3L1xx devices also include a low power charge pump in the PMU module for use in low power modes (PM8) to further reduce the power consumption of the device.

Figure 4.2 shows the power system configuration of these devices.

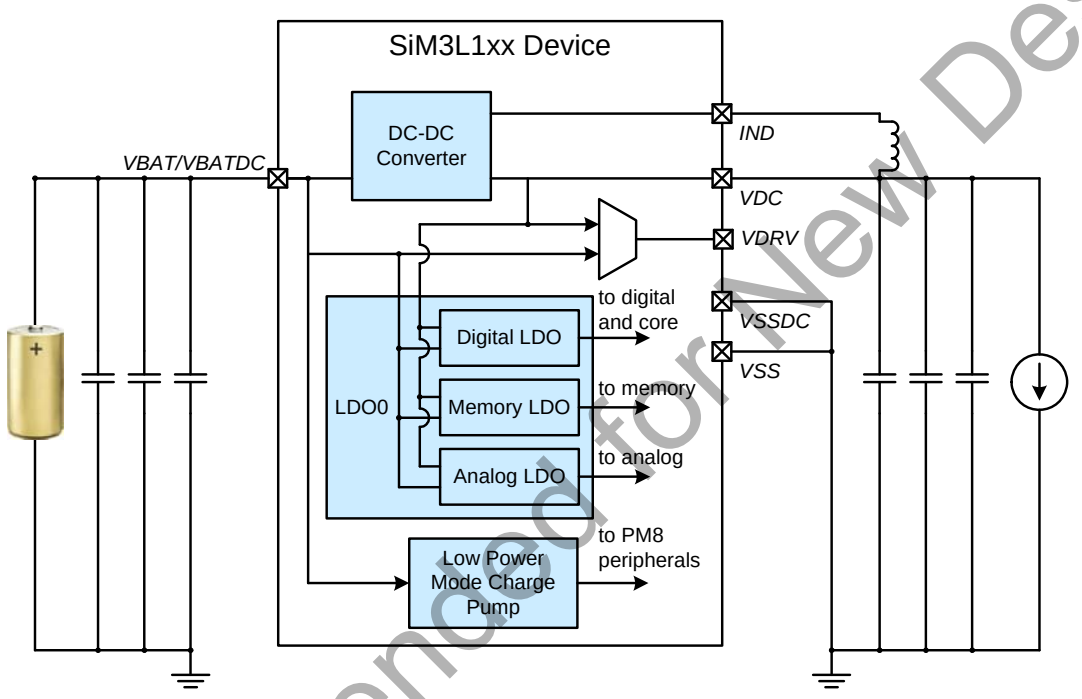

Figure 4.2. SiM3L1xx Power

4.1.1. DC-DC Buck Converter (DCDC0)

SiM3L1xx devices include an on-chip step-down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with a programmable output voltage that should be at least 0.45 V lower than the input battery voltage; if this criteria is not met and the converter can no longer operate, the output of the dc-dc converter automatically connects to the battery. The dc-dc converter can supply up to 100 mA and can be used to power the MCU and/or external devices in the system.

The dc-dc converter has a built in voltage reference and oscillator and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current.

The dc-dc converter includes the following features:

- Efficiently utilizes the energy stored in a battery, extending its operational lifetime.
- Input range: 1.8 to 3.8 V.
- Output range: 1.25 to 3.8 V in 50 mV (1.25–1.8 V) or 100 mV (1.8–3.8 V) steps.
- Supplies up to 100 mA.
- Includes a voltage reference and an oscillator.

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- Supports synchronizing the regulator switching with the system clock.
- Automatically limits the peak inductor current if the load current rises beyond a safe limit.
- Automatically goes into bypass mode if the battery voltage cannot provide sufficient headroom.
- Sources current, but cannot sink current.

4.1.2. Three Low Dropout LDO Regulators (LDO0)

The SiM3L1xx devices include one LDO0 module with three low dropout regulators. Each of these regulators have independent switches to select the battery voltage or the output of the dc-dc converter as the input to each LDO, and an adjustable output voltage.

The LDOs consume little power and provide flexibility in choosing a power supply for the system. Each regulator can be independently adjusted between 0.8 and 1.9 V output.

4.1.3. Voltage Supply Monitor (VMON0)

The SiM3L1xx devices include a voltage supply monitor that can monitor the main supply voltage. This module includes the following features:

- Main supply “VBAT Low” (VBAT below the early warning threshold) notification.
- Holds the device in reset if the main VBAT supply drops below the VBAT Reset threshold.

The voltage supply monitor allows devices to function in known, safe operating conditions without the need for external hardware.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3L1xx manages the power systems of the device. It manages the power-up sequence during power on and the wake up sources for PM8. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins.

The VDRV pin powers external circuitry from either the VBAT battery input voltage or the output of the dc-dc converter on VDC. The PMU includes an internal switch to select one of these sources for the VDRV pin.

The PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power.

The PMU module includes the following features:

- Provides the enable or disable for the analog power system, including the three LDO regulators.
- Up to 14 pin wake inputs can wake the device from Power Mode 8.
- The Low Power Timer, RTC0 (alarms and oscillator failure), Comparator 0, Advanced Capture Counter, LCD0 VBAT monitor, UART0, low power mode charge pump failure, and the RESET pin can also serve as wake sources for Power Mode 8.
- Controls which 4 kB RAM blocks are retained while in Power Mode 8.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM8.
- Specialized charge pump to reduce power consumption in PM8.

Provides control for the internal switch between VBAT and VDC to power the VDRV pin for external circuitry.

4.1.5. Device Power Modes

The SiM3L1xx devices feature seven low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), Advanced Capture Counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0) and Power Mode 4

Normal Mode and Power Mode 4 are fully operational modes with code executing from flash memory. PM4 is the same as Normal Mode, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs.

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4.1.5.2. Power Mode 1 and Power Mode 5

Power Mode 1 and Power Mode 5 are fully operational modes with code executing from RAM. PM5 is the same as PM1, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. Compared with the corresponding flash operational mode (Normal or PM4), the active power consumption of the device in these modes is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAMdoesnot require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2 and Power Mode 6

In Power Mode 2 and Power Mode 6, the core halts and the peripherals continue to run at the selected clock speed. PM6 is the same as PM2, but with the clocks operating at a lower speed. This enables power to be conserved by reducing the LDO regulator outputs. To place the device in PM2 or PM6, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 or PM6 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0, PM6 can achieve similar power consumption to PM3, but with faster wake times and the ability to wake on any interrupt.

4.1.5.4. Power Mode 3

In Power Mode 3 the core and peripheral clocks are halted. The available sources to wake from PM3 are controlled by the Power Management Unit (PMU). A special Fast Wake option allows the core to wake faster by keeping the LFOSC0 or RTC0 clock active. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

Before entering PM3, the DMA controller should be disabled, and the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be cleared to indicate that PM3 is the desired power mode. For fast wake, the core clocks (AHB and APB) should be configured to run from the LPOSC, and the PM3 Fast wake option and clock source should be selected in the PM3CN register.

The device will enter PM3 on a WFI or WFE instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 8

In Power Mode 8, the core and most peripherals are completely powered down, but all registers and selected RAM blocks retain their state. The LDO regulators are disabled, so all active circuitry operates directly from VBAT. Alternatively, the PMU has a specialized VBAT-divided-by-2 charge pump that can power some internal modules while in PM8 to save power. The fully operational functions in this mode are: LPTIMER0 , RTC0, UART0 running from RTC0TCLK, PMU Pin Wake, the advanced capture counter, and the LCD controller.

This mode provides the lowest power consumption for the device, but requires an appropriate wake up source or reset to exit. The available wake up or reset sources to wake from PM8 are controlled by the Power Management Unit (PMU). The available wake up sources are: Low Power Timer (LPTIMER0), RTC0 (alarms and oscillator failure notification), Comparator 0 (CMP0), advanced capture counter (ACCTR0), LCD VBAT monitor (LCD0), UART0, low power mode charge pump failure, and PMU Pin Wake. The available reset sources are: RESET pin, VBAT supply monitor, Comparator 0, Comparator 1, low power mode charge pump failure, RTC0 oscillator failure, or a PMU wake event.

Before entering PM8, the desired wake source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the CLKCTRL0_CONFIG register should be set to indicate that PM8 is the desired power mode.

The device will enter PM8 on a WFI or WFE instruction, and remain in PM8 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

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4.1.5.6. Power Mode Summary

The power modes described above are summarized in Table 4.1. Table 3.2 and Table 3.3 provide more information on the power consumption and wake up times for each mode.

Table 4.1. SiM3L1xx Power Modes

Mode	Description	Notes
Normal	■ Core operating at full speed ■ Code executing from flash	■ Full device operation
Power Mode 1 (PM1)	■ Core operating at full speed ■ Code executing from RAM	■ Full device operation ■ Higher CPU bandwidth than PM0 (RAM can operate with zero wait states at any frequency)
Power Mode 2 (PM2)	■ Core halted ■ AHB, APB and all peripherals operational at full speed	■ Fast wakeup from any interrupt source
Power Mode 3 (PM3)	■ All clocks to core and peripherals stopped ■ Faster wake enabled by keeping LFOSC0 or RTC0TCLK active	■ Wake on any wake source or reset source defined in the PMU
Power Mode 4 (PM4)	■ Core operating at low speed ■ Code executing from flash	■ Same capabilities as PM0, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 5 (PM5)	■ Core operating at low speed ■ Code executing from RAM	■ Same capabilities as PM1, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power
Power Mode 6 (PM6)	■ Core halted ■ AHB, APB and all peripherals operational at low speed	■ Same capabilities as PM2, operating at lower speed ■ Lower clock speed enables lower LDO output settings to save power ■ When running from LFOSC0, power is similar to PM3, but the device wakes much faster
Power Mode 8 (PM8)	■ Low power sleep ■ LDO regulators are disabled and all active circuitry operates directly from VBAT ■ The following functions are available: ACCTR0, RTC0, UART0 running from RTC0TCLK, LPTIMER0, port match, and the LCD controller ■ Register and RAM state retention	■ Lowest power consumption ■ Wake on any wake source or reset source defined in the PMU

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4.1.6. Process/Voltage/Temperature Monitor (TIMER2 and PVTOSC0)

The Process/Voltage/Temperature monitor consists of two modules (TIMER2 and PVTOSC0) designed to monitor the digital circuit performance of the SiM3L1xx device.

The PVT oscillator (PVTOSC0) consists of two oscillators, one operating from the memory LDO and one operating from the digital LDO. These oscillators have two independent speed options and provide the clocks for two 16-bit timers in the TIMER2 module using the EX input. By monitoring the resulting counts of the TIMER2 timers, firmware can monitor the current device performance and increase the scalable LDO regulator (LDO0) output voltages as needed or decrease the output voltages to save power.

The PVT monitor has the following features:

- Two separate oscillators and timers for the memory and digital logic voltage domains.
- Two oscillator output divider settings.
- Provides a method for monitoring digital performance to allow firmware to adjust the scalable LDO regulator output voltages to the lowest level possible, saving power.

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4.2. I/O

4.2.1. General Features

The SiM3L1xx ports have the following features:

- 5 V tolerant.
- Push-pull or open-drain output modes to the VIO or VIORF voltage level.
- Analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs each provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB0 only) to generate simple square waves and pulses.

4.2.2. Crossbar

The SiM3L1xx devices have one crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O, and peripherals can be moved around the chip as needed to ease layout constraints.

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4.3. Clocking

The SiM3L1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, the PLL0 Oscillator, and the VIORFCLK pin input. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock or set to the AHB clock divided by two.

The Clock Control module on SiM3L1xx devices allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.

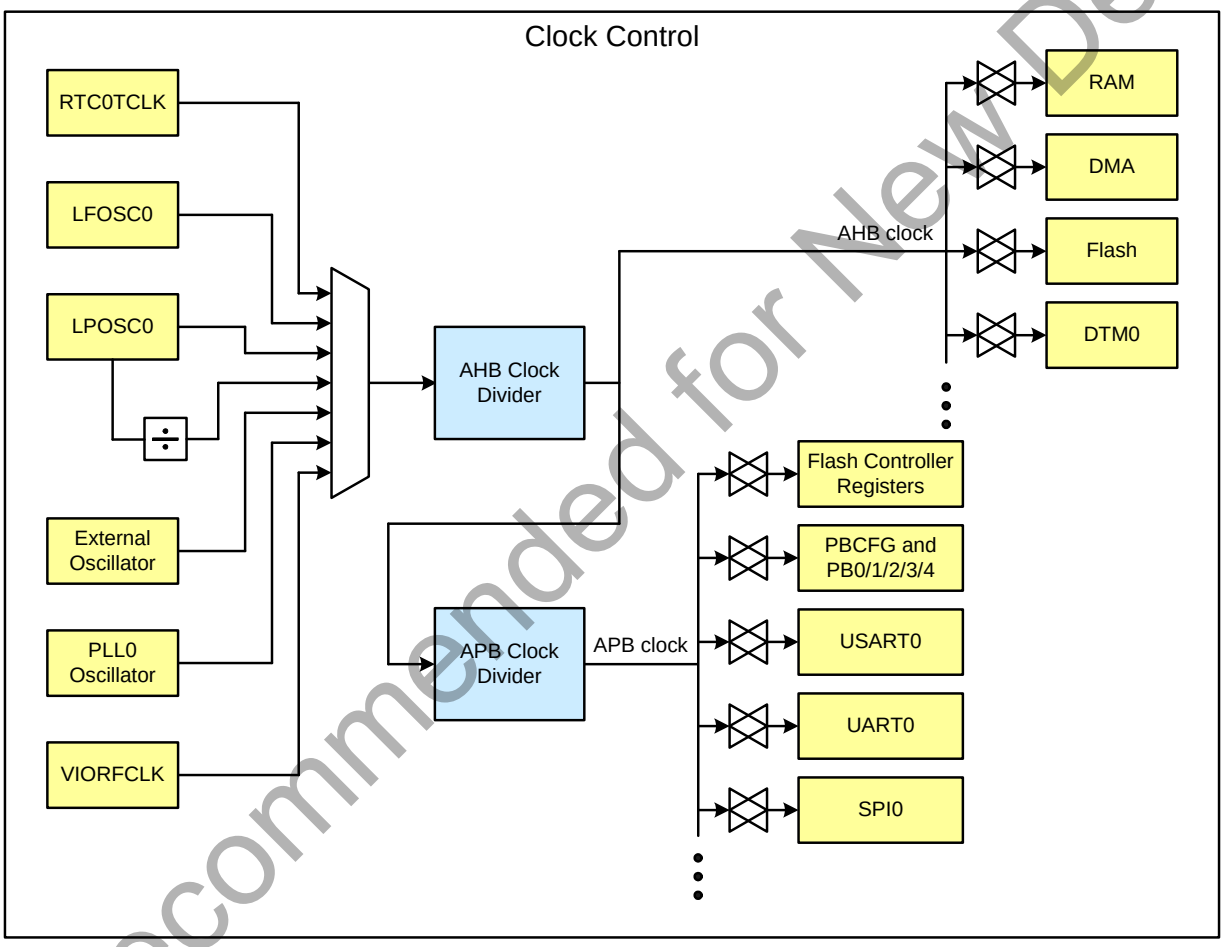

Figure 4.3. SiM3L1xx Clocking

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4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Three output ranges with output frequencies ranging from 23 to 50 MHz.
- Multiple reference frequency inputs, including the RTC0 oscillator, Low Power Oscillator, and external oscillator.
- Three output modes: Free-Running Digitally-Controlled Oscillator, Frequency-Locked, and Phase-Locked.
- Able to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.\
- All output frequency updates (including dithering and spectrum spreading) can be temporarily suspended using the STALL bit during noise-sensitive measurements.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3L1xx devices and enables or disables automatically, as needed.

The default output frequency of this oscillator is factory calibrated to 20 MHz, and a divided 2.5 MHz version of this clock is also available as an AHB clock source.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC) provides a low power internal clock source for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator, and the RTC1 and RTC2 pins do not need to be shorted together.

The Low Frequency Oscillator has the following features:

- 16.4 kHz output frequency.

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, resonator, RC, C, or CMOS oscillators.
- Support for external CMOS frequencies from 10 kHz to 50 MHz.
- Support for external crystal frequencies from 10 kHz to 25 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

Not Recommended for New Designs

4.4. Integrated LCD Controller (LCD0)

SiM3L1xx devices contain an LCD segment driver and on-chip bias generation that supports static, 2-mux, 3-mux and 4-mux LCDs with 1/2 or 1/3 bias. The on-chip charge pump with programmable output voltage allows software contrast control which is independent of the supply voltage. LCD timing is derived from the RTC timer clock (RTC0TCLK) to allow precise control over the refresh rate.

The SiM3L1xx devices use registers to store the enabled/disabled state of individual LCD segments. All LCD waveforms are generated on-chip based on the contents of these registers with flexible waveform control to reduce power consumption wherever possible. An LCD blinking function is also supported on a subset of LCD segments.

The LCD0 module has the following features:

- Up to 40 segment pins and 4 common pins.
- Supports LCDs with 1/2 or 1/3 bias.
- Includes an on-chip charge pump with programmable output that allows firmware to control the contrast independent of the supply voltage.
- The RTC timer clock (RTC0TCLK) determines the LCD timing and refresh rate.
- All LCD waveforms are generated on-chip based on the contents of the LCD0 registers with flexible waveform control.
- LCD segments can be placed in a discharge state for a configurable number of RTC clock cycles before switching to the next state to reduce power consumption due to display loading.
- Includes a VBAT monitor that can serve as a wakeup source for Power Mode 8.
- Supports four hardware auto-contrast modes: bypass, constant, minimum, and auto-bypass.
- Supports hardware blinking for up to 8 segments.

Not Recommended for New Designs

4.5. Data Peripherals

4.5.1. 10-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 10 channels.
- DMA crossbar supports DTM0, DTM1, DTM2, SARADC0, IDAC0, I2C0, SPI0, SPI1, USART0, AES0, ENCDEC0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.5.2. Data Transfer Managers (DTM0, DTM1, DTM2)

The Data Transfer Manager is a module that collects DMA request signals from various peripherals and generates a series of master DMA requests based on a state-driven configuration. This master request drives a set of DMA channels to perform functions such as assembling and transferring communication packets to external devices. This capability saves power by allowing the core to remain in a low power mode during complex transfer operations. A combination of simple and peripheral scatter-gather DMA configurations can be used to perform complex operations while reducing memory requirements.

The DTM acts as a side channel for the peripheral's DMA control signals. When active, it manages the DMA control signals for the peripherals. When the DTMn module is inactive, the peripherals communicate directly to the DMA module.

The DTMn module has the following features:

- State descriptions stored in RAM with up to 15 states supported per module.
- Supports up to 15 source peripherals and up to 15 destination peripherals per module, in addition to memory or peripherals that do not require a data request.
- Includes error detection and an optional transfer timeout.
- Includes notifications for state transitions.

4.5.3. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for multiple 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Electronic Codebook (ECB), Cipher-Block Chaining (CBC), and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

Not Recommended for New Designs

4.5.4. 16/32-bit Enhanced CRC (ECRC0)

The ECRC module is designed to provide hardware calculations for flash memory verification and communications protocols. In addition to calculating a result from direct writes from firmware, the ECRC module can automatically snoop the APB bus and calculate a result from data written to or read from a particular peripheral. This allows for an automatic CRC result without directly feeding data through the ECRC module.

The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The 16-bit polynomial is fully programmable.

The ECRC module includes the following features:

- Support for a programmable 16-bit polynomial and one fixed 32-bit polynomial.
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32-, 16-, or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Automatic APB bus snooping.
- Support for DMA writes using firmware request mode.

4.5.5. Encoder / Decoder (ENCDEC0)

The encoder / decoder module supports Manchester and Three-out-of-Six encoding and decoding from either firmware or DMA operations.

This module has the following features:

- Supports Manchester and Three-out-of-Six encoding and decoding.
- Automatic flag clearing when writing the input or reading the output data registers.
- Writing to the input data register automatically initiates an encode or decode operation.
- Optional output in one’s complement format.
- Hardware error detection for invalid input data during decode operations, which helps reduce power consumption and packet turn-around time.
- Flexible byte swapping on the input or output data.

Not Recommended for New Designs

4.6. Counters/Timers

4.6.1. 32-bit Timer (TIMER0, TIMER1, TIMER2)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.

TIMER0 and TIMER1 have the following features:

- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Period and duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

TIMER2 does not support the standard input/output features of TIMER0 and TIMER1. The TIMER2 EX signal is internally connected to the outputs of the PVTOSC0 oscillators. TIMER2 can use any of the counting modes that use EX as an input, including up/down mode, edge capture mode, and pulse capture mode. The TIMER2 CT signal is disconnected.

4.6.2. Enhanced Programmable Counter Array (EPCA0)

The Enhanced Programmable Counter Array (EPCA) module is a timer/counter system allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

This module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers.
- Pulse-Width Modulation (PWM) waveform generation.

Not Recommended for New Designs

4.6.3. Real-Time Clock (RTC0)

The RTC module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3L1xx devices.

The RTC module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC timer clock can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal Low Frequency Oscillator or with an external 32.768 kHz crystal (no additional resistors or capacitors necessary).
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- The RTC timer clock (RTC0CLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.
- The RTC module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER) module runs from the RTC timer clock (RTC0CLK), allowing the LPTIMER to operate even if the AHB and APB clocks are disabled. The LPTIMER counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on low-frequency RTC timer clock (RTC0TCLK).
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.
- Supports PWM with configurable period and duty cycle.
- The LPTIMER module can be powered from the low power mode charge pump for lowest possible power consumption while in PM8.

4.6.5. Watchdog Timer (WDTIMER0)

The WDTIMER module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

Not Recommended for New Designs

4.6.6. Low Power Mode Advanced Capture Counter (ACCTR0)

The SiM3L1xx devices contain a low-power Advanced Capture Counter module that runs from the RTC0 clock domain and can be used with digital inputs, switch topology circuits (reed switches), or with LC resonant circuits. For switch topology circuits, the module charges one or two external lines by pulsing internal pull-up resistors and detecting whether the reed switch is open or closed. For LC resonant circuits, the inputs are periodically energized to produce a dampened sine wave and configurable discriminator circuits detect the resulting decay time-constant.

The advanced capture counter has the following general features:

- Single or differential inputs supporting single, dual, and quadrature modes of operation.
- Variety of interrupt and PM8 wake up sources.
- Provides feedback of the direction history, current and previous states, and condition flags.

The advanced capture counter has the following features for switch circuit topologies:

- Ultra low power input comparators.
- Supports a wide range of pull-up resistor values with a self-calibration engine.
- Asymmetrical integrators for low-pass filtering and switch debounce.
- Two 24-bit counters and two 24-bit digital threshold comparators.
- Supports switch flutter detection.

For LC resonant circuit topologies, the advanced capture counter includes:

- Separate minimum and maximum count registers and polarity, pulse, and toggle controls.
- Zone-based programmable timing.
- Two input comparators with support for a positive side input bias at VIO divided by 2.
- Supports a configurable excitation pulse width based on a 40 MHz oscillator and timer or an external digital stop signal.
- Two 8-bit peak counters that saturate at full scale for detecting the number of LC resonant peaks.
- Two discriminators with programmable thresholds.
- Supports a sample and hold mode for Wheatstone bridges.

All devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0). Table 4.2 lists the supported inputs and outputs for each of the packages.

Table 4.2. SiM3L1xx Supported Advanced Capture Counter Inputs and Outputs

Input/Output	SiM3L1x7	SiM3L1x6	SiM3L1x4
ACCTR0_IN0	✓	✓	✓
ACCTR0_IN1	✓	✓	✓
ACCTR0_LCIN0	✓	✓	
ACCTR0_LCIN1	✓	✓	✓
ACCTR0_STOP0	✓	✓	✓
ACCTR0_STOP1	✓	✓	✓
ACCTR0_LCPUL0	✓	✓	
ACCTR0_LCPUL1	✓	✓	
ACCTR0_LCBIAS0	✓	✓	
ACCTR0_LCBIAS1	✓	✓	
ACCTR0_DBG0	✓	✓	
ACCTR0_DBG1	✓	✓	

Not Recommended for New Designs

4.7. Communications Peripherals

4.7.1. USART (USART0)

The USART uses two signals (TX and RX) to communicate serially with an external device. In addition to these signals, the USART module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.7.2. UART (UART0)

The low-power UART uses two signals (TX and RX) to communicate serially with an external device.

The UART0 module can operate in PM8 mode by taking the clock directly from the RTC0 time clock (RTC0TCLK) and running from the low power mode charge pump. This will allow the system to conserve power while transmitting or receiving UART traffic. The UART supports standard baud-rates of 9600, 4800, 2400 and 1200 in this low power mode.

The UART0 module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX).
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Independent inversion correction for TX and RX signals.
- Parity error, frame error, overrun, and underrun detection.
- Half-duplex support.

Not Recommended for New Designs

- Multiple loop-back modes supported.
- Multi-processor communications support.
- Operates at 9600, 4800, 2400, or 1200 baud in Power Mode 8.

4.7.3. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI0 and SPI1 modules include the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Support for multiple masters on the same data lines.

In addition, the SPI modules include several features to support autonomous DMA transfers:

- Hardware NSS control.
- Programmable FIFO threshold levels.
- Configurable FIFO data widths.
- Master or slave hardware flow control for the MISO and MOSI signals.

SPI1 is on fixed pins and supports additional flow control options using a fixed input (SPI1CTS). Neither SPI1 nor the flow control input are on the crossbar.

4.7.4. I2C (I2C0)

The I2C interface is a two-wire, bi-directional serial bus. The clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C0 module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.
- Spike suppression up to 2 times the APB period.

Not Recommended for New Designs

4.8. Analog

4.8.1. 12-Bit Analog-to-Digital Converter (SARADC0)

The SARADC0 module on SiM3L1xx devices implements the Successive Approximation Register (SAR) ADC architecture. The key features of the module are as follows:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- DC offset cancellation.
- Automatic result notification with multiple programmable thresholds.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Non-burst mode operation can also automatically accumulate multiple conversions, but a conversion start is required for each conversion.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to eight sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.8.2. 10-Bit Digital-to-Analog Converter (IDAC0)

The IDAC module takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O and on demand output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources.
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

4.8.3. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The low power comparator module includes the following features:

- Multiple sources for the positive and negative inputs, including VBAT, VREF, and 8 I/O pins.
- Two outputs available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- 6-bit programmable reference divider.

Not Recommended for New Designs

4.9. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- AHB peripheral clocks to flash and RAM are enabled.
- Clocks to all APB peripherals other than the Watchdog Timer and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VBAT Supply Monitor and power-on resets, the RESET pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the low frequency oscillator as its clock source. Program execution begins at location 0x00000000.

All RSTSRC0 registers may be locked against writes by setting the CLKRSTL bit in the LOCK0_PERIPHLOCK0 register to 1.

The reset sources can also optionally reset individual modules, including the low power mode charge pump, UART0, LCD0, advanced capture counter (ACCTR0), and RTC0.

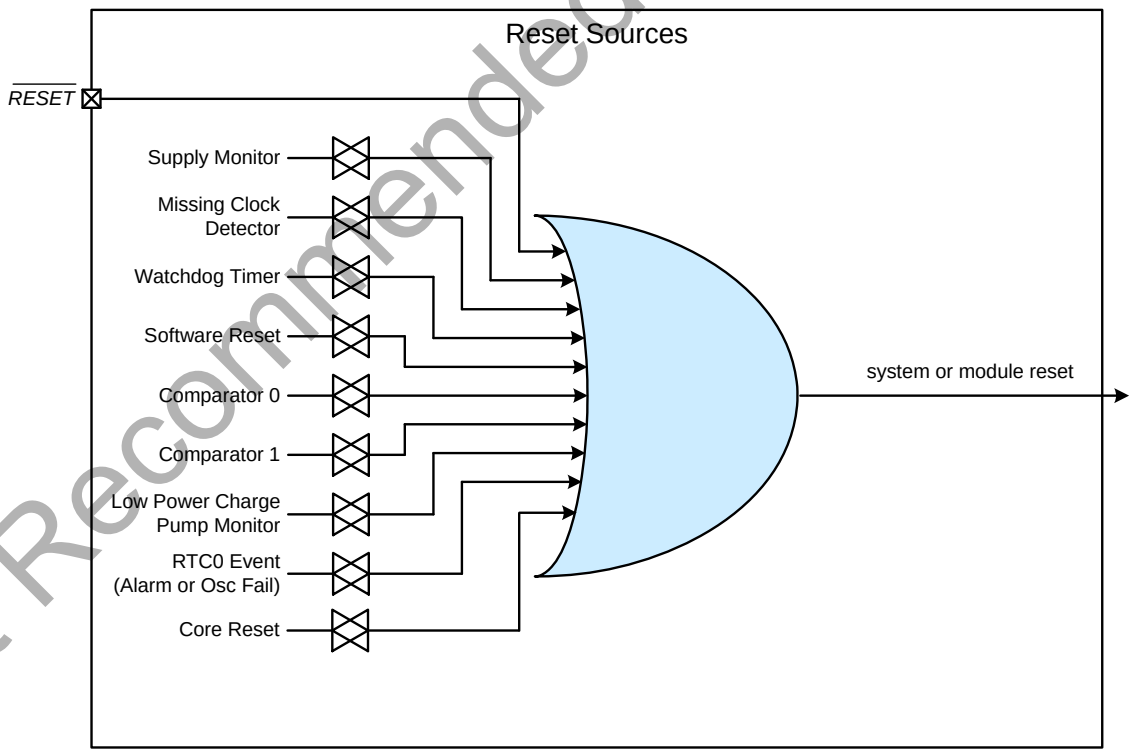

Figure 4.4. SiM3L1xx Reset Sources Block Diagram

Not Recommended for New Designs

4.10. Security

The peripherals on the SiM3L1xx devices have a register lock and key mechanism that prevents undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written to the KEY register to modify bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can be read, regardless of the peripheral's lock state.

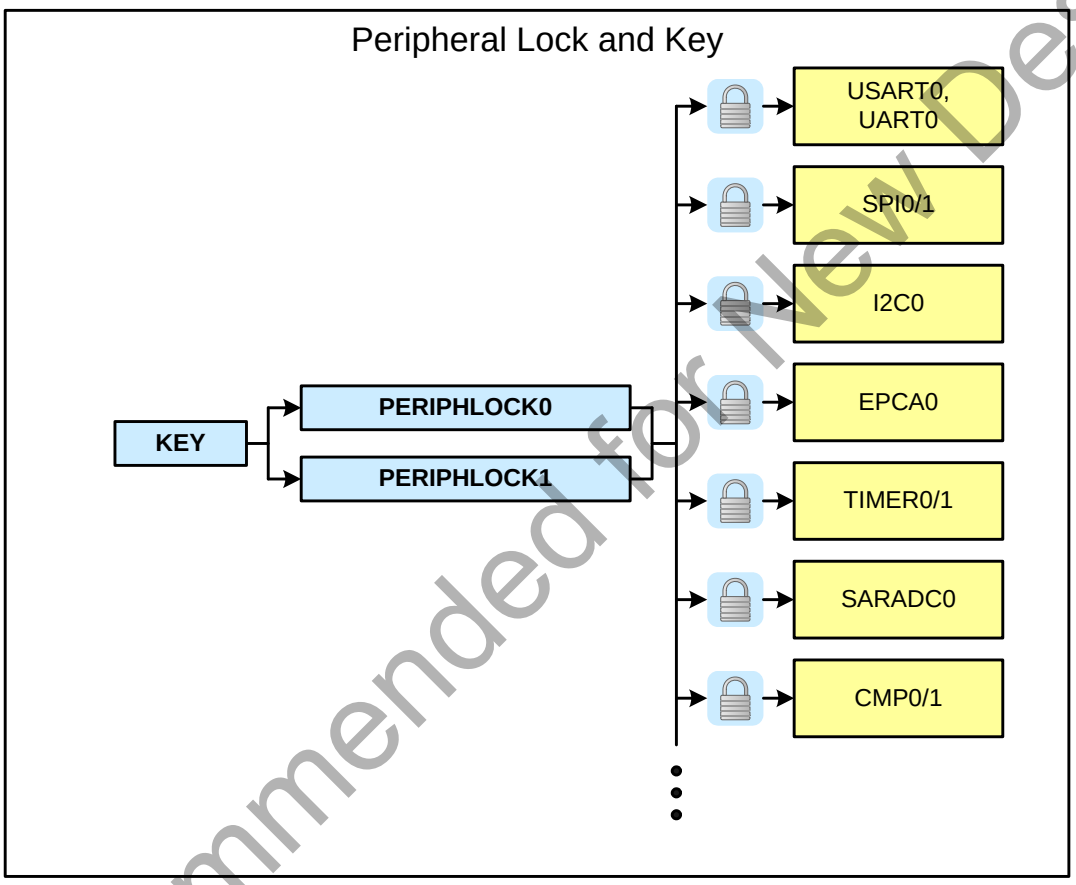

Figure 4.5. SiM3L1xx Security Block Diagram

4.11. On-Chip Debugging

The SiM3L1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3L1x7 devices only, and does not include boundary scan capabilites. The ETM interface is supported on SiM3L1x7, and SiM3L1x6 devices only. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages. Serial Wire Viewer is supported on all SiM3Lxxx devices.

Most peripherals on SiM3L1xx devices have the option to halt or continue functioning when the core halts in debug mode.

Not Recommended for New Designs

5. Ordering Information

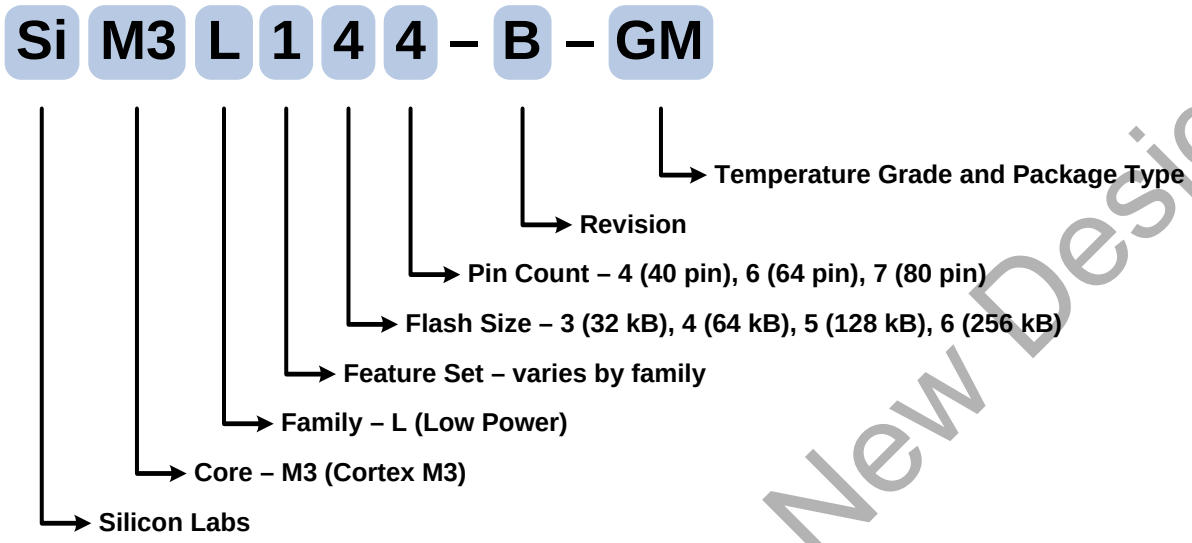

Figure 5.1. SiM3L1xx Part Numbering

All devices in the SiM3L1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 50 MHz.
- **PLL.**
- **10-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Encoder/Decoder.**
- **DC-DC Buck Converter.**
- **Timers:** 3 x 32-bit (6 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced)
- **ADC:** 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **Comparator:** 2 x low current.
- **Serial Buses:** 2 x USART, 2 x SPI, 1 x I2C

Additionally, all devices in the SiM3L1xx family include the low power mode advanced capture counter (ACCTR0), though the smaller packages (SiM3L1x4) only support some of the external inputs and outputs.

Not Recommended for New Designs

Table 5.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	LCD Segments	Digital Port I/Os	Digital Port I/Os on the Crossbar	Number of SARADC0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	Number of ACCTR0 Inputs and Outputs	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Lead-free (RoHS Compliant)	Package
SiM3L167-C-GQ	256	32	160 (4x40)	62	38	24	15/15	14	12	✓	✓	✓	✓	TQFP-80
SiM3L166-C-GM	256	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L166-C-GQ	256	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L164-C-GM	256	32		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L157-C-GQ	128	32	160 (4x40)	62	38	24	15/15	14	12	✓	✓	✓	✓	TQFP-80
SiM3L156-C-GM	128	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L156-C-GQ	128	32	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L154-C-GM	128	32		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L146-C-GM	64	16	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L146-C-GQ	64	16	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L144-C-GM	64	16		28	26	20	9/10	11	5			✓	✓	QFN-40
SiM3L136-C-GM	32	8	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	QFN-64
SiM3L136-C-GQ	32	8	128 (4x32)	51	34	23	14/12	11	12		✓	✓	✓	TQFP-64
SiM3L134-C-GM	32	8		28	26	20	9/10	11	5			✓	✓	QFN-40

Not Recommended for New Designs

6. Pin Definitions

6.1. SiM3L1x7 Pin Definitions

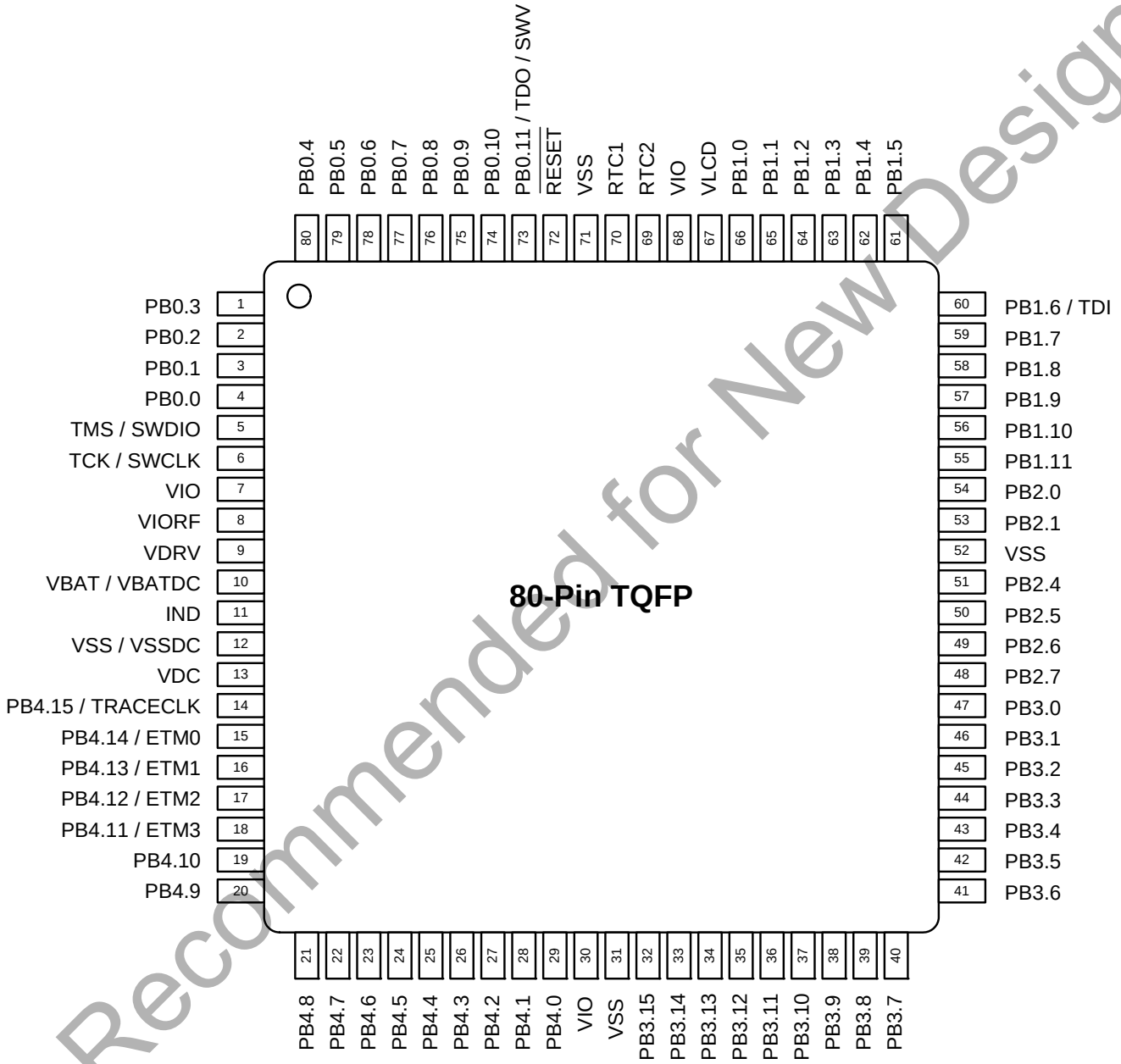

Figure 6.1. SiM3L1x7-GQ Pinout

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	12 31 52 71							
VSSDC	Ground (DC-DC)	12							
VIO	Power (I/O)	7 30 68							
VIORF	Power (RF I/O)	8							
VBAT/ VBATDC		10							
VDRV		9							
VDC		13							
VLCD	Power (LCD Charge Pump)	67							
IND	DC-DC Inductor	11							
$\overline{\text{RESET}}$	Active-low Reset	72							
TCK/ SWCLK	JTAG / Serial Wire	6							
TMS/ SWDIO	JTAG / Serial Wire	5							
RTC1	RTC Oscillator Input	70							
RTC2	RTC Oscillator Output	69							

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.0	Standard I/O	4	VIO	✓	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	3	VIO	✓	✓		✓	INT0.1 WAKE.1	ADC0.21 VREFGND CMP0N.0
PB0.2	Standard I/O	2	VIO	✓	✓		✓	INT0.2 WAKE.2	ADC0.22 CMP1P.0 XTAL2
PB0.3	Standard I/O	1	VIO	✓	✓		✓	INT0.3 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.4	Standard I/O	80	VIO	✓	✓		✓	INT0.4 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.5	Standard I/O	79	VIO	✓	✓		✓	INT0.5 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.6	Standard I/O	78	VIO	✓	✓		✓	INT0.6 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.7	Standard I/O	77	VIO	✓	✓		✓	INT0.7 WAKE.7	ACCTR0_LCIN0
PB0.8	Standard I/O	76	VIO	✓	✓		✓	LPT0T0 LPT0OUT0 INT0.8 WAKE.8	ACCTR0_LCIN1

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.9	Standard I/O	75	VIO	✓	✓		✓	LPT0T1 INT0.9 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.10	Standard I/O	74	VIO	✓	✓		✓	LPT0T2 INT0.10 WAKE.10 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB0.11/ TDO/SWV	Standard I/O / JTAG / Serial Wire Viewer	73	VIO	✓	✓		✓	LPT0T3 LPT0OUT1 INT0.11 WAKE.11	ADC0.3 CMP1N.1
PB1.0	Standard I/O	66	VIO	✓	✓	LCD0.39		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2
PB1.1	Standard I/O	65	VIO	✓	✓	LCD0.38		LPT0T5 INT0.13 ACCTR0_LCBIAS1	CMP0N.2
PB1.2	Standard I/O	64	VIO	✓	✓	LCD0.37		LPT0T6 INT0.14 UART0_TX	CMP1P.2
PB1.3	Standard I/O	63	VIO	✓	✓	LCD0.36		LPT0T7 INT0.15 UART0_RX	CMP1N.2
PB1.4	Standard I/O	62	VIO	✓	✓	LCD0.35		ACCTR0_DBG0	ADC0.4
PB1.5	Standard I/O	61	VIO	✓	✓	LCD0.34		ACCTR0_DBG1	ADC0.5
PB1.6/TDI	Standard I/O / JTAG	60	VIO	✓	✓	LCD0.33			ADC0.6
PB1.7	Standard I/O	59	VIO	✓	✓	LCD0.32		RTC0TCLK_OUT	ADC0.7

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB1.8	Standard I/O	58	VIO	✓	✓	LCD0.31			CMP0P.3
PB1.9	Standard I/O	57	VIO	✓	✓	LCD0.30			CMP0N.3
PB1.10	Standard I/O	56	VIO	✓	✓	LCD0.29			CMP1P.3
PB1.11	Standard I/O	55	VIO	✓	✓	LCD0.28			CMP1N.3
PB2.0	Standard I/O	54	VIORF	✓	✓			LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.8 CMP0P.4
PB2.1	Standard I/O	53	VIORF	✓	✓			LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.9 CMP0N.4
PB2.4	Standard I/O	51	VIORF	✓	✓			LPT0T12 INT1.4 SPI1_SCLK	ADC0.10 CMP0P.5
PB2.5	Standard I/O	50	VIORF	✓	✓			LPT0T13 INT1.5 SPI1_MISO	ADC0.11 CMP0N.5
PB2.6	Standard I/O	49	VIORF	✓	✓			LPT0T14 INT1.6 SPI1_MOSI	ADC0.12 CMP1P.5
PB2.7	Standard I/O	48	VIORF	✓	✓			INT1.7 SPI1_NSS	ADC0.13 CMP1N.5
PB3.0	Standard I/O	47	VIO	✓	✓	LCD0.27		INT1.8	ADC0.14
PB3.1	Standard I/O	46	VIO	✓	✓	LCD0.26		INT1.9	ADC0.15
PB3.2	Standard I/O	45	VIO	✓	✓	LCD0.25		INT1.10	ADC0.16
PB3.3	Standard I/O	44	VIO	✓	✓	LCD0.24		INT1.11	ADC0.17

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.4	Standard I/O	43	VIO	✓	✓	LCD0.23		INT1.12	CMP0P.6
PB3.5	Standard I/O	42	VIO	✓	✓	LCD0.22		INT1.13	CMP0N.6
PB3.6	Standard I/O	41	VIO	✓	✓	LCD0.21		INT1.14	CMP1P.6
PB3.7	Standard I/O	40	VIO	✓	✓	LCD0.20		INT1.15	CMP1N.6
PB3.8	Standard I/O	39	VIO		✓	LCD0.19			CMP0P.7
PB3.9	Standard I/O	38	VIO		✓	LCD0.18			CMP0N.7
PB3.10	Standard I/O	37	VIO		✓	LCD0.17			CMP1P.7
PB3.11	Standard I/O	36	VIO		✓	LCD0.16			CMP1N.7
PB3.12	Standard I/O	35	VIO		✓	LCD0.15			ADC0.18
PB3.13	Standard I/O	34	VIO		✓	LCD0.14			ADC0.19
PB3.14	Standard I/O	33	VIO		✓	COM0.3			
PB3.15	Standard I/O	32	VIO		✓	COM0.2			
PB4.0	Standard I/O	29	VIO		✓	COM0.1			
PB4.1	Standard I/O	28	VIO		✓	COM0.0			
PB4.2	Standard I/O	27	VIO		✓	LCD0.13			
PB4.3	Standard I/O	26	VIO		✓	LCD0.12			
PB4.4	Standard I/O	25	VIO		✓	LCD0.11			
PB4.5	Standard I/O	24	VIO		✓	LCD0.10			
PB4.6	Standard I/O	23	VIO		✓	LCD0.9		PMU_Asleep	
PB4.7	Standard I/O	22	VIO		✓	LCD0.8			
PB4.8	Standard I/O	21	VIO		✓	LCD0.7			

Not Recommended for New Designs

Table 6.1. Pin Definitions and Alternate Functions for SiM3L1x7 (Continued)

Pin Name	Type	Pin Numbers (TQFP-80)	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB4.9	Standard I/O	20	VIO		✓	LCD0.6			
PB4.10	Standard I/O	19	VIO		✓	LCD0.5			
PB4.11/ ETM3	Standard I/O / ETM	18	VIO		✓	LCD0.4			
PB4.12/ ETM2	Standard I/O / ETM	17	VIO		✓	LCD0.3			
PB4.13/ ETM1	Standard I/O / ETM	16	VIO		✓	LCD0.2			
PB4.14/ ETM0	Standard I/O / ETM	15	VIO		✓	LCD0.1			
PB4.15/ TRACE-CLK	Standard I/O / ETM	14	VIO		✓	LCD0.0			

Not Recommended for New Designs

6.2. SiM3L1x6 Pin Definitions

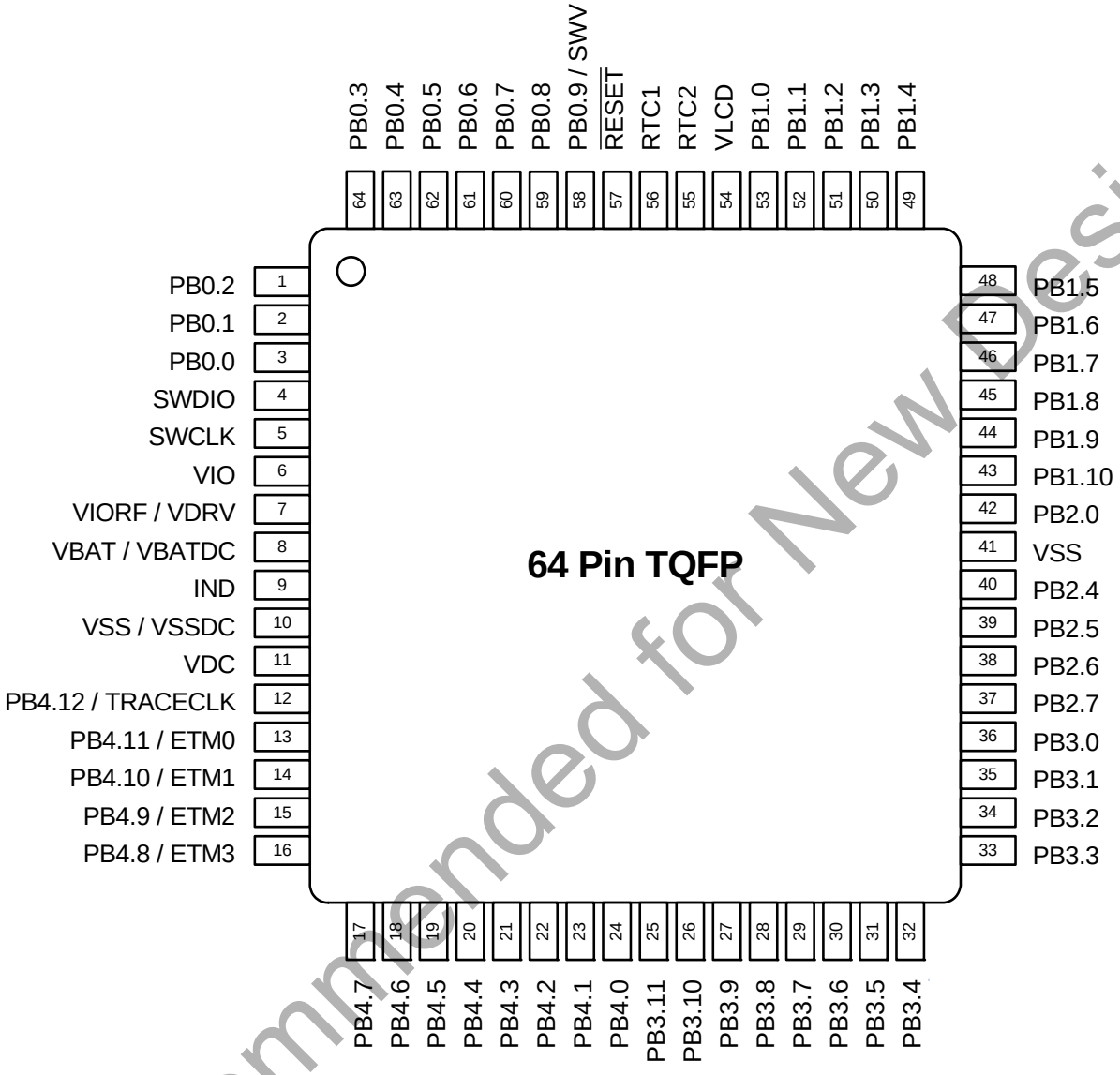

Figure 6.2. SiM3L1x6-GQ Pinout

Not Recommended for New Designs

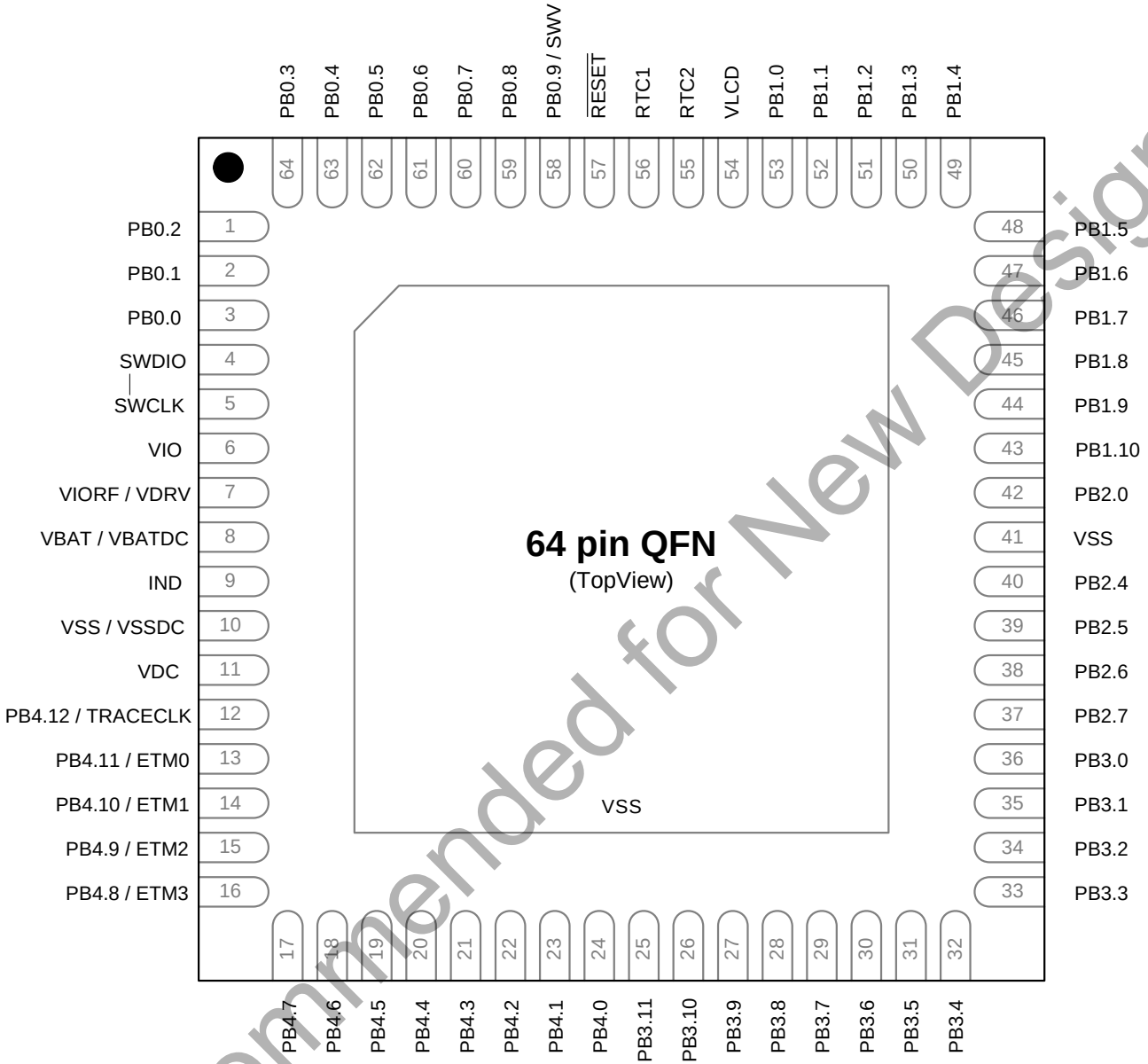

Figure 6.3. SiM3L1x6-GM Pinout

Not Recommended for New Designs

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	10 41							
VSSDC	Ground (DC-DC)	10							
VIO	Power (I/O)	6							
VIORF / VDRV	Power (RF I/O)	7							
VBAT / VBATDC		8							
VDC		11							
VLCD	Power (LCD Charge Pump)	54							
IND	DC-DC Inductor	9							
$\overline{\text{RESET}}$	Active-low Reset	57							
SWCLK	Serial Wire	5							
SWDIO	Serial Wire	4							
RTC1	RTC Oscillator Input	56							
RTC2	RTC Oscillator Output	55							
PB0.0	Standard I/O	3	VIO	XBR 0	✓		✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	2	VIO	XBR 0	✓		✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Not Recommended for New Designs

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	1	VIO	XBR 0	✓		✓	INT0.2 WAKE.3	ADC0.23 CMP1N.0 XTAL1
PB0.3	Standard I/O	64	VIO	XBR 0	✓		✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	63	VIO	XBR 0	✓		✓	INT0.4 WAKE.5 ACCTR0_STOP0	ACCTR0_IN0
PB0.5	Standard I/O	62	VIO	XBR 0	✓		✓	INT0.5 WAKE.6 ACCTR0_STOP1	ACCTR0_IN1
PB0.6	Standard I/O	61	VIO	XBR 0	✓		✓	INT0.6 WAKE.7	ACCTR0_LCIN0
PB0.7	Standard I/O	60	VIO	XBR 0	✓		✓	LPT0T0 LPT0OUT0 INT0.7 WAKE.8	ACCTR0_LCIN1
PB0.8	Standard I/O	59	VIO	XBR 0	✓		✓	LPT0T1 INT0.8 WAKE.9 ACCTR0_LCPUL0	ADC0.1 CMP0N.1
PB0.9/SWV	Standard I/O /Serial Wire Viewer	58	VIO	XBR 0	✓		✓	LPT0T2 INT0.9 WAKE.10 LPT0OUT1 ACCTR0_LCPUL1	ADC0.2 CMP1P.1
PB1.0	Standard I/O	53	VIO	XBR 0	✓	LCD0.31		LPT0T4 INT0.12 ACCTR0_LCBIAS0	CMP0P.2

Not Recommended for New Designs

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB1.1	Standard I/O	52	VIO	XBR0	✓	LCD0.30		LPT0T5 INT0.13 ACCTR0_LCBIAS1	CMP0N.2
PB1.2	Standard I/O	51	VIO	XBR0	✓	LCD0.29		LPT0T6 INT0.14 UART0_TX	CMP1P.2
PB1.3	Standard I/O	50	VIO	XBR0	✓	LCD0.28		LPT0T7 INT0.15 UART0_RX	CMP1N.2
PB1.4	Standard I/O	49	VIO	XBR0	✓	LCD0.27		ACCTR0_DBG0	ADC0.3
PB1.5	Standard I/O	48	VIO	XBR0	✓	LCD0.26		ACCTR0_DBG1	ADC0.4
PB1.6	Standard I/O	47	VIO	XBR0	✓	LCD0.25		RTC0TCLK_OUT	ADC0.5
PB1.7	Standard I/O	46	VIO	XBR0	✓	LCD0.24			CMP0P.3
PB1.8	Standard I/O	45	VIO	XBR0	✓	LCD0.23			CMP0N.3
PB1.9	Standard I/O	44	VIO	XBR0	✓	LCD0.22			CMP1P.3
PB1.10	Standard I/O	43	VIO	XBR0	✓	LCD0.21			CMP1N.3
PB2.0	Standard I/O	42	VIORF	XBR0	✓			LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.6 CMP0P.4
PB2.4	Standard I/O	40	VIORF	XBR0	✓			LPT0T12 INT1.4 SPI1_SCLK	ADC0.7 CMP0P.5

Not Recommended for New Designs

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.5	Standard I/O	39	VIORF	XBR0	✓			LPT0T13 INT1.5 SPI1_MISO	ADC0.8 CMP0N.5
PB2.6	Standard I/O	38	VIORF	XBR0	✓			LPT0T14 INT1.6 SPI1_MOSI	ADC0.9 CMP1P.5
PB2.7	Standard I/O	37	VIORF	XBR0	✓			INT1.7 SPI1_NSS	ADC0.10 CMP1N.5
PB3.0	Standard I/O	36	VIO	XBR0	✓	LCD0.20		INT1.8	ADC0.11
PB3.1	Standard I/O	35	VIO	XBR0	✓	LCD0.19		INT1.9	ADC0.12
PB3.2	Standard I/O	34	VIO	XBR0	✓	LCD0.18		INT1.10	CMP0P.6
PB3.3	Standard I/O	33	VIO	XBR0	✓	LCD0.17		INT1.11	CMP0N.6
PB3.4	Standard I/O	32	VIO	XBR0	✓	LCD0.16		INT1.12	CMP0P.7
PB3.5	Standard I/O	31	VIO	XBR0	✓	LCD0.15		INT1.13	CMP0N.7
PB3.6	Standard I/O	30	VIO	XBR0	✓	LCD0.14		INT1.14	CMP1P.7
PB3.7	Standard I/O	29	VIO	XBR0	✓	LCD0.13		INT1.15	CMP1N.7
PB3.8	Standard I/O	28	VIO		✓	LCD0.12			ADC0.13
PB3.9	Standard I/O	27	VIO		✓	LCD0.11			ADC0.14
PB3.10	Standard I/O	26	VIO		✓	COM0.3			
PB3.11	Standard I/O	25	VIO		✓	COM0.2			

Not Recommended for New Designs

Table 6.2. Pin Definitions and Alternate Functions for SiM3L1x6 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	LCD Interface	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB4.0	Standard I/O	24	VIO		✓	COM0.1			
PB4.1	Standard I/O	23	VIO		✓	COM0.0			
PB4.2	Standard I/O	22	VIO		✓	LCD0.10			ADC0.19
PB4.3	Standard I/O	21	VIO		✓	LCD0.9			
PB4.4	Standard I/O	20	VIO		✓	LCD0.8			
PB4.5	Standard I/O	19	VIO		✓	LCD0.7			
PB4.6	Standard I/O	18	VIO		✓	LCD0.6		PMU_Asleep	
PB4.7	Standard I/O	17	VIO		✓	LCD0.5			
PB4.8/ETM3	Standard I/O / ETM	16	VIO		✓	LCD0.4			
PB4.9/ETM2	Standard I/O / ETM	15	VIO		✓	LCD0.3			
PB4.10/ ETM1	Standard I/O / ETM	14	VIO		✓	LCD0.2			
PB4.11/ ETM0	Standard I/O / ETM	13	VIO		✓	LCD0.1			
PB4.12/ TRACECLK	Standard I/O / ETM	12	VIO		✓	LCD0.0			

Not Recommended for New Designs

6.3. SiM3L1x4 Pin Definitions

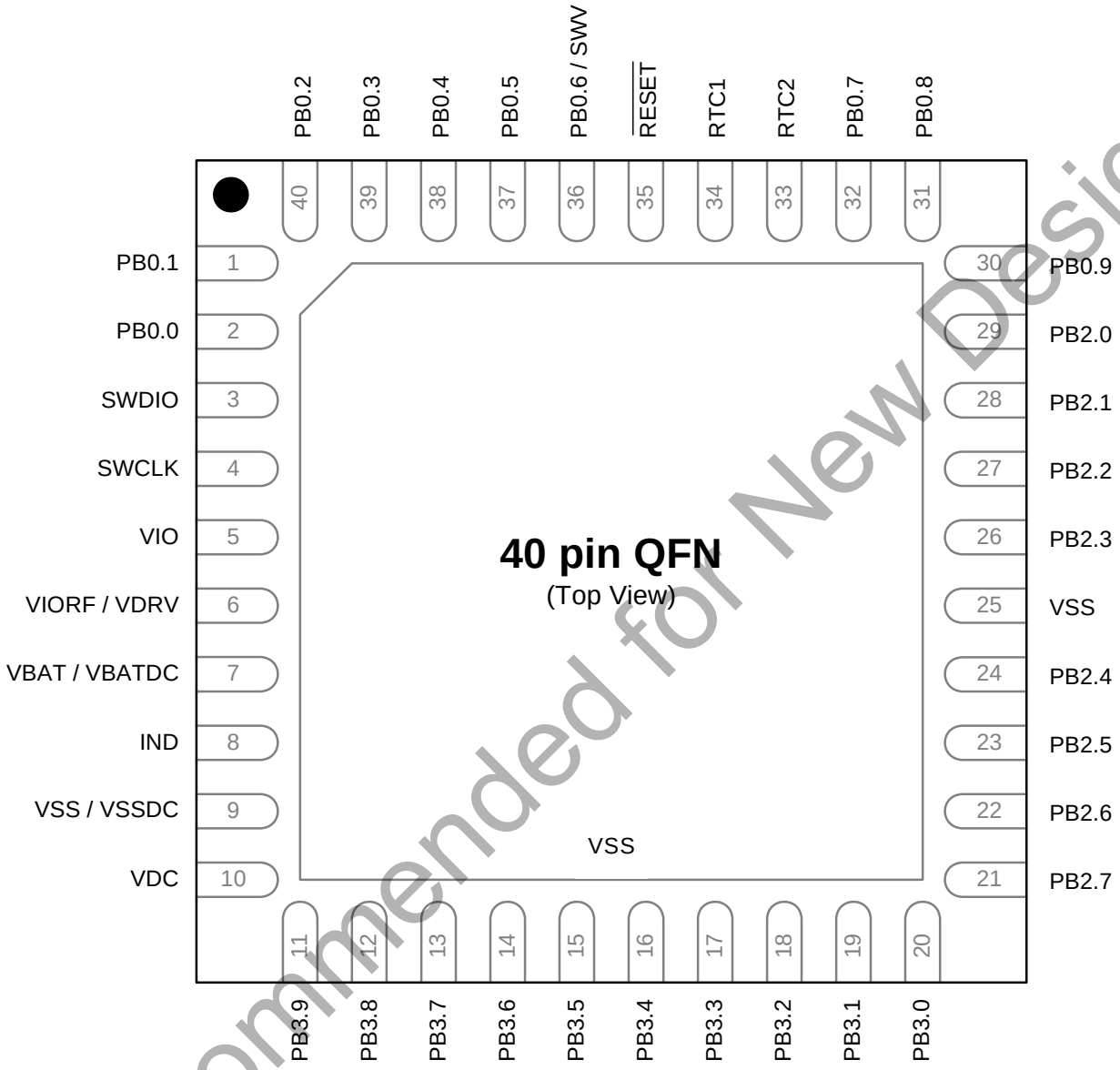

Figure 6.4. SiM3L1x4-GM Pinout

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
VSS	Ground	9 25						
VSSDC	Ground (DC-DC)	9						
VIO	Power (I/O)	5						
VIORF / VDRV	Power (RF I/O)	6						
VBAT / VBATDC		7						
VDC		10						
IND	DC-DC Inductor	8						
$\overline{\text{RESET}}$	Active-low Reset	35						
SWCLK	Serial Wire	4						
SWDIO	Serial Wire	3						
RTC1	RTC Oscillator Input	34						
RTC2	RTC Oscillator Output	33						
PB0.0	Standard I/O	2	VIO	XBR0	✓	✓	INT0.0 WAKE.0	ADC0.20 VREF CMP0P.0
PB0.1	Standard I/O	1	VIO	XBR0	✓	✓	INT0.1 WAKE.2	ADC0.22 CMP0N.0 CMP1P.0 XTAL2

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB0.2	Standard I/O	40	VIO	XBR0	✓	✓	INT0.2 WAKE.3	ADC0.23 CMP0N.1 CMP1N.0 XTAL1
PB0.3	Standard I/O	39	VIO	XBR0	✓	✓	INT0.3 WAKE.4	ADC0.0 CMP0P.1 IDAC0
PB0.4	Standard I/O	38	VIO	XBR0	✓	✓	INT0.4 WAKE.5	ACCTR0_IN0
PB0.5	Standard I/O	37	VIO	XBR0	✓	✓	INT0.5 WAKE.6	ACCTR0_IN1
PB0.6/SWV	Standard I/O /Serial Wire Viewer	36	VIO	XBR0	✓	✓	LPT0T0 LPT0OUT0 INT0.6 WAKE.8	
PB0.7	Standard I/O	32	VIO	XBR0	✓	✓	LPT0T6 INT0.7 UART0_TX	CMP1P.2
PB0.8	Standard I/O	31	VIO	XBR0	✓	✓	LPT0T7 INT0.8 UART0_RX	CMP1N.2
PB0.9	Standard I/O	30	VIO	XBR0	✓	✓	LPT0T1 INT0.9 RTC0TCLK_OUT	ADC0.1
PB2.0	Standard I/O	29	VIORF	XBR0	✓		LPT0T8 INT1.0 WAKE.12 SPI1_CTS	ADC0.2 CMP0P.4

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB2.1	Standard I/O	28	VIORF	XBR0	✓		LPT0T9 INT1.1 WAKE.13 VIORFCLK	ADC0.3 CMP0N.4
PB2.2	Standard I/O	27	VIORF	XBR0	✓		LPT0T10 INT1.2 WAKE.14	ADC0.4 CMP1P.4
PB2.3	Standard I/O	26	VIORF	XBR0	✓		LPT0T11 INT1.3 WAKE.15	ADC0.5 CMP1N.4
PB2.4	Standard I/O	24	VIORF	XBR0	✓		LPT0T12 INT1.4 SPI1_SCLK	ADC0.6 CMP0P.5
PB2.5	Standard I/O	23	VIORF	XBR0	✓		LPT0T13 INT1.5 SPI1_MISO	ADC0.7 CMP0N.5
PB2.6	Standard I/O	22	VIORF	XBR0	✓		LPT0T14 INT1.6 SPI1_MOSI	ADC0.8 CMP1P.5
PB2.7	Standard I/O	21	VIORF	XBR0	✓		INT1.7 SPI1_NSS	ADC0.9 CMP1N.5
PB3.0	Standard I/O	20	VIO	XBR0	✓		INT1.8	CMP0N.7
PB3.1	Standard I/O	19	VIO	XBR0	✓		INT1.9	CMP1P.7
PB3.2	Standard I/O	18	VIO	XBR0	✓		INT1.10	CMP1N.7
PB3.3	Standard I/O	17	VIO	XBR0	✓		INT1.11	ADC0.10
PB3.4	Standard I/O	16	VIO	XBR0	✓		INT1.12	ADC0.11
PB3.5	Standard I/O	15	VIO	XBR0	✓		INT1.13	ADC0.12

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3L1x4 (Continued)

Pin Name	Type	Pin Numbers	I/O Voltage Domain	Crossbar Capability	Port Match	Output Toggle Logic	External Trigger Inputs / Digital Functions	Analog Functions
PB3.6	Standard I/O	14	VIO	XBR0	✓		INT1.14	ADC0.13
PB3.7	Standard I/O	13	VIO	XBR0	✓		INT1.15	ADC0.14
PB3.8	Standard I/O	12	VIO		✓			ADC0.15
PB3.9	Standard I/O	11	VIO		✓			ADC0.16

Not Recommended for New Designs

6.4. TQFP-80 Package Specifications

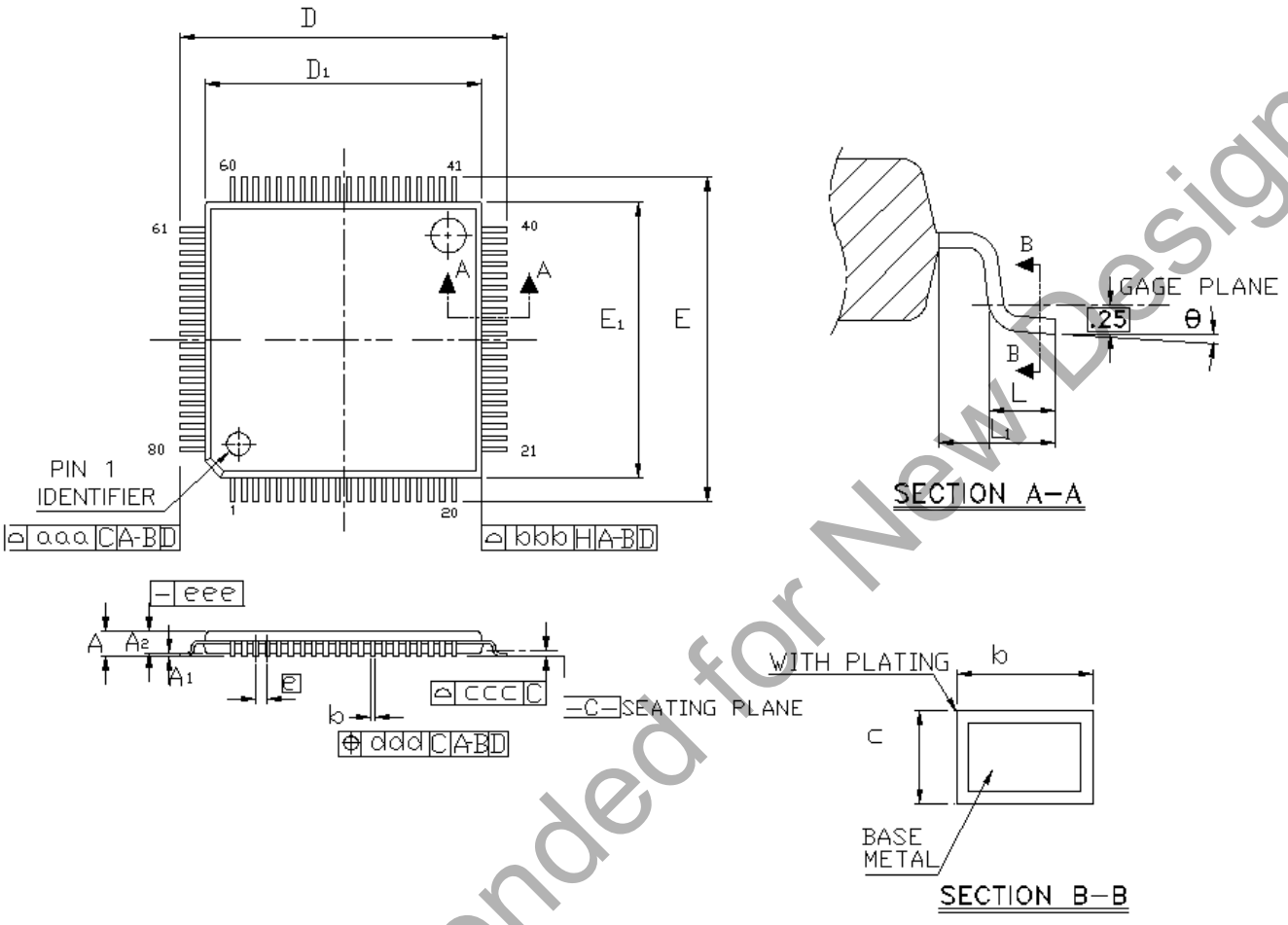

Figure 6.5. TQFP-80 Package Drawing

Not Recommended for New Designs

Table 6.4. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	1.00 Ref		
Θ	0°	3.5°	7°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

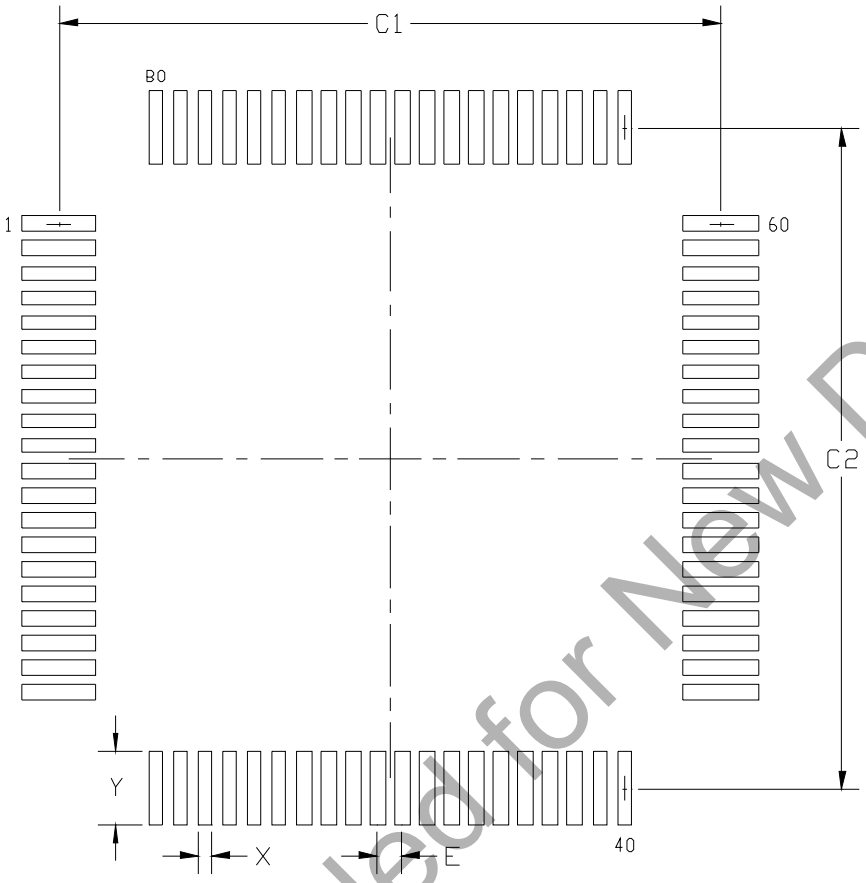

Figure 6.6. TQFP-80 Landing Diagram

Table 6.5. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Not Recommended for New Designs

6.4.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.4.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.4.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.5. QFN-64 Package Specifications

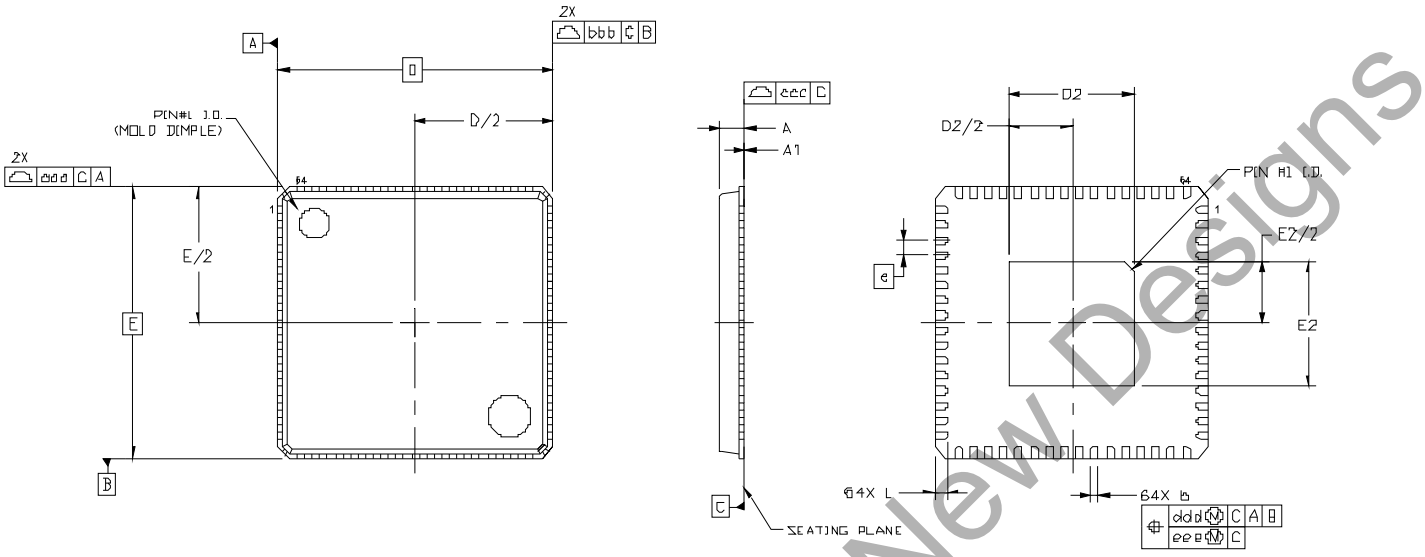

Figure 6.7. QFN-64 Package Drawing

Table 6.6. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

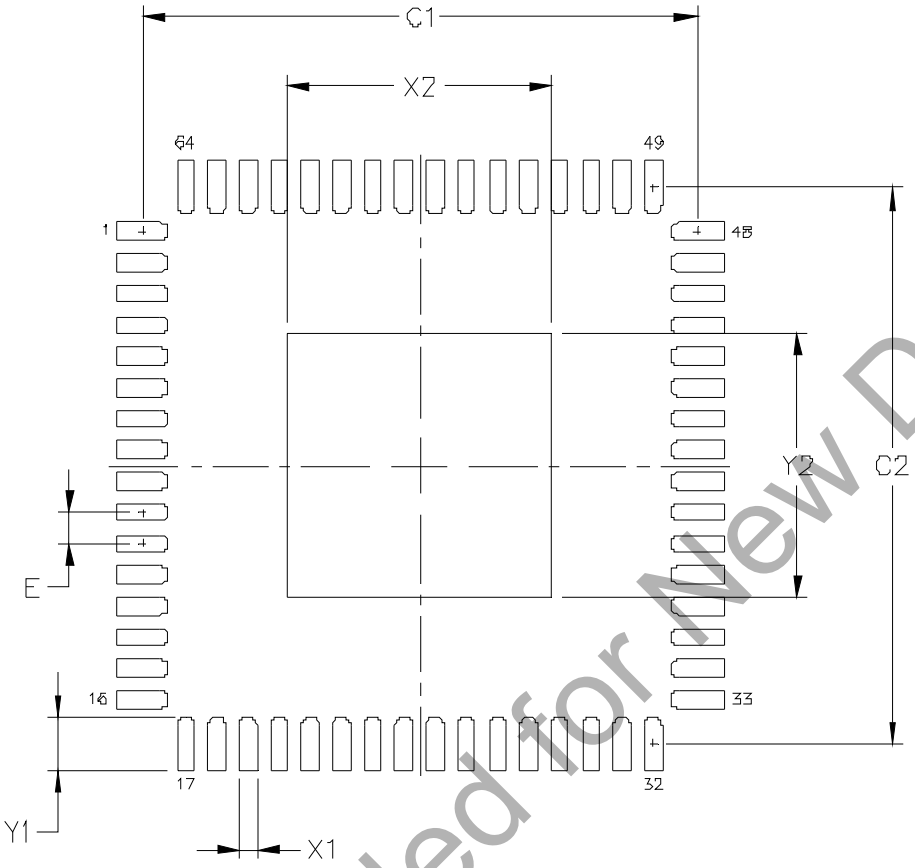

Figure 6.8. QFN-64 Landing Diagram

Table 6.7. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Not Recommended for New Designs

6.5.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.5.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.6. TQFP-64 Package Specifications

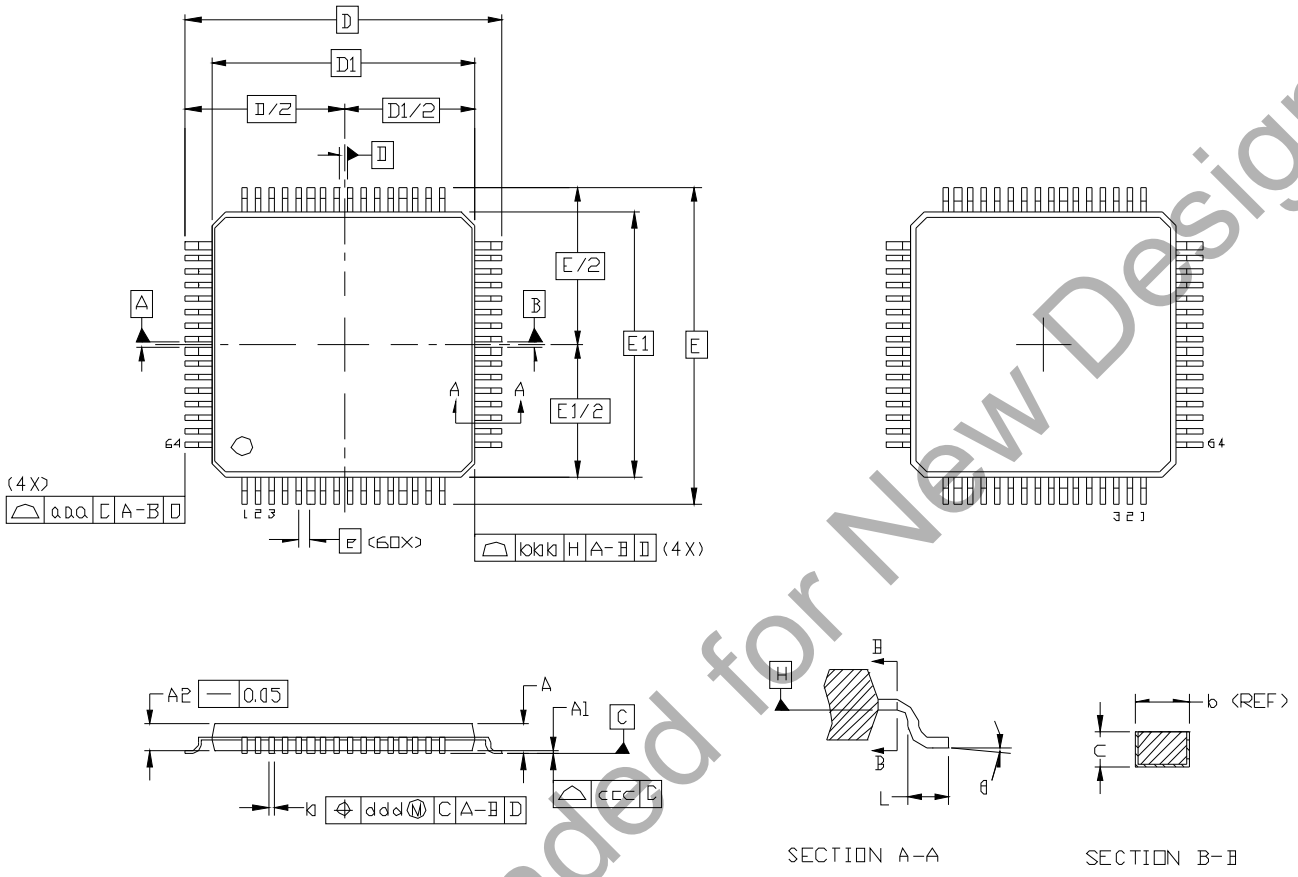

Figure 6.9. TQFP-64 Package Drawing

Not Recommended for New Designs

Table 6.8. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

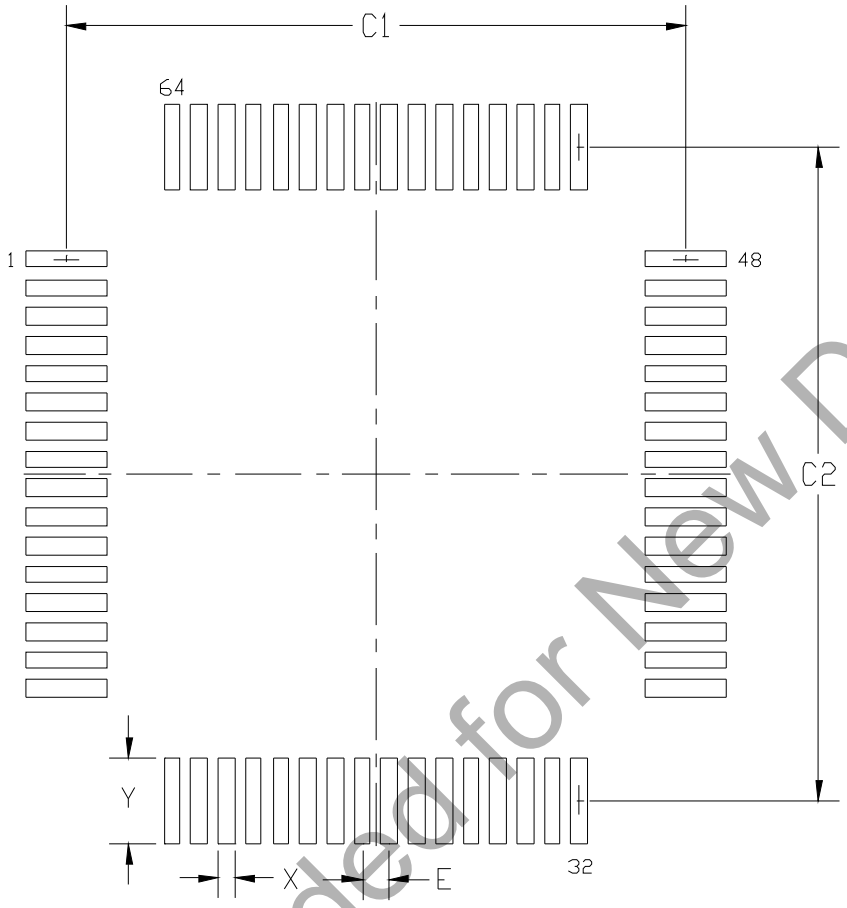

Figure 6.10. TQFP-64 Landing Diagram

Table 6.9. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Not Recommended for New Designs

6.6.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.6.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.7. QFN-40 Package Specifications

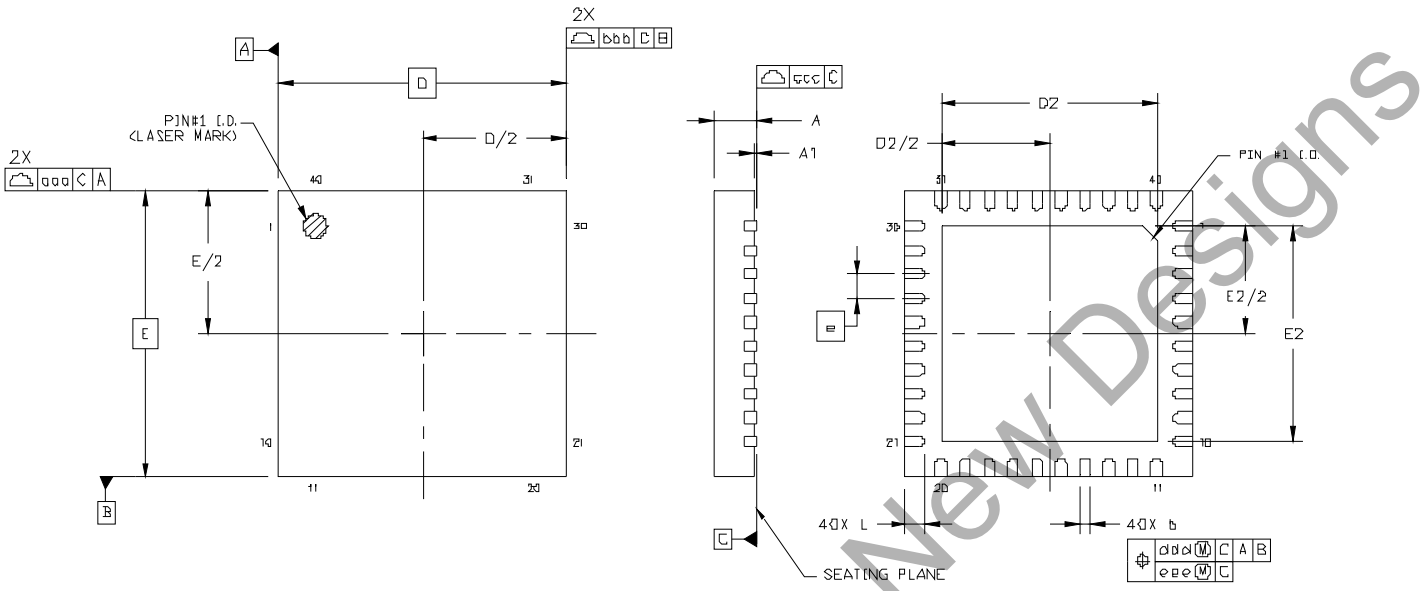

Figure 6.11. QFN-40 Package Drawing

Table 6.10. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

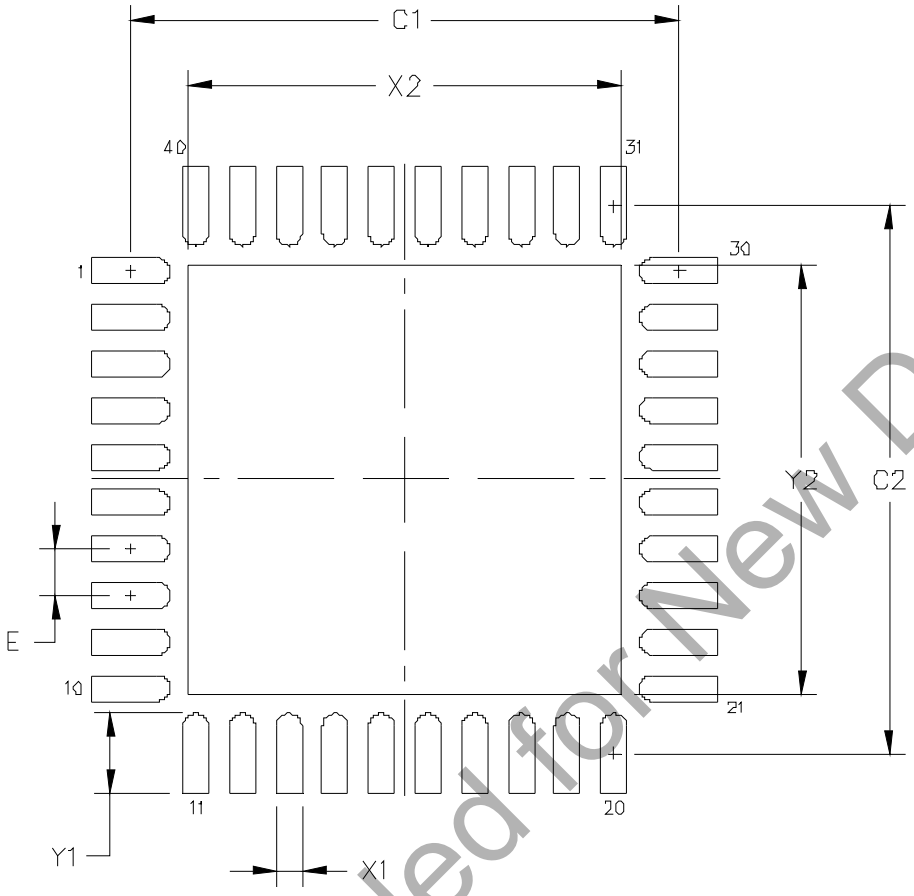

Figure 6.12. QFN-40 Landing Diagram

Table 6.11. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Not Recommended for New Designs

6.7.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.7.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

7. Revision Specific Behavior

This chapter describes any differences between released revisions of the device.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, and 7.3 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

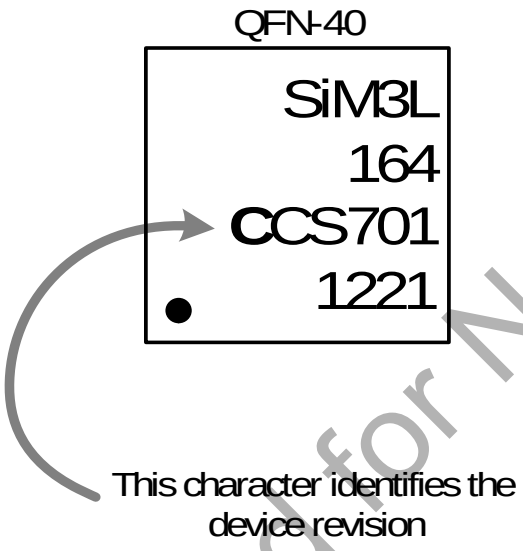

Figure 7.1. SiM3L1x7-GQ Revision Information

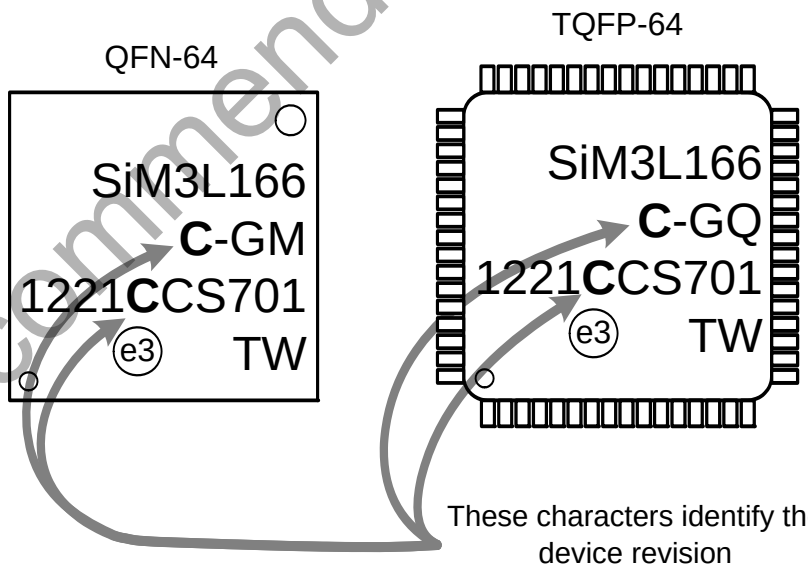

Figure 7.2. SiM3L1x6-GM and SiM3L1x6-GQ Revision Information

Not Recommended for New Designs

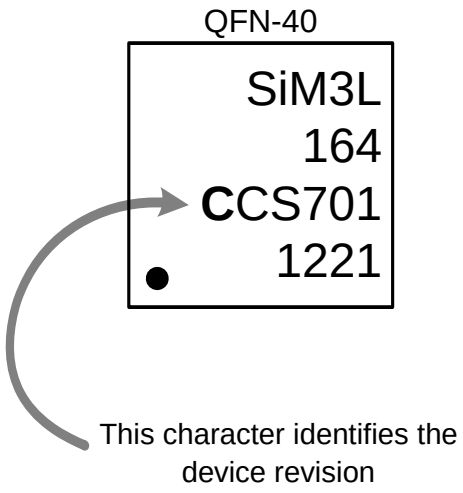

Figure 7.3. SiM3L1x4-GM Revision Information

Not Recommended for New Designs

Document Change List

Revision 0.5 to Revision 1.0

- Updated Electrical Specifications Tables with latest characterization data and production test limits.
- Added missing signal ACCTR0_LCPUL1 to Table 6.2, “Pin Definitions and Alternate Functions for SiM3L1x6,” on page 64.
- Removed ACCTR0_LCIN1 and ACCTR0_STOP0/1 signals from Table 6.3, “Pin Definitions and Alternate Functions for SiM3L1x4,” on page 70.
- Updated Figure 6.8, “TFBGA-80 Package Drawing,” on page 79.

Revision 1.0 to Revision 1.1

- Removed all references to BGA-80 and the parts SiM3L167-C-GL and SiM3L157-C-GL.

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