THE DATASHEET OF

SIM3C146-B-GMR

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SiM3C1xx

High-Performance, Low-Power, 32-Bit Precision32™ MCU Family with up to 256 kB of Flash

32-bit ARM® Cortex™-M3 CPU

- 80 MHz maximum frequency
- Single-cycle multiplication, hardware division support
- Nested vectored interrupt control (NVIC) with 16 priority levels

Memory

- 32–256 kB Flash, in-system programmable
- 8–32 kB SRAM (including 4 kB retention SRAM)
- 16-channel DMA controller
- External bus interface supports up to 16 MB of external memory and a parallel LCD interface with QVGA resolution

Power Management

- Low drop-out (LDO) regulator
- Power-on reset circuit and brownout detectors
- 5-to-3.3 V 150 mA regulator supports up to 5 V input supply
- Adjustable external regulator supports up to 3.6 V, 1000 mA
- Multiple power modes supported for low power optimization

Low Power Features

- 85 nA current mode with voltage supply monitor enabled
- Low-current RTC: 350 nA internal LFO, 620 nA external crystal
- 12 µs wakeup (lowest power mode); 1.5 µs analog setting time
- 275 µA/MHz active current
- Clocks can be gated off from unused peripherals to save power
- Flexible clock divider: Reduce operational frequency up to 128x

Clock Sources

- Internal oscillator with PLL: 23–80 MHz, reduced EMI mode
- Low power internal oscillator: 20 MHz and 2.5 MHz modes
- Low frequency internal oscillator: 16.4 kHz
- External oscillators: Crystal, RC, C, CMOS and RTC Crystal

Temperature Range: –40 to +85 °C

Package Options

- QFN options: 40-pin (6 x 6 mm), 64-pin (9 x 9 mm)
- TQFP options: 64-pin (10 x 10 mm), 80-pin (12 x 12 mm)
- LGA option: 92-pin (7 x 7 mm)

Analog Peripherals

- 2 x 12-Bit Analog-to-Digital Converters: Up to 250 ksps 12-bit mode or 1 Msps 10-bit mode, internal or external reference
- 2 x 10-Bit Current-mode Digital-to-Analog Converters, four-word buffer enables 12-bit operation
- 2 x Low-current comparators
- 16-Channel Capacitance-to-Digital: Fast, <1 µA wake-on-touch
- 2 x Current-to-Voltage Converter, up to 6 mA input range

Digital and Communication Peripherals

- 2 x USARTs and 2 x UARTs with IrDA and ISO7816 SmartCard
- 3 x SPIs, 2 x I2C, I^2S (receive and transmit), 16/32-bit CRC
- 128/192/256-bit Hardware AES Encryption

Timers/Counters

- 2 x 32-bit or 4 x 16-bit timers with capture/compare
- 2 x 16-bit, 2-channel counters with capture/compare/PWM
- 16-bit, 6-channel counter with capture/compare/PWM and dead-time controller with differential outputs
- 16-bit low power timer/pulse counter operational in sleep
- 32-bit real time clock (RTC) with multiple alarms
- Watchdog timer

Up to 65 Flexible I/O

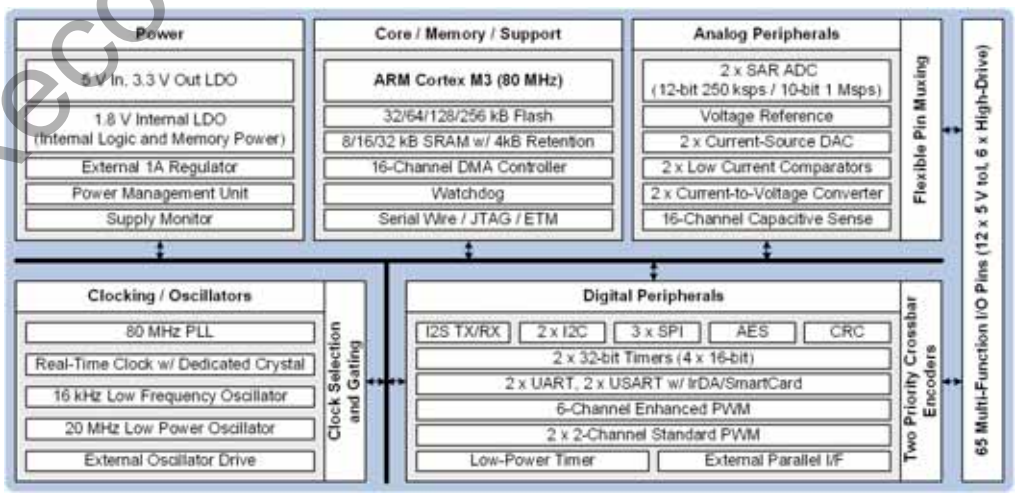
- Up to 59 contiguous GPIO with two priority crossbars providing flexibility in pin assignments; 12 x 5 V tolerant GPIO
- Up to 6 programmable high drive capable (5–300 mA, 1.8–6 V) I/O can drive LEDs, power MOSFETs, buzzers, etc.

On-Chip Debugging

- Serial wire debug (SWD) or JTAG (no boundary scan), serial wire viewer (SWV)
- Cortex-M3 embedded trace macrocell (ETM)

Supply Voltage

- 2.7 to 5.5 V (regulator enabled)
- 1.8 to 3.6 V (regulator disabled)



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1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the SiM3C1xx device family.

1.1.1. SiM3U1xx/SiM3C1xx Reference Manual

The Silicon Laboratories SiM3U1xx/SiM3C1xx Reference Manual provides detailed functional descriptions for the SiM3C1xx devices.

1.1.2. Hardware Access Layer (HAL) API Description

The Silicon Laboratories Hardware Access Layer (HAL) API provides C-language functions to modify and read each bit in the SiM3C1xx devices. This description can be found in the SiM3xxxx HAL API Reference Manual.

1.1.3. ARM Cortex-M3 Reference Manual

The ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM Cortex-M3 reference documentation. The online reference manual can be found here:
http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm3/index.html#cortexm3.

1.2. Conventions

The block diagrams in this document use the following formatting conventions:

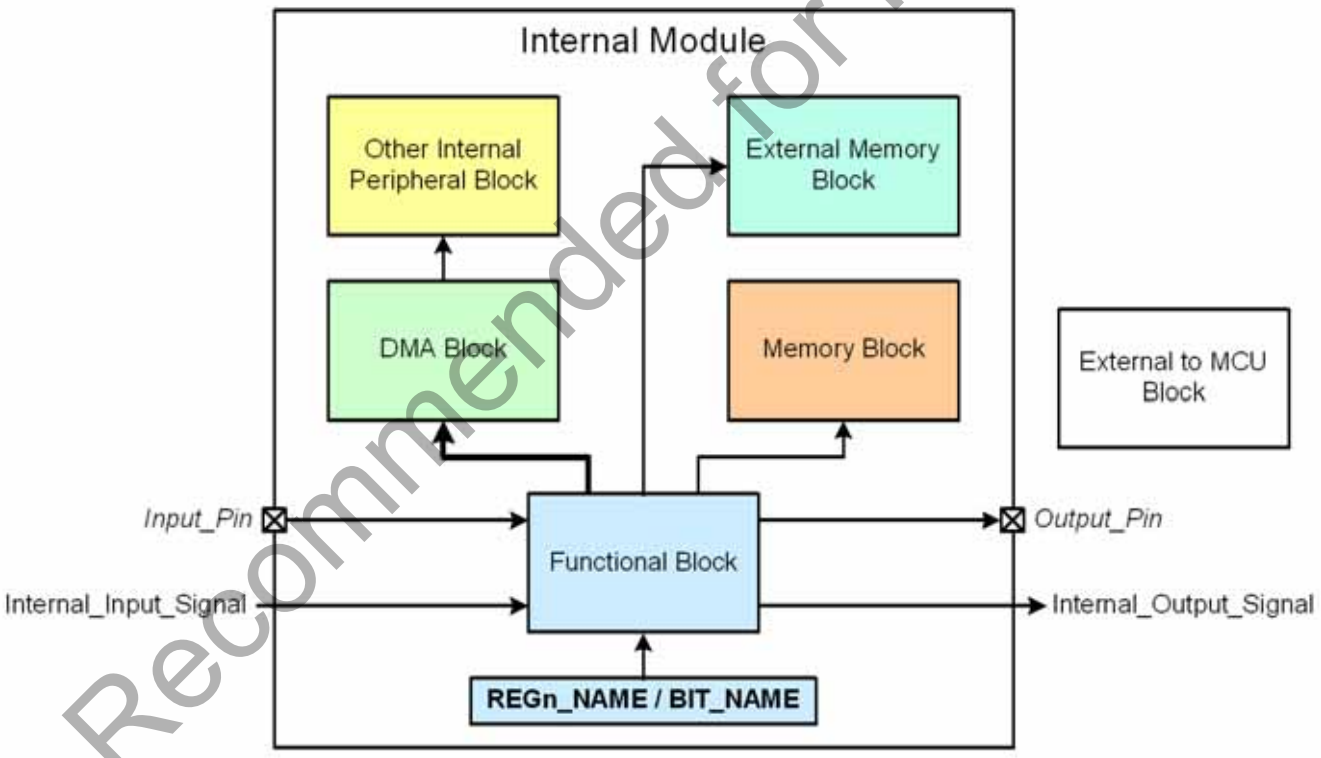

Figure 1.1. Block Diagram Conventions

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2. Typical Connection Diagrams

This section provides typical connection diagrams for SiM3C1xx devices.

2.1. Power

Figure 2.1 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is in use.

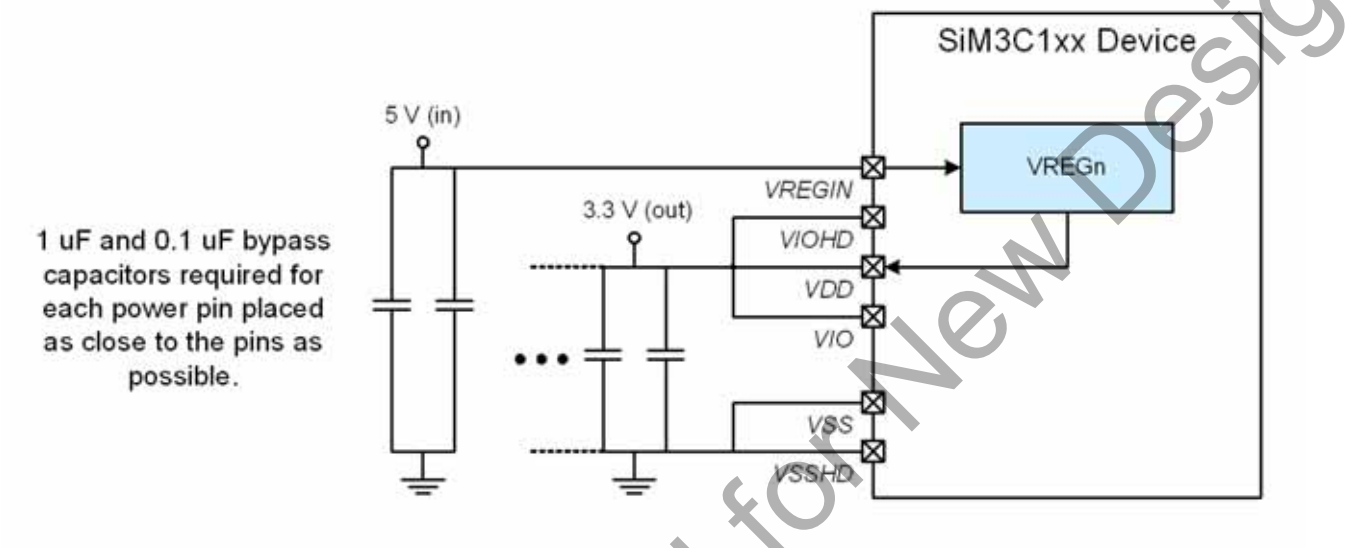

Figure 2.1. Connection Diagram with Voltage Regulator Used

Figure 2.2 shows a typical connection diagram for the power pins of the SiM3C1xx devices when the internal regulator is not used.

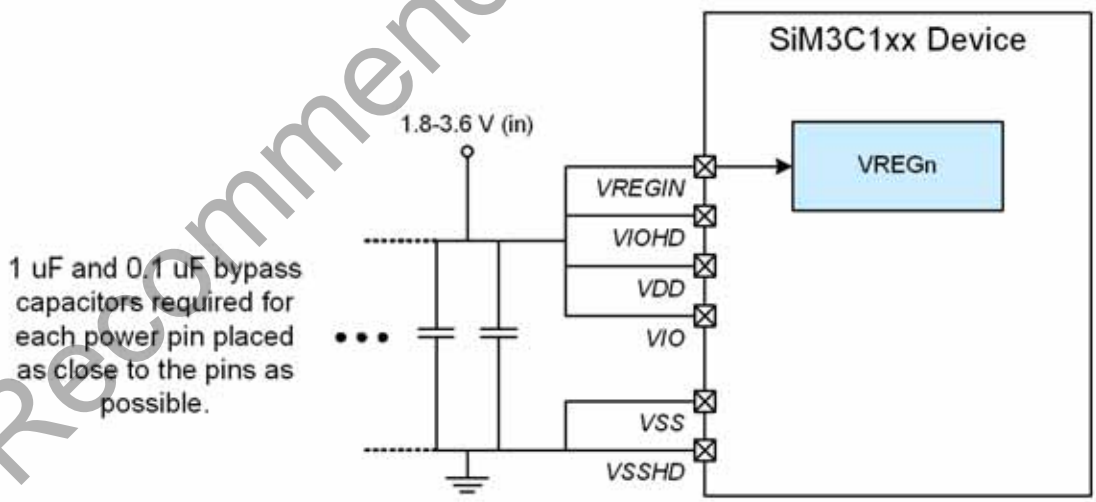

Figure 2.2. Connection Diagram with Voltage Regulator Not Used

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3. Electrical Specifications

3.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 3.1, unless stated otherwise.

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	—	3.6	V
Operating Supply Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	4	—	5.5	V
		EXTVREG0 Used	3.0	—	3.6	V
Operating Supply Voltage on VIO	V_{IO}		1.8	—	V_{DD}	V
Operating Supply Voltage on VIOHD	V_{IOHD}	HV Mode (default)	2.7	—	6.0	V
		LV Mode	1.8	—	3.6	V
Voltage on I/O pins, Port Bank 0, 1 and 2 I/O	V_{IN}		V_{SS}	—	V_{IO}	V
Voltage on I/O pins, Port Bank 3 I/O and $\overline{\text{RESET}}$	V_{IN}	SiM3C1x7 PB3.0–PB3.7 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x7 PB3.8 - PB3.11	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x6 PB3.0–PB3.5 and $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x6 PB3.6–PB3.9	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
		SiM3C1x4 $\overline{\text{RESET}}$	V_{SS}	—	V_{IO}+2.0	V
		SiM3C1x4 PB3.0–PB3.3	V_{SS}	—	Lowest of V_{IO}+2.0 or V_{REGIN}	V
Voltage on I/O pins, Port Bank 4 I/O	V_{IN}		V_{SSHD}	—	V_{IOHD}	V
System Clock Frequency (AHB)	f_{AHB}		0	—	80	MHz
Peripheral Clock Frequency (APB)	f_{APB}		0	—	50	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C
Operating Junction Temperature	T_J		–40	—	105	°C

Note: All voltages with respect to V_{SS}.

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Table 3.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	33	36.5	mA
		F_{AHB} = F_{APB} = 20 MHz	—	10.5	13.3	mA
		F_{AHB} = F_{APB} = 2.5 MHz	—	2.0	3.8	mA
Normal Mode[2,3,4,5]—Full speed with code executing from Flash, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	22	24.9	mA
		F_{AHB} = F_{APB} = 20 MHz	—	7.8	10	mA
		F_{AHB} = F_{APB} = 2.5 MHz	—	1.2	3	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	30.5	35.5	mA
		F_{AHB} = F_{APB} = 20 MHz	—	8.5	—	mA
		F_{AHB} = F_{APB} = 2.5 MHz	—	1.7	—	mA
Power Mode 1[2,3,4,6]—Full speed with code executing from RAM, peripheral clocks OFF	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	20	23	mA
		F_{AHB} = F_{APB} = 20 MHz	—	5.3	—	mA
		F_{AHB} = F_{APB} = 2.5 MHz	—	1.0	—	mA
Power Mode 2[2,3,4]—Core halted with peripheral clocks ON	I_{DD}	F_{AHB} = 80 MHz, F_{APB} = 40 MHz	—	19	22	mA
		F_{AHB} = F_{APB} = 20 MHz	—	7.8	—	mA
		F_{AHB} = F_{APB} = 2.5 MHz	—	1.3	—	mA
Power Mode 3[2,3]	I_{DD}	V_{DD} = 1.8 V, T_A = 25 °C	—	175	—	µA
		V_{DD} = 3.0 V, T_A = 25 °C	—	250	—	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 9[2,3]—Low Power Shutdown with VREG0 disabled, powered through VDD and VIO	I_{DD}	RTC Disabled, V_{DD} = 1.8 V, T_A = 25 °C	—	85	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 1.8 V, T_A = 25 °C	—	350	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 1.8 V, T_A = 25 °C	—	620	—	nA
		RTC Disabled, V_{DD} = 3.0 V, T_A = 25 °C	—	145	—	nA
		RTC w/ 16.4 kHz LFO, V_{DD} = 3.0 V, T_A = 25 °C	—	500	—	nA
		RTC w/ 32.768 kHz Crystal, V_{DD} = 3.0 V, T_A = 25 °C	—	800	—	nA
Power Mode 9[2,3]—Low Power Shutdown with VREG0 in low-power mode, VDD and VIO powered through VREG0 (Includes VREG0 current)	I_{VREGIN}	RTC Disabled, VREGIN = 5 V, T_A = 25 °C	—	300	—	nA
		RTC w/ 16.4 kHz LFO, VREGIN = 5 V, T_A = 25 °C	—	650	—	nA
		RTC w/ 32.768 kHz Crystal, VREGIN = 5 V, T_A = 25 °C	—	950	—	nA
VIOHD Current (High-drive I/O disabled)	I_{VIOHD}	HV Mode (default)	—	2.5	5	µA
		LV Mode	—	2	—	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Peripheral Supply Currents						
Voltage Regulator (VREG0)	I_{VREGIN}	Normal Mode, T_A = 25 °C BGDIS = 0, SUSEN = 0	—	300	—	µA
		Normal Mode, T_A = 85 °C BGDIS = 0, SUSEN = 0	—	—	650	µA
		Suspend Mode, T_A = 25 °C BGDIS = 0, SUSEN = 1	—	75	—	µA
		Suspend Mode, T_A = 85 °C BGDIS = 0, SUSEN = 1	—	—	115	µA
		Sleep Mode, T_A = 25 °C BGDIS = 1, SUSEN = X	—	90	—	nA
		Sleep Mode, T_A = 85 °C BGDIS = 1, SUSEN = X	—	—	500	nA
Voltage Regulator (VREG0) Sense	$I_{VRSENSE}$	SENSEEN = 1	—	3	—	µA
External Regulator (EXTVREG0)	$I_{EXTVREG}$	Regulator	—	215	250	µA
		Current Sensor	—	7	—	µA
PLL0 Oscillator (PLL0OSC)	I_{PLLOSC}	Operating at 80 MHz	—	1.75	1.86	mA
Low-Power Oscillator (LPOSC0)	I_{LPOSC}	Operating at 20 MHz	—	190	—	µA
		Operating at 2.5 MHz	—	40	—	µA
Low-Frequency Oscillator (LFOSC0)	I_{LFOSC}	Operating at 16.4 kHz, T_A = 25 °C	—	215	—	nA
		Operating at 16.4 kHz, T_A = 85 °C	—	—	500	nA

Notes:

1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Oscillator (EXTOSC0)[8]	I_{EXTOSC}	FREQCN = 111	—	3.8	4.7	mA
		FREQCN = 110	—	840	950	µA
		FREQCN = 101	—	185	220	µA
		FREQCN = 100	—	65	80	µA
		FREQCN = 011	—	25	30	µA
		FREQCN = 010	—	10	15	µA
		FREQCN = 001	—	5	10	µA
		FREQCN = 000	—	3	8	µA
SARADC0, SARADC1	I_{SARADC}	Sampling at 1 Msps, highest power mode settings.	—	1.2	1.5	mA
		Sampling at 250 ksps, lowest power mode settings.	—	390	510	µA
Temperature Sensor	I_{TSENSE}		—	75	105	µA
Internal SAR Reference	I_{REFFS}	Normal Power Mode	—	680	750	µA
		Low Power Mode	—	160	190	µA
VREF0	I_{REFP}		—	75	100	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CMPMD = 11	—	0.5	—	µA
		CMPMD = 10	—	3	—	µA
		CMPMD = 01	—	10	—	µA
		CMPMD = 00	—	25	—	µA
Capacitive Sensing (CAPSENSE0)	I_{CS}	Continuous Conversions	—	55	80	µA
IDAC0[7], IDAC1[7]	I_{IDAC}		—	75	90	µA
IVC0[7]	I_{IVC}	I_{IN} = 0	—	1.5	2.5	µA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	25	µA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

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Table 3.2. Power Consumption (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Current on VDD						
Write Operation	$I_{FLASH-W}$		—	—	8	mA
Erase Operation	$I_{FLASH-E}$		—	—	15	mA

Notes:
1. Perhipheral currents drop to zero when peripheral clock and peripheral are disabled, unless otherwise noted.
2. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
3. Includes all peripherals that cannot have clocks gated in the Clock Control module.
4. Includes supply current from internal regulator and PLL0OSC (>20 MHz) or LPOSC0 (<=20 MHz).
5. Flash execution numbers use 2 wait states for 80 MHz and 0 wait states at 20 MHz or less.
6. RAM execution numbers use 0 wait states for all frequencies.
7. IDAC output current and IVC input current not included.
8. Bias current only. Does not include dynamic current from oscillator running at speed.

Table 3.3. Power Mode Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Mode 2 Wake Time	t_{PM2}		4	—	5	clocks
Power Mode 3 Fast Wake Time	t_{PM3FW}		—	425	—	µs
Power Mode 9 Wake Time	t_{PM9}		—	12	—	µs

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Table 3.4. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} High Supply Monitor Threshold (VDDHITHEN = 1)	V_{VDDMH}	Early Warning	2.10	2.20	2.30	V
		Reset	1.95	2.05	2.1	V
V_{DD} Low Supply Monitor Threshold (VDDHITHEN = 0)	V_{VDDML}	Early Warning	1.81	1.85	1.88	V
		Reset	1.70	1.74	1.77	V
V_{REGIN} Supply Monitor Threshold	V_{VREGM}	Early Warning	4.2	4.4	4.6	V
Power-On Reset (POR) Threshold	V_{POR}	Rising Voltage on V_{DD}	—	1.4	—	V
		Falling Voltage on V_{DD}	0.8	1	1.3	V
V_{DD} Ramp Time	t_{RMP}	Time to $V_{DD} \geq 1.8$ V	10	—	3000	µs
Reset Delay from POR	t_{POR}	Relative to $V_{DD} \geq V_{POR}$	3	—	100	ms
Reset Delay from non-POR source	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
$\overline{\text{RESET}}$ Low Time to Generate Reset	t_{RSTL}		50	—	—	ns
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	$F_{AHB} > 1$ MHz	—	0.4	1	ms
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7.5	13	kHz
V_{DD} Supply Monitor Turn-On Time	t_{MON}		—	2	—	µs

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Table 3.5. On-Chip Regulators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Regulator Characteristics (VREG0, Supplied from VREGIN Pin)						
Output Voltage (at VDD pin)	V_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 0	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = 1	3.15	3.3	3.4	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 500 µA	2.3	2.8	3.6	V
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X I_{DDOUT} = 5 mA	2.1	2.65	3.3	V
Output Current (at VDD pin)*	I_{DDOUT}	$4 \le V_{REGIN} \le 5.5$ BGDIS = 0, SUSEN = X	—	—	150	mA
		$4 \le V_{REGIN} \le 5.5$ BGDIS = 1, SUSEN = X	—	—	5	mA
Output Load Regulation	V_{DDLR}	BGDIS = 0	—	0.1	1	mV/mA
Output Capacitance	C_{VDD}		1	—	10	µF

***Note:** Total current VREG0 is capable of providing. Any current consumed by the SiM3C1xx reduces the current available to external devices powered from VDD.

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Table 3.6. External Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Range (at VREGIN)	V_{REGIN}		3.0	—	3.6	V
Output Voltage (at EXREGOUT)	$V_{EXREGOUT}$	Programmable in 100 mV steps	1.8	—	3.6	V
NPN Current Drive	I_{NPN}	400 mV Dropout	12	—	—	mA
PNP Current Drive	I_{PNP}	$V_{EXREGBD} > V_{REGIN}$- 1.5 V	–6	—	—	mA
EXREGBD Voltage (PNP Mode)	$V_{EXREGBD}$	V_{REGIN} >= 3.5 V	V_{REGIN} – 2.0	—	—	V
		V_{REGIN} < 3.5 V	1.5	—	—	V
Standalone Mode Output Current	$I_{EXTREGBD}$	400 mV Dropout	—	—	11.5	mA
External Capacitance with External BJT	C_{BJT}		4.7	—	—	µF
Standalone Mode Load Regulation	$LR_{STAND-ALONE}$		—	1	—	mV/mA
Standalone Mode External Capacitance	$C_{STAND-ALONE}$		47	—	—	nF
Current Limit Range	I_{LIMIT}	1 Ω Sense Resistor	10	—	720	mA
Current Limit Accuracy			—	—	10	%
Foldback Limit Accuracy			—	—	20	%
Current Sense Resistor	R_{SENSE}		—	—	1	Ω
Internal Pull-Down	R_{PD}		—	5	—	kΩ
Internal Pull-Up	R_{PU}		—	10	—	kΩ
Current Sensor						
Sensing Pin Voltage	$V_{EXTREGSP}$ $V_{EXTREGSN}$	Measured at EXTREGSP or EXTREGSN pin	2.2	—	V_{REGIN}	V
Differential Sensing Voltage	V_{DIFF}	($V_{EXTREGSP}$ – $V_{EXTREGSN}$)	10	—	1600	mV
Current at EXTREGSN Pin	$I_{EXTREGSN}$		—	8	—	µA
Current at EXTREGSP Pin	$I_{EXTREGSP}$		—	V_{DIFF} x 200 + 12	—	µA

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Table 3.7. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Write Time[1]	t_{WRITE}	One 16-bit Half Word	20	21	22	µs
Erase Time[1]	t_{ERASE}	One Page	20	21	22	ms
	t_{ERALL}	Full Device	20	21	22	ms
V_{DD} Voltage During Programming	V_{PROG}		1.8	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
Retention[2]	t_{RET}	T_A = 25 °C, 1k Cycles	10	100	—	Years

Notes:
1. Does not include sequencing time before and after the write/erase operation, which may take up to 35 µs. During a sequential write operation, this extra time is only taken prior to the first write and after the last write.
2. Additional Data Retention Information is published in the Quarterly Quality and Reliability Report.

Table 3.8. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase-Locked Loop (PLL0OSC)						
Calibrated Output Frequency*	$f_{PLL0OSC}$	Full Temperature and Supply Range	77	79	80	MHz
Power Supply Sensitivity*	$PSS_{PLL0OSC}$	T_A = 25 °C, Fout = 79 MHz	—	430	—	ppm/V
Temperature Sensitivity*	$TS_{PLL0OSC}$	V_{DD} = 3.3 V, Fout = 79 MHz	—	95	—	ppm/°C
Adjustable Output Frequency Range	$f_{PLL0OSC}$		23	—	80	MHz
Lock Time	$t_{PLL0LOCK}$	f_{REF} = 20 MHz, $f_{PLL0OSC}$ = 80 MHz, M=24, N=99, LOCKTH = 0	—	1.7	—	µs
		f_{REF} = 32 kHz, $f_{PLL0OSC}$ = 80 MHz, M=0, N=2440, LOCKTH = 0	—	91	—	µs

***Note:** PLL0OSC in free-running oscillator mode.

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Table 3.8. Internal Oscillators (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Power Oscillator (LPOSC0)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	19	20	21	MHz
		T_A = 25 °C, V_{DD} = 3.3 V	19.5	20	20.5	MHz
Divided Oscillator Frequency	f_{LPOSCD}	Full Temperature and Supply Range	2.375	2.5	2.625	MHz
Power Supply Sensitivity	PSS_{LPOSC}	T_A = 25 °C	—	0.5	—	%/V
Temperature Sensitivity	TS_{LPOSC}	V_{DD} = 3.3 V	—	55	—	ppm/°C
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		T_A = 25 °C, V_{DD} = 3.3 V	15.8	16.4	17.3	kHz
Power Supply Sensitivity	PSS_{LFOSC}	T_A = 25 °C	—	2.4	—	%/V
Temperature Sensitivity	TS_{LFOSC}	V_{DD} = 3.3 V	—	0.2	—	%/°C
RTC0 Oscillator (RTC0OSC)						
Missing Clock Detector Trigger Frequency	f_{RTCMCD}		—	8	15	kHz
RTC Robust Duty Cycle Range	DC_{RTC}		25	—	55	%

***Note:** PLL0OSC in free-running oscillator mode.

Table 3.9. External Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency*	f_{CMOS}		0	—	50	MHz
External Input CMOS Clock High Time	t_{CMOSH}		9	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		9	—	—	ns
External Crystal Clock Frequency	f_{XTAL}		0.01	—	30	MHz

***Note:** Minimum of 10 kHz during debug operations.

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Table 3.10. SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N_{bits}	12 Bit Mode		12		Bits
		10 Bit Mode		10		Bits
Supply Voltage Requirements (VDD)	V_{ADC}	High Speed Mode	2.2	—	3.6	V
		Low Power Mode	1.8	—	3.6	V
Throughput Rate (High Speed Mode)	f_S	12 Bit Mode	—	—	250	ksps
		10 Bit Mode	—	—	1	Msps
Throughput Rate (Low Power Mode)	f_S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t_{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
SAR Clock Frequency	f_{SAR}	High Speed Mode	—	—	16.24	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t_{CNV}	10-Bit Conversion, SAR Clock = 16 MHz, APB Clock = 40 MHz		762.5		ns
Sample/Hold Capacitor	C_{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C_{IN}	High Quality Inputs	—	18	—	pF
		Normal Inputs	—	20	—	pF
Input Mux Impedance	R_{MUX}	High Quality Inputs	—	300	—	Ω
		Normal Inputs	—	550	—	Ω
Voltage Reference Range	V_{REF}		1	—	V_{DD}	V
Input Voltage Range[1]	V_{IN}	Gain = 1	0	—	V_{REF}	V
		Gain = 0.5	0	—	$2xV_{REF}$	V
Power Supply Rejection Ratio	$PSRR_{ADC}$		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode[2]	—	±1	±1.9	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

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Table 3.10. SAR ADC (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode[2]	–1	±0.7	1.8	LSB
		10 Bit Mode	—	±0.2	±0.5	LSB
Offset Error (using VREFGND)	E_{OFF}	12 Bit Mode, VREF =2.4 V	–2	0	2	LSB
		10 Bit Mode, VREF =2.4 V	–1	0	1	LSB
Offset Temperatue Coefficient	TC_{OFF}		—	0.004	—	LSB/°C
Slope Error[3]	E_M	12 Bit Mode	–0.07	–0.02	0.02	%
Dynamic Performance with 10 kHz Sine Wave Input 1 dB below full scale, Max throughput						
Signal-to-Noise	SNR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	62	66	—	dB
		10 Bit Mode	58	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	78	—	dB
		10 Bit Mode	—	77	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	–79	—	dB
		10 Bit Mode	—	–74	—	dB

Notes:
1. Absolute input pin voltage is limited by the lower of the supply at VDD and VIO.
2. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
3. The maximum code in 12-bit mode is 0xFFFC. The Slope Error is referenced from the maximum code.

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Table 3.11. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	N_{bits}			10		Bits
Integral Nonlinearity	INL		—	±0.5	±2	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL		—	±0.5	±1	LSB
Output Compliance Range	V_{OCR}		—	—	V_{DD} – 1.0	V
Full Scale Output Current	I_{OUT}	2 mA Range	2.0	2.046	2.10	mA
		1 mA Range	0.99	1.023	1.05	mA
		0.5 mA Range	493	511.5	525	µA
Offset Error	E_{OFF}		—	250	—	nA
Full Scale Error Tempco	TC_{FS}	2 mA Range	—	100	—	ppm/°C
VDD Power Supply Rejection Ratio		2 mA Range	—	-220	—	ppm/V
Test Load Impedance (to V_{SS})	R_{TEST}		—	1	—	kΩ
Dynamic Performance						
Output Settling Time to 1/2 LSB		min output to max output	—	1.2	—	µs
Startup Time			—	3	—	µs

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Table 3.12. Capacitive Sense

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single Conversion Time (Default Configuration)	t_{single}	12-bit Mode	—	25	—	µs
		13-bit Mode	—	27	—	µs
		14-bit Mode	—	29	—	µs
		16-bit Mode	—	33	—	µs
Maximum External Capacitive Load	C_L	Highest Gain Setting (default)	—	45	—	pF
		Lowest Gain Setting	—	500	—	pF
Maximum External Series Impedance	C_L	Highest Gain Setting (default)	—	50	—	kΩ

Table 3.13. Current-to-Voltage Converter (IVC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{DDIVC}		2.2	—	3.6	V
Input Pin Voltage	V_{IN}		2.2	—	VDD	V
Minimum Input Current (source)	I_{IN}		100	—	—	µA
Integral Nonlinearity	INL_{IVC}		–0.6	—	0.6	%
Full Scale Output	V_{IVCOUT}		—	1.65	—	V
Slope	M_{IVC}	Input Range 1 mA (INxRANGE = 101)	1.55	1.65	1.75	V/mA
		Input Range 2 mA (INxRANGE = 100)	795	830	860	mV/mA
		Input Range 3 mA (INxRANGE = 011)	525	550	570	mV/mA
		Input Range 4 mA (INxRANGE = 010)	390	415	430	mV/mA
		Input Range 5 mA (INxRANGE = 001)	315	330	340	mV/mA
		Input Range 6 mA (INxRANGE = 000)	260	275	285	mV/mA
Settling Time to 0.1%	V_{IVCOUT}		—	—	500	ns

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Table 3.14. Voltage Reference Electrical Characteristics

V_{DD} = 1.8 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}	–40 to +85 °C, V_{DD} = 1.8–3.6 V	1.62	1.65	1.68	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-Chip Precision Reference (VREF0)						
Valid Supply Range	V_{DD}	VREF2X = 0	1.8	—	3.6	V
		VREF2X = 1	2.7	—	3.6	V
Output Voltage	V_{REFP}	25 °C ambient, VREF2X = 0	1.195	1.2	1.205	V
		25 °C ambient, VREF2X = 1	2.39	2.4	2.41	V
Short-Circuit Current	I_{SC}		—	—	10	mA
Temperature Coefficient	TC_{VREFP}		—	25	—	ppm/°C
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to VREFGND	—	4.5	—	ppm/µA
Load Capacitor	C_{VREFP}	Load = 0 to 200 µA to VREFGND	0.1	—	—	µF
Turn-on Time	$t_{VREFPON}$	4.7 µF tantalum, 0.1 µF ceramic bypass	—	3.8	—	ms
		0.1 µF ceramic bypass	—	200	—	µs
Power Supply Rejection	$PSRR_{VREFP}$	VREF2X = 0	—	320	—	ppm/V
		VREF2X = 1	—	560	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 250 ksps; VREF = 3.0 V	—	5.25	—	µA

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Table 3.15. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	760	—	mV
Offset Error*	E_{OFF}	T_A = 0 °C	—	±14	—	mV
Slope	M		—	2.8	—	mV/°C
Slope Error*	E_M		—	±120	—	µV/°C
Linearity			—	1	—	°C
Turn-on Time			—	1.8	—	µs
***Note:** Represents one standard deviation from the mean.						

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Table 3.16. Comparator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CMPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CMPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.4	—	µs
		–100 mV Differential	—	3.5	—	µs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CMPHYP = 00	—	0.4	—	mV
		CMPHYP = 01	—	8	—	mV
		CMPHYP = 10	—	16	—	mV
		CMPHYP = 11	—	33	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CMPHYN = 00	—	0.4	—	mV
		CMPHYN = 01	—	–8	—	mV
		CMPHYN = 10	—	–16	—	mV
		CMPHYN = 11	—	–33	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CMPHYP = 00	—	0.5	—	mV
		CMPHYP = 01	—	6	—	mV
		CMPHYP = 10	—	12	—	mV
		CMPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CMPHYN = 00	—	0.5	—	mV
		CMPHYN = 01	—	–6.0	—	mV
		CMPHYN = 10	—	–12	—	mV
		CMPHYN = 11	—	–24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CMPHYP = 00	—	0.6	—	mV
		CMPHYP = 01	—	4.5	—	mV
		CMPHYP = 10	—	9.5	—	mV
		CMPHYP = 11	—	19	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CMPHYN = 00	—	0.6	—	mV
		CMPHYN = 01	—	–4.5	—	mV
		CMPHYN = 10	—	–9.5	—	mV
		CMPHYN = 11	—	–19	—	mV

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Table 3.16. Comparator (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CMPHYP = 00	—	1.4	—	mV
		CMPHYP = 01	—	4	—	mV
		CMPHYP = 10	—	8	—	mV
		CMPHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CMPHYN = 00	—	1.4	—	mV
		CMPHYN = 01	—	–4	—	mV
		CMPHYN = 10	—	–8	—	mV
		CMPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		–0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}	PB2 Pins	—	7.5	—	pF
		PB3 Pins	—	10.5	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	75	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}		–10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C
Reference DAC Resolution	N_{Bits}			6		bits

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Table 3.17. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard I/O (PB0, PB1, and PB2), 5 V Tolerant I/O (PB3), and $\overline{\text{RESET}}$						
Output High Voltage*	V_{OH}	Low Drive, I_{OH} = –2 mA	V_{IO} – 0.7	—	—	V
		High Drive, I_{OH} = –5 mA	V_{IO} – 0.7	—	—	V
Output Low Voltage*	V_{OL}	Low Drive, I_{OL} = 3 mA	—	—	0.6	V
		High Drive, I_{OL} = 12.5 mA	—	—	0.6	V
Input High Voltage	V_{IH}	1.8 ≤ V_{IO} ≤ 2.0	0.7 x V_{IO}	—	—	V
		2.0 ≤ V_{IO} ≤ 3.6	V_{IO} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
Pin Capacitance	C_{IO}	PB0, PB1 and PB2 Pins	—	4	—	pF
		PB3 Pins	—	7	—	pF
Weak Pull-Up Current (Input Voltage = 0 V)	I_{PU}	V_{IO} = 1.8	–6	–3.5	–2	µA
		V_{IO} = 3.6	–30	–20	–10	µA
Input Leakage (Pullups off or Analog)	I_{LK}	0 ≤ V_{IN} ≤ V_{IO}	–1	—	1	µA
Input Leakage Current of Port Bank 3 I/O, V_{IN} above V_{IO}	I_L	V_{IO} < V_{IN} < V_{IO}+2.0 V (pins without EXREG functions)	0	5	150	µA
		V_{IO} < V_{IN} < V_{REGIN} (pins with EXREG functions)	0	5	150	µA
High Drive I/O (PB4)						
Output High Voltage	V_{OH}	Standard Mode, Low Drive, I_{OH} = –3 mA	V_{IOHD} – 0.7	—	—	V
		Standard Mode, High Drive, I_{OH} = –10 mA	V_{IOHD} – 0.7	—	—	V
Output Low Voltage	V_{OL}	Standard Mode, Low Drive, I_{OH} = 3 mA	—	—	0.6	V
		Standard Mode, High Drive, I_{OH} = 12.5 mA	—	—	0.6	V
Output Rise Time	t_R	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

Not Recommended for New Designs

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t_F	Slew Rate Mode 0, V_{IOHD} = 5 V	—	50	—	ns
		Slew Rate Mode 1, V_{IOHD} = 5 V	—	300	—	ns
		Slew Rate Mode 2, V_{IOHD} = 5 V	—	1	—	µs
		Slew Rate Mode 3, V_{IOHD} = 5 V	—	3	—	µs
Input High Voltage	V_{IH}	1.8 V≤ V_{IOHD} ≤ 2.0 V	0.7 x V_{IOHD}	—	—	V
		2.0 V≤ V_{IOHD} ≤ 6 V	V_{IOHD} – 0.6	—	—	V
Input Low Voltage	V_{IL}		—	—	0.6	V
N-Channel Sink Current Limit (2.7 V ≤ V_{IOHD} ≤ 6 V, V_{OL} = 0.8 V) See Figure 3.1	I_{SINKL}	Mode 0	—	1.75	—	mA
		Mode 1	—	2.5	—	
		Mode 2	—	3.5	—	
		Mode 3	—	4.75	—	
		Mode 4	—	7	—	
		Mode 5	—	9.5	—	
		Mode 6	—	14	—	
		Mode 7	—	18.75	—	
		Mode 8	—	28.25	—	
		Mode 9	—	37.5	—	
		Mode 10	—	56.25	—	
		Mode 11	—	75	—	
		Mode 12	—	112.5	—	
		Mode 13	—	150	—	
		Mode 14	—	225	—	
		Mode 15	—	300	—	
Total N-Channel Sink Current on P4.0-P4.5 (DC)	I_{SINKLT}		—	—	400	mA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

Not Recommended for New Designs

Table 3.17. Port I/O (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
P-Channel Source Current Limit (2.7 V ≤ VIOHD ≤ 6 V, V_{OH} = VIOHD – 0.8 V) See Figure 3.2	I_{SRCL}	Mode 0	—	0.8	—	mA
		Mode 1	—	1.25	—	
		Mode 2	—	1.75	—	
		Mode 3	—	2.5	—	
		Mode 4	—	3.5	—	
		Mode 5	—	4.75	—	
		Mode 6	—	7	—	
		Mode 7	—	9.5	—	
		Mode 8	—	14	—	
		Mode 9	—	18.75	—	
		Mode 10	—	28.25	—	
		Mode 11	—	37.5	—	
		Mode 12	—	56.25	—	
		Mode 13	—	75	—	
		Mode 14	—	112.5	—	
		Mode 15	—	150	—	
Total P-Channel Source Current on P4.0-P4.5 (DC)	I_{SRCLT}		—	—	400	mA
Pin Capacitance	C_{IO}		—	30	—	pF
Weak Pull-Up Current in Low Voltage Mode	I_{PU}	V_{IOHD} = 1.8 V	–6	–3.5	–2	µA
		V_{IOHD} = 3.6 V	–30	–20	–10	µA
Weak Pull-Up Current in High Voltage Mode	I_{PU}	V_{IOHD} = 2.7 V	–15	–10	–5	µA
		V_{IOHD} = 6 V	–30	–20	–10	µA
Input Leakage (Pullups off)	I_{LK}		–1	—	1	µA

***Note:** $\overline{\text{RESET}}$ does not drive to logic high. Specifications for $\overline{\text{RESET}}$ V_{OL} adhere to the low drive setting.

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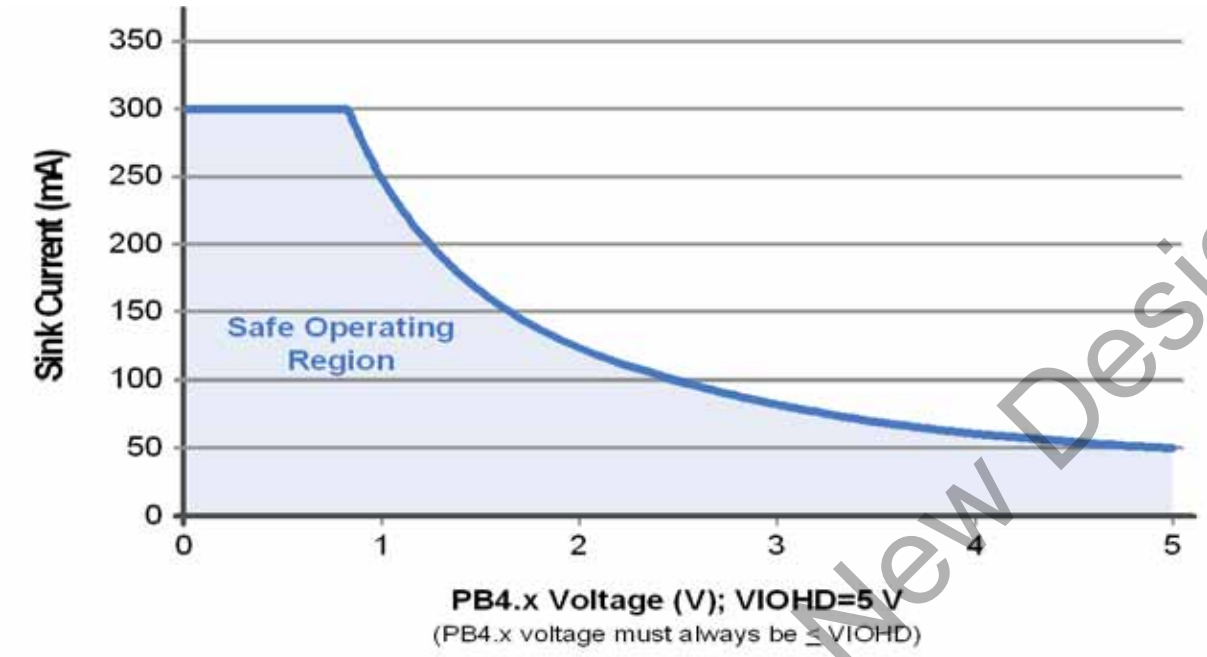

Figure 3.1. Maximum Sink Current vs. PB4.x Pin Voltage

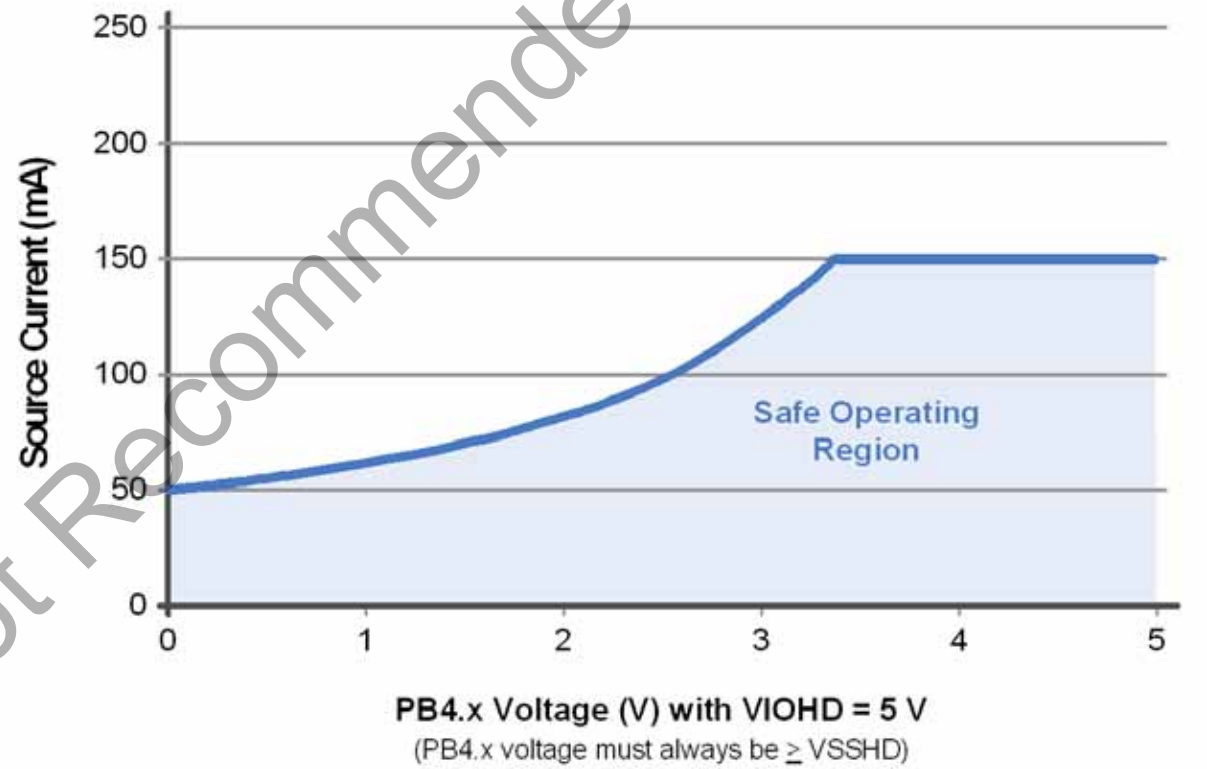

Figure 3.2. Maximum Source Current vs. PB4.x Pin Voltage

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3.2. Thermal Conditions

Table 3.18. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	θ_{JA}	LGA-92 Packages	—	35	—	°C/W
		TQFP-80 Packages	—	40	—	°C/W
		QFN-64 Packages	—	25	—	°C/W
		TQFP-64 Packages	—	30	—	°C/W
		QFN-40 Packages	—	30	—	°C/W
***Note:** Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.						

3.3. Absolute Maximum Ratings

Stresses above those listed under Table 3.19 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3.19. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on VDD	V_{DD}		V_{SS}–0.3	4.2	V
Voltage on VREGIN	V_{REGIN}	EXTVREG0 Not Used	V_{SS}–0.3	6.0	V
		EXTVREG0 Used	V_{SS}–0.3	3.6	V
Voltage on VIO	V_{IO}		V_{SS}–0.3	4.2	V
Voltage on VIOHD	V_{IOHD}		V_{SS}–0.3	6.5	V
Voltage on I/O pins, non Port Bank 3 I/O	V_{IN}	$\overline{\text{RESET}}$, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		$\overline{\text{RESET}}$, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		Port Bank 0, 1, and 2 I/O	V_{SS}–0.3	V_{IO}+0.3	V
		Port Bank 4 I/O	V_{SSHD}–0.3	V_{IOHD}+0.3	V
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

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Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Voltage on I/O pins, Port Bank 3 I/O	V_{IN}	SiM3C1x7, PB3.0–PB3.7, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x7, PB3.0–PB3.7, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x7, PB3.8 - PB3.11	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} \geq 3.3$ V	V_{SS}–0.3	5.8	V
		SiM3C1x6, PB3.0–PB3.5, $V_{IO} < 3.3$ V	V_{SS}–0.3	V_{IO}+2.5	V
		SiM3C1x6, PB3.6–PB3.9	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
		SiM3C1x4, PB3.0–PB3.3	V_{SS}–0.3	Lowest of V_{IO}+2.5, V_{REGIN}+0.3, or 5.8	V
Total Current Sunk into Supply Pins	I_{SUPP}	V_{DD}, V_{REGIN}, V_{IO}, V_{IOHD}	—	400	mA
Total Current Sourced out of Ground Pins	I_{VSS}	V_{SS}, V_{SSHD}	400	—	mA
Current Sourced or Sunk by Any I/O Pin	I_{PIO}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Current Injected on Any I/O Pin	I_{INJ}	PB0, PB1, PB2, PB3, and $\overline{\text{RESET}}$	–100	100	mA
		PB4	–300	300	mA
Total Injected Current on I/O Pins	ΣI_{INJ}	Sum of all I/O and $\overline{\text{RESET}}$	–400	400	mA

***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.

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Table 3.19. Absolute Maximum Ratings (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Power Dissipation at T_A = 85 °C	P_D	LGA-92 Package	—	570	mW
		TQFP-80 Package	—	500	mW
		QFN-64 Package	—	800	mW
		TQFP-64 Package	—	650	mW
		QFN-40 Package	—	650	mW
***Note:** VSS and VSSHD provide separate return current paths for device supplies, but are not isolated. They must always be connected to the same potential on board.					

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4. Precision32™ SiM3C1xx System Overview

The SiM3C1xx Precision32™ devices are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 5.1 for specific product feature selection and part ordering numbers.

- **Core:**
  - 32-bit ARM Cortex-M3 CPU.
  - 80 MHz maximum operating frequency.
  - Branch target cache and prefetch buffers to minimize wait states.
- **Memory:** 32–256 kB Flash; in-system programmable, 8–32 kB SRAM (including 4 kB retention SRAM, which preserves state in PM9 mode).
- **Power:**
  - Low drop-out (LDO) regulator for CPU core voltage.
  - Power-on reset circuit and brownout detectors.
  - 3.3 V output LDO for direct power from 5 V supplies.
  - External transistor regulator.
  - Power Management Unit (PMU).
- **I/O: Up to 65 total multifunction I/O pins:**
  - Up to six programmable high-power capable (5–300 mA with programmable current limiting, 1.8–5 V).
  - Up to twelve 5 V tolerant general purpose pins.
  - Two flexible peripheral crossbars for peripheral routing.
- **Clock Sources:**
  - Internal oscillator with PLL: 23–80 MHz with ± 1.5% accuracy in free-running mode.
  - Low-power internal oscillator: 20 MHz and 2.5 MHz modes.
  - Low-frequency internal oscillator: 16.4 kHz.
  - External RTC crystal oscillator: 32.768 kHz.
  - External oscillator: Crystal, RC, C, CMOS clock modes.
  - Programmable clock divider allows any oscillator source to be divided by binary factor from 1-128.
- **Data Peripherals:**
  - 16-Channel DMA Controller.
  - 128/192/256-bit Hardware AES Encryption.
  - 16/32-bit CRC.
- **Timers/Counters and PWM:**
  - 6-channel Enhanced Programmable Counter Array (EPCAn) supporting advanced PWM and capture/compare.
  - 2 x 2-channel Standard Programmable Counter Array (PCAn) supporting PWM and capture/compare.
  - 2 x 32-bit Timers - can be split into 4 x 16-bit Timers, support PWM and capture/compare.
  - Real Time Clock (RTCn).
  - Low Power Timer.
  - Watchdog Timer.
- **Communications Peripherals:**
  - External Memory Interface.
  - 2 x USARTs and 2 x UARTs with IrDA and ISO7816 SmartCard support.
  - 3 x SPIs.
  - 2 x I2C.
  - I^2S (receive and transmit).
- **Analog:**
  - 2 x 12-Bit Analog-to-Digital Converters (SARADC).
  - 2 x 10-Bit Digital-to-Analog Converter (IDAC).
  - 16-Channel Capacitance-to-Digital Converter (CAPSENSE).
  - 2 x Low-Current Comparators (CMP).
  - 1 x Current-to-Voltage Converter (IVC) module with two channels.
- **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the SiM3C1xx devices are truly standalone system-on-a-chip solutions. The Flash memory is reprogrammable in-circuit, providing non-

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volatile data storage and allowing field upgrades of the firmware. User firmware has complete control of all peripherals and may individually shut down and gate the clocks of any or all peripherals for power savings.

The on-chip debugging interface (SWJ-DP) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 1.8 to 3.6 V operation over the industrial temperature range (–40 to +85 °C). The Port I/O and RESET pins are powered from the IO supply voltage. The SiM3C1xx devices are available in 40-pin or 64-pin QFN, 64-pin or 80-pin TQFP, or 92-pin LGA packages. All package options are lead-free and RoHS compliant. See Table 5.1 for ordering information. A block diagram is included in Figure 4.1.

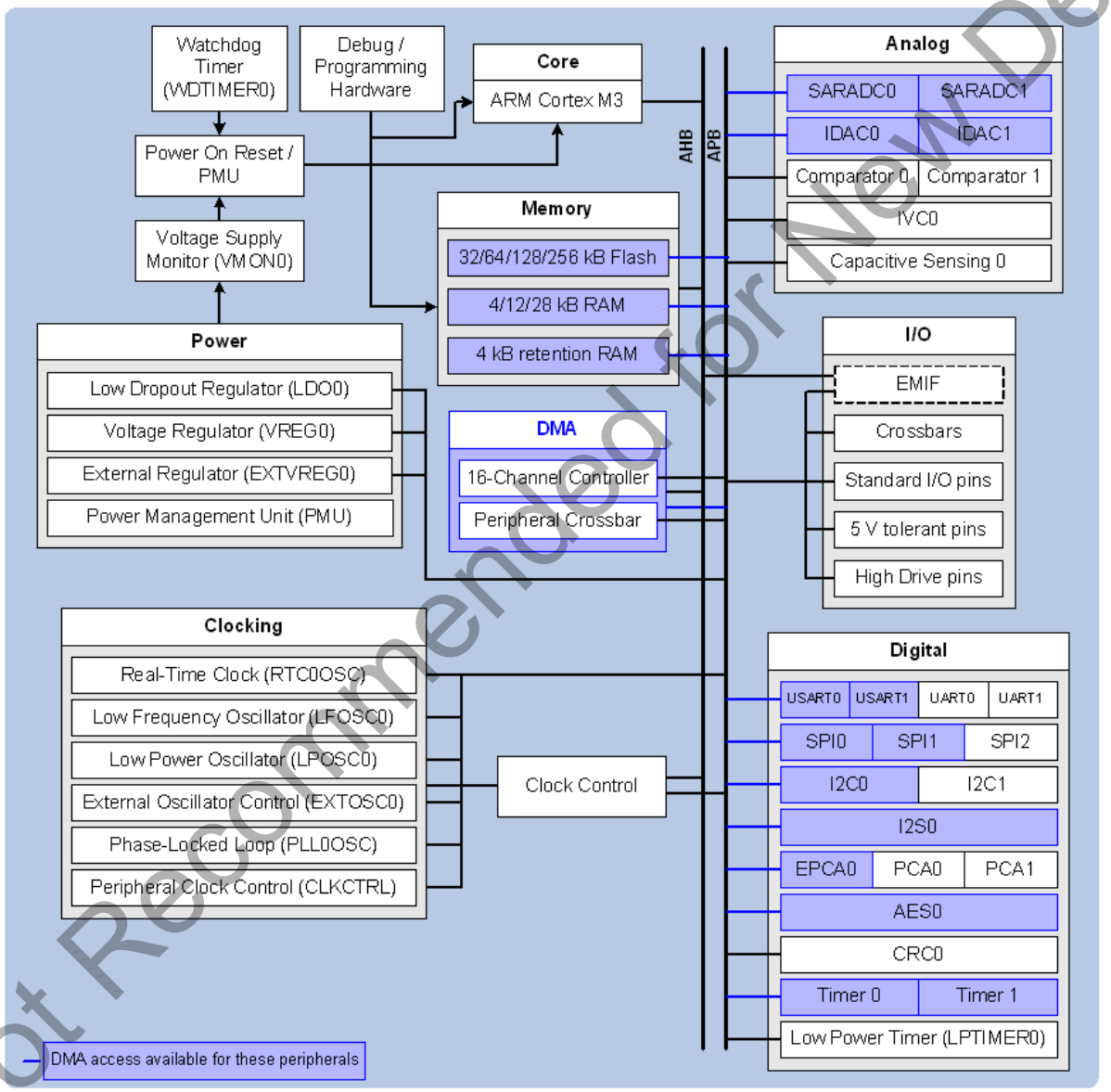

Figure 4.1. Precision32™ SiM3C1xx Family Block Diagram

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4.1. Power

4.1.1. LDO and Voltage Regulator (VREG0)

The SiM3C1xx devices include two internal regulators: the core LDO Regulator and the Voltage Regulator (VREG0).

The LDO Regulator converts a 1.8–3.6 V supply to the core operating voltage of 1.8 V. This LDO consumes little power and provides flexibility in choosing a power supply for the system.

The Voltage Regulator regulates from 5.5 to 2.7 V and can serve as an input to the LDO. This allows the device to be powered from up to a 5.5 V supply without any external components other than bypass capacitors.

4.1.2. Voltage Supply Monitor (VMON0)

The SiM3C1xx devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware. The supply monitor includes additional circuitry that can monitor the main supply voltage and the VREGIN input voltage divided by 4 (VREGIN / 4).

The supply monitor module includes the following features:

- Main supply “VDD Low” (VDD below the early warning threshold) notification.
- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.
- VREGIN divided by 4 (VREGIN / 4) supply “VREGIN Low” notification.

4.1.3. External Regulator (EXTVREG0)

The External Regulator provides all the circuitry needed for a high-power regulator except the power transistor (NPN or PNP) and current sensing resistor (if current limiting is enabled).

The External Regulator module has the following features:

- Interfaces with either an NPN or PNP external transistor that serves as the pass device for the high current regulator.
- Automatic current limiting.
- Automatic foldback limiting.
- Sources up to 1 A for use by external circuitry.
- Variable output voltage from 1.8–3.6 V in 100 mV steps.

4.1.4. Power Management Unit (PMU)

The Power Management Unit on the SiM3C1xx manages the power systems of the device. On power-up, the PMU ensures the core voltages are a proper value before core instruction execution begins. It also recognizes and manages the various wake sources for low-power modes of the device.

The PMU module includes the following features:

- Up to 16 pin wake inputs can wake the device from Power Mode 9.
- The Low Power Timer, RTC0 (alarms and oscillator fail), Comparator 0, and the $\overline{\text{RESET}}$ pin can also serve as wake sources for Power Mode 9.
- All PM9 wake sources (except for the $\overline{\text{RESET}}$ pin) can also reset the Low Power Timer or RTC0 modules.
- Disables the level shifters to pins and peripherals to further reduce power usage in PM9. These level shifters must be re-enabed by firmware after exiting PM9.
- Provides a PMU_Asleep signal to a pin as an indicator that the device is in PM9.

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4.1.5. Device Power Modes

The SiM3C1xx devices feature four low power modes in addition to normal operating mode. Several peripherals provide wake up sources for these low power modes, including the Low-Power Timer (LPT0), RTC0 (alarms and oscillator failure notification), Comparator 0, and PMU Pin Wake.

In addition, all peripherals can have their clocks disabled to reduce power consumption whenever a peripheral is not being used using the clock control (CLKCTRL) registers.

4.1.5.1. Normal Mode (Power Mode 0)

Normal Mode is the default mode of the device. The core and peripherals are fully operational, and instructions are executed from flash memory.

4.1.5.2. Power Mode 1

In Power Mode 1 the core and peripherals are fully operational, with instructions executing from RAM. Compared with Normal Mode, the active power consumption of the device in PM1 is reduced. Additionally, at higher speeds in PM1, the core throughput can also be increased because RAM does not require additional wait states that reduce the instruction fetch speed.

4.1.5.3. Power Mode 2

In Power Mode 2 the core halts and any enabled peripherals continue to run at the selected clock speed. The power consumption in PM2 corresponds to the AHB and APB clocks left enabled, thus the power can be tuned to the optimal level for the needs of the application. To place the device in PM2, the core should execute a wait-for-interrupt (WFI) or wait-for-event (WFE) instruction. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM2 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Syncronization Barrier) operation prior to the WFI to ensure all bus accesses complete. When operating from the LFOSC0 with the DMACTRL0 AHB clock disabled, PM2 can achieve similar power consumption to PM3, but with the ability to wake on APB-clocked interrupts. For example, enabling only the APB clock to the Ports will allow the firmware to wake on a PMATCH0, PBEXT0 or PBEXT1 interrupt with minimal impact on the supply current.

4.1.5.4. Power Mode 3

In Power Mode 3, the AHB and APB clocks are halted. The device may only wake from enabled interrupt sources which do not require the APB clock (RTC0ALRM, RTC0FAIL, LPTIMER0, VDDLOW and VREGLOW). A special fast wake option allows the device to operate at a very low level from the RTC0TCLK or LFOSC0 oscillator while in PM3, but quickly switch to the faster LPOSC0 when the wake event occurs. Because the current consumption of these blocks is minimal, it is recommended to use the fast wake option.

The device will enter PM3 on a WFI or WFE instruction. Because all AHB master clocks are disabled, the LPOSC will automatically halt and go into a low-power suspended state. If the WFI instruction is called from an interrupt service routine, the interrupt that wakes the device from PM3 must be of a sufficient priority to be recognized by the core. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

4.1.5.5. Power Mode 9

In Power Mode 9, the core and all peripherals are halted, all clocks are stopped, and the pins and peripherals are set to a lower power mode. In addition, standard RAM contents are not preserved, though retention RAM contents are still available after exiting the power mode. This mode provides the lowest power consumption for the device, but requires an appropriate reset to exit. The available reset sources to wake from PM9 are controlled by the Power Management Unit (PMU).

Before entering PM9, the desired reset source(s) should be configured in the PMU. The SLEEPDEEP bit in the ARM System Control Register should be set, and the PMSEL bit in the RSTSRC0_CONFIG register must be set to indicate that PM9 is the desired power mode.

The device will enter PM9 on a WFI or WFE instruction, and remain in PM9 until a reset configured by the PMU occurs. It is recommended to perform both a DSB (Data Synchronization Barrier) and an ISB (Instruction Synchronization Barrier) operation prior to the WFI to ensure all bus access is complete.

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4.2. I/O

4.2.1. General Features

The SiM3C1xx ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Option for high or low output drive strength.
- Port Match allows the device to recognize a change on a port pin value.
- Internal pull-up resistors are enabled or disabled on a port-by-port basis.
- Two external interrupts with up to 16 inputs provide monitoring capability for external signals.
- Internal Pulse Generator Timer (PB2 only) to generate simple square waves.
- A subset of pins can also serve as inputs to the Port Mapped Level Shifters available on the High Drive Pins.

4.2.2. High Drive Pins (PB4)

The High Drive pins have the following additional features:

- Programmable safe state: high, low, or high impedance.
- Programmable drive strength and slew rates.
- Programmable hardware current limiting.
- Powered from a separate source (VIOHD, which can be up to 6 V) from the rest of the device.
- Supports various functions, including GPIO, UART1 pins, EPCA0 pins, or Port Mapped Level Shifting.

4.2.3. 5 V Tolerant Pins (PB3)

The 5 V tolerant pins can be connected to external circuitry operating at voltages above the device supply without needing extra components to shift the voltage level.

4.2.4. Crossbars

The SiM3C1xx devices have two Crossbars with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The Crossbars have a fixed priority for each I/O function and assign these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the Crossbars skip that pin when assigning the next selected resource. Additionally, the Crossbars will skip port pins whose associated bits in the PBSKIPEN registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

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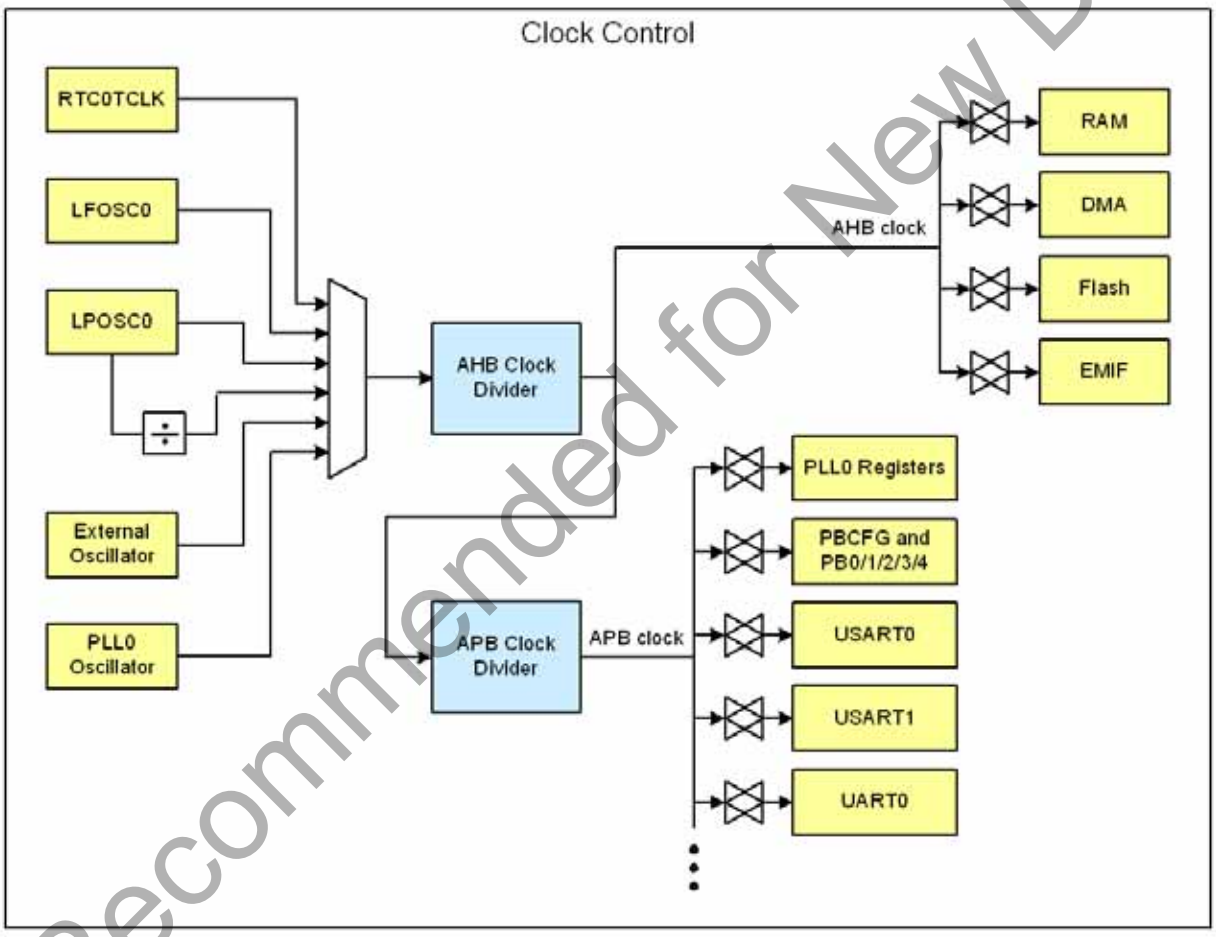
4.3. Clocking

The SiM3C1xx devices have two system clocks: AHB and APB. The AHB clock services memory peripherals and is derived from one of seven sources: the RTC0 timer clock (RTC0TCLK), the Low Frequency Oscillator, the Low Power Oscillator, the divided Low Power Oscillator, the External Oscillator, and the PLL0 Oscillator. In addition, a divider for the AHB clock provides flexible clock options for the device. The APB clock services data peripherals and is synchronized with the AHB clock. The APB clock can be equal to the AHB clock (if AHB is less than or equal to 50 MHz) or set to the AHB clock divided by two.

Clock Control allows the AHB and APB clocks to be turned off to unused peripherals to save system power. Any registers in a peripheral with disabled clocks will be unable to be accessed until the clocks are enabled. Most peripherals have clocks off by default after a power-on reset.



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4.3.1. PLL (PLL0)

The PLL module consists of a dedicated Digitally-Controlled Oscillator (DCO) that can be used in Free-Running mode without a reference frequency, Frequency-Locked to a reference frequency, or Phase-Locked to a reference frequency. The reference frequency for Frequency-Lock and Phase-Lock modes can use one of multiple sources (including the external oscillator) to provide maximum flexibility for different application needs. Because the PLL module generates its own clock, the DCO can be locked to a particular reference frequency and then moved to Free-Running mode to reduce system power and noise.

The PLL module includes the following features:

- Five output ranges with output frequencies ranging from 23 to 80 MHz.
- Multiple reference frequency inputs.
- Three output modes: free-running DCO, frequency-locked, and phase-locked.
- Ability to sense the rising edge or falling edge of the reference source.
- DCO frequency LSB dithering to provide finer average output frequencies.
- Spectrum spreading to reduce generated system noise.
- Low jitter and fast lock times.
- Ability to suspend all output frequency updates (including dithering and spectrum spreading) using the STALL bit during jitter-sensitive operations.

4.3.2. Low Power Oscillator (LPOSC0)

The Low Power Oscillator is the default AHB oscillator on SiM3C1xx devices and enables or disables automatically, as needed.

The Low Power Oscillator has the following features:

- 20 MHz and divided 2.5 MHz frequencies available for the AHB clock.
- Automatically starts and stops as needed.

4.3.3. Low Frequency Oscillator (LFOSC0)

The low frequency oscillator (LFOSC0) provides a low power internal clock source running at approximately 16.4 kHz for the RTC0 timer and other peripherals on the device. No external components are required to use the low frequency oscillator

4.3.4. External Oscillators (EXTOSC0)

The EXTOSC0 external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. The external oscillator output may be selected as the AHB clock or used to clock other modules independent of the AHB clock selection.

The External Oscillator control has the following features:

- Support for external crystal, RC, C, or CMOS oscillators.
- Support external CMOS frequencies from 10 kHz to 50 MHz and external crystal frequencies from 10 kHz to 30 MHz.
- Various drive strengths for flexible crystal oscillator support.
- Internal frequency divide-by-two option available.

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4.4. Data Peripherals

4.4.1. 16-Channel DMA Controller

The DMA facilitates autonomous peripheral operation, allowing the core to finish tasks more quickly without spending time polling or waiting for peripherals to interrupt. This helps reduce the overall power consumption of the system, as the device can spend more time in low-power modes.

The DMA controller has the following features:

- Utilizes ARM PrimeCell uDMA architecture.
- Implements 16 channels.
- DMA crossbar supports SARADC0, SARADC1, IDAC0, IDAC1, I2C0, I2S0, SPI0, SPI1, USART0, USART1, AES0, EPCA0, external pin triggers, and timers.
- Supports primary, alternate, and scatter-gather data structures to implement various types of transfers.
- Access allowed to all AHB and APB memory space.

4.4.2. 128/192/256-bit Hardware AES Encryption (AES0)

The basic AES block cipher is implemented in hardware. The integrated hardware support for Cipher Block Chaining (CBC) and Counter (CTR) algorithms results in identical performance, memory bandwidth, and memory footprint between the most basic Electronic Codebook (ECB) algorithm and these more complex algorithms. This hardware accelerator translates to more core bandwidth available for other functions or a power savings for low-power applications.

The AES module includes the following features:

- Operates on 4-word (16-byte) blocks.
- Supports key sizes of 128, 192, and 256 bits for both encryption and decryption.
- Generates the round key for decryption operations.
- All cipher operations can be performed without any firmware intervention for a set of 4-word blocks (up to 32 kB).
- Support for various chained and stream-ciphering configurations with XOR paths on both the input and output.
- Internal 4-word FIFOs to facilitate DMA operations.
- Integrated key storage.
- Hardware acceleration for Cipher-Block Chaining (CBC) and Counter (CTR) algorithms utilizing integrated counterblock generation and previous-block caching.

4.4.3. 16/32-bit CRC (CRC0)

The CRC module is designed to provide hardware calculations for Flash memory verification and communications protocols.

The CRC module supports four common polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3). The three supported 16-bit polynomials are 0x1021 (CCITT-16), 0x3D65 (IEC16-MBus), and 0x8005 (ZigBee, 802.15.4, and USB).

The CRC module includes the following features:

- Support for four common polynomials (one 32-bit and three 16-bit options).
- Byte-level bit reversal for the CRC input.
- Byte-order reorientation of words for the CRC input.
- Word or half-word bit reversal of the CRC result.
- Ability to configure and seed an operation in a single register write.
- Support for single-cycle parallel (unrolled) CRC computation for 32- or 8-bit blocks.
- Capability to CRC 32 bits of data per peripheral bus (APB) clock.
- Support for DMA writes using firmware request mode.

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4.5. Counters/Timers and PWM

4.5.1. Programmable Counter Array (EPCA0, PCA0, PCA1)

The SiM3C1xx devices include two types of PCA module: Enhanced and Standard.

The Enhanced Programmable Counter Array (EPCA0) and Standard Programmable Counter Array (PCA0, PCA1) modules are timer/counter systems allowing for complex timing or waveform generation. Multiple modules run from the same main counter, allowing for synchronous output waveforms.

The Enhanced PCA module is multi-purpose, but is optimized for motor control applications. The EPCA module includes the following features:

- Three sets of channel pairs (six channels total) capable of generating complementary waveforms.
- Center- and edge-aligned waveform generation.
- Programmable dead times that ensure channel pairs are never both active at the same time.
- Programmable clock divisor and multiple options for clock source selection.
- Waveform update scheduling.
- Option to function while the core is inactive.
- Multiple synchronization triggers and outputs.
- Pulse-Width Modulation (PWM) waveform generation.
- High-speed square wave generation.
- Input capture mode.
- DMA capability for both input capture and waveform generation.
- PWM generation halt input.

The Standard PCA module (PCA) includes the following features:

- Two independent channels.
- Center- and edge-aligned waveform generation.
- Programmable clock divisor and multiple options for clock source selection.
- Pulse-Width Modulation waveform generation.

4.5.2. 32-bit Timer (TIMER0, TIMER1)

Each timer module is independent, and includes the following features:

- Operation as a single 32-bit or two independent 16-bit timers.
- Clocking options include the APB clock, the APB clock scaled using an 8-bit prescaler, the external oscillator, or falling edges on an external input pin (synchronized to the APB clock).
- Auto-reload functionality in both 32-bit and 16-bit modes.
- Up/Down count capability, controlled by an external input pin.
- Rising and falling edge capture modes.
- Low or high pulse capture modes.
- Duty cycle capture mode.
- Square wave output mode, which is capable of toggling an external pin at a given rate with 50% duty cycle.
- 32- or 16-bit pulse-width modulation mode.

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4.5.3. Real-Time Clock (RTC0)

The RTC0 module includes a 32-bit timer that allows up to 36 hours of independent time-keeping when used with a 32.768 kHz watch crystal. The RTC0 provides three alarm events in addition to a missing clock event, which can also function as interrupt, reset, or wakeup sources on SiM3C1xx devices.

The RTC0 module includes internal loading capacitors that are programmable to 16 discrete levels, allowing compatibility with a wide range of crystals.

The RTC0 output can be buffered and routed to a port bank pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode. The module also includes a low power internal low frequency oscillator that reduces low power mode current and is available for other modules to use as a clock source.

The RTC module includes the following features:

- 32-bit timer (supports up to 36 hours) with three separate alarms.
- Option for one alarm to automatically reset the RTC timer.
- Missing clock detector.
- Can be used with the internal low frequency oscillator (LFOSC0), an external 32.768 kHz crystal (no additional resistors or capacitors necessary), or with an external CMOS clock.
- Programmable internal loading capacitors support a wide range of external 32.768 kHz crystals.
- Operates directly from VDD and remains operational even when the device goes into its lowest power down mode.
- The RTC timer clock (RTC0TCLK) can be buffered and routed to an I/O pin to provide an accurate, low frequency clock to other devices while the core is in its lowest power down mode.

4.5.4. Low Power Timer (LPTIMER0)

The Low Power Timer (LPTIMER0) module runs from the clock selected by the RTC0 module, allowing the LPTIMER0 to operate even if the AHB and APB clocks are disabled. The LPTIMER0 counter can increment using one of two clock sources: the clock selected by the RTC0 module, or rising or falling edges of an external signal.

The Low Power Timer includes the following features:

- Runs on a low-frequency clock (RTC0TCLK)
- The LPTIMER counter can increment using one of two clock sources: the RTC0TCLK or rising or falling edges of an external signal.
- Overflow and threshold-match detection, which can generate an interrupt, reset the timer, or wake some devices from low power modes.
- Timer reset on threshold-match allows square-wave generation at a variable output frequency.

4.5.5. Watchdog Timer (WDTIMER0)

The WDTIMER0 module includes a 16-bit timer, a programmable early warning interrupt, and a programmable reset period. The timer registers are protected from inadvertent access by an independent lock and key interface.

The watchdog timer runs from the low frequency oscillator (LFOSC0).

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Optional interrupt to warn when the Watchdog Timer is nearing the reset trip value.
- Lock-out feature to prevent any modification until a system reset.

Not Recommended for New Designs

4.6. Communications Peripherals

4.6.1. External Memory Interface (EMIF0)

The External Memory Interface (EMIF0) allows external parallel asynchronous devices, like SRAMs and LCD controllers, to appear as part of the system memory map. The EMIF0 module includes the following features:

- Provides a memory mapped view of multiple external devices.
- Support for byte, half-word and word accesses regardless of external device data-width.
- Error indicator for certain invalid transfers.
- Minimum external timing allows for 3 clocks per write or 4 clocks per read.
- Output bus can be shared between non-muxed and muxed devices.
- Available extended address output allows for up to 24-bit address with 8-bit parallel devices.
- Support for 8-bit and 16-bit (muxed-mode only) devices with up to two chip-select signals.
- Support for internally muxed devices with dynamic address shifting.
- Fully programmable control signal waveforms.

4.6.2. USART (USART0, USART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device. In addition to these signals, the USART0 module can optionally use a clock (UCLK) or hardware handshaking (RTS and CTS).

The USART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud rate generators.
- Synchronous or asynchronous transmissions and receptions.
- Clock master or slave operation with programmable polarity and edge controls.
- Up to 5 Mbaud (synchronous or asynchronous, TX or RX, and master or slave) or 1 Mbaud Smartcard (TX or RX).
- Individual enables for generated clocks during start, stop, and idle states.
- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation (with separate enables).
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.
- Multi-processor communications support.

4.6.3. UART (UART0, UART1)

The USART uses two signals (TX and RX) and a predetermined fixed baud rate to communicate with a single device.

The UART module provides the following features:

- Independent transmitter and receiver configurations with separate 16-bit baud-rate generators.
- Asynchronous transmissions and receptions.
- Up to 5 Mbaud (TX or RX) or 1 Mbaud Smartcard (TX or RX).

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- Internal transmit and receive FIFOs with flush capability and support for byte, half-word, and word reads and writes.
- Data bit lengths from 5 to 9 bits.
- Programmable inter-packet transmit delays.
- Auto-baud detection with support for the LIN SYNC byte.
- Automatic parity generation (with enable).
- Automatic start and stop generation.
- Transmit and receive hardware flow-control.
- Independent inversion correction for TX, RX, RTS, and CTS signals.
- IrDA modulation and demodulation with programmable pulse widths.
- Smartcard ACK/NACK support.
- Parity error, frame error, overrun, and underrun detection.
- Multi-master and half-duplex support.
- Multiple loop-back modes supported.

4.6.4. SPI (SPI0, SPI1)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports up to 10 MHz clock in master mode and 5 MHz clock in slave mode.
- Support for all clock phase and slave select (NSS) polarity modes.
- 16-bit programmable clock rate.
- Programmable MSB-first or LSB-first shifting.
- 8-byte FIFO buffers for both transmit and receive data paths to support high speed transfers.
- Programmable FIFO threshold level to request data service for DMA transfers.
- Support for multiple masters on the same data lines.

4.6.5. I2C (I2C0, I2C1)

The I2C interface is a two-wire, bi-directional serial bus. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte oriented with the I2C interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the APB clock as a master or slave, which can be faster than allowed by the I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The I2C module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Can operate down to APB clock divided by 32768 or up to APB clock divided by 8.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to disable all slave states.
- Programmable clock high and low period.
- Programmable data setup/hold times.

Not Recommended for New Designs

- Spike suppression up to 2 times the APB period.

4.6.6. I²S (I2S0)

The I²S module receives digital data from an external source over a data line in the standard I²S, left-justified, right-justified, or time domain multiplexing format, de-serializes the data, and generates requests to transfer the data using the DMA. The module also reads stereo audio samples from the DMA, serializes the data, and sends it out of the chip on a data line in the same standard serial format for digital audio. The I²S receive interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync), and SD (data input). The block's transmit interface consists of 3 signals: SCK (bit clock), WS (word select or frame sync) and SD (data output).

The I²S module includes the following features:

- Master or slave capability.
- Flexible 10-bit clock divider with 8-bit fractional clock divider provides support for various common sampling frequencies (16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz) for up to two 32-bit channels.
- Support for DMA data transfers.
- Support for various data formats.
- Time Division Multiplexing

Not Recommended for New Designs

4.7. Analog

4.7.1. 12-Bit Analog-to-Digital Converters (SARADC0, SARADC1)

The SARADC0 and SARADC1 modules on SiM3C1xx devices are Successive Approximation Register (SAR) Analog to Digital Converters (ADCs). The key features of the SARADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 250 k samples per second in 12-bit mode or 1 M samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger with hardware channel select.
- Output data window comparator allows automatic range checking.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete, multiple conversion complete, and FIFO overflow and underflow flags and interrupts supported.
- Flexible output data formatting.
- Sequencer allows up to 8 sources to be automatically scanned using one of four channel characteristic profiles without software intervention.
- Eight-word conversion data FIFO for DMA operations.
- Multiple SARADC modules can work together synchronously or by interleaving samples.
- Includes two internal references (1.65 V fast-settling, 1.2/2.4 V precision), support for an external reference, and support for an external signal ground.

4.7.2. Sample Sync Generator (SSG0)

The SSG module includes a phase counter and a pulse generator. The phase counter is a 4-bit free-running counter clocked from the SARADC module clock. Counting-up from zero, the phase counter marks sixteen equally-spaced events for any number of SARADC modules. The ADCs can use this phase counter to start a conversion. The programmable pulse generator creates a 50% duty cycle pulse with a period of 16 phase counter ticks. Up to four programmable outputs available to external devices can be driven by the pulse generator with programmable polarity and a defined output setting when the pulse generator is stopped.

The Sample Sync Generator module has the following features:

- Connects multiple modules together to perform synchronized actions.
- Outputs a clock synchronized to the internal sampling clock used by any number of SARADC modules to pins for use by external devices.
- Includes a phase counter, pulse generator, and up to four programmable outputs.

4.7.3. 10-Bit Digital-to-Analog Converter (IDAC0, IDAC1)

The IDAC takes a digital value as an input and outputs a proportional constant current on a pin. The IDAC module includes the following features:

- 10-bit current DAC with support for four timer, up to seven external I/O, on demand, and SSG0 output update triggers.
- Ability to update on rising, falling, or both edges for any of the external I/O trigger sources (DACnTx).
- Supports an output update rate greater than 600 k samples per second.
- Support for three full-scale output modes: 0.5 mA, 1.0 mA and 2.0 mA.
- Four-word FIFO to aid with high-speed waveform generation or DMA interactions.
- Individual FIFO overrun, underrun, and went-empty interrupt status sources.
- Support for multiple data packing formats, including: single 10-bit sample per word, dual 10-bit samples per word, or four 8-bit samples per word.
- Support for left- and right-justified data.

Not Recommended for New Designs

4.7.4. 16-Channel Capacitance-to-Digital Converter (CAPSENSE0)

The Capacitance Sensing module measures capacitance on external pins and converts it to a digital value. The CAPSENSE module has the following features:

- Multiple start-of-conversion sources (CSnTx).
- Option to convert to 12, 13, 14, or 16 bits.
- Automatic threshold comparison with programmable polarity (“less than or equal” or “greater than”).
- Four operation modes: single conversion, single scan, continuous single conversion, and continuous scan.
- Auto-accumulate mode that will take and average multiple samples together from a single start of conversion signal.
- Single bit retry options available to reduce the effect of noise during a conversion.
- Supports channel bonding to monitor multiple channels connected together with a single conversion.
- Scanning option allows the module to convert a single or series of channels and compare against the threshold while the AHB clock is stopped and the core is in a low power mode.

4.7.5. Low Current Comparators (CMP0, CMP1)

The Comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The Low Power Comparator module includes the following features:

- Multiple sources for the positive and negative poles, including VDD, VREF, and 8 I/O pins.
- Two outputs are available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.

4.7.6. Current-to-Voltage Converter (IVC0)

The IVC module provides inputs to the SARADCn modules so the input current can be measured. The IVC module has the following features:

- Two independent channels.
- Programmable input ranges (1–6 mA full-scale).

Not Recommended for New Designs

4.8. Reset Sources

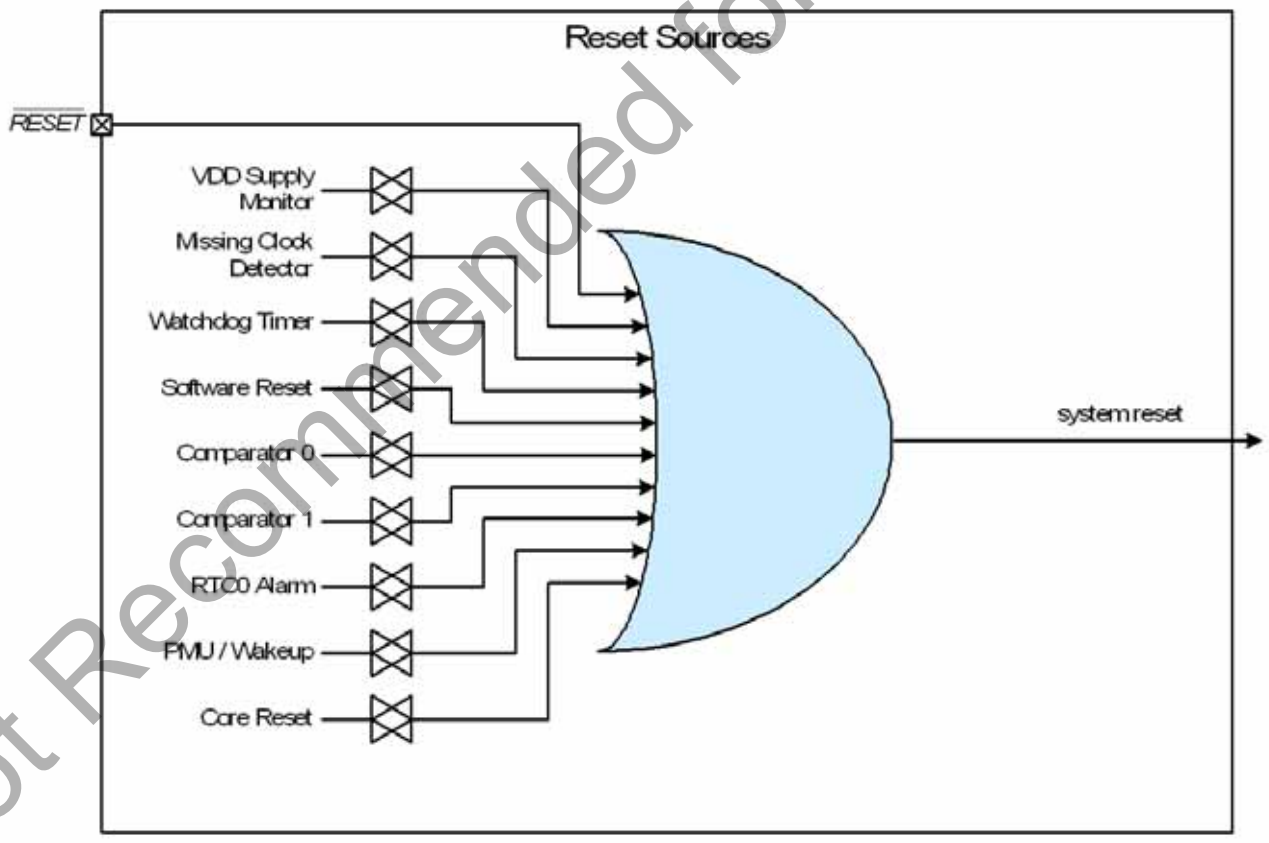
Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.
- Clocks to all AHB peripherals are enabled.
- Clocks to all APB peripherals other than Watchdog Timer, EMIF0, and DMAXBAR are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the $\overline{\text{RESET}}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x00000000.

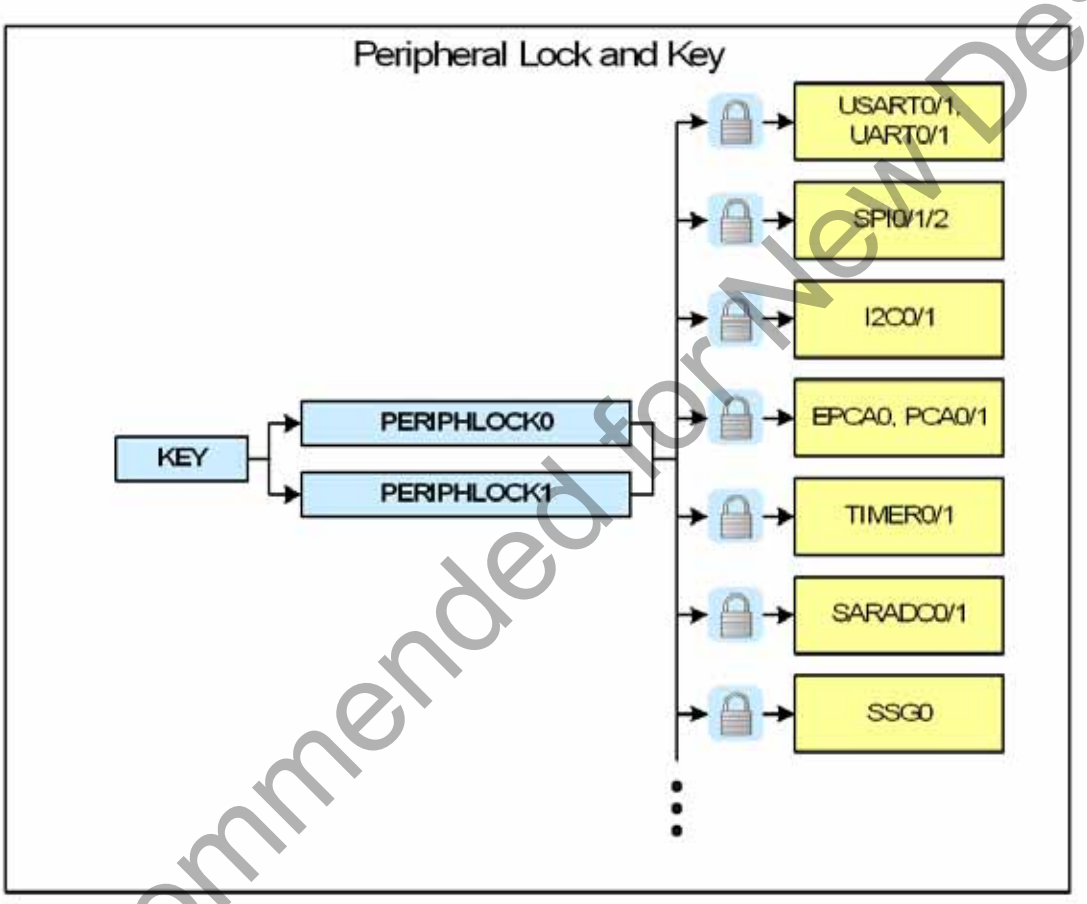


Not Recommended for New Designs

4.9. Security

The peripherals on the SiM3C1xx devices have a register lock and key mechanism that prevents any undesired accesses of the peripherals from firmware. Each bit in the PERIPHLOCKx registers controls a set of peripherals. A key sequence must be written in order to the KEY register to modify any of the bits in PERIPHLOCKx. Any subsequent write to KEY will then inhibit any accesses of PERIPHLOCKx until it is unlocked again through KEY. Reading the KEY register indicates the current status of the PERIPHLOCKx lock state.

If a peripheral's registers are locked, all writes will be ignored. The registers can always be read, regardless of the peripheral's lock state.



4.10. On-Chip Debugging

The SiM3C1xx devices include JTAG and Serial Wire programming and debugging interfaces and ETM for instruction trace. The JTAG interface is supported on SiM3C1x7 and SiM3C1x6 devices only, and does not include boundary scan capabiites. The ETM interface is supported on SiM3C1x7 devices. The JTAG and ETM interfaces can be optionally enabled to provide more visibility while debugging at the cost of using several Port I/O pins. Additionally, if the core is configured for Serial Wire (SW) mode and not JTAG, then the Serial Wire Viewer (SWV) is available to provide a single pin to send out TPIU messages on SiM3C1x7 and SiM3C1x6 devices.

Most peripherals have the option to halt or continue functioning when the core halts in debug mode.

Not Recommended for New Designs

5. Ordering Information

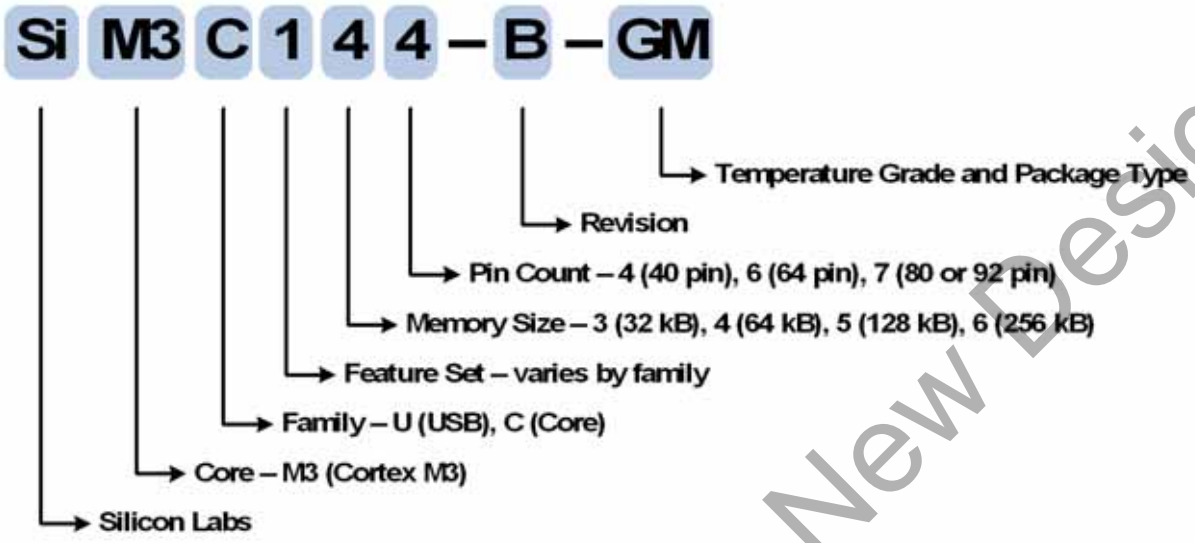


Figure 5.1. SiM3C1xx Part Numbering

All devices in the SiM3C1xx family have the following features:

- **Core:** ARM Cortex-M3 with maximum operating frequency of 80 MHz.
- **Flash Program Memory:** 32-256 kB, in-system programmable.
- **RAM:** 8–32 kB SRAM, with 4 kB retention SRAM.
- **I/O:** Up to 65 multifunction I/O pins, including high-drive and 5 V-tolerant pins.
- **Clock Sources:** Internal and external oscillator options.
- **16-Channel DMA Controller.**
- **128/192/256-bit AES.**
- **16/32-bit CRC.**
- **Timers:** 2 x 32-bit (4 x 16-bit).
- **Real-Time Clock.**
- **Low-Power Timer.**
- **PCA:** 1 x 6 channels (Enhanced), 2 x 2 channels (Standard). PWM, capture, and clock generation capabilites.
- **ADC:** 2 x 12-bit 250 ksps (10-bit 1 Msps) SAR.
- **DAC:** 2 x 10-bit IDAC.
- **Temperature Sensor.**
- **Internal VREF.**
- **16-channel Capacitive Sensing (CAPSENSE).**
- **Comparator:** 2 x low current.
- **Current to Voltage Converter (IVC).**
- **Serial Buses:** 2 x USART, 2 x UART, 3 x SPI, 2 x I2C, 1 x I^2S.

The inclusion of some features varies across different members of the device family. The differences are detailed in Table 5.1.

Not Recommended for New Designs

Table 5.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (kB)	External Memory Interface (EMIF)	Maximum Number of EMIF Address/Data Pins	Digital Port I/Os (Total)	Digital Port I/Os with High Drive Capability	Number of SARADC0 Channels	Number of SARADC1 Channels	Number of CAPSENSE0 Channels	Number of Comparator 0/1 Inputs (+/-)	Number of PMU Pin Wake Sources	JTAG Debugging Interface	ETM Debugging Interface	Serial Wire Debugging Interface	Lead-free (RoHS Compliant)	Package
SiM3C167-B-GM	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C167-B-GQ*	256	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C166-B-GM	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C166-B-GQ*	256	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C164-B-GM	256	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C157-B-GM	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	LGA-92
SiM3C157-B-GQ*	128	32	✓	24	65	6	16	16	16	8/8	16	✓	✓	✓	✓	TQFP-80
SiM3C156-B-GM	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C156-B-GQ*	128	32	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C154-B-GM	128	32			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C146-B-GM	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C146-B-GQ*	64	16	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C144-B-GM	64	16			28	4	7	11	12	3/3	10			✓	✓	QFN-40
SiM3C136-B-GM	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	QFN-64
SiM3C136-B-GQ*	32	8	✓	16	50	4	13	15	15	6/6	15	✓		✓	✓	TQFP-64
SiM3C134-B-GM	32	8			28	4	7	11	12	3/3	10			✓	✓	QFN-40

***Note:** End of life.

Not Recommended for New Designs

6. Pin Definitions and Packaging Information

6.1. SiM3C1x7 Pin Definitions

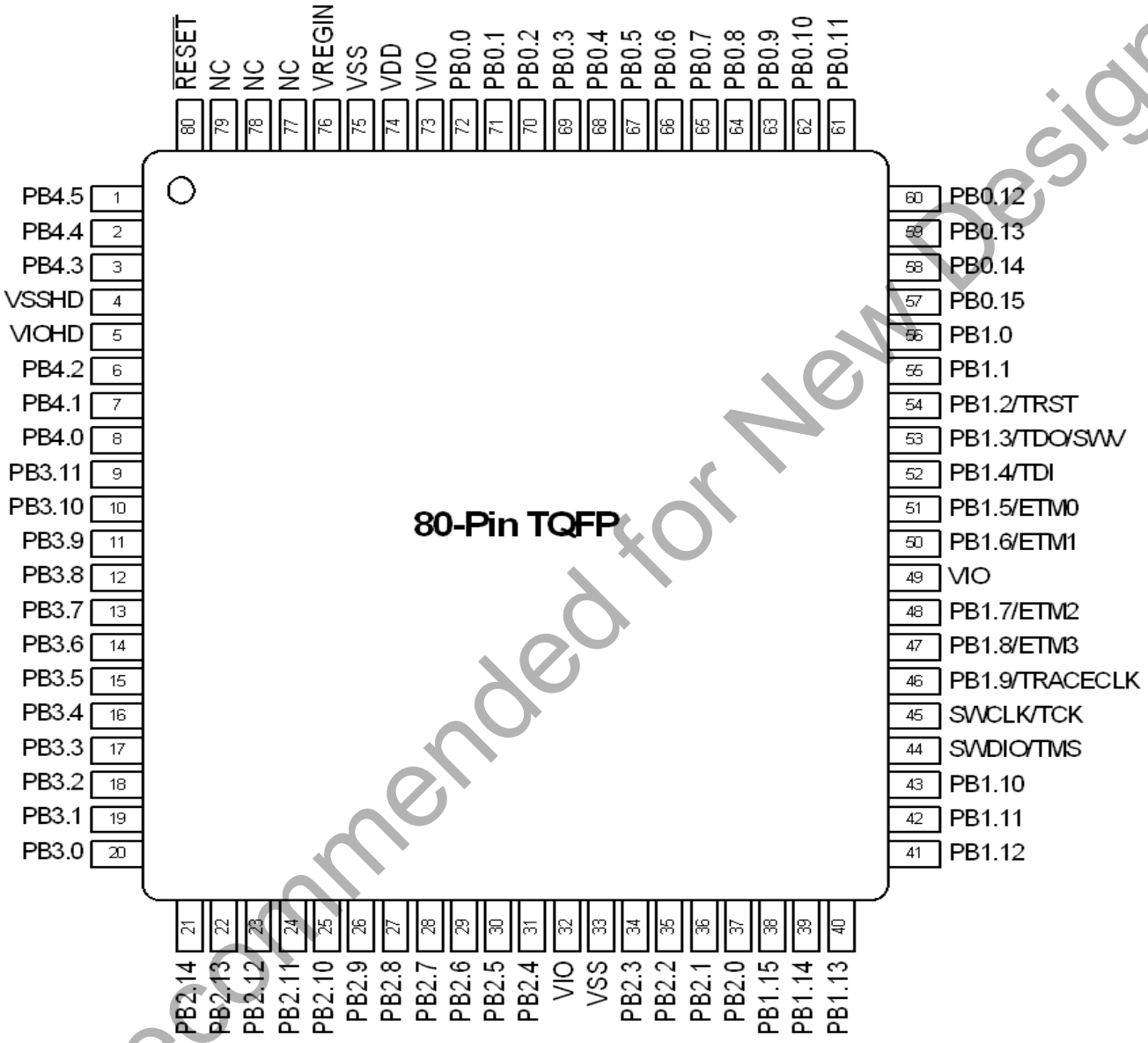
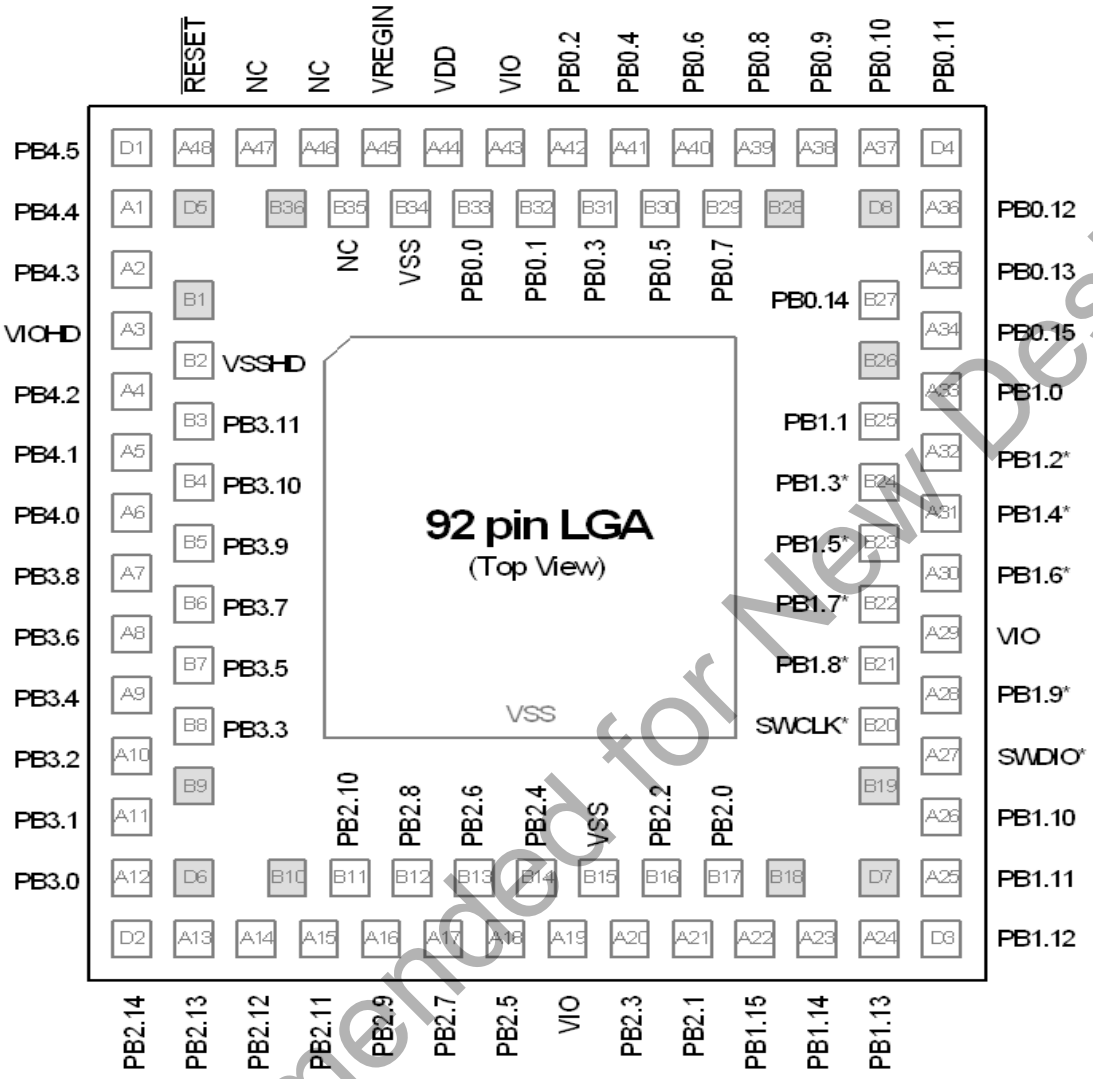


Figure 6.1. SiM3C1x7-GQ Pinout

Not Recommended for New Designs



*Noted pins are listed in the pinout table and 80-pin TQFP package figure with additional names. These alternate functions are also present on the 92-pin LGA package and are identical to those on the 80-pin TQFP package.

Figure 6.2. SiM3C1x7-GM Pinout

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	33 75	B15 B34							
VDD	Power (Core)	74	A44							
VIO	Power (I/O)	32 49 73	A19 A29 A43							
VREGIN	Power (Regulator)	76	A45							
VSSHD	Ground (High Drive)	4	B2							
VIOHD	Power (High Drive)	5	A3							
$\overline{\text{RESET}}$	Active-low Reset	80	A48							
SWCLK/TCK	Serial Wire/JTAG	45	B20							
SWDIO/TMS	Serial Wire/JTAG	44	A27							
PB0.0	Standard I/O	72	B33	XBR0	✓					ADC0.0
PB0.1	Standard I/O	71	B32	XBR0	✓					ADC0.1 CS0.0
PB0.2	Standard I/O	70	A42	XBR0	✓					ADC0.2 CS0.1
PB0.3	Standard I/O	69	B31	XBR0	✓					ADC0.3 CS0.2
PB0.4	Standard I/O	68	A41	XBR0	✓					ADC0.4 CS0.3
PB0.5	Standard I/O	67	B30	XBR0	✓					ADC0.5 CS0.4
PB0.6	Standard I/O	66	A40	XBR0	✓					CS0.5
PB0.7	Standard I/O	65	B29	XBR0	✓					ADC0.6 CS0.6 IVC0.0

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	64	A39	XBR0	✓					ADC0.7 CS0.7 IVC0.1
PB0.9	Standard I/O	63	A38	XBR0	✓					ADC0.8 RTC1
PB0.10	Standard I/O	62	A37	XBR0	✓					RTC2
PB0.11	Standard I/O	61	D4	XBR0	✓					ADC0.9 VREFGND
PB0.12	Standard I/O	60	A36	XBR0	✓					ADC0.10 VREF
PB0.13	Standard I/O	59	A35	XBR0	✓					IDAC0
PB0.14	Standard I/O	58	B27	XBR0	✓					IDAC1
PB0.15	Standard I/O	57	A34	XBR0	✓					XTAL1
PB1.0	Standard I/O	56	A33	XBR0	✓					XTAL2
PB1.1	Standard I/O	55	B25	XBR0	✓					ADC0.11
PB1.2/TRST	Standard I/O /JTAG	54	A32	XBR0	✓					
PB1.3/TDO/ SWV	Standard I/O /JTAG/ Serial Wire Viewer	53	B24	XBR0	✓					ADC0.12 ADC1.12
PB1.4/TDI	Standard I/O /JTAG	52	A31	XBR0	✓					ADC0.13 ADC1.13
PB1.5/ETM0	Standard I/O /ETM	51	B23	XBR0	✓					ADC0.14 ADC1.14
PB1.6/ETM1	Standard I/O /ETM	50	A30	XBR0	✓					ADC0.15 ADC1.15
PB1.7/ETM2	Standard I/O /ETM	48	B22	XBR0	✓					ADC1.11 CS0.8
PB1.8/ETM3	Standard I/O /ETM	47	B21	XBR0	✓					ADC1.10 CS0.9

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.9/ TRACECLK	Standard I/O /ETM	46	A28	XBR0	✓					ADC1.9
PB1.10	Standard I/O	43	A26	XBR0	✓	A23m/ A15			DMA0T1	ADC1.8
PB1.11	Standard I/O	42	A25	XBR0	✓	A22m/ A14			DMA0T0	ADC1.7
PB1.12	Standard I/O	41	D3	XBR0	✓	A21m/ A13				ADC1.6
PB1.13	Standard I/O	40	A24	XBR0	✓	A20m/ A12			ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.14	Standard I/O	39	A23	XBR0	✓	A19m/ A11			ADC1T15 WAKE.1	ADC1.4 CS0.11
PB1.15	Standard I/O	38	A22	XBR0	✓	A18m/ A10			WAKE.2	ADC1.3 CS0.12
PB2.0	Standard I/O	37	B17	XBR1	✓	A17m/ A9	LSI0	Yes	INT0.0 INT1.0 WAKE.3	ADC1.2 CS0.13
PB2.1	Standard I/O	36	A21	XBR1	✓	A16m/ A8	LSI1	Yes	INT0.1 INT1.1 WAKE.4	ADC1.1 CS0.14
PB2.2	Standard I/O	35	B16	XBR1	✓	AD15m/ A7	LSI2	Yes	INT0.2 INT1.2 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB2.3	Standard I/O	34	A20	XBR1	✓	AD14m/ A6	LSI3	Yes	INT0.3 INT1.3 WAKE.6	
PB2.4	Standard I/O	31	B14	XBR1	✓	AD13m/ A5	LSI4	Yes	INT0.4 INT1.4 WAKE.7	
PB2.5	Standard I/O	30	A18	XBR1	✓	AD12m / A4	LSI5	Yes	INT0.5 INT1.5	

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.6	Standard I/O	29	B13	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.7	Standard I/O	28	A17	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.8	Standard I/O	27	B12	XBR1	✓	AD9m/ A1		Yes		
PB2.9	Standard I/O	26	A16	XBR1	✓	AD8m/ A0		Yes		
PB2.10	Standard I/O	25	B11	XBR1	✓	AD7m/ D7		Yes		
PB2.11	Standard I/O	24	A15	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.12	Standard I/O	23	A14	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.13	Standard I/O	22	A13	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.14	Standard I/O	21	D2	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB3.0	5 V Tolerant I/O	20	A12	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB3.1	5 V Tolerant I/O	19	A11	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2
PB3.2	5 V Tolerant I/O	18	A10	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.3	5 V Tolerant I/O	17	B8	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.4	5 V Tolerant I/O	16	A9	XBR1	✓	$\overline{OE}$			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.5	5 V Tolerant I/O	15	B7	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.6	5 V Tolerant I/O	14	A8	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
PB3.7	5 V Tolerant I/O	13	B6	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.8	5 V Tolerant I/O	12	A7	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.9	5 V Tolerant I/O	11	B5	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN
PB3.10	5 V Tolerant I/O	10	B4	XBR1	✓				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.11	5 V Tolerant I/O	9	B3	XBR1	✓				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD

Not Recommended for New Designs

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.0	High Drive I/O	8	A6				LSO0			
PB4.1	High Drive I/O	7	A5				LSO1			
PB4.2	High Drive I/O	6	A4				LSO2			
PB4.3	High Drive I/O	3	A2				LSO3			
PB4.4	High Drive I/O	2	A1				LSO4			
PB4.5	High Drive I/O	1	D1				LSO5			

Note: All unnamed pins on the LGA-92 package are no-connect pins. They should be soldered to the PCB for mechanical stability, but have no internal connections to the device.

Not Recommended for New Designs

6.2. SiM3C1x6 Pin Definitions

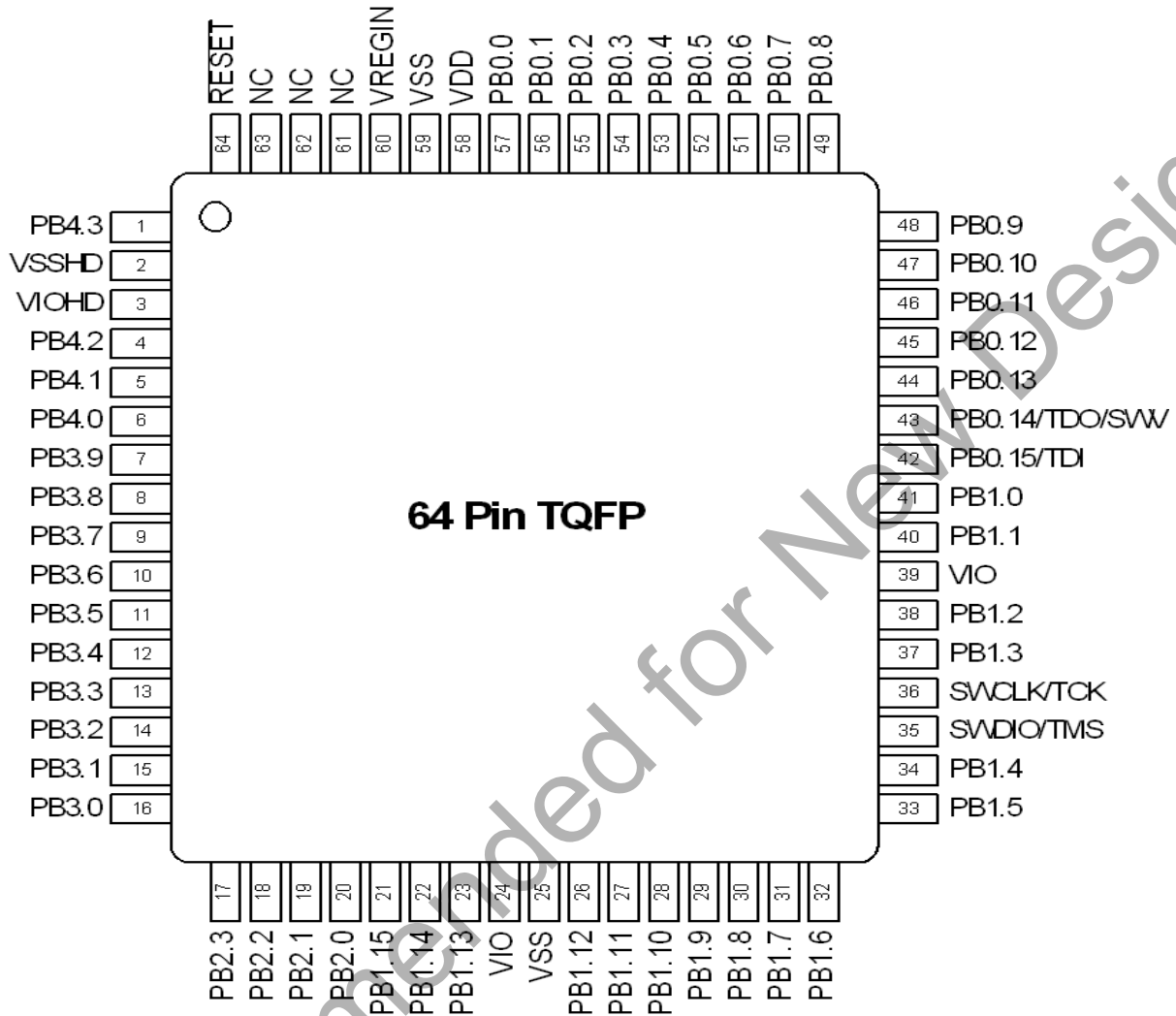


Figure 6.3. SiM3C1x6-GQ Pinout

Not Recommended for New Designs

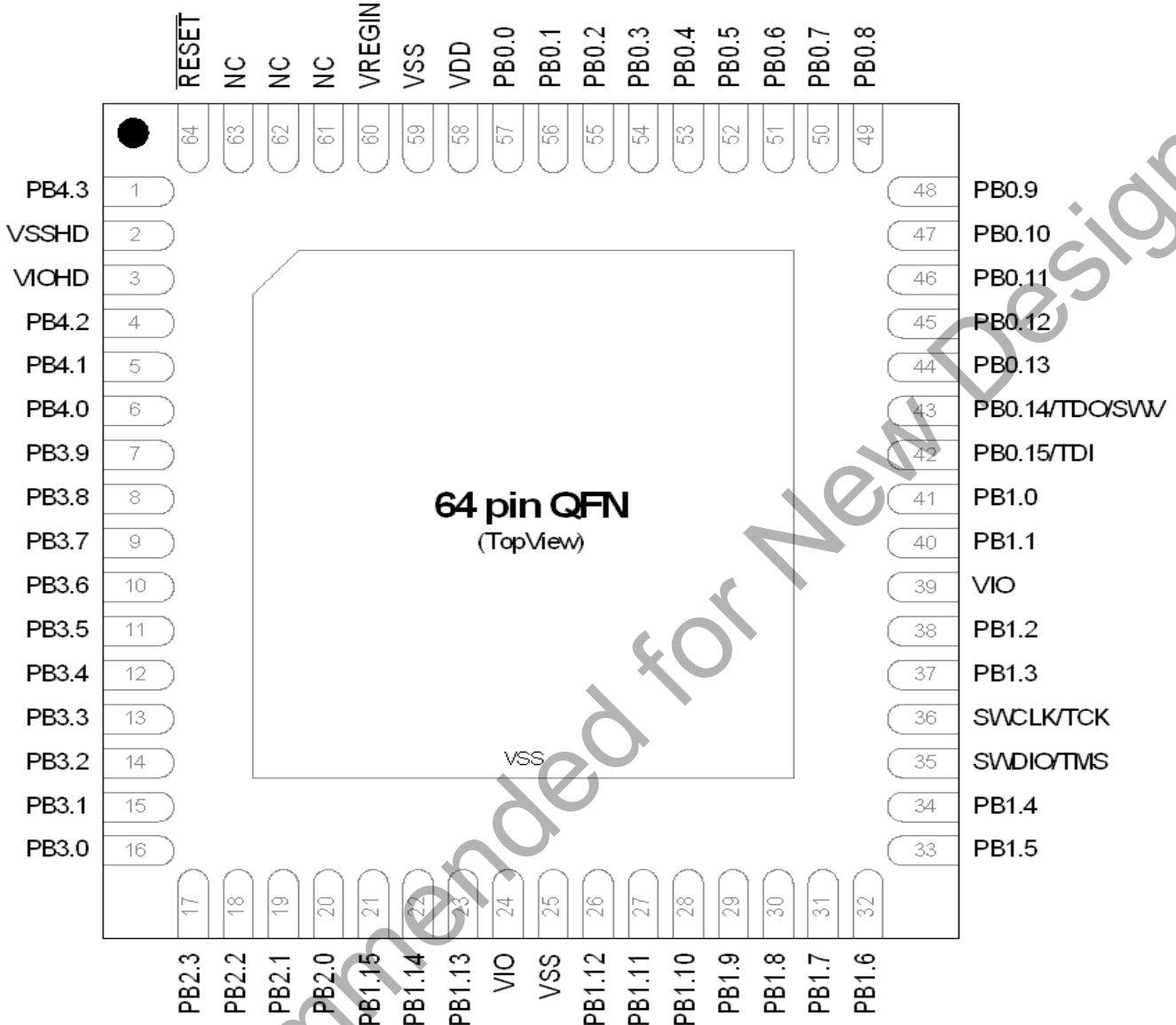


Figure 6.4. SiM3C1x6-GM Pinout

Not Recommended for New Designs

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	25 59							
VDD	Power (Core)	58							
VIO	Power (I/O)	24 39							
VREGIN	Power (Regulator)	60							
VSSHD	Ground (High Drive)	2							
VIOHD	Power (High Drive)	3							
$\overline{\text{RESET}}$	Active-low Reset	64							
SWCLK/TCK	Serial Wire / JTAG	36							
SWDIO/TMS	Serial Wire / JTAG	35							
PB0.0	Standard I/O	57	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	56	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	55	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	54	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	53	XBR0	✓					ADC0.6 CS0.5 IVC0.0
PB0.5	Standard I/O	52	XBR0	✓					ADC0.7 CS0.6 IVC0.1
PB0.6	Standard I/O	51	XBR0	✓					ADC0.8 CS0.7 RTC1

Not Recommended for New Designs

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.7	Standard I/O	50	XBR0	✓					RTC2
PB0.8	Standard I/O	49	XBR0	✓					ADC0.9 VREFGND
PB0.9	Standard I/O	48	XBR0	✓					ADC0.10 VREF
PB0.10	Standard I/O	47	XBR0	✓					ADC1.6 IDAC0
PB0.11	Standard I/O	46	XBR0	✓					IDAC1
PB0.12	Standard I/O	45	XBR0	✓					XTAL1
PB0.13	Standard I/O	44	XBR0	✓					XTAL2
PB0.14/TDO/ SWV	Standard I/O / JTAG / Serial Wire Viewer	43	XBR0	✓					ADC0.12 ADC1.12
PB0.15/TDI	Standard I/O / JTAG	42	XBR0	✓					ADC0.13 ADC1.13
PB1.0	Standard I/O	41	XBR0	✓					ADC0.14 ADC1.14
PB1.1	Standard I/O	40	XBR0	✓					ADC0.15 ADC1.15
PB1.2	Standard I/O	38	XBR0	✓					ADC1.11 CS0.8
PB1.3	Standard I/O	37	XBR0	✓					ADC1.10 CS0.9
PB1.4	Standard I/O	34	XBR0	✓					ADC1.8
PB1.5	Standard I/O	33	XBR0	✓					ADC1.7
PB1.6	Standard I/O	32	XBR0	✓				ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.7	Standard I/O	31	XBR0	✓	AD15m/ A7			ADC1T15 WAKE.1	ADC1.4 CS0.11

Not Recommended for New Designs

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.8	Standard I/O	30	XBR0	✓	AD14m/ A6			WAKE.2	ADC1.3 CS0.12
PB1.9	Standard I/O	29	XBR0	✓	AD13m/ A5			WAKE.3	ADC1.2 CS0.13
PB1.10	Standard I/O	28	XBR0	✓	AD12m/ A4			DMA0T1 WAKE.4	ADC1.1 CS0.14
PB1.11	Standard I/O	27	XBR0	✓	AD11m/ A3			DMA0T0 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.12	Standard I/O	26	XBR0	✓	AD10m/ A2			WAKE.6	
PB1.13	Standard I/O	23	XBR0	✓	AD9m/ A1				
PB1.14	Standard I/O	22	XBR0	✓	AD8m/ A0				
PB1.15	Standard I/O	21	XBR0	✓	AD7m/ D7				
PB2.0	Standard I/O	20	XBR1	✓	AD6m/ D6	LSI0	Yes	INT0.0 INT1.0	
PB2.1	Standard I/O	19	XBR1	✓	AD5m/ D5	LSI1	Yes	INT0.1 INT1.1	
PB2.2	Standard I/O	18	XBR1	✓	AD4m/ D4	LSI2	Yes	INT0.2 INT1.2	CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.3	Standard I/O	17	XBR1	✓	AD3m/ D3	LSI3	Yes	INT0.3 INT1.3	CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	16	XBR1	✓	AD2m/ D2				CMP0P.1 CMP1P.1
PB3.1	5 V Tolerant I/O	15	XBR1	✓	AD1m/ D1				CMP0N.1 CMP1N.1

Not Recommended for New Designs

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.2	5 V Tolerant I/O	14	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0 WAKE.8	CMP0P.2 CMP1P.2
PB3.3	5 V Tolerant I/O	13	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9	CMP0N.2 CMP1N.2
PB3.4	5 V Tolerant I/O	12	XBR1	✓	$\overline{OE}$			INT0.5 INT1.5 WAKE.10	CMP0P.3 CMP1P.3
PB3.5	5 V Tolerant I/O	11	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11	CMP0N.3 CMP1N.3
PB3.6	5 V Tolerant I/O	10	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12	CMP0P.4 CMP1P.4 EXREGSP
PB3.7	5 V Tolerant I/O	9	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13	CMP0N.4 CMP1N.4 EXREGSN
PB3.8	5 V Tolerant I/O	8	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14	CMP0P.5 CMP1P.5 EXREGOUT

Not Recommended for New Designs

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

Not Recommended for New Designs

6.3. SiM3C1x4 Pin Definitions

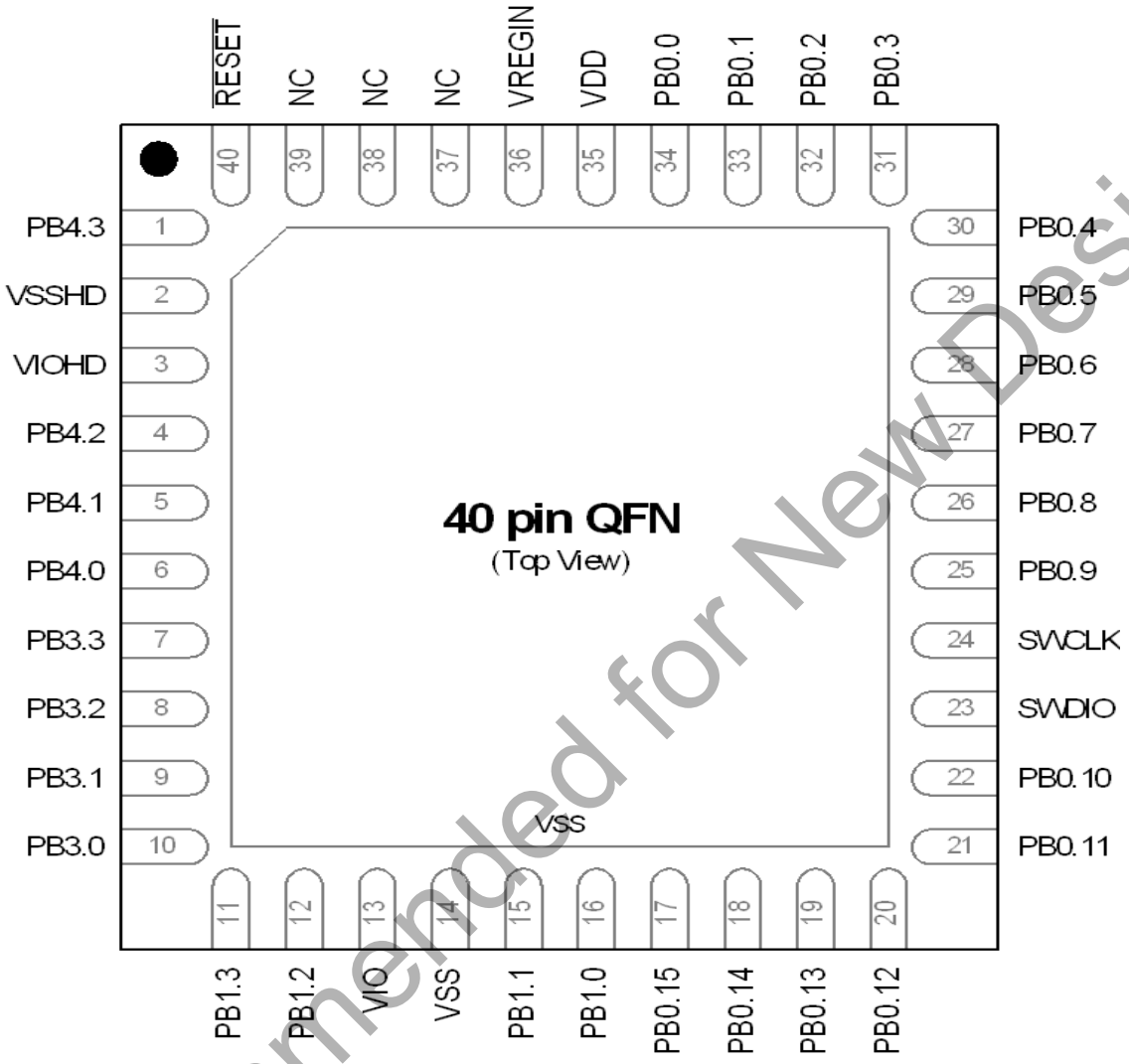


Figure 6.5. SiM3C1x4-GM Pinout

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	14					
VDD	Power (Core)	35					
VIO	Power (I/O)	13					
VREGIN	Power (Regulator)	36					
VSSHD	Ground (High Drive)	2					
VIOHD	Power (High Drive)	3					
$\overline{\text{RESET}}$	Active-low Reset	40					
SWCLK	Serial Wire	24					
SWDIO	Serial Wire	23					
PB0.0	Standard I/O	34	XBR0	✓			ADC0.8 CS0.7 RTC1
PB0.1	Standard I/O	33	XBR0	✓			RTC2
PB0.2	Standard I/O	32	XBR0	✓			ADC0.9 CS0.0 VREFGND
PB0.3	Standard I/O	31	XBR0	✓			ADC0.10 CS0.1 VREF
PB0.4	Standard I/O	30	XBR0	✓			ADC1.6 CS0.2 IDAC0
PB0.5	Standard I/O	29					IDAC1
PB0.6	Standard I/O	28	XBR0	✓			ADC0.0 CS0.3 XTAL1
PB0.7	Standard I/O	27	XBR0	✓			ADC0.1 CS0.4 XTAL2

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	✓			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	✓			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	✓		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	✓		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	✓		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	✓		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	✓		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	✓		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	✓		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	✓		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	✓			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	✓			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	✓		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

Not Recommended for New Designs

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

Not Recommended for New Designs

6.4. LGA-92 Package Specifications

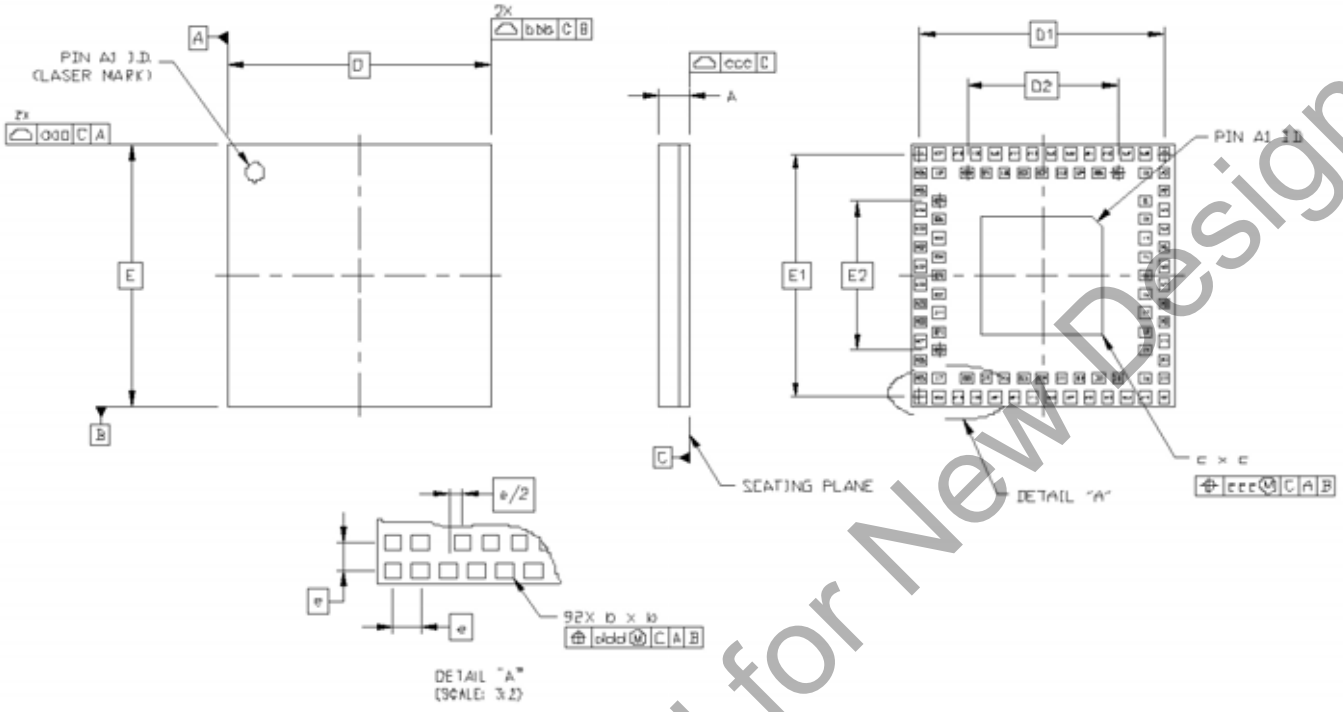


Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

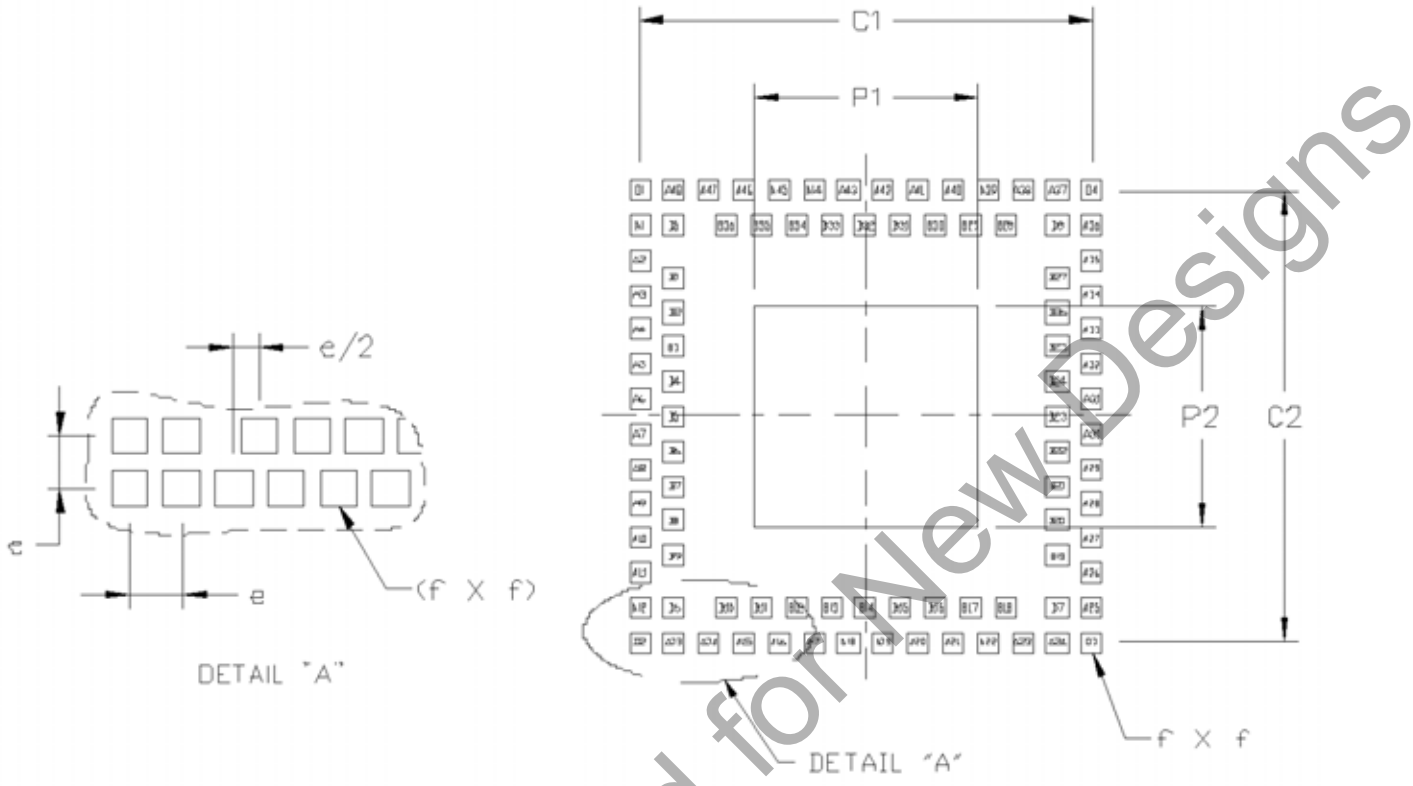


Figure 6.7. LGA-92 Landing Diagram

Table 6.5. LGA-92 Landing Diagram Dimensions

Dimension	Typical	Max
C1	6.50	—
C2	6.50	—
e	0.50	—
f	—	0.35
P1	—	3.20
P2	—	3.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
3. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
4. This land pattern design is based on the IPC-7351 guidelines.

Not Recommended for New Designs

6.4.1. LGA-92 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.4.2. LGA-92 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 2 x 2 array of 1.25 mm square openings on 1.60 mm pitch should be used for the center ground pad.

6.4.3. LGA-92 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.5. TQFP-80 Package Specifications

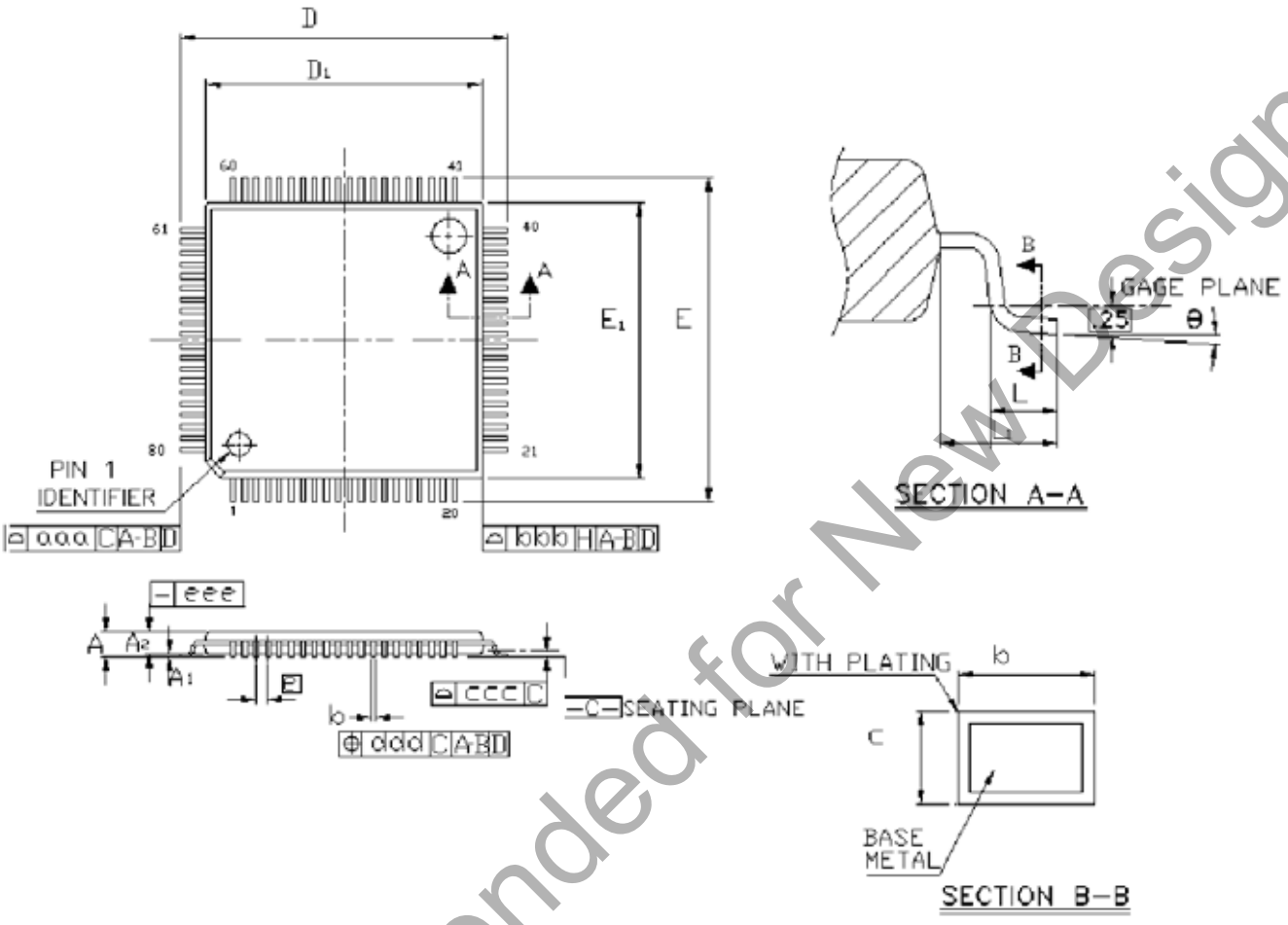


Figure 6.8. TQFP-80 Package Drawing

Table 6.6. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		

Not Recommended for New Designs

Table 6.6. TQFP-80 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
L	0.45	0.60	0.75
L1		1.00 Ref	
Θ	0°	3.5°	7°
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.08	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Not Recommended for New Designs

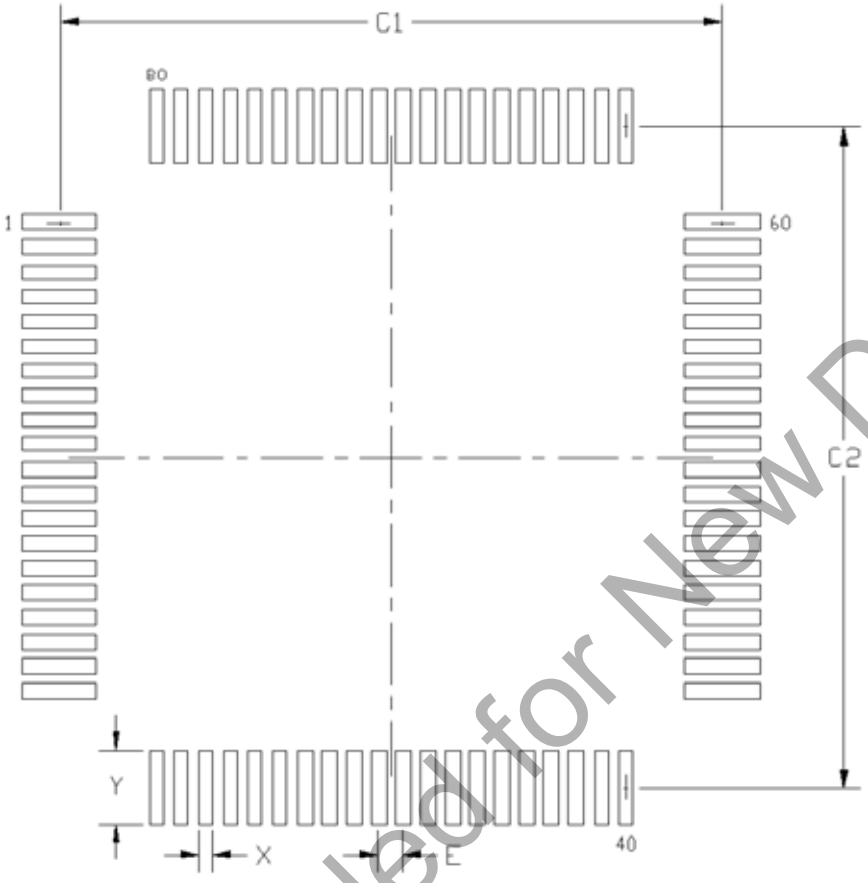


Figure 6.9. TQFP-80 Landing Diagram

Table 6.7. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Not Recommended for New Designs

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.6. QFN-64 Package Specifications

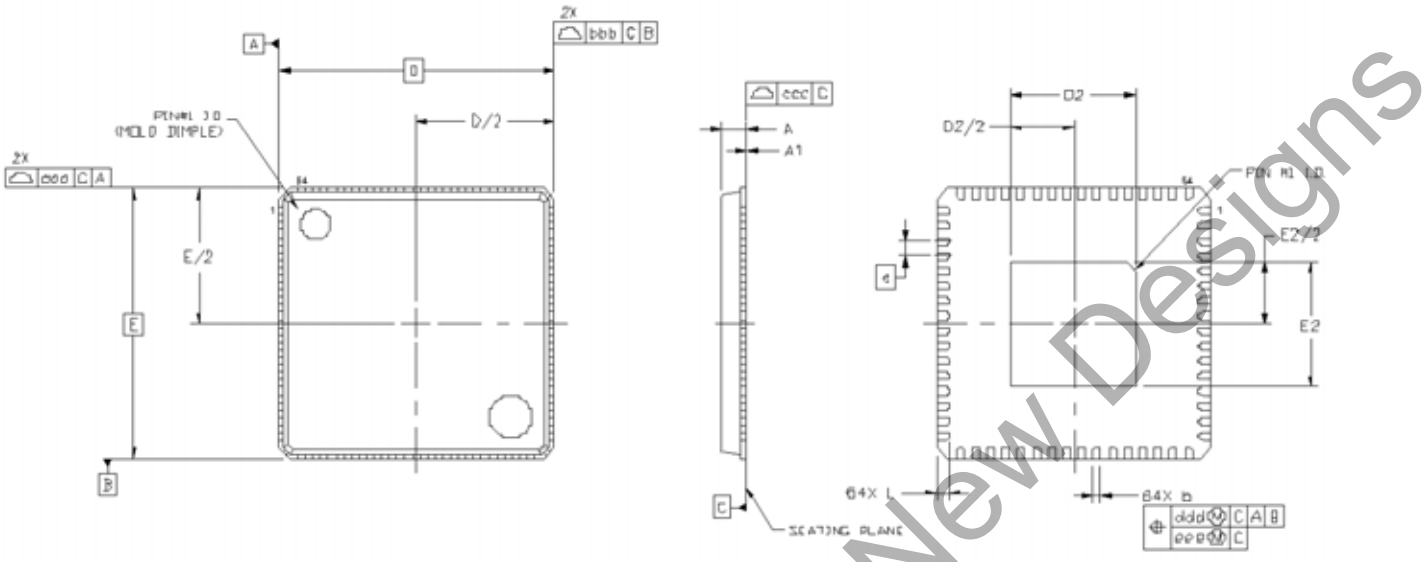


Figure 6.10. QFN-64 Package Drawing

Table 6.8. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

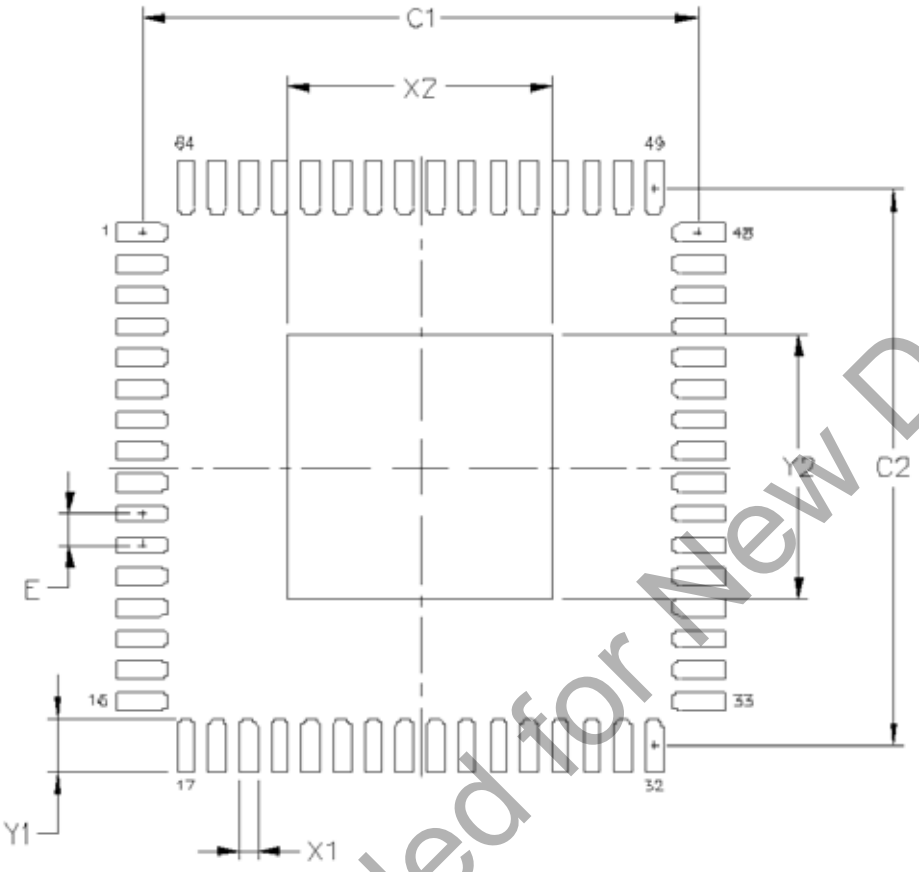


Figure 6.11. QFN-64 Landing Diagram

Table 6.9. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Not Recommended for New Designs

6.6.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.6.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.7. TQFP-64 Package Specifications

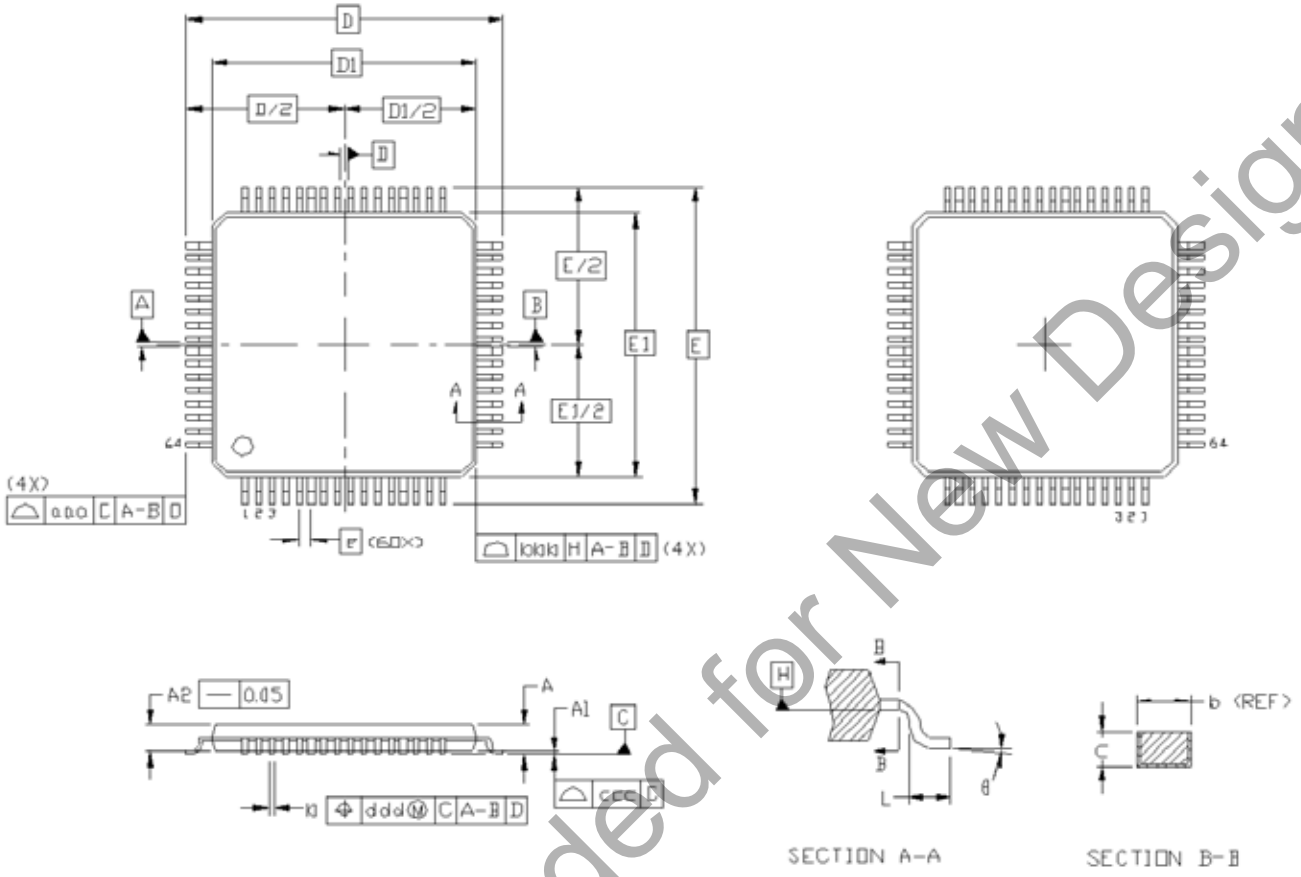


Figure 6.12. TQFP-64 Package Drawing

Table 6.10. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°

Not Recommended for New Designs

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

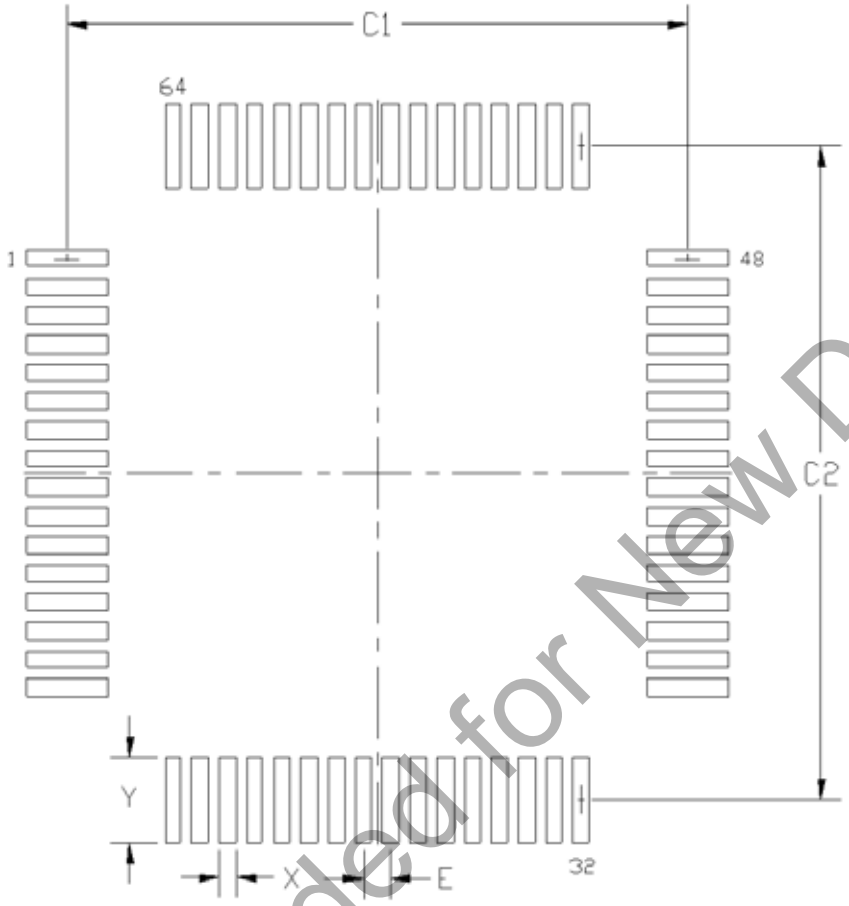


Figure 6.13. TQFP-64 Landing Diagram

Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Not Recommended for New Designs

6.7.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.7.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.8. QFN-40 Package Specifications

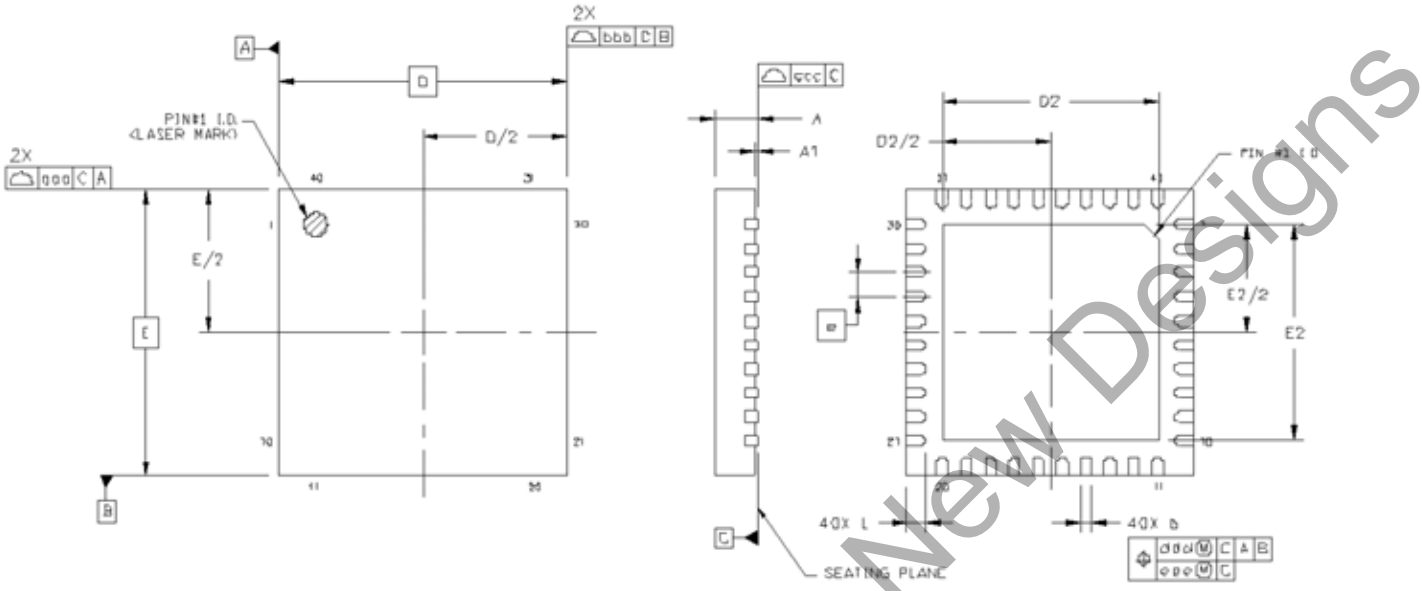


Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

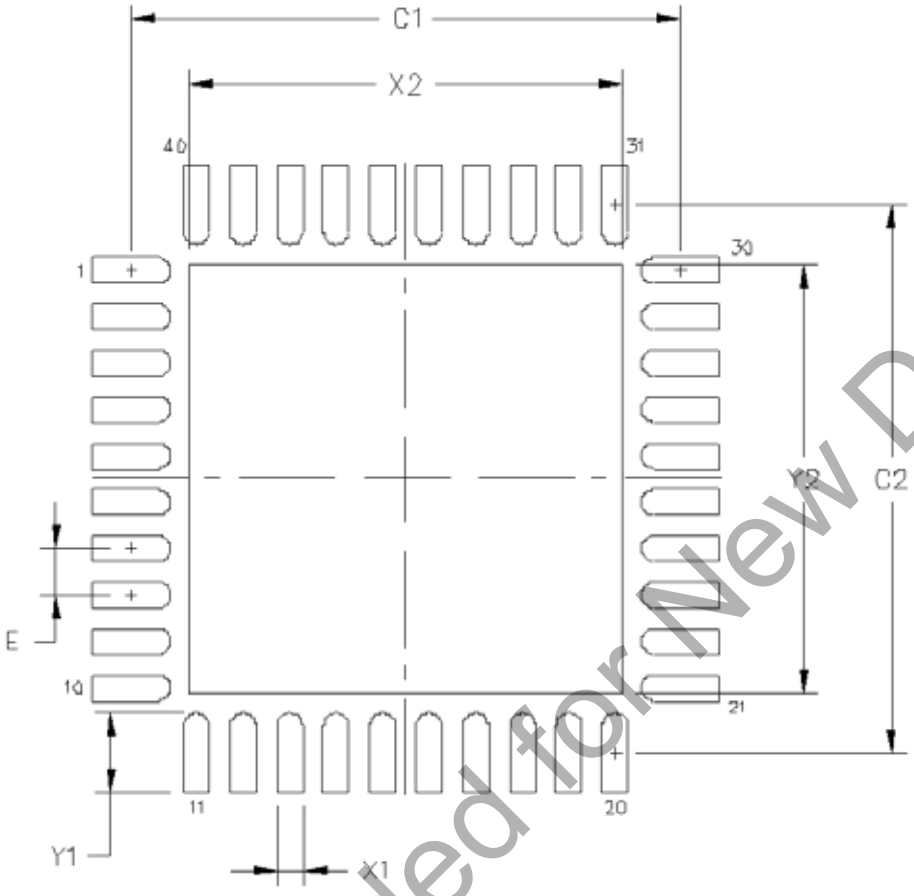


Figure 6.15. QFN-40 Landing Diagram

Table 6.13. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Not Recommended for New Designs

6.8.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.8.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.8.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

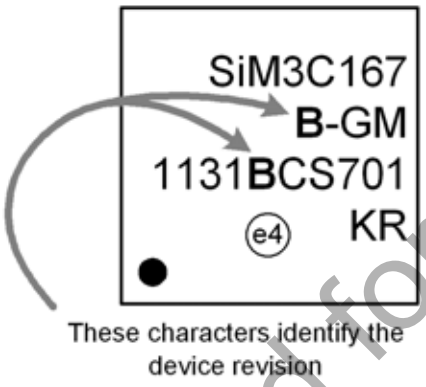


Figure 7.1. LGA-92 SiM3C1x7 Revision Information

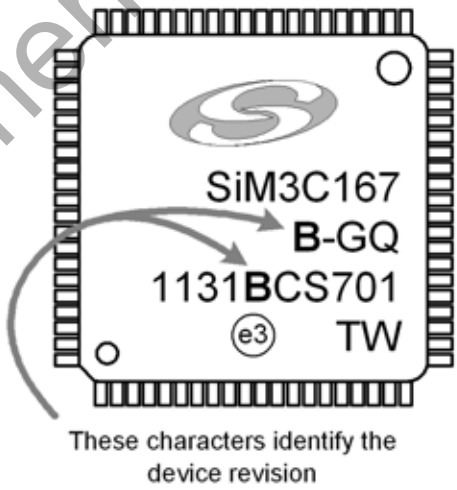


Figure 7.2. TQFP-80 SiM3C1x7 Revision Information

Not Recommended for New Designs

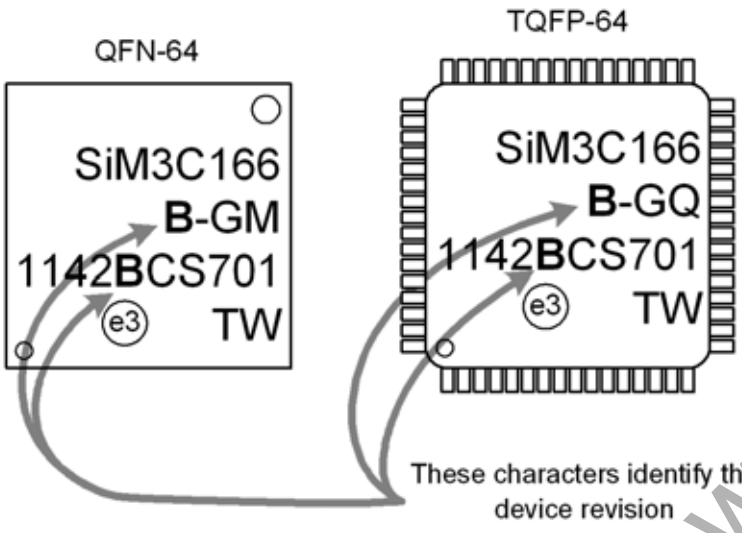


Figure 7.3. SiM3C1x6 Revision Information

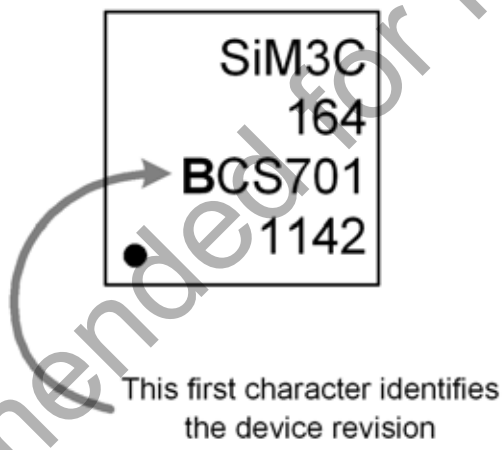


Figure 7.4. SiM3C1x4 Revision Information

7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.

Not Recommended for New Designs

Document Change List

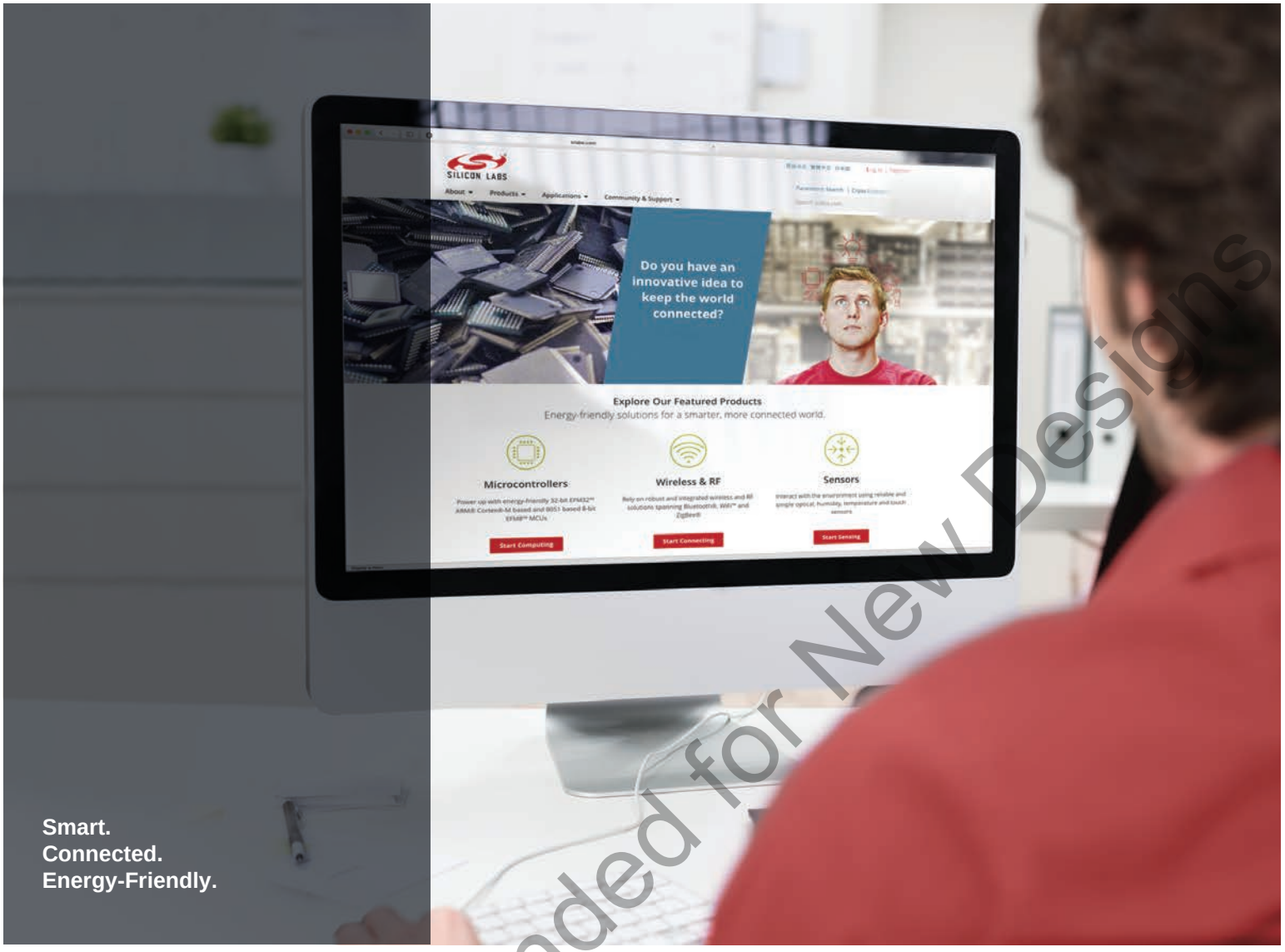
Revision 1.0 to Revision 1.1

- Added end of life note to Table 5.1, “Product Selection Guide,” on page 50.

Revision 0.8 to Revision 1.0

- Added block diagram to front page; updated feature bullet lists.
- Electrical Specifications Tables Additions:
  - Voltage Regulator Current Sense Supply Current, Typ = 3 µA (Table 3.2)
  - Power Mode 2 Wake Time, Min = 4 clocks, Max = 5 clocks (Table 3.3)
  - External Crystal Clock Frequency, Min = 0.01 MHz, Max = 30 MHz (Table 3.9)
  - Added /RESET pin characteristics (Table 3.17)
- Electrical Specifications Tables Removals:
  - Power Mode 3 Wake Time (Table 3.3)
- Electrical Specifications Tables Corretions/Adjustments:
  - IVC Supply Current, Max = 2.5 µA (Table 3.2)
  - VREG0 Output Voltage Normal Mode, Min = 3.15 V (Table 3.5)
  - VREG0 Output Voltage Suspend Mode, Min = 3.15 V (Table 3.5)
  - External Regulator Internal Pull-Down, Typ = 5 kΩ (Table 3.6)
  - External Regulator Internal Pull-Up, Typ = 10 kΩ (Table 3.6)
  - Flash Memory Endurance, Typ = 100k write/erase cycles (Table 3.7)
  - Flash Memory Retention, Min = 10 Years, Typ = 100 Years (Table 3.7)
  - Low Power Oscillator Frequency, Min = 19.5 MHz, Max = 20.5 MHz (Table 3.8)
  - SAR Dynamic Performance : consolidated all specs. (Table 3.10)
  - IDAC Full Scale Output Current 1 mA Range, Min = 0.99 mA (Table 3.11)
  - IDAC Full Scale Output Current 0.5 mA Range, Min = 493 µA (Table 3.11)
  - IVC Slope @ 1 mA, Min = 1.55 V/mA, Max = 1.75 V/mA (Table 3.13)
  - IVC Slope @ 2 mA, Min = 795 mV/mA, Max = 860 mV/mA (Table 3.13)
  - IVC Slope @ 3 mA, Min = 525 mV/mA, Max = 570 mV/mA (Table 3.13)
  - IVC Slope @ 4 mA, Min = 390 mV/mA, Max = 430 mV/mA (Table 3.13)
  - IVC Slope @ 5 mA, Min = 315 mV/mA (Table 3.13)
  - IVC Slope @ 6 mA, Min = 260 mV/mA (Table 3.13)
  - Temperature Sensor Slope Error, Type = ±120 µV/C (Table 3.15)
  - Comparator Input Offset Voltage, Min = –10 mV, Max = 10 mV (Table 3.16)
- “4. Precision32™ SiM3C1xx System Overview” :
  - Updated Power Modes discussion.
  - Refined and updated feature bullet lists.
- Updated and clarified RTC timer clock output. The RTC output is now referred to as "RTC0TCLK".
- “6. Pin Definitions and Packaging Information” : Renamed RTC0OSC_OUT function to RTC0TCLK_OUT for consistency.
- “7. Revision Specific Behavior” : Updated revision identification drawings to better match physical appearance of packages.

Not Recommended for New Designs



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