



**THE DATASHEET OF  
R7FA6M2AF3CFB#AA0**



Leading performance 120-MHz Arm® Cortex®-M4 core, up to 1-MB code flash memory, 384-KB SRAM, Capacitive Touch Sensing Unit, Ethernet MAC Controller, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

## Features

### ■ Arm Cortex-M4 Core with Floating Point Unit (FPU)

- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

### ■ Memory

- Up to 1-MB code flash memory (40 MHz zero wait states)
- 32-KB data flash memory (125,000 erase/write cycles)
- Up to 384-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity

- Ethernet MAC Controller (ETHERC)
- Ethernet DMA Controller (EDMAC)
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver
- Serial Communications Interface (SCI) with FIFO × 10
- Serial Peripheral Interface (SPI) × 2
- I<sup>2</sup>C bus interface (IIC) × 3
- Controller Area Network (CAN) × 2
- Serial Sound Interface Enhanced (SSIE)
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8-bit or 16-bit bus space is selectable per area
  - SDRAM support

### ■ Analog

- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Temperature Sensor (TSN)

### ■ Timers

- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 6
- Low Power Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety

- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management

- Low power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption

- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSU)
- Parallel Data Capture Unit (PDC)

### ■ Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General-Purpose I/O Ports

- Up to 110 input/output pins
  - Up to 1 CMOS input
  - Up to 109 CMOS input/output
    - Up to 21 input/output 5 V tolerant
    - Up to 18 high current (20 mA)

### ■ Operating Voltage

- VCC: 2.7 to 3.6 V

### ■ Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

## 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 1-MB code flash memory
- 384-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC), USBFS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Analog peripherals.

### 1.1 Function Outline

**Table 1.1 Arm core**

Feature	Functional description
Arm Cortex-M4 core	<ul style="list-style-type: none"> <li>• Maximum operating frequency: up to 120 MHz</li> <li>• Arm Cortex-M4 core:               <ul style="list-style-type: none"> <li>- Revision: r0p1-01rel0</li> <li>- ARMv7E-M architecture profile</li> <li>- Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008.</li> </ul> </li> <li>• Arm Memory Protection Unit (Arm MPU):               <ul style="list-style-type: none"> <li>- Armv7 Protected Memory System Architecture</li> <li>- 8 protect regions.</li> </ul> </li> <li>• SysTick timer:               <ul style="list-style-type: none"> <li>- Driven by SYSTICCLK (LOCO) or ICLK.</li> </ul> </li> </ul>

**Table 1.2 Memory**

Feature	Functional description
Code flash memory	Maximum 1-MB code flash memory. See section 53, Flash Memory in User's Manual.
Data flash memory	32-KB data flash memory. See section 53, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 error correction capability using ECC. Parity check is performed for other areas. See section 51, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 52, Standby SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: <ul style="list-style-type: none"> <li>• Single-chip mode</li> <li>• SCI or USB boot mode.</li> </ul> See section 3, Operating Modes in User's Manual.
Resets	14 resets: <ul style="list-style-type: none"> <li>• RES pin reset</li> <li>• Power-on reset</li> <li>• Voltage monitor 0 reset</li> <li>• Voltage monitor 1 reset</li> <li>• Voltage monitor 2 reset</li> <li>• Independent watchdog timer reset</li> <li>• Watchdog timer reset</li> <li>• Deep Software Standby reset</li> <li>• SRAM parity error reset</li> <li>• SRAM ECC error reset</li> <li>• Bus master MPU error reset</li> <li>• Bus slave MPU error reset</li> <li>• Stack pointer error reset</li> <li>• Software reset.</li> </ul> See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	<ul style="list-style-type: none"> <li>• Main clock oscillator (MOSC)</li> <li>• Sub-clock oscillator (SOSC)</li> <li>• High-speed on-chip oscillator (HOCO)</li> <li>• Middle-speed on-chip oscillator (MOCO)</li> <li>• Low-speed on-chip oscillator (LOCO)</li> <li>• PLL frequency synthesizer</li> <li>• IWDT-dedicated on-chip oscillator</li> <li>• Clock out support.</li> </ul> See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 11, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 10, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 12, Low Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 13, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 14, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.

**Table 1.3 System (2 of 2)**

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual.

**Table 1.4 Event link**

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

**Table 1.5 Direct memory access**

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMAC module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

**Table 1.6 External bus interface**

Feature	Functional description
External buses	<ul style="list-style-type: none"> <li>CS area (EXBIU): Connected to the external devices (external memory interface)</li> <li>SDRAM area (EXBIU): Connected to the SDRAM (external memory interface)</li> <li>QSPI area (EXBIUT2): Connected to the QSPI (external device interface).</li> </ul>

**Table 1.7 Timers (1 of 2)**

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Low Power Asynchronous General-Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Low Power Asynchronous General-Purpose Timer (AGT) in User's Manual.

**Table 1.7 Timers (2 of 2)**

Feature	Functional description
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

**Table 1.8 Communication interfaces (1 of 2)**

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> <li>• Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))</li> <li>• 8-bit clock synchronous interface</li> <li>• Simple IIC (master-only)</li> <li>• Simple SPI</li> <li>• Smart card interface.</li> </ul> The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 32, Serial Communications Interface (SCI) in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 33, IrDA Interface in User's Manual.
I <sup>2</sup> C bus interface (IIC)	The 3-channel I <sup>2</sup> C bus interface (IIC) conforms with and provides a subset of the NXP I <sup>2</sup> C (Inter-Integrated Circuit) bus interface functions. See section 34, I <sup>2</sup> C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 36, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I <sup>2</sup> S (Inter-Integrated Sound) 2ch, 4ch, 6ch, 8ch, Word Select (WS) Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 39, Serial Sound Interface Enhanced (SSIE) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 37, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 35, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 31, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

**Table 1.8 Communication interfaces (2 of 2)**

Feature	Functional description
Ethernet MAC (ETHERC)	One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 41, SD/MMC Host Interface (SDHI) in User's Manual.

**Table 1.9 Analog**

Feature	Functional description
12-bit A/D Converter (ADC12)	Two units of successive approximation 12-bit A/D Converter (ADC12) are provided. Analog input channels are selectable up to 13 in unit 0 and up to 9 in unit 1. Each 2 analog inputs of unit 0 and 1 are assigned to same port (AN005/AN105, AN006/AN106), up to 20 ports are available as analog input. The temperature sensor output and an internal reference voltage are selectable for conversion of each unit 0 and 1. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 45, 12-Bit A/D Converter (ADC12) in User's Manual.
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 46, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature sensor (TSN)	The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 47, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 48, High-Speed Analog Comparator (ACMPHS) in User's Manual.

**Table 1.10 Human machine interfaces**

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 49, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

**Table 1.11 Graphics**

Feature	Functional description
Parallel Data Capture (PDC) unit	One Parallel Data Capture (PDC) unit is provided to communicate with external I/O devices, including image sensors, and to transfer parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 42, Parallel Data Capture Unit (PDC) in User's Manual.

**Table 1.12 Data processing**

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 38, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 50, Data Operation Circuit (DOC) in User's Manual.
Sampling Rate Converter (SRC)	The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 40, Sampling Rate Converter (SRC) in User's Manual.

**Table 1.13 Security**

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	<ul style="list-style-type: none"> <li>• Security algorithms: <ul style="list-style-type: none"> <li>- Symmetric algorithms: AES, 3DES, and ARC4</li> <li>- Asymmetric algorithms: RSA, DSA, and ECC.</li> </ul> </li> <li>• Other support features: <ul style="list-style-type: none"> <li>- TRNG (True Random Number Generator)</li> <li>- Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5</li> <li>- 128-bit unique ID.</li> </ul> </li> </ul> See section 44, Secure Cryptographic Engine (SCE7) in User's Manual.

**Table 1.14 I/O ports**

Feature	Functional description
Programmable I/O ports	<ul style="list-style-type: none"> <li>• I/O ports for the 145-pin LGA, 144-pin LQFP <ul style="list-style-type: none"> <li>- I/O pins: 109</li> <li>- Input pins: 1</li> <li>- Pull-up resistors: 110</li> <li>- N-ch open-drain outputs: 109</li> <li>- 5-V tolerance: 21</li> </ul> </li> <li>• I/O ports for the 100-pin LQFP <ul style="list-style-type: none"> <li>- I/O pins: 75</li> <li>- Input pins: 1</li> <li>- Pull-up resistors: 76</li> <li>- N-ch open-drain outputs: 75</li> <li>- 5-V tolerance: 14</li> </ul> </li> </ul>

## 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

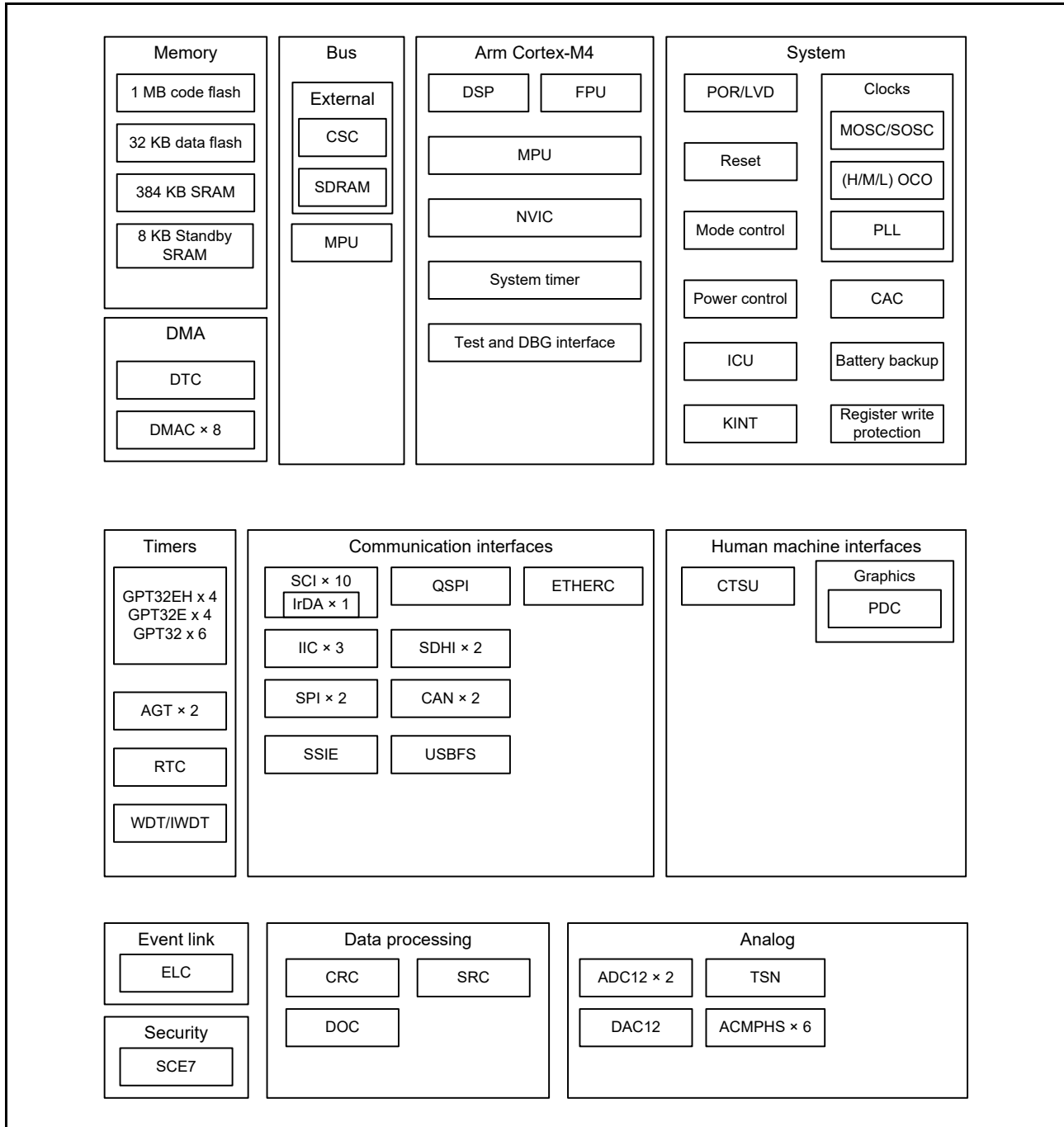


Figure 1.1 Block diagram

### 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.15 shows a list of products.

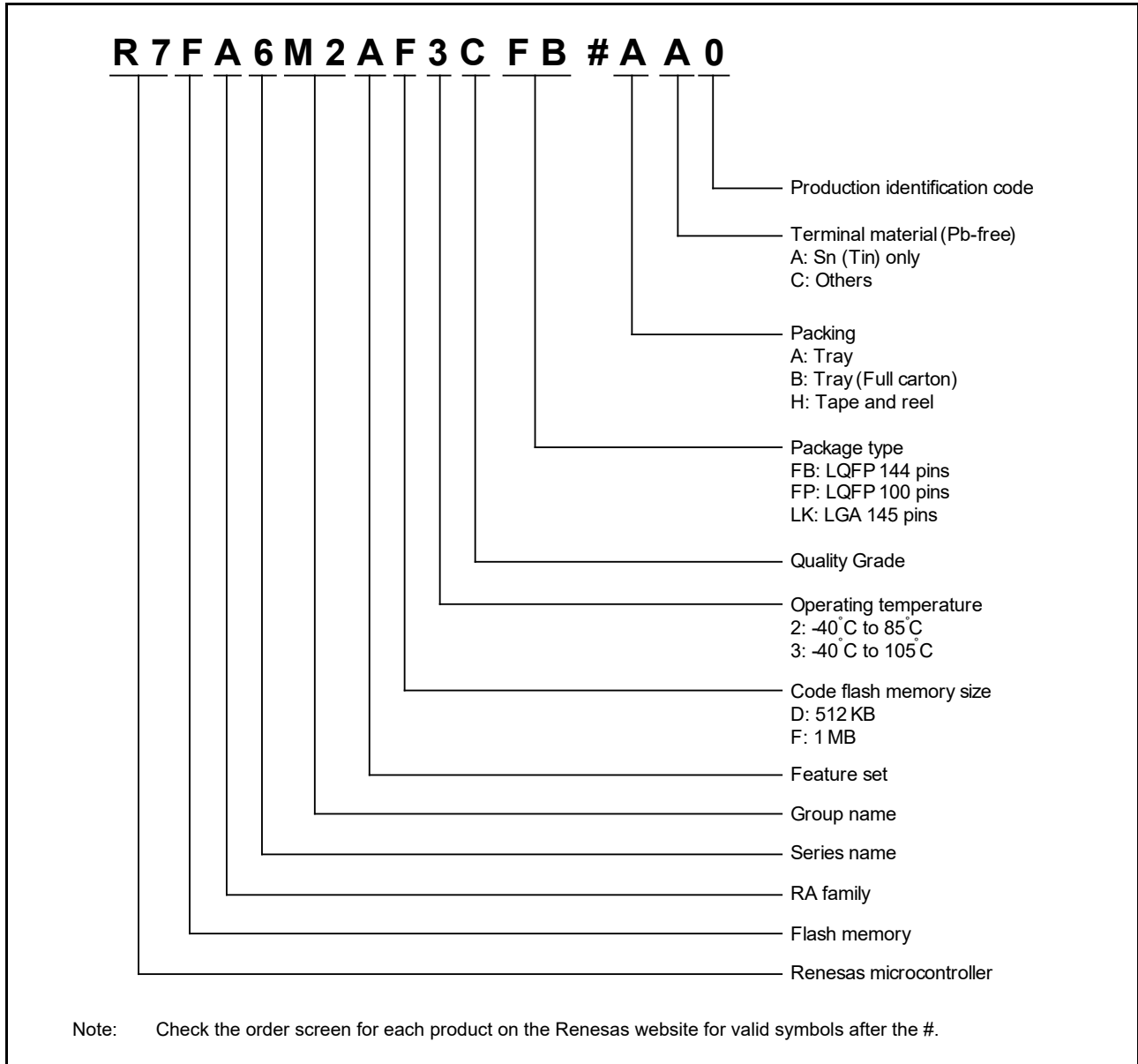


Figure 1.2 Part numbering scheme

**Table 1.15 Product list**

Product part number	Package	Code flash	Data flash	SRAM	Operating temperature
R7FA6M2AF2CLK	PTLG0145KA-A	1 MB	32 KB	384 KB	-40 to +85°C
R7FA6M2AF3CLK					-40 to +105°C
R7FA6M2AF3CFB	PLQP0144KA-B	512 KB	32 KB	384 KB	-40 to +105°C
R7FA6M2AF3CFP	PLQP0100KB-B				-40 to +105°C
R7FA6M2AD2CLK	PTLG0145KA-A	512 KB	32 KB	384 KB	-40 to +85°C
R7FA6M2AD3CLK					-40 to +105°C
R7FA6M2AD3CFB	PLQP0144KA-B	512 KB	32 KB	384 KB	-40 to +105°C
R7FA6M2AD3CFP	PLQP0100KB-B				-40 to +105°C

## 1.4 Function Comparison

**Table 1.16 Functional comparison**

Function	Part numbers		
	R7FA6M2AF2CLK/ R7FA6M2AD2CLK/ R7FA6M2AF3CLK/ R7FA6M2AD3CLK	R7FA6M2AF3CFB/ R7FA6M2AD3CFB	R7FA6M2AF3CFP/ R7FA6M2AD3CFP
Pin count	145	144	100
Package	LGA	LQFP	LQFP
Code flash memory	1 MB/512 KB		
Data flash memory	32 KB		
SRAM	384 KB		
Parity	352 KB		
ECC	32 KB		
Standby SRAM	8 KB		
System	CPU clock	120 MHz	
	Backup registers	512 B	
	ICU	Yes	
	KINT	8	
Event link	ELC	Yes	
DMA	DTC	Yes	
	DMAC	8	
BUS	External bus	16-bit bus	8-bit bus
	SDRAM	Yes	No
Timers	GPT32EH	4	4
	GPT32E	4	4
	GPT32	6	6
	AGT	2	2
	RTC	Yes	
	WDT/IWDT	Yes	
Communication	SCI	10	
	IIC	3	2
	SPI	2	
	SSIE	1	
	QSPI	1	
	SDHI	2	
	CAN	2	
	USBFS	Yes	
	ETHERC	1	
Analog	ADC12	Unit0: 13 Unit1: 9 Shared channel pin: 2*1	Unit0: 11 Unit1: 8 Shared channel pin: 2*1
	3ch-S/H	Unit0: 1 (3ch) Unit1: 1 (3ch)	
	DAC12	2	
	ACMPHS	6	
	TSN	Yes	
HMI	CTSU	18	12
	Graphics	PDC	Yes
Data processing	CRC	Yes	
	DOC	Yes	
	SRC	Yes	
Security	SCE7		
I/O ports	I/O pins	109	75
	Input pins	1	1
	Pull-up resistors	110	76
	N-ch open-drain outputs	109	75
	5-V tolerance	21	14

Note 1. Some input channels of the ADC units are sharing same port pin.

## 1.5 Pin Functions

Table 1.17 Pin functions (1 of 5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect it to the system power supply. Connect this pin to VSS by a 0.1- $\mu$ F capacitor. Place the capacitor close to the pin.
	VCL0	-	Connect to VSS through a 0.1- $\mu$ F smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOU and XCIN.
	XCOU	Output	
	EBCLK	Output	Outputs the external bus clock for external devices
	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
	SWO	Output	Serial wire trace output pin
	External bus interface	RD	Output
WR		Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low
WR0 to WR1		Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active-low
BC0 to BC1		Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active-low
ALE		Output	Address latch signal when address/data multiplexed bus is selected
WAIT		Input	Input pin for wait request signals in access to the external space, active-low
CS0 to CS7		Output	Select signals for CS areas, active-low
A00 to A20		Output	Address bus
D00 to D15		I/O	Data bus
A00/D00 to A15/D15		I/O	Address/data multiplexed bus

Table 1.17 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active-low
	RAS	Output	SDRAM low address strobe signal, active-low
	CAS	Output	SDRAM column address strobe signal, active-low
	WE	Output	SDRAM write enable signal, active-low
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08
	A00 to A15	Output	Address bus
DQ00 to DQ15	I/O	Data bus	
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOUWP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
	AGT	AGTEE0, AGTEE1	Input
AGTIO0, AGTIO1		I/O	External event input and pulse output pins
AGTO0, AGTO1		Output	Pulse output pins
AGTOA0, AGTOA1		Output	Output compare match A output pins
AGTOB0, AGTOB1		Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0 to SCL9	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDA0 to SDA9	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active-low	
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock
	SDA0 to SDA2	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	SSIDATA0	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)

**Table 1.17 Pin functions (3 of 5)**

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	Receive data
	CTX0, CTX1	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode	

Table 1.17 Pin functions (4 of 5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission
	ET0_RX_ER	Input	Receive error pin. Functions as signal to recognize an error during reception
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO
ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI	
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins
	SD0CD, SD1CD	Input	SD card detection pins
	SD0WP	Input	SD write-protect signals
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

**Table 1.17 Pin functions (5 of 5)**

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	Input pins for the analog signals to be processed by the ADC12. AN005 & AN105 and AN006 & AN106 are assigned to same port pin
	AN100 to AN102, AN105 to AN107, AN116 to AN118	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
	ADTRG1	Input	
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter
ACMPHS	VCOU	Output	Comparator output pin
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator
CTS	TS00 to TS17	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
I/O ports	P000 to P009, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P214	I/O	General-purpose input/output pins
	P300 to P313	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P506, P508, P511, P512	I/O	General-purpose input/output pins
	P600 to P605, P608 to P614	I/O	General-purpose input/output pins
	P700 to P705, P708 to P713	I/O	General-purpose input/output pins
P800, P801	I/O	General-purpose input/output pins	
PDC	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock

### 1.6 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments.

**R7FA6M2AX2CLK**

	A	B	C	D	E	F	G	H	J	K	L	M	N		
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13	
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOU	VBATT	P701	P404	P511	VCC	12	
11	VCC_USB	VSS_USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11	
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10	
9	P203	P313	P202	VSS						P004	P006	P009	P008	9	
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8	
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7	
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6	
5	P309	P311	P308	P303	NC						P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4	
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3	
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2	
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N		

**Figure 1.3 Pin assignment for 145-pin LGA (top view)**

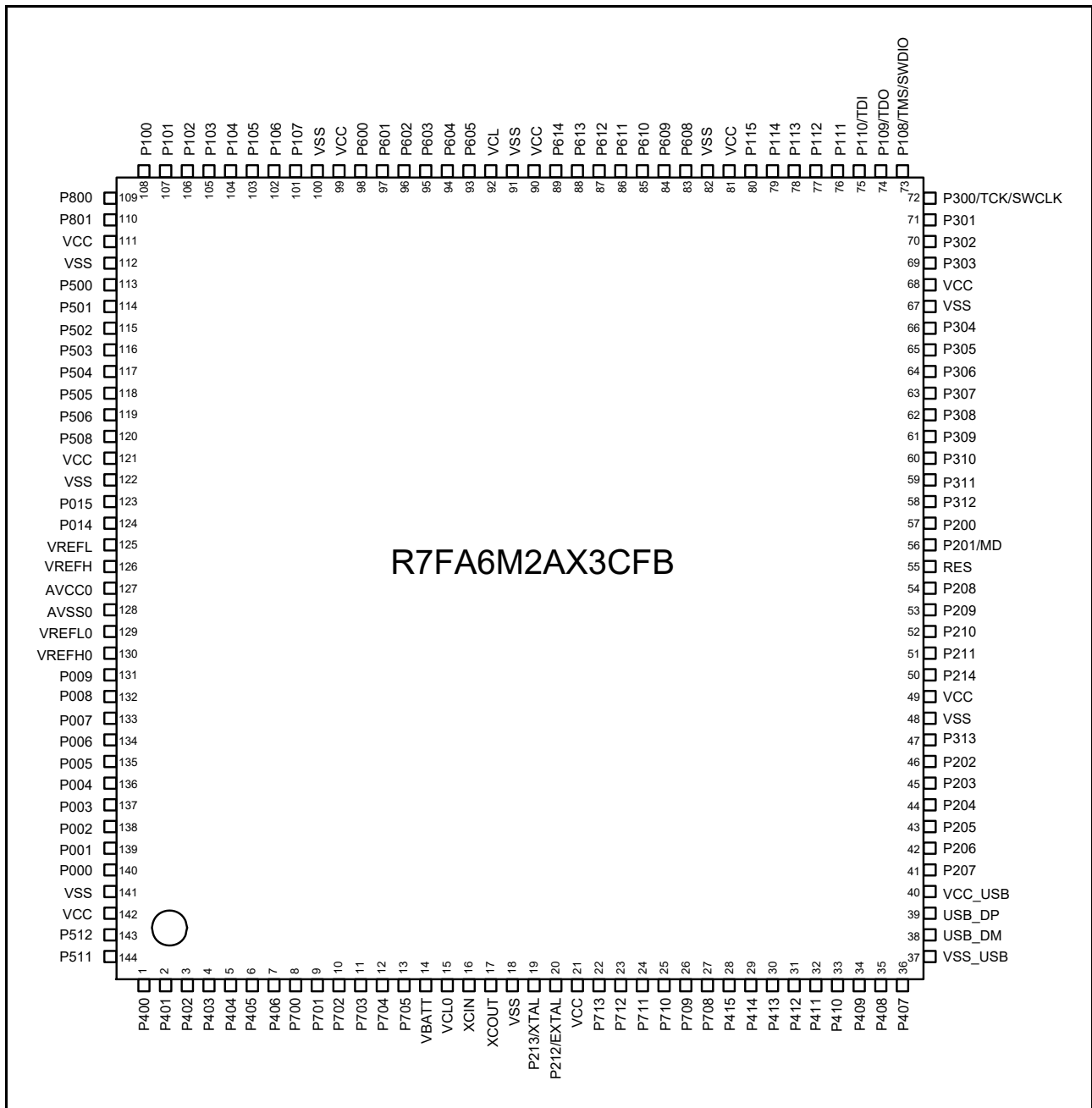


Figure 1.4 Pin assignment for 144-pin LQFP (top view)

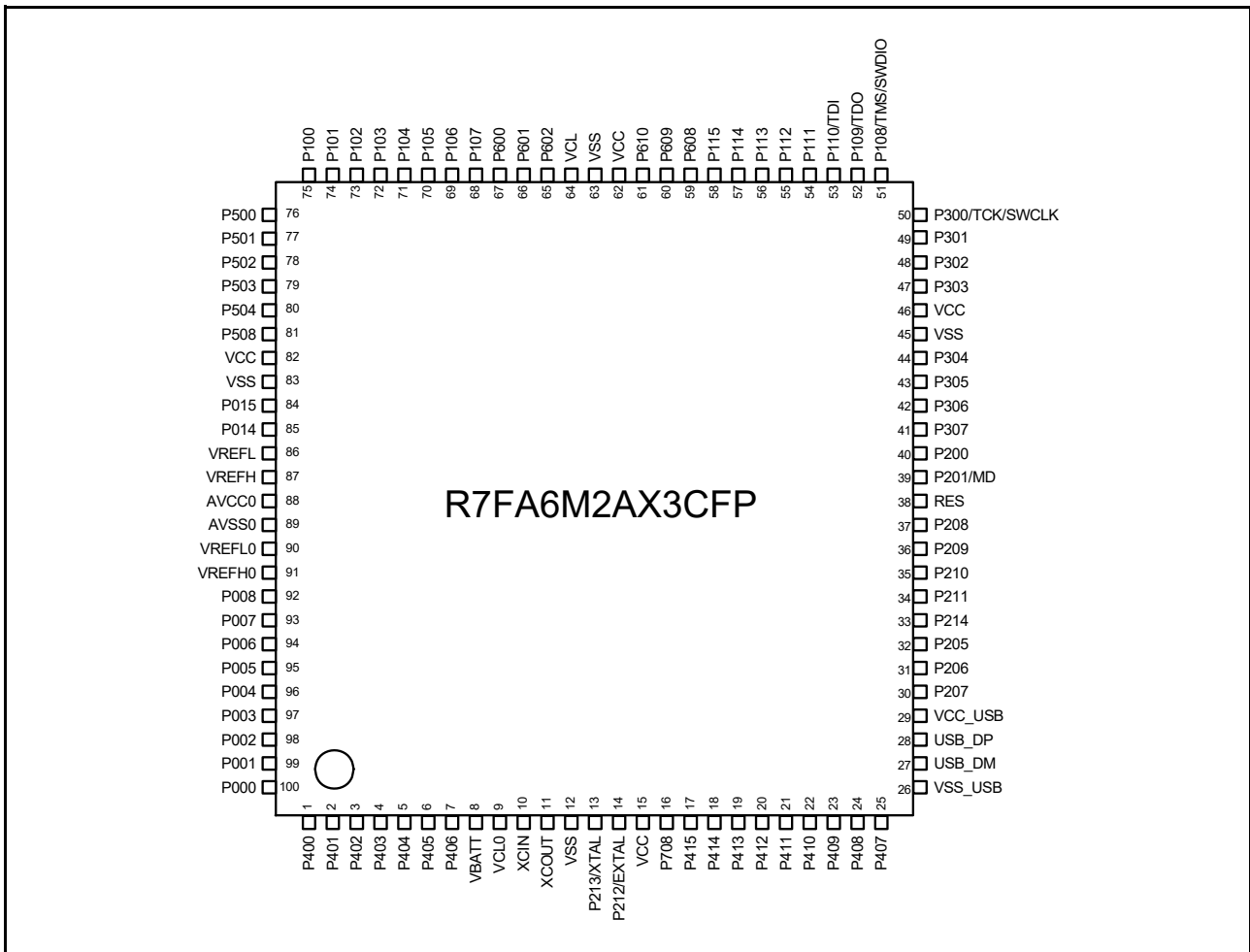


Figure 1.5 Pin assignment for 100-pin LQFP (top view)

1.7 Pin Lists

Pin number	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces								Analog			HMI						
							External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MI) (25 MHz)	ETHERC (RMII) (50 MHz)	SDHI	ADC12	DAC12, ACOMP	CTSU	PDC					
N13	1	1			IRQ0	P400			AGTIO1			GTIOC6A			SCK4	SCK7	SCL0_A		AUDIO_CLK	ET0_WOL	ET0_WOL			ADTRG1						
L11	2	2			IRQ5-DS	P401				GTETRGA		GTIOC6B		CTX0	CTS4_RTS4/SS4	TXD7/MOSI7/SDA7	SDA0_A			ET0_MDC	ET0_MDC									
M13	3	3	CACREF		IRQ4-DS	P402			AGTIO0/AGTIO1					RTIC0	CRX0			AUDIO_CLK	ET0_MDI0	ET0_MDI0									VSYNC	
K11	4	4				P403			AGTIO0/AGTIO1			GTIOC3A		RTIC1		CTS7_RTS7/SS7			SSIBCK0_A	ET0_LINKSTA	ET0_LINKSTA	SD1DA17_B							PIXD7	
L12	5	5				P404						GTIOC3B		RTIC2					SSILRCK0/SIFS0_A	ET0_EXOUT	ET0_EXOUT	SD1DA16_B							PIXD6	
L13	6	6				P405						GTIOC1A							SSITXD0_A	ET0_TXEN	RMII0_TXD_EN_B	SD1DA15_B							PIXD5	
J10	7	7				P406						GTIOC1B						SSLB3_C	SSIRXD0_A	ET0_RXER	RMII0_TXD1_B	SD1DA14_B							PIXD4	
H10	8					P700						GTIOC5A						MISOB_C		ET0_ETXD1	RMII0_TXD0_B	SD1DA13_B							PIXD3	
K12	9					P701						GTIOC5B						MOSIB_C		ET0_ETXD0	REF50CK0_B	SD1DA12_B							PIXD2	
K13	10					P702						GTIOC6A						RSPCKB_C		ET0_ERXD1	RMII0_RXD0_B	SD1DA11_B							PIXD1	
J11	11					P703						GTIOC6B						SSLB0_C		ET0_ERXD0	RMII0_RXD1_B	SD1DA10_B					VCOU		PIXD0	
H11	12					P704			AGT00						CTX0			SSLB1_C		ET0_RXCLK	RMII0_RX_ER_B	SD1CLK_B							HSYNC	
G11	13					P705			AGTIO0						CRX0			SSLB2_C		ET0_CRS	RMII0_CRS_DV_B	SD1CMD_B							PIXCLK	
J12	14	8	VBATT																											
J13	15	9	VCL0																											
H13	16	10	XCIN																											
H12	17	11	XCOU																											
F12	18	12	VSS																											
G12	19	13	XTAL		IRQ2	P213				GTETRGC		GTIOC0A				TXD1/MOSI1/SDA1													ADTRG1	
G13	20	14	EXTAL		IRQ3	P212			AGTEE1	GTETRGD		GTIOC0B				RXD1/MISO1/SC L1														
F13	21	15	VCC																											
G10	22					P713			AGTOA0			GTIOC2A																	TS17	
F11	23					P712			AGTOB0			GTIOC2B																	TS16	
E13	24					P711			AGTEE0							CTS1_RTS1/SS1					ET0_TXCLK								TS15	
E12	25					P710										SCK1					ET0_TXER								TS14	
F10	26					IRQ10	P709									TXD1/MOSI1/SDA1					ET0_ETXD2								TS13	
D13	27	16	CACREF		IRQ11	P708										RXD1/MISO1/SC L1		SSLA3_B	AUDIO_CLK	ET0_ETXD3									TS12	PCKO
E11	28	17			IRQ8	P415						GTIOC0A						SSLA2_B		ET0_TXEN	RMII0_TXD_EN_A	SD0CD						TS11	PIXD5	
D12	29	18			IRQ9	P414						GTIOC0B						SSLA1_B		ET0_RXER	RMII0_TXD1_A	SD0WP						TS10	PIXD4	
E10	30	19				P413				GTOUUP						CTS0_RTS0/SS0		SSLA0_B		ET0_ETXD1	RMII0_TXD0_A	SD0CLK_A						TS09	PIXD3	
C13	31	20				P412			AGTEE1	GTOULO						SCK0		RSPCKA_B		ET0_ETXD0	REF50CK0_A	SD0CMD_A							TS08	PIX02
D11	32	21			IRQ4	P411			AGTOA1	GTOVUP		GTIOC9A				TXD0/MOSI0/SDA0	CTS3_RTS3/SS3	MOSIA_B		ET0_ERXD1	RMII0_RXD0_A	SD0DA10_A						TS07	PIX01	
C12	33	22			IRQ5	P410			AGTOB1	GTOVLO		GTIOC9B				RXD0/MISO0/SC L0	SCK3	MISOA_B		ET0_ERXD0	RMII0_RXD1_A	SD0DA11_A						TS06	PIXD0	
B13	34	23			IRQ6	P409				GTOVUP		GTIOC10A				TXD3/MOSI3/SDA3				ET0_RXCLK	RMII0_RX_ER_A							TS05	HSYNC	
D10	35	24			IRQ7	P408				GTOVLO		GTIOC10B					USB_ID			ET0_CRS	RMII0_CRS_DV_A							TS04	PIXCLK	
A13	36	25				P407			AGTIO0						RTIC0	USB_VBUS	CTS4_RTS4/SS4	SDA0_B	SSLB3_A		ET0_EXOUT	ET0_EXOUT						ADTRG0	TS03	
B11	37	26	VSS_US B																											
A12	38	27																												
B12	39	28																												
A11	40	29	VCC_US B																											





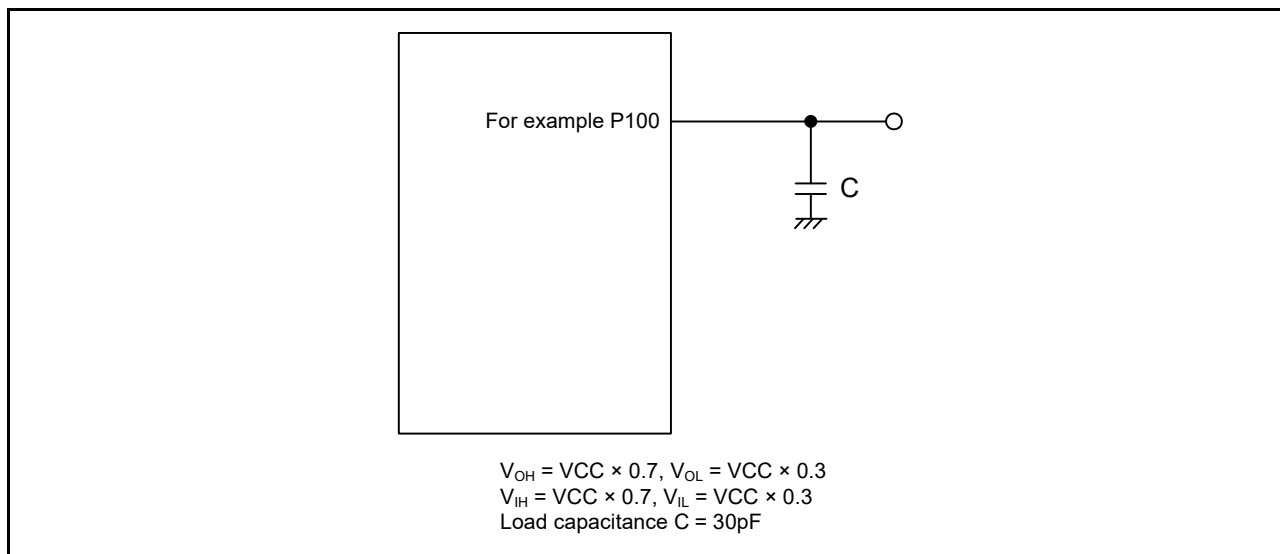


## 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- $VCC = AVCC0 = VCC\_USB = VBATT = 2.7$  to  $3.6$  V
- $2.7 \leq VREFH0/VREFH \leq AVCC0$
- $VSS = AVSS0 = VREFL0/VREFL = VSS\_USB = 0$  V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.



**Figure 2.1** Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

### 2.1 Absolute Maximum Ratings

**Table 2.1** Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	$VCC, VCC\_USB$ *2	-0.3 to +4.0	V
VBATT power supply voltage	VBATT	-0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	$V_{in}$	-0.3 to $VCC + 0.3$	V
Input voltage (5 V-tolerant ports*1)	$V_{in}$	-0.3 to $VCC + 4.0$ (max. 5.8)	V
Reference power supply voltage	$VREFH/VREFH0$	-0.3 to $AVCC0 + 0.3$	V
Analog power supply voltage	$AVCC0$ *2	-0.3 to +4.0	V
Analog input voltage	$V_{AN}$	-0.3 to $AVCC0 + 0.3$	V
Operating temperature*3, *4, *5	$T_{opr}$	-40 to +85 -40 to +105	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

**Caution:** Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, and P708 to P713 are 5 V tolerant.

Note 2. Connect  $AVCC0$  and  $VCC\_USB$  to  $VCC$ .

Note 3. See [section 2.2.1,  \$T\_f/T\_a\$  Definition](#).

Note 4. Contact a Renesas Electronics sales office for information on derating operation when  $T_a = +85^\circ\text{C}$  to  $+105^\circ\text{C}$ . Derating is the systematic reduction of load for improved reliability.

Note 5. The upper limit of operating temperature is  $85^\circ\text{C}$  or  $105^\circ\text{C}$ , depending on the product. For details, see [section 1.3, Part Numbering](#).

**Table 2.2 Recommended operating conditions**

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB		-	VCC	-	V
	VSS_USB		-	0	-	V
VBATT power supply voltage	VBATT		1.65*2	-	3.6	V
Analog power supply voltages	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter, or the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Note 2. Low CL crystal cannot be used below VBATT = 1.8 V.

## 2.2 DC Characteristics

### 2.2.1 $T_j/T_a$ Definition

**Table 2.3 DC characteristics**

Conditions: Products with operating temperature ( $T_a$ ) -40 to +105°C.

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	$T_j$	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that  $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$ ,  
where total power consumption =  $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times VCC$ .

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#). If the part number shows the operation temperature to 85°C, then  $T_j$  max is 105°C, otherwise, it is 125°C.

### 2.2.2 I/O $V_{IH}$ , $V_{IL}$

**Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$  (1 of 2)**

Parameter	Symbol	Min	Typ	Max	Unit	
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI (except RSPCK)	$V_{IH}$	$VCC \times 0.8$	-	V
			$V_{IL}$	-	$VCC \times 0.2$	
	D00 to D15, DQ00 to DQ15	$V_{IH}$	$VCC \times 0.7$	-	-	
		$V_{IL}$	-	-	$VCC \times 0.3$	
	ETHERC	$V_{IH}$	2.3	-	-	
		$V_{IL}$	-	-	$VCC \times 0.2$	
	IIC (SMBus)*1	$V_{IH}$	2.1	-	-	
		$V_{IL}$	-	-	0.8	
IIC (SMBus)*2	$V_{IH}$	2.1	-	$VCC + 3.6$ (max 5.8)		
	$V_{IL}$	-	-	0.8		
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*1	$V_{IH}$	$VCC \times 0.7$	-	V
			$V_{IL}$	-	-	
		$\Delta V_T$	$VCC \times 0.05$	-	-	

Table 2.4 I/O  $V_{IH}$ ,  $V_{IL}$  (2 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	
Schmitt trigger input voltage	Peripheral function pin	IIC (except for SMBus)*2		$V_{IH}$	$VCC \times 0.7$	-	$VCC + 3.6$ (max 5.8)	V	
				$V_{IL}$	-	-	$VCC \times 0.3$		
				$\Delta V_T$	$VCC \times 0.05$	-	-		
		5 V-tolerant ports*3, *7		$V_{IH}$	$VCC \times 0.8$	-	$VCC + 3.6$ (max 5.8)		
				$V_{IL}$	-	-	$VCC \times 0.2$		
				$\Delta V_T$	$VCC \times 0.05$	-	-		
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	$V_{IH}$	$V_{BATT} \times 0.8$	-		$V_{BATT} + 0.3$
					$V_{IL}$	-	-		$V_{BATT} \times 0.2$
					$\Delta V_T$	$V_{BATT} \times 0.05$	-		-
				When VCC power supply is selected	$V_{IH}$	$VCC \times 0.8$	-		Higher voltage either $VCC + 0.3$ V or $V_{BATT} + 0.3$ V
					$V_{IL}$	-	-		$VCC \times 0.2$
					$\Delta V_T$	$VCC \times 0.05$	-		-
	When not using the Battery Backup Function		$V_{IH}$	$VCC \times 0.8$	-	$VCC + 0.3$			
			$V_{IL}$	-	-	$VCC \times 0.2$			
			$\Delta V_T$	$VCC \times 0.05$	-	-			
	Other input pins*4		$V_{IH}$	$VCC \times 0.8$	-	-			
			$V_{IL}$	-	-	$VCC \times 0.2$			
			$\Delta V_T$	$VCC \times 0.05$	-	-			
Ports	5 V-tolerant ports*5, *7		$V_{IH}$	$VCC \times 0.8$	-	$VCC + 3.6$ (max 5.8)	V		
			$V_{IL}$	-	-	$VCC \times 0.2$			
	Other input pins*6		$V_{IH}$	$VCC \times 0.8$	-	-			
			$V_{IL}$	-	-	$VCC \times 0.2$			

Note 1. SCL0\_B (P204), SCL1\_B, SDA1\_B (total 3 pins).

Note 2. SCL0\_A, SDA0\_A, SCL0\_B (P408), SDA0\_B, SCL1\_A, SDA1\_A, SCL2, SDA2 (total 8 pins).

Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 22 pins).

Note 4. All input pins except for the peripheral function pins already described in the table.

Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713 (total 21 pins).

Note 6. All input pins except for the ports already described in the table.

Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O  $I_{OH}$ ,  $I_{OL}$ Table 2.5 I/O  $I_{OH}$ ,  $I_{OL}$ 

Parameter			Symbol	Min	Typ	Max	Unit	
Permissible output current (average value per pin)	Ports P000 to P009, P201	-	$I_{OH}$	-	-	-2.0	mA	
			$I_{OL}$	-	-	2.0	mA	
	Ports P014, P015	-	$I_{OH}$	-	-	-4.0	mA	
			$I_{OL}$	-	-	4.0	mA	
	Ports P205, P206, P407 to P415, P602, P708 to P713 (total 18 pins)	Low drive*1		$I_{OH}$	-	-	-2.0	mA
				$I_{OL}$	-	-	2.0	mA
		Middle drive*2		$I_{OH}$	-	-	-4.0	mA
				$I_{OL}$	-	-	4.0	mA
		High drive*3		$I_{OH}$	-	-	-20	mA
				$I_{OL}$	-	-	20	mA
	Other output pins*4	Low drive*1		$I_{OH}$	-	-	-2.0	mA
				$I_{OL}$	-	-	2.0	mA
		Middle drive*2		$I_{OH}$	-	-	-4.0	mA
				$I_{OL}$	-	-	4.0	mA
		High drive*3		$I_{OH}$	-	-	-16	mA
				$I_{OL}$	-	-	16	mA
Permissible output current (max value per pin)	Ports P000 to P009, P201	-	$I_{OH}$	-	-	-4.0	mA	
			$I_{OL}$	-	-	4.0	mA	
	Ports P014, P015	-	$I_{OH}$	-	-	-8.0	mA	
			$I_{OL}$	-	-	8.0	mA	
	Ports P205, P206, P407 to P415, P602, P708 to P713 (total 18 pins)	Low drive*1		$I_{OH}$	-	-	-4.0	mA
				$I_{OL}$	-	-	4.0	mA
		Middle drive*2		$I_{OH}$	-	-	-8.0	mA
				$I_{OL}$	-	-	8.0	mA
		High drive*3		$I_{OH}$	-	-	-40	mA
				$I_{OL}$	-	-	40	mA
	Other output pins*4	Low drive*1		$I_{OH}$	-	-	-4.0	mA
				$I_{OL}$	-	-	4.0	mA
		Middle drive*2		$I_{OH}$	-	-	-8.0	mA
				$I_{OL}$	-	-	8.0	mA
		High drive*3		$I_{OH}$	-	-	-32	mA
				$I_{OL}$	-	-	32	mA
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins		$\Sigma I_{OH}(\max)$	-	-	-80	mA	
			$\Sigma I_{OL}(\max)$	-	-	80	mA	

**Caution:** To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100  $\mu$ s.

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. Except for P200, which is an input port.

2.2.4 I/O  $V_{OH}$ ,  $V_{OL}$ , and Other CharacteristicsTable 2.6 I/O  $V_{OH}$ ,  $V_{OL}$ , and other characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC	$V_{OL}$	-	-	0.4	V	$I_{OL} = 3.0 \text{ mA}$
		$V_{OL}$	-	-	0.6		$I_{OL} = 6.0 \text{ mA}$
	IIC*1	$V_{OL}$	-	-	0.4		$I_{OL} = 15.0 \text{ mA}$ (ICFER.FMPE = 1)
		$V_{OL}$	-	0.4	-		$I_{OL} = 20.0 \text{ mA}$ (ICFER.FMPE = 1)
	ETHERC	$V_{OH}$	VCC - 0.5	-	-		$I_{OH} = -1.0 \text{ mA}$
		$V_{OL}$	-	-	0.4		$I_{OL} = 1.0 \text{ mA}$
	Ports P205, P206, P407 to P415, P602, P708 to P713 (total of 18 pins)*2	$V_{OH}$	VCC - 1.0	-	-		$I_{OH} = -20 \text{ mA}$ VCC = 3.3 V
		$V_{OL}$	-	-	1.0		$I_{OL} = 20 \text{ mA}$ VCC = 3.3 V
	Other output pins	$V_{OH}$	VCC - 0.5	-	-		$I_{OH} = -1.0 \text{ mA}$
		$V_{OL}$	-	-	0.5		$I_{OL} = 1.0 \text{ mA}$
Input leakage current	RES	$ I_{in} $	-	-	5.0	$\mu\text{A}$	$V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$
	Port P200		-	-	1.0		$V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$
Three-state leakage current (off state)	5 V-tolerant ports	$ I_{TS} $	-	-	5.0	$\mu\text{A}$	$V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$
	Other ports (except for port P200)		-	-	1.0		$V_{in} = 0 \text{ V}$ $V_{in} = \text{VCC}$
Input pull-up MOS current	Ports P0 to PB	$I_p$	-300	-	-10	$\mu\text{A}$	VCC = 2.7 to 3.6 V $V_{in} = 0 \text{ V}$
Input capacitance	USB_DP, USB_DM, and ports P014, P015, P400, P401, P511, P512	$C_{in}$	-	-	16	pF	$V_{bias} = 0 \text{ V}$ $V_{amp} = 20 \text{ mV}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$
	Other input pins		-	-	8		

Note 1. SCL0\_A, SDA0\_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

2.2.5 Operating and Standby Current

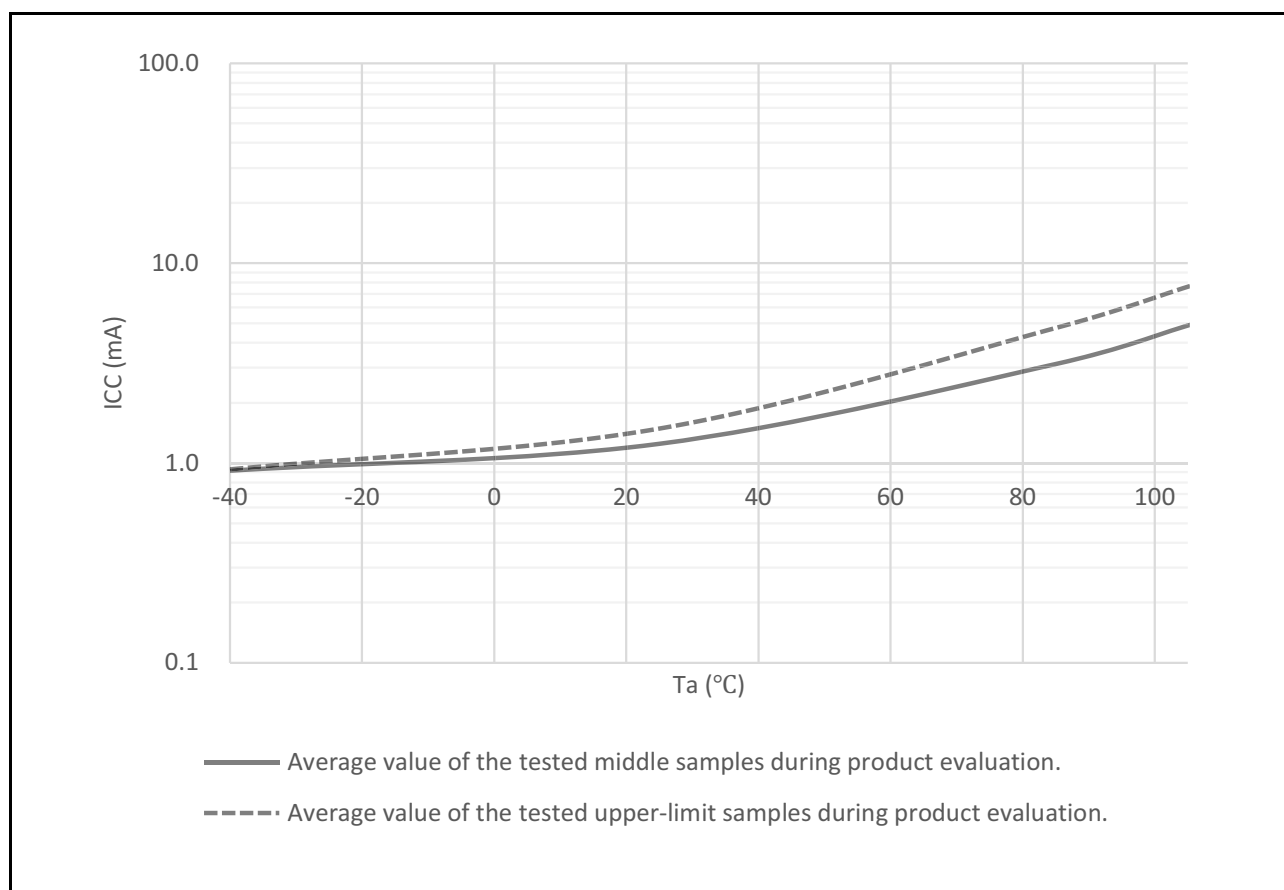
Table 2.7 Operating and standby current (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions			
Supply current*1	I <sub>CC</sub> *3	Maximum*2		-	-	102*2	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz		
		CoreMark®*5		-	19	-			
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	26		-	
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	12		-	
		Sleep mode*5, *6		-	10	40			
		Increase during BGO operation	Data flash P/E		-	6		-	
			Code flash P/E		-	8		-	
		Low-speed mode*5		-	1.3	-		ICLK = 1 MHz	
		Subosc-speed mode*5		-	1.2	-		ICLK = 32.768 kHz	
		Software Standby mode		-	1.3	15		Ta ≤ 85°C	
	-			1.3	24	Ta ≤ 105°C			
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit	-	29	67	μA	Ta ≤ 85°C		
			-	29	96	μA	Ta ≤ 105°C		
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low power function disabled		-	11.6	32.4	Ta ≤ 85°C	
			Power-on reset circuit low power function enabled		-	11.6	40	Ta ≤ 105°C	
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	4.9	23.5	Ta ≤ 85°C	
			When a crystal oscillator for low clock loads is in use		-	4.9	31	Ta ≤ 105°C	
			When a crystal oscillator for standard clock loads is in use		-	4.4	-	-	
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		-	1.0	-	-	
			When a crystal oscillator for standard clock loads is in use		-	1.4	-	-	
When a crystal oscillator for low clock loads is in use			-	0.9	-	V <sub>BATT</sub> = 1.8 V, VCC = 0 V			
		-	1.1	-	V <sub>BATT</sub> = 3.3 V, VCC = 0 V				
		-	1.0	-	V <sub>BATT</sub> = 1.8 V, VCC = 0 V				
		-	1.6	-	V <sub>BATT</sub> = 3.3 V, VCC = 0 V				
Analog power supply current	A <sub>I<sub>CC</sub></sub>	During 12-bit A/D conversion		-	0.8	1.1	mA	-	
		During 12-bit A/D conversion with S/H amp		-	2.3	3.3	mA	-	
		ACMPHS (1 unit)		-	100	150	μA	-	
		Temperature sensor		-	0.1	0.2	mA	-	
		During D/A conversion (per unit)	Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
		Waiting for A/D, D/A conversion (all units)		-	0.9	1.6	mA	-	
		ADC12, DAC12 in standby modes (all units)*8		-	2	8	μA	-	
Reference power supply current (VREFH0)	A <sub>I<sub>REFH0</sub></sub>	During 12-bit A/D conversion (unit 0)		-	70	120	μA	-	
		Waiting for 12-bit A/D conversion (unit 0)		-	0.07	0.5	μA	-	
		ADC12 in standby modes (unit 0)		-	0.07	0.5	μA	-	
Reference power supply current (VREFH)	A <sub>I<sub>REFH</sub></sub>	During 12-bit A/D conversion (unit 1)		-	70	120	μA	-	
		During D/A conversion (per unit)	Without AMP output		-	0.1	0.4	mA	-
			With AMP output		-	0.1	0.4	mA	-
		Waiting for 12-bit A/D (unit 1), D/A (all units) conversion		-	0.07	0.8	μA	-	
		ADC12 unit 1 in standby modes		-	0.07	0.8	μA	-	

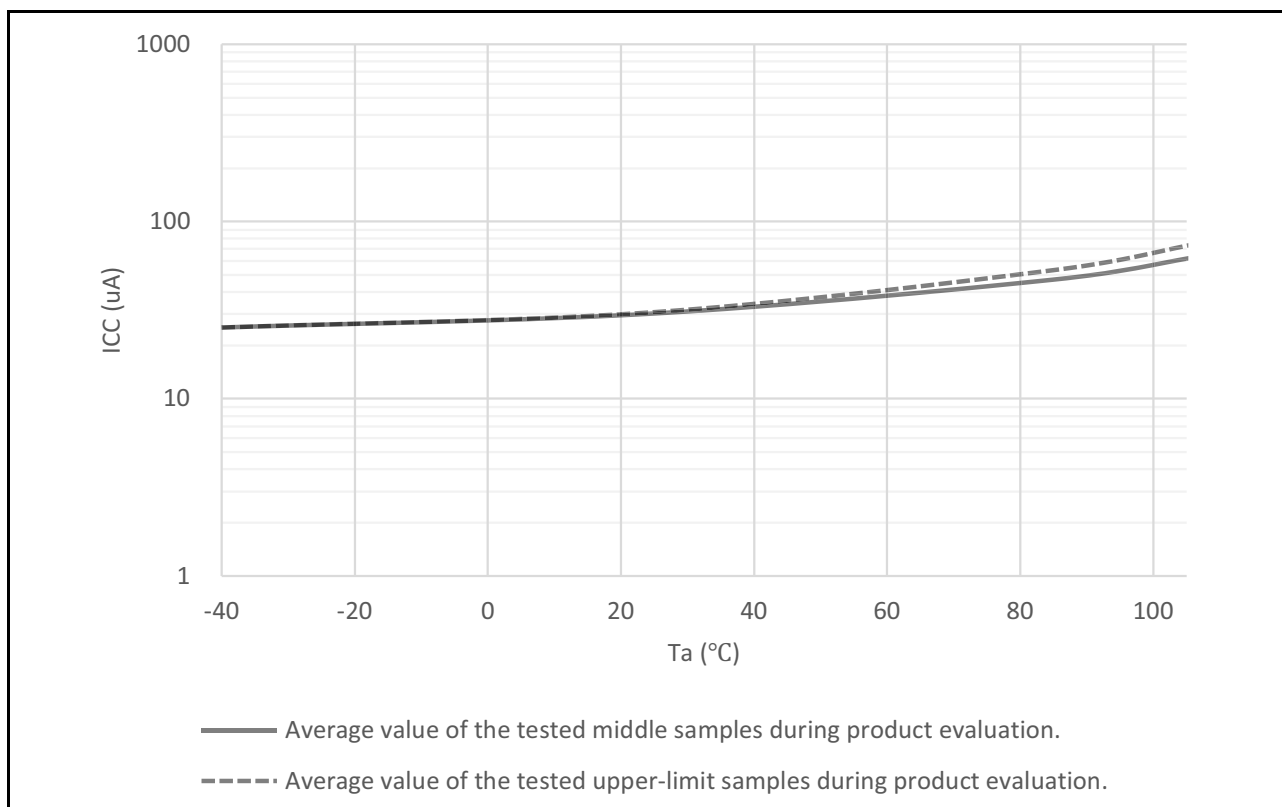
**Table 2.7 Operating and standby current (2 of 2)**

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
USB operating current	Low speed	USB	I <sub>CCUSBLS</sub>	-	3.5	6.5	mA	VCC_USB
	Full speed	USB	I <sub>CCUSBFS</sub>	-	4.0	10.0	mA	VCC_USB

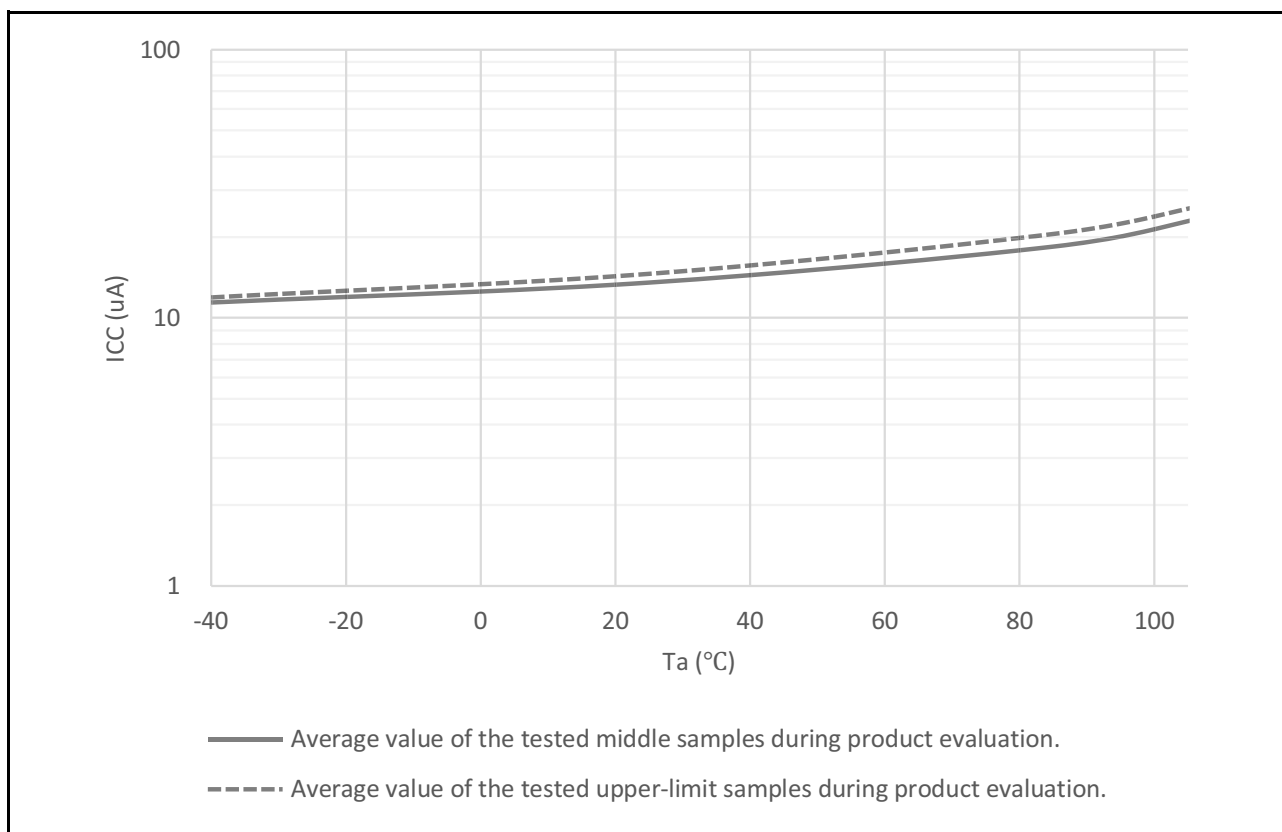
- Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
- Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
- Note 3. I<sub>CC</sub> depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)  
 I<sub>CC</sub> Max. = 0.61 × f + 29 (maximum operation in High-speed mode)  
 I<sub>CC</sub> Typ. = 0.08 × f + 2.6 (normal operation in High-speed mode)  
 I<sub>CC</sub> Typ. = 0.1 × f + 1.2 (Low-speed mode)  
 I<sub>CC</sub> Max. = 0.09 × f + 29 (Sleep mode).
- Note 4. This does not include the BGO operation.
- Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
- Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
- Note 7. When using ETHERC, PCLKA frequency is such that PCLKA = ICLK.
- Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D Converter 1 Module Stop bit) are in the module-stop state.



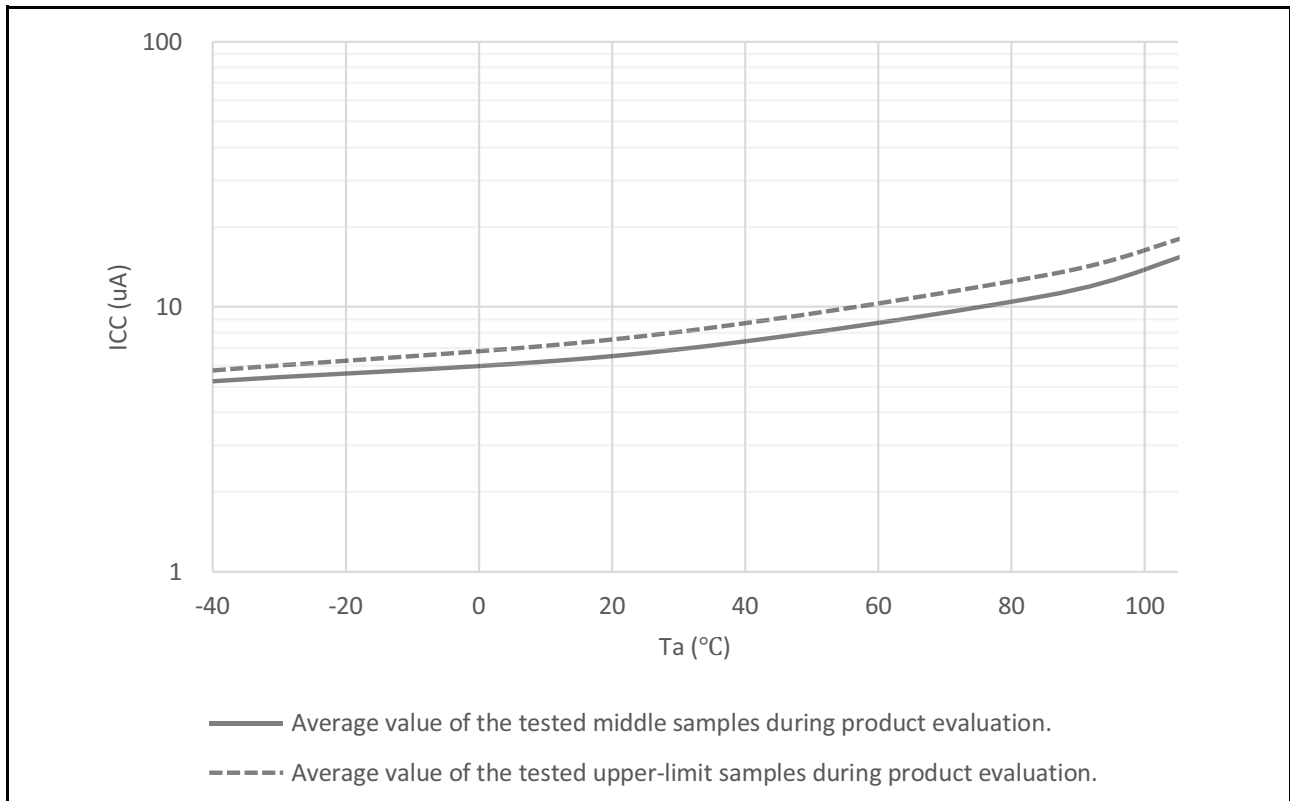
**Figure 2.2 Temperature dependency in Software Standby mode (reference data)**



**Figure 2.3** Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)



**Figure 2.4** Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)



**Figure 2.5** Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)

### 2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.8** Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V	-
	Voltage monitor 0 reset enabled at startup		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Note 2. This applies when VBATT is used.

**Table 2.9** Rise and fall gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency  $f_{r(VCC)}$  within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds  $VCC \pm 10\%$ , the allowable voltage change rising and falling gradient  $dt/dVCC$  must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.6 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	$dt/dVCC$	1.0	-	-	ms/V	When VCC change exceeds $VCC \pm 10\%$

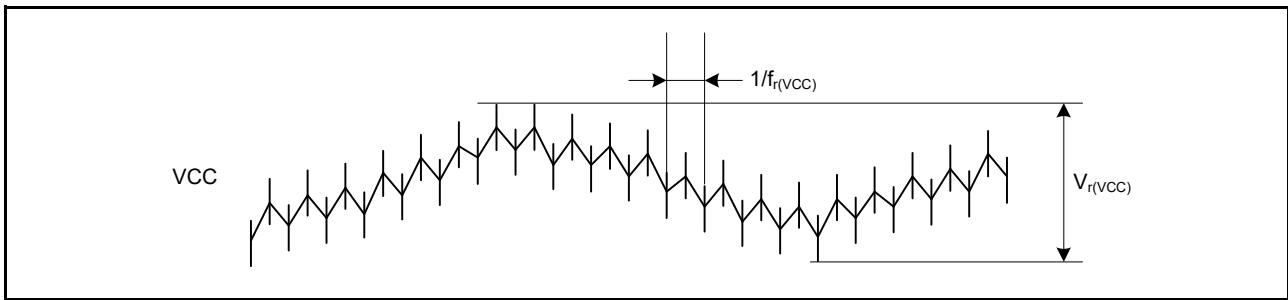


Figure 2.6 Ripple waveform

## 2.3 AC Characteristics

### 2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2		-	-	120	
	Peripheral module clock (PCLKB)*2		-	-	60	
	Peripheral module clock (PCLKC)*2		_*3	-	60	
	Peripheral module clock (PCLKD)*2		-	-	120	
	Flash interface clock (FCLK)*2		_*1	-	60	
	External bus clock (BCLK)*2		-	-	120	
	EBCLK pin output		-	-	60	
SDCLK pin output	VCC ≥ 3.0 V		-	-	120	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2, *3		_*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	
	External bus clock (BCLK)		-	-	1	
EBCLK pin output		-	-	1		

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

**Table 2.12 Operation frequency value in Subosc-speed mode**

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	29.4	-	36.1	kHz
	Peripheral module clock (PCLKA)*2		-	-	36.1	
	Peripheral module clock (PCLKB)*2		-	-	36.1	
	Peripheral module clock (PCLKC)*2, *3		-	-	36.1	
	Peripheral module clock (PCLKD)*2		-	-	36.1	
	Flash interface clock (FCLK)*1, *2		29.4	-	36.1	
	External bus clock (BCLK)*2		-	-	36.1	
	EBCLK pin output		-	-	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.

Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.

Note 3. The ADC12 cannot be used.

### 2.3.2 Clock Timing

**Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	$t_{Bcyc}$	16.6	-	-	ns	Figure 2.7
EBCLK pin output high pulse width	$t_{CH}$	3.3	-	-	ns	
EBCLK pin output low pulse width	$t_{CL}$	3.3	-	-	ns	
EBCLK pin output rise time	$t_{Cr}$	-	-	5.0	ns	
EBCLK pin output fall time	$t_{Cf}$	-	-	5.0	ns	
SDCLK pin output cycle time	$t_{SDcyc}$	8.33	-	-	ns	
SDCLK pin output high pulse width	$t_{CH}$	1.0	-	-	ns	
SDCLK pin output low pulse width	$t_{CL}$	1.0	-	-	ns	
SDCLK pin output rise time	$t_{Cr}$	-	-	3.0	ns	
SDCLK pin output fall time	$t_{Cf}$	-	-	3.0	ns	
EXTAL external clock input cycle time	$t_{EXcyc}$	41.66	-	-	ns	Figure 2.8
EXTAL external clock input high pulse width	$t_{EXH}$	15.83	-	-	ns	
EXTAL external clock input low pulse width	$t_{EXL}$	15.83	-	-	ns	
EXTAL external clock rise time	$t_{EXr}$	-	-	5.0	ns	
EXTAL external clock fall time	$t_{EXf}$	-	-	5.0	ns	
Main clock oscillator frequency	$f_{MAIN}$	8	-	24	MHz	-
Main clock oscillation stabilization wait time (crystal) *1	$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.9
LOCO clock oscillation frequency	$f_{LOCO}$	29.4912	32.768	36.0448	kHz	-
LOCO clock oscillation stabilization wait time	$t_{LOCOWT}$	-	-	60.4	$\mu$ s	Figure 2.10
ILOCO clock oscillation frequency	$f_{ILOCO}$	13.5	15	16.5	kHz	-
MOCO clock oscillation frequency	$F_{MOCO}$	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization wait time	$t_{MOCOWT}$	-	-	15.0	$\mu$ s	-

**Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)**

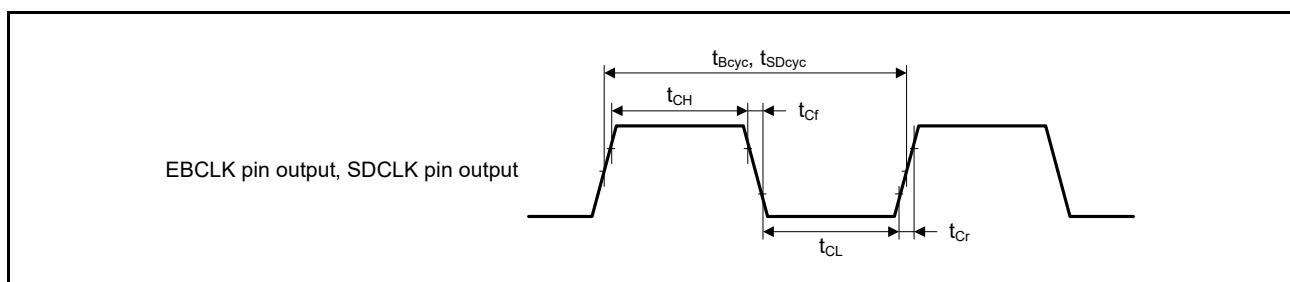
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL	$f_{\text{HOCO16}}$	15.78	16	16.22	MHz	$-20 \leq T_a \leq 105^\circ\text{C}$
		$f_{\text{HOCO18}}$	17.75	18	18.25		
		$f_{\text{HOCO20}}$	19.72	20	20.28		
	With FLL	$f_{\text{HOCO16}}$	15.71	16	16.29		$-40 \leq T_a \leq -20^\circ\text{C}$
		$f_{\text{HOCO18}}$	17.68	18	18.32		
		$f_{\text{HOCO20}}$	19.64	20	20.36		
		$f_{\text{HOCO16}}$	15.960	16	16.040	-40 $\leq T_a \leq 105^\circ\text{C}$ Sub-clock frequency accuracy is $\pm 50$ ppm.	
		$f_{\text{HOCO18}}$	17.955	18	18.045		
		$f_{\text{HOCO20}}$	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		$t_{\text{HOCOWT}}$	-	-	64.7	$\mu\text{s}$	-
FLL stabilization wait time		$t_{\text{FLLWT}}$	-	-	1.8	ms	-
PLL clock frequency		$f_{\text{PLL}}$	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		$t_{\text{PLLWT}}$	-	-	174.9	$\mu\text{s}$	Figure 2.11

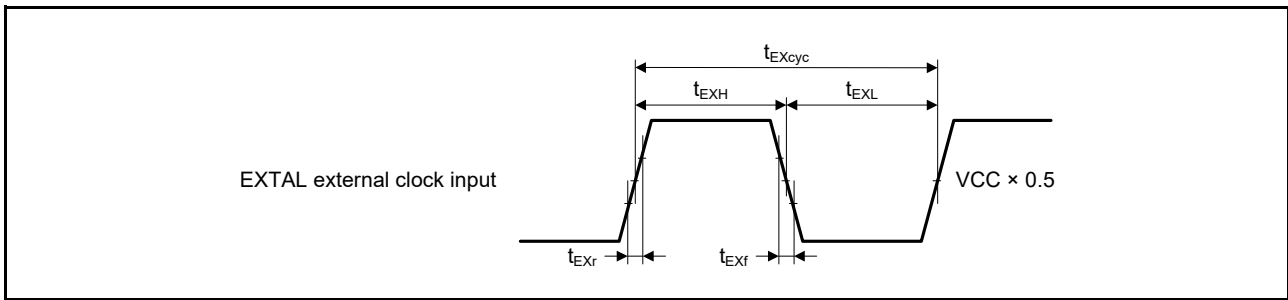
- Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.  
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.
- Note 2. This is the time from release from reset state until the HOCO oscillation frequency ( $f_{\text{HOCO}}$ ) reaches the range for guaranteed operation.

**Table 2.14 Clock timing for the sub-clock oscillator**

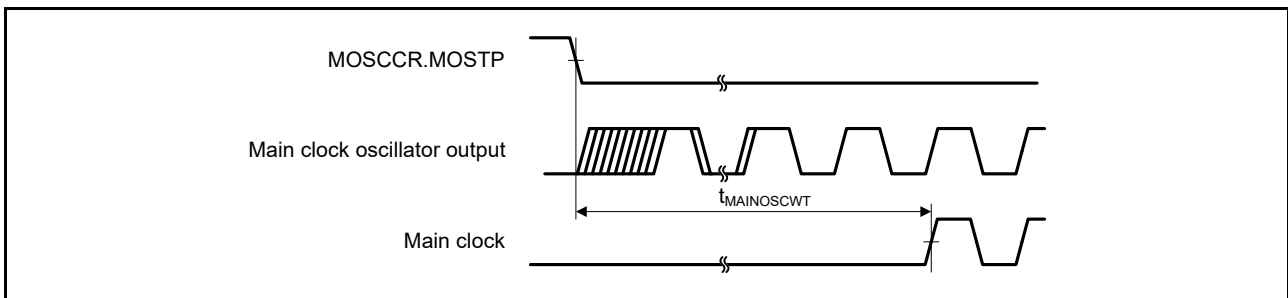
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	$f_{\text{SUB}}$	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{\text{SUBOSCWT}}$	-	-	-*1	s	Figure 2.12

- Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.  
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

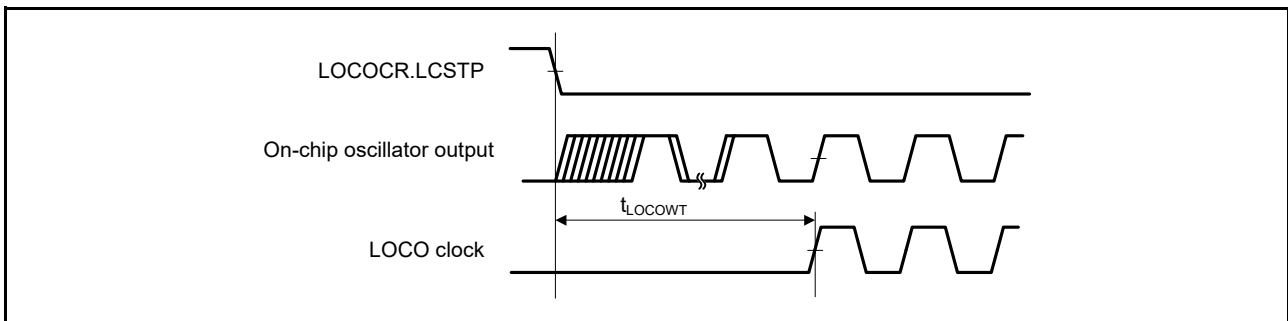
**Figure 2.7 EBCLK and SDCLK output timing**



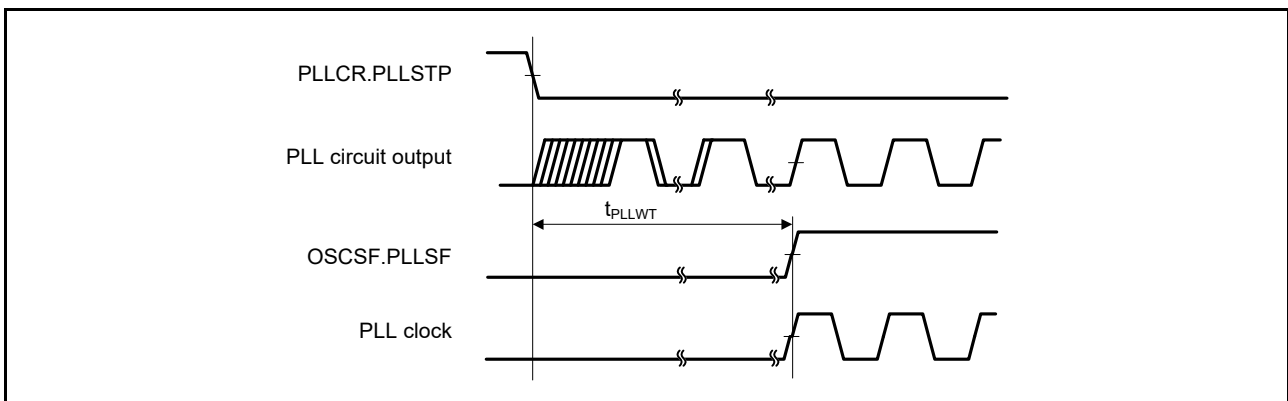
**Figure 2.8** EXTAL external clock input timing



**Figure 2.9** Main clock oscillation start timing



**Figure 2.10** LOCO clock oscillation start timing



**Figure 2.11** PLL clock oscillation start timing

Note: Only operate the PLL after the main clock oscillation has stabilized.

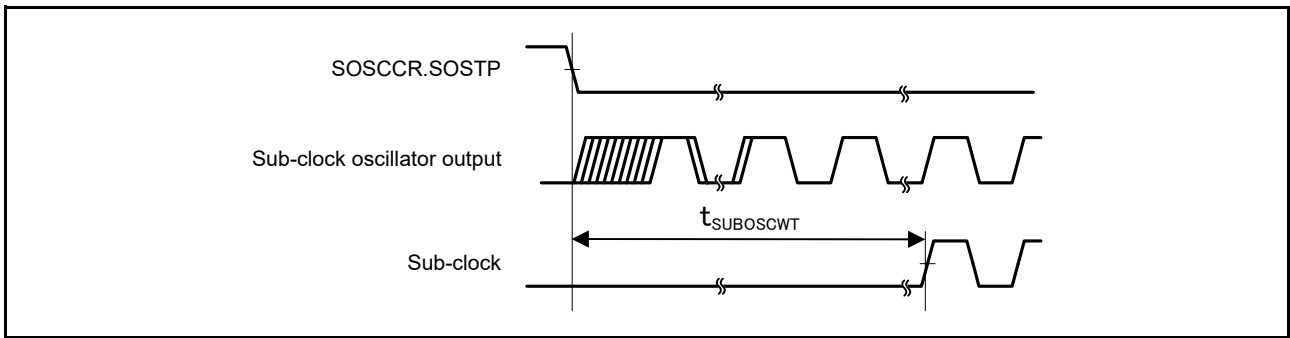


Figure 2.12 Sub-clock oscillation start timing

### 2.3.3 Reset Timing

Table 2.15 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	$t_{RESWP}$	1	-	-	ms	Figure 2.13
	Deep Software Standby mode	$t_{RESWD}$	0.6	-	-	ms	Figure 2.14
	Software Standby mode, Subosc-speed mode	$t_{RESWS}$	0.3	-	-	ms	
	All other	$t_{RESW}$	200	-	-	$\mu$ s	
Wait time after RES cancellation		$t_{RESWT}$	-	29	32	$\mu$ s	Figure 2.13
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		$t_{RESW2}$	-	320	390	$\mu$ s	-

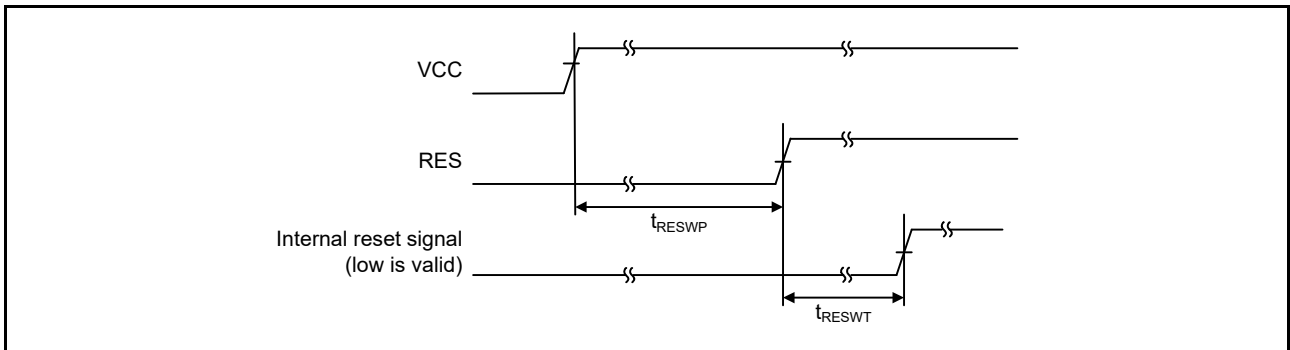


Figure 2.13 Power-on reset timing

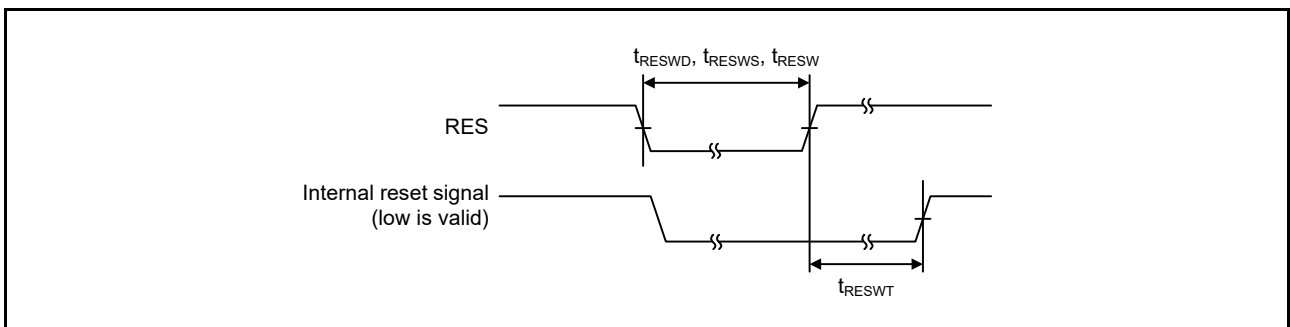


Figure 2.14 Reset input timing

## 2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	$t_{SBYMC}$	-	2.4*9	2.8*9	ms	Figure 2.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	$t_{SBYPC}$	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	$t_{SBYEX}$	-	230*9	280*9	$\mu$ s	
		System clock source is PLL with main clock oscillator*5	$t_{SBYPE}$	-	570*9	700*9	$\mu$ s	
	System clock source is sub-clock oscillator*8		$t_{SBYSC}$	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		$t_{SBYLO}$	-	1.2*9	1.4*9	ms	
	System clock source is HOCO clock oscillator*6		$t_{SBYHO}$	-	240*9, *10	300*9, *10	$\mu$ s	
	System clock source is MOCO clock oscillator*7		$t_{SBYMO}$	-	220*9	300*9	$\mu$ s	
Recovery time from Deep Software Standby mode			$t_{DSBY}$	-	0.65	1.0	ms	Figure 2.16
Wait time after cancellation of Deep Software Standby mode			$t_{DSBYWT}$	34	-	35	$t_{cyc}$	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		$t_{SNZ}$	-	35*9, *10	70*9, *10	$\mu$ s	Figure 2.17
	High-speed mode when system clock source is MOCO (8 MHz)		$t_{SNZ}$	-	11*9	14*9	$\mu$ s	

- Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:  
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).
- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC} (\text{MOSCWTCR} = Xh) = t_{SBYMC} (\text{MOSCWTCR} = 05h) + (t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = 05h))$
- Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC} (\text{MOSCWTCR} = Xh) = t_{SBYMC} (\text{MOSCWTCR} = 05h) + (t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = 05h))$
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC} (\text{MOSCWTCR} = Xh) = t_{SBYMC} (\text{MOSCWTCR} = 01h) + (t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = 01h))$
- Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:  
 $t_{SBYMC} (\text{MOSCWTCR} = Xh) = t_{SBYMC} (\text{MOSCWTCR} = 01h) + (t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = Xh) - t_{\text{MAINOSCWT}} (\text{MOSCWTCR} = 01h))$
- Note 6. The HOCO frequency is 20 MHz.
- Note 7. The MOCO frequency is 8 MHz.
- Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
- Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:  
STCONR.STCON[1:0] = 00b:16  $\mu$ s (typical), 34  $\mu$ s (maximum)  
STCONR.STCON[1:0] = 11b:16  $\mu$ s (typical), 104  $\mu$ s (maximum).
- Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16  $\mu$ s (typical) or 18  $\mu$ s (maximum) is added as the HOCO wait time.

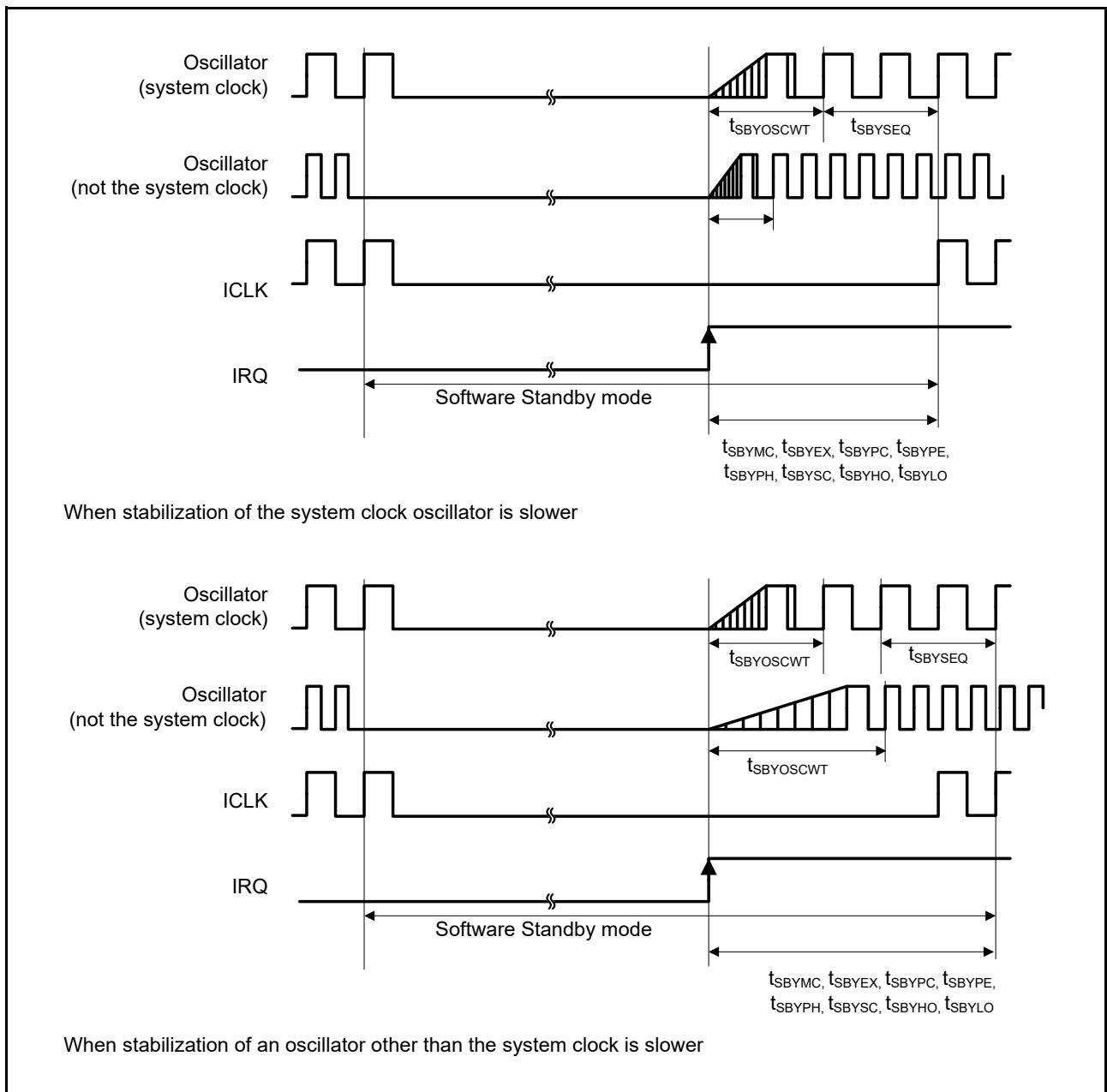


Figure 2.15 Software Standby mode cancellation timing

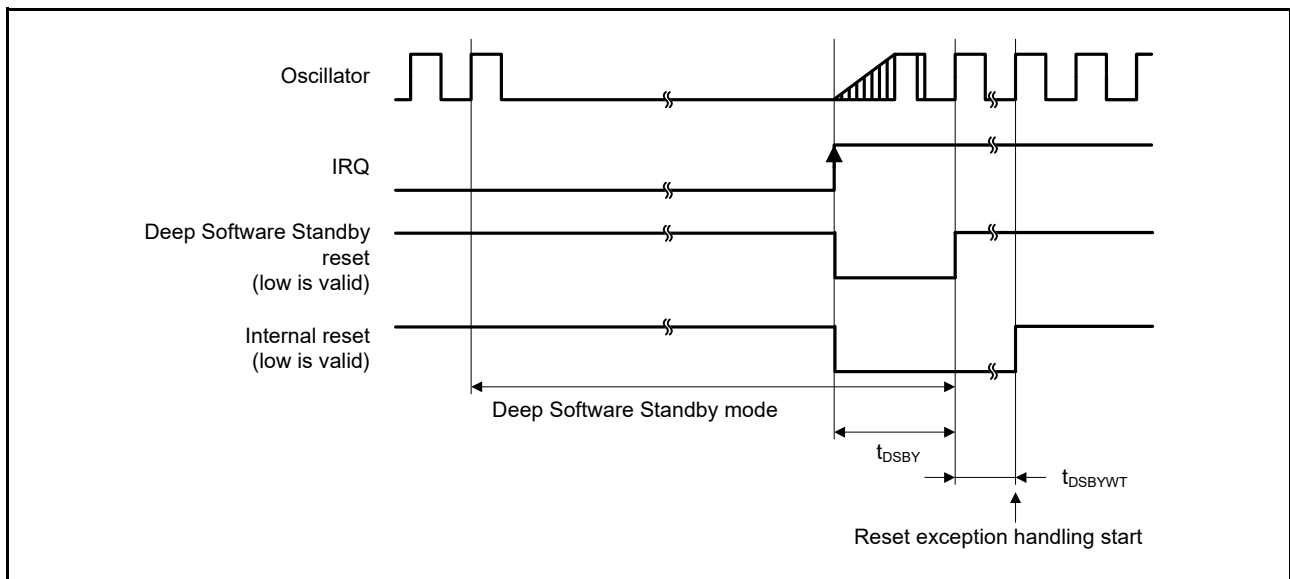


Figure 2.16 Deep Software Standby mode cancellation timing

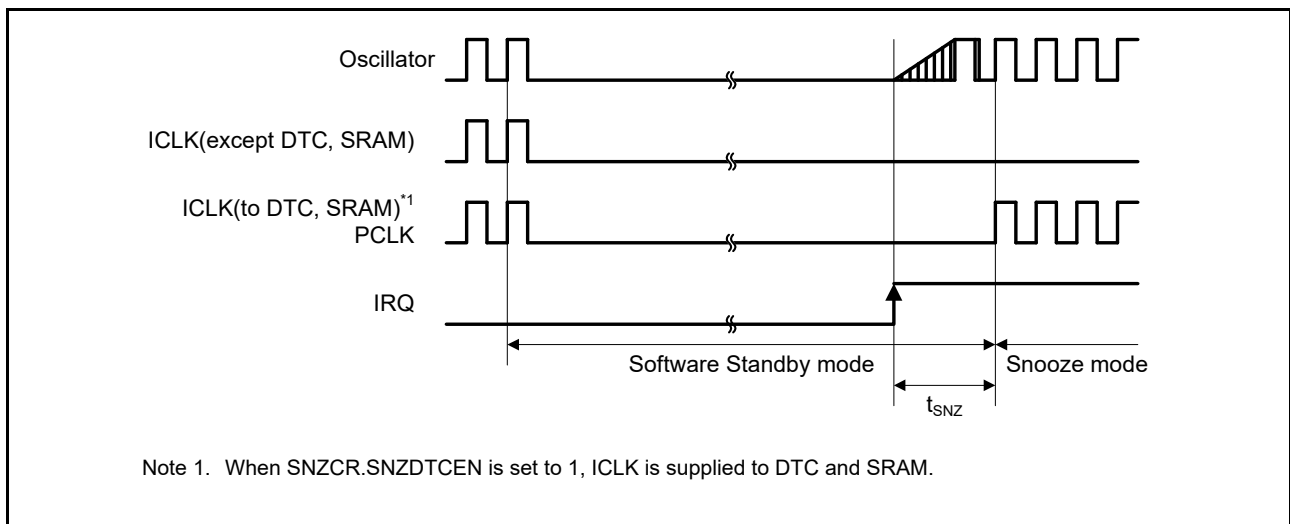


Figure 2.17 Recovery timing from Software Standby mode to Snooze mode

### 2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	$t_{NMIW}$	200	-	-	ns	NMI digital filter disabled	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	$t_{IRQW}$	200	-	-	ns	IRQ digital filter disabled	
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.

Note: If the clock source is switched, add 4 clock cycles of the switched source.

- Note 1.  $t_{Pcyc}$  indicates the PCLKB cycle.
- Note 2.  $t_{NMICK}$  indicates the cycle of the NMI digital filter sampling clock.
- Note 3.  $t_{IRQCK}$  indicates the cycle of the IRQi digital filter sampling clock.

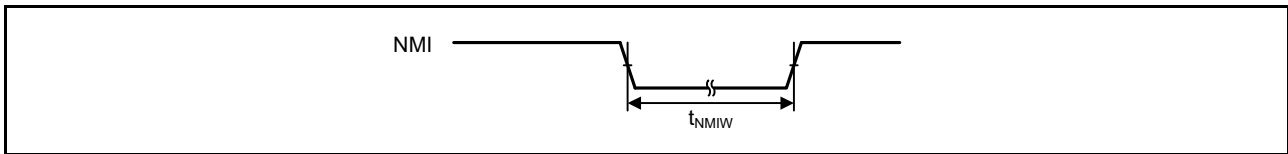


Figure 2.18 NMI interrupt input timing

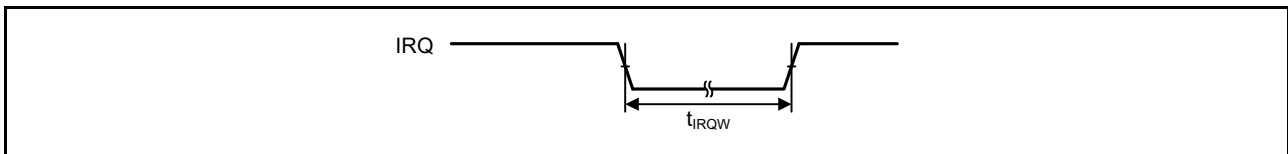


Figure 2.19 IRQ interrupt input timing

### 2.3.6 Bus Timing

**Table 2.18 Bus timing (1 of 2)**

Condition 1: When using the CS area controller (CSC).  
 BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz.  
 VCC = AVCC0 = VCC\_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0.  
 Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.  
 EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.  
 Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).  
 BCLK = SDCLK = 8 to 120 MHz.  
 VCC = AVCC0 = VCC\_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0.  
 Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF.  
 High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.  
 BCLK = SDCLK = 8 to 60 MHz.  
 VCC = AVCC0 = VCC\_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0.  
 Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF.  
 High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	$t_{AD}$	-	12.5	ns	Figure 2.20 to Figure 2.25
Byte control delay	$t_{BCD}$	-	12.5	ns	
CS delay	$t_{CSD}$	-	12.5	ns	
ALE delay time	$t_{ALEd}$	-	12.5	ns	
RD delay	$t_{RSD}$	-	12.5	ns	
Read data setup time	$t_{RDS}$	12.5	-	ns	
Read data hold time	$t_{RDH}$	0	-	ns	
WR/WRn delay	$t_{WRD}$	-	12.5	ns	
Write data delay	$t_{WDD}$	-	12.5	ns	
Write data hold time	$t_{WDH}$	0	-	ns	
WAIT setup time	$t_{WTS}$	12.5	-	ns	Figure 2.26
WAIT hold time	$t_{WTH}$	0	-	ns	

**Table 2.18 Bus timing (2 of 2)**

Condition 1: When using the CS area controller (CSC).

BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz.

VCC = AVCC0 = VCC\_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0.

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.

EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).

BCLK = SDCLK = 8 to 120 MHz.

VCC = AVCC0 = VCC\_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0.

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF.

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.

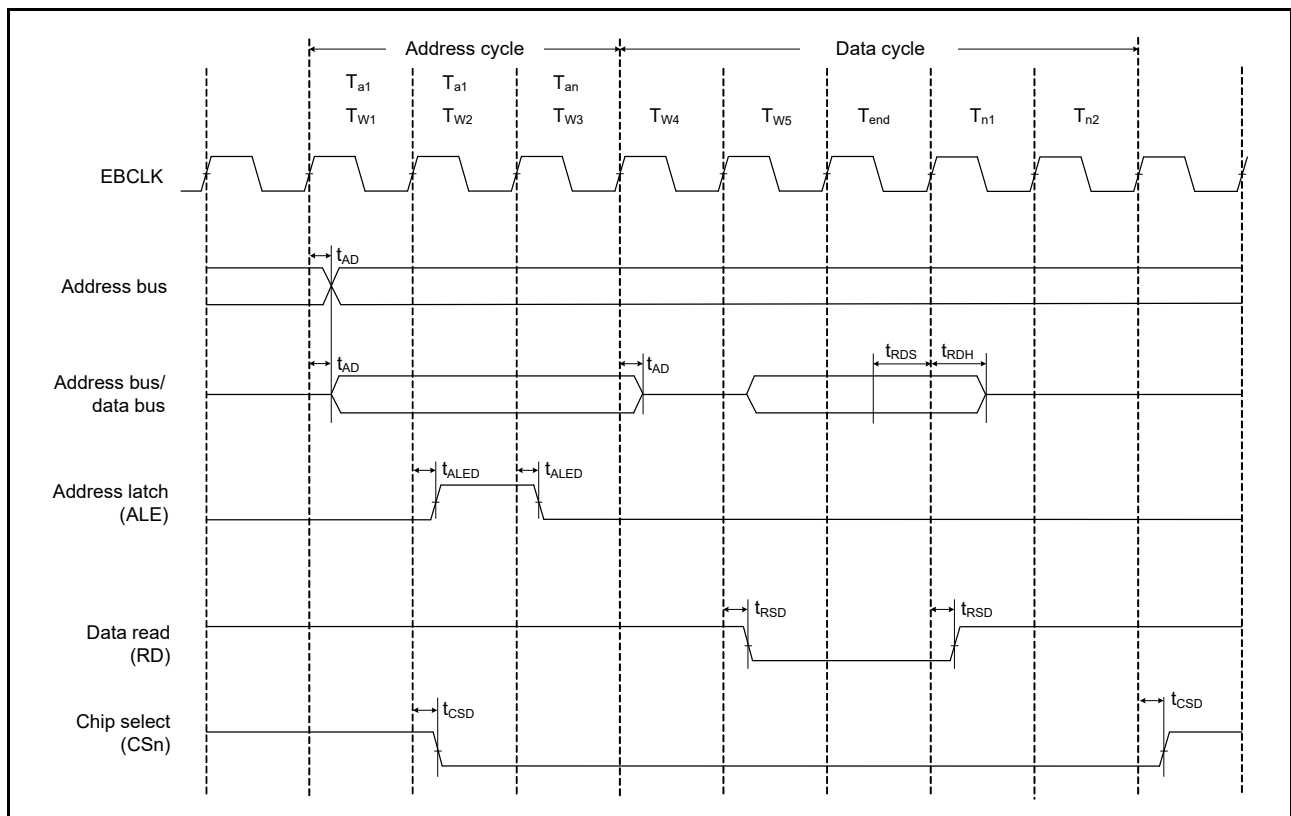
BCLK = SDCLK = 8 to 60 MHz.

VCC = AVCC0 = VCC\_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0.

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF.

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	$t_{AD2}$	0.8	6.8	ns	Figure 2.27 to Figure 2.30
CS delay 2 (SDRAM)	$t_{CSD2}$	0.8	6.8	ns	
DQM delay (SDRAM)	$t_{DQMD}$	0.8	6.8	ns	
CKE delay (SDRAM)	$t_{CKED}$	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	$t_{RDS2}$	2.9	-	ns	
Read data hold time 2 (SDRAM)	$t_{RDH2}$	1.5	-	ns	
Write data delay 2 (SDRAM)	$t_{WDD2}$	-	6.8	ns	
Write data hold time 2 (SDRAM)	$t_{WDH2}$	0.8	-	ns	
WE delay (SDRAM)	$t_{WED}$	0.8	6.8	ns	
RAS delay (SDRAM)	$t_{RASD}$	0.8	6.8	ns	
CAS delay (SDRAM)	$t_{CASD}$	0.8	6.8	ns	



**Figure 2.20 Address/data multiplexed bus read access timing**

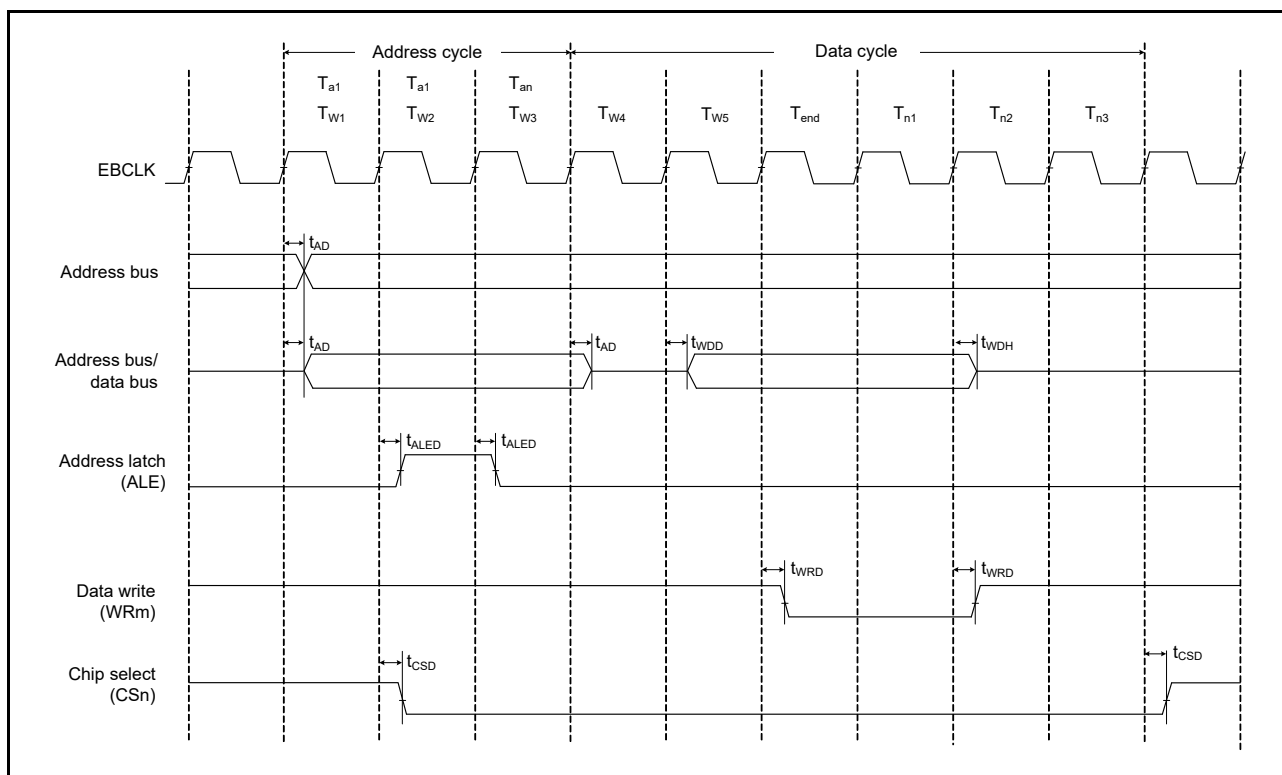


Figure 2.21 Address/data multiplexed bus write access timing

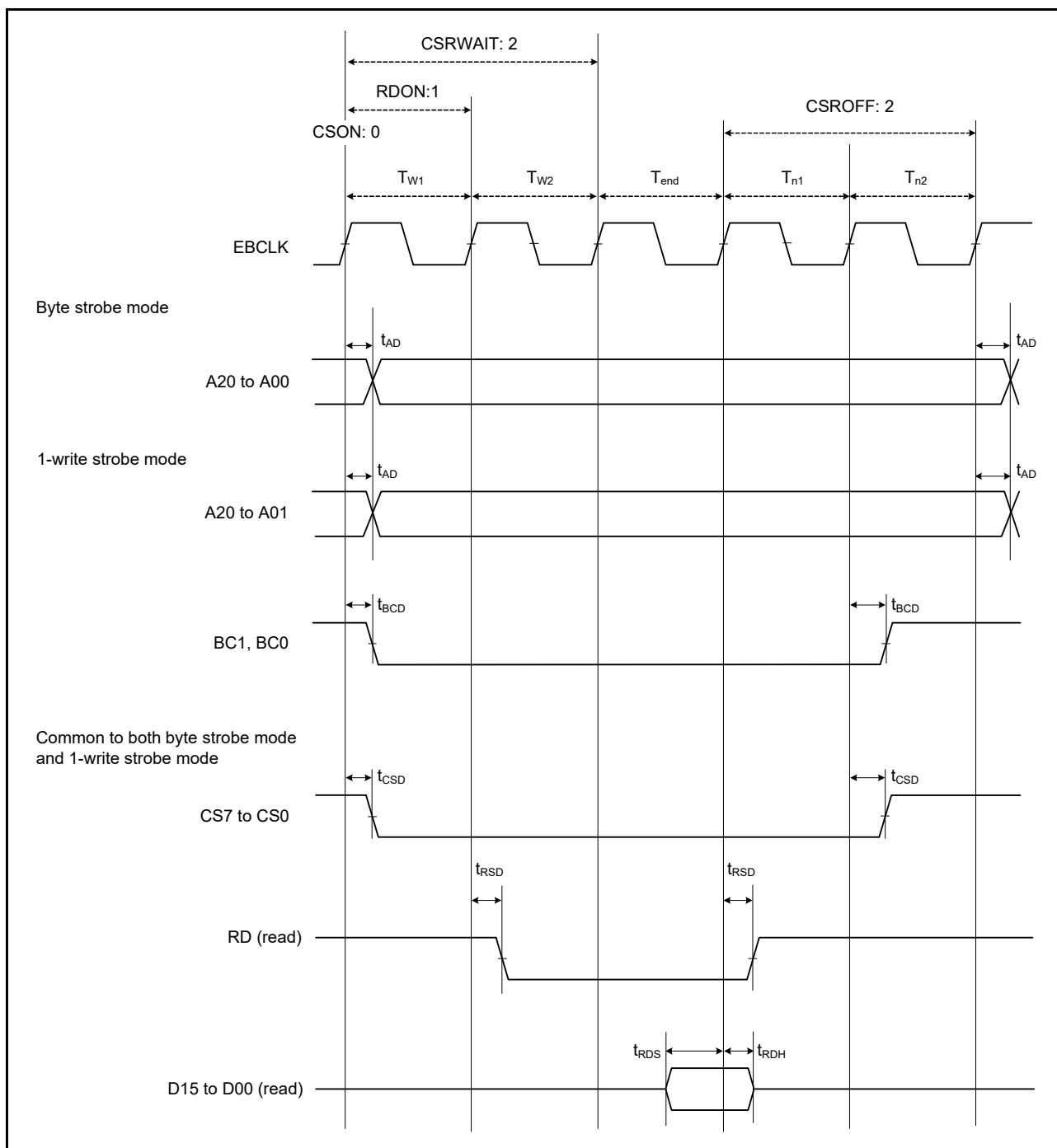


Figure 2.22 External bus timing for normal read cycle with bus clock synchronized

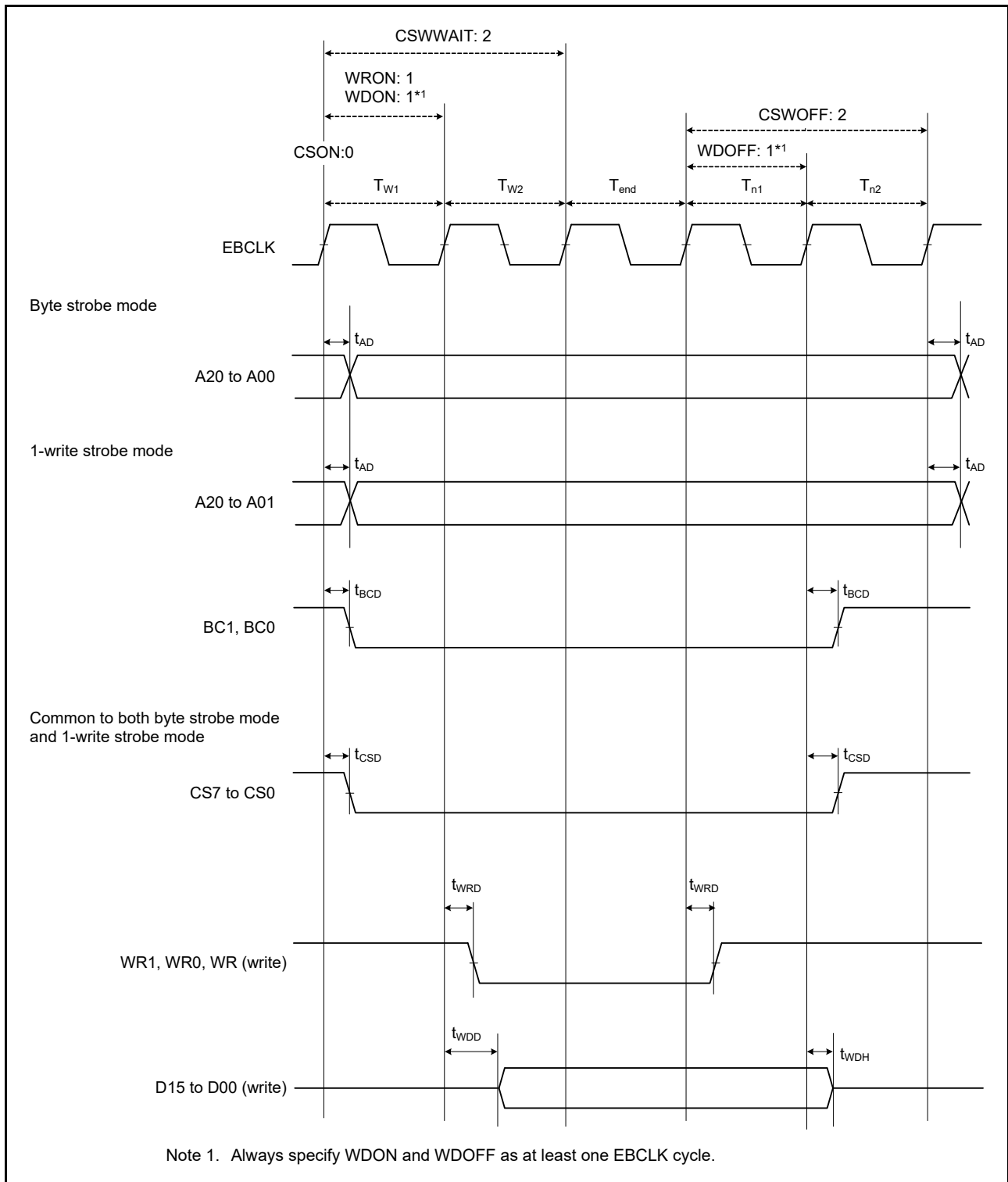


Figure 2.23 External bus timing for normal write cycle with bus clock synchronized

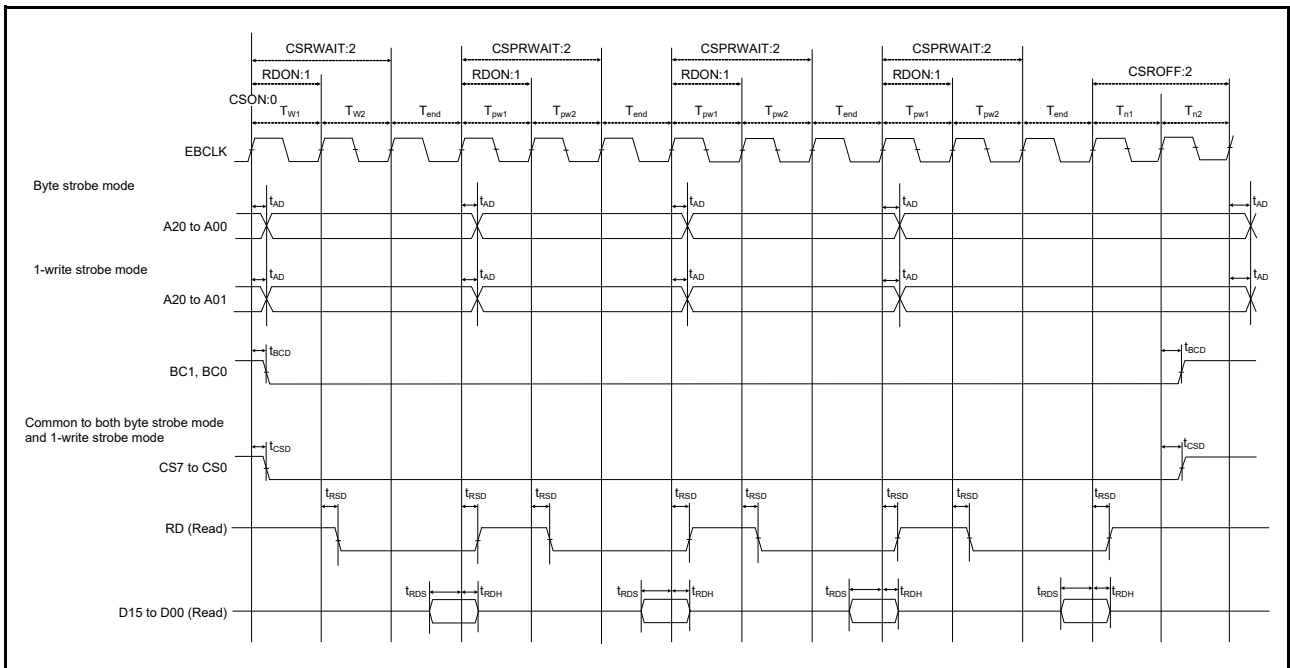


Figure 2.24 External bus timing for page read cycle with bus clock synchronized

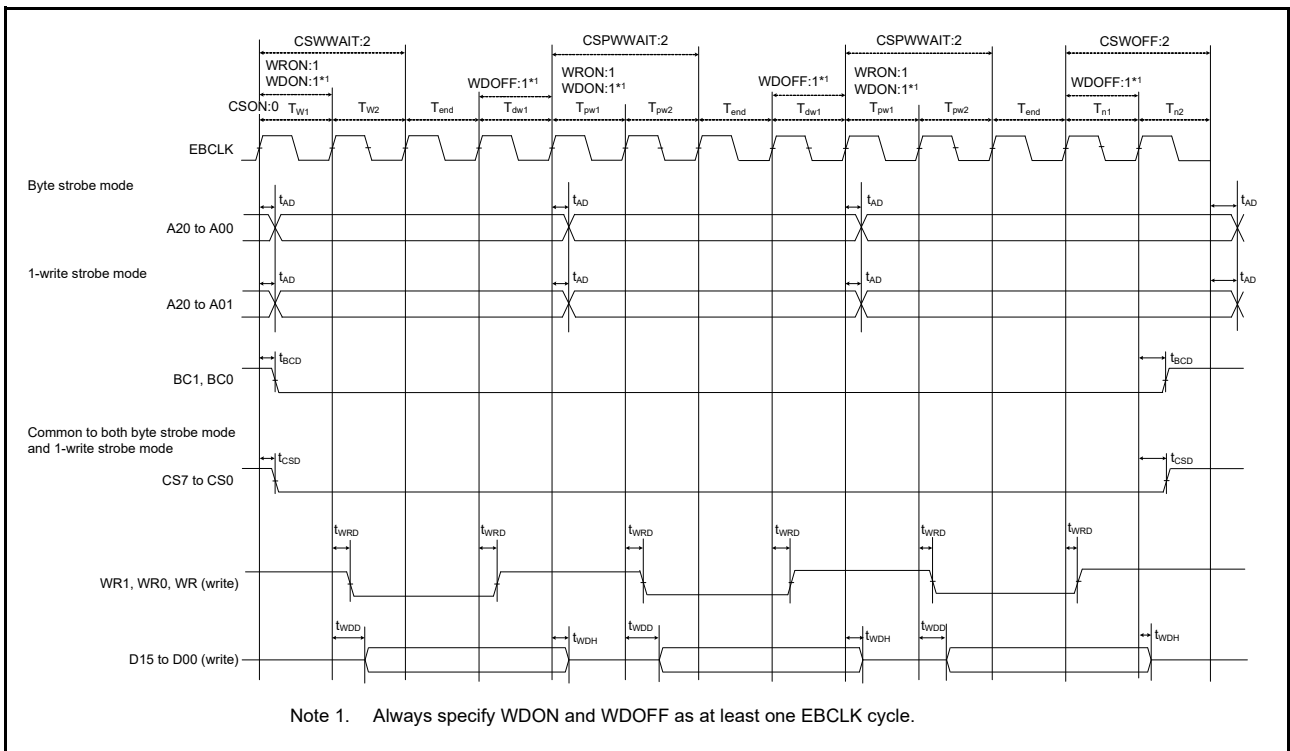


Figure 2.25 External bus timing for page write cycle with bus clock synchronized

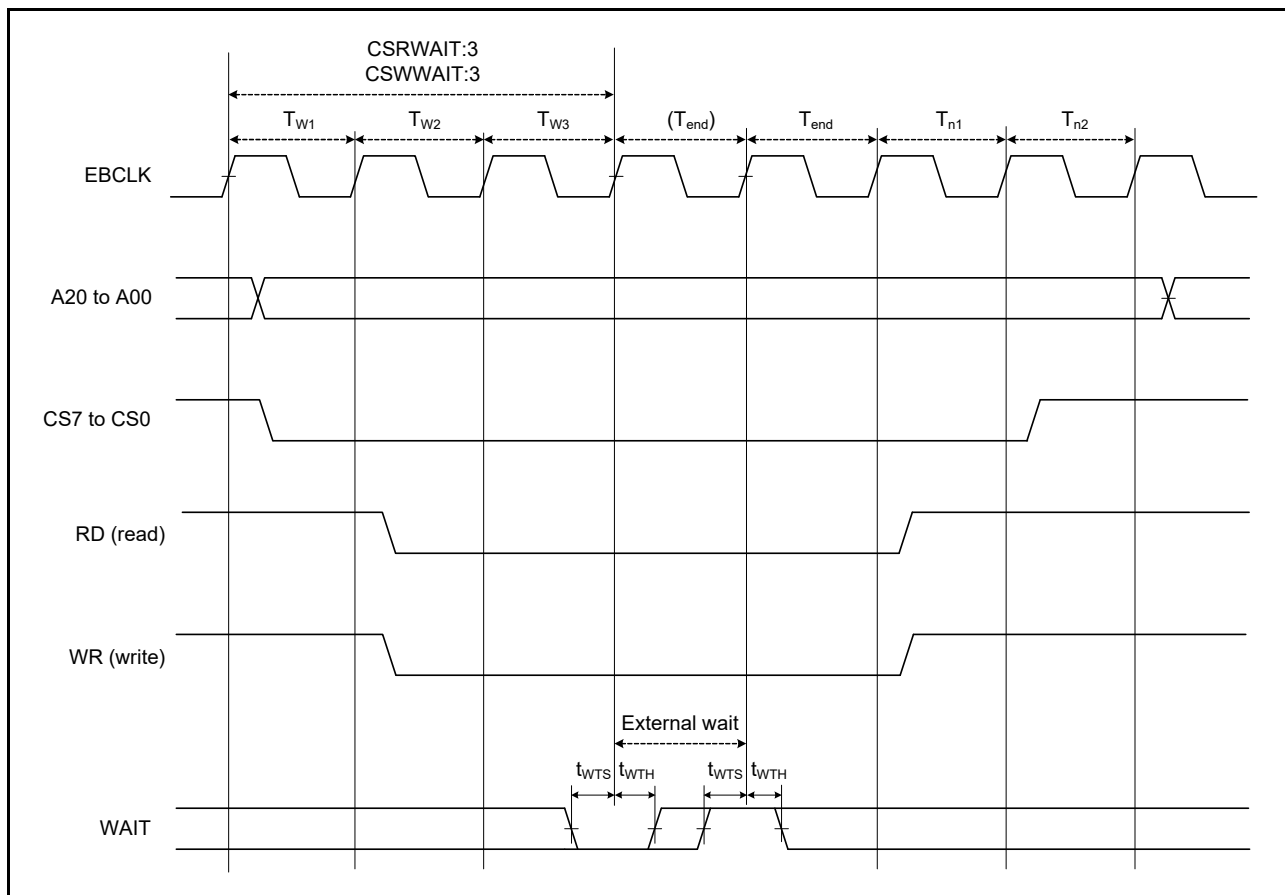


Figure 2.26 External bus timing for external wait control

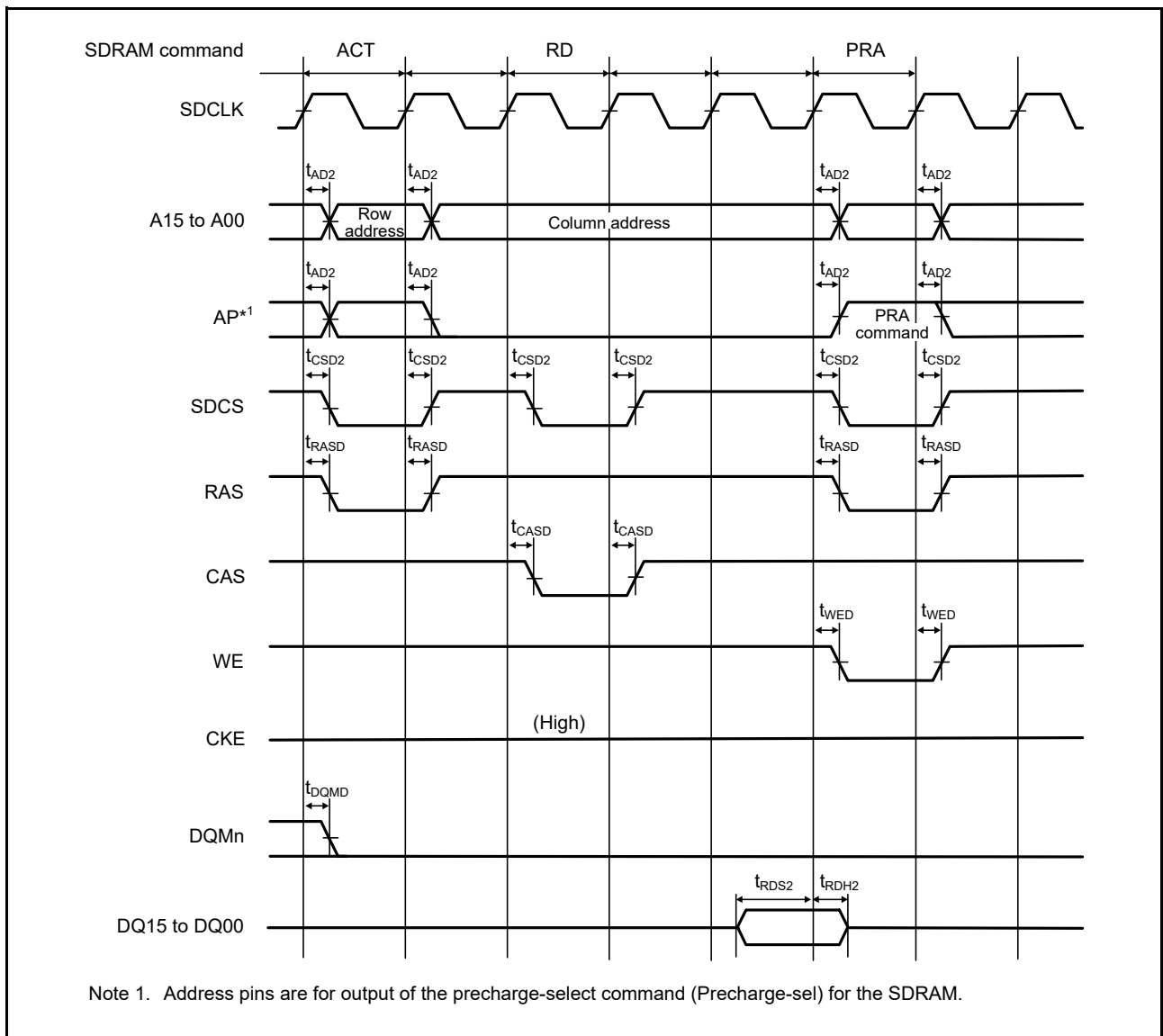


Figure 2.27 SDRAM single read timing

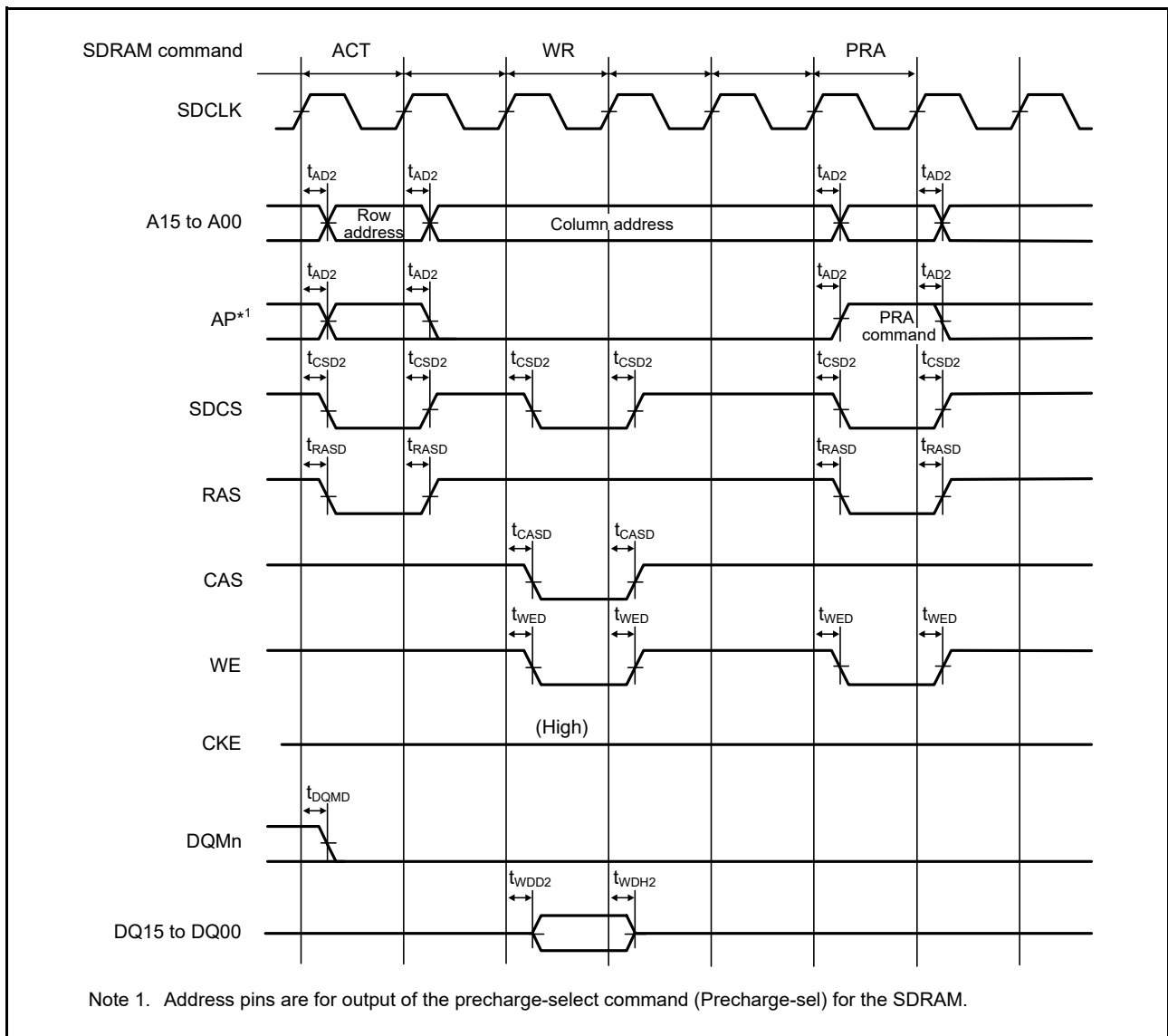


Figure 2.28 SDRAM single write timing

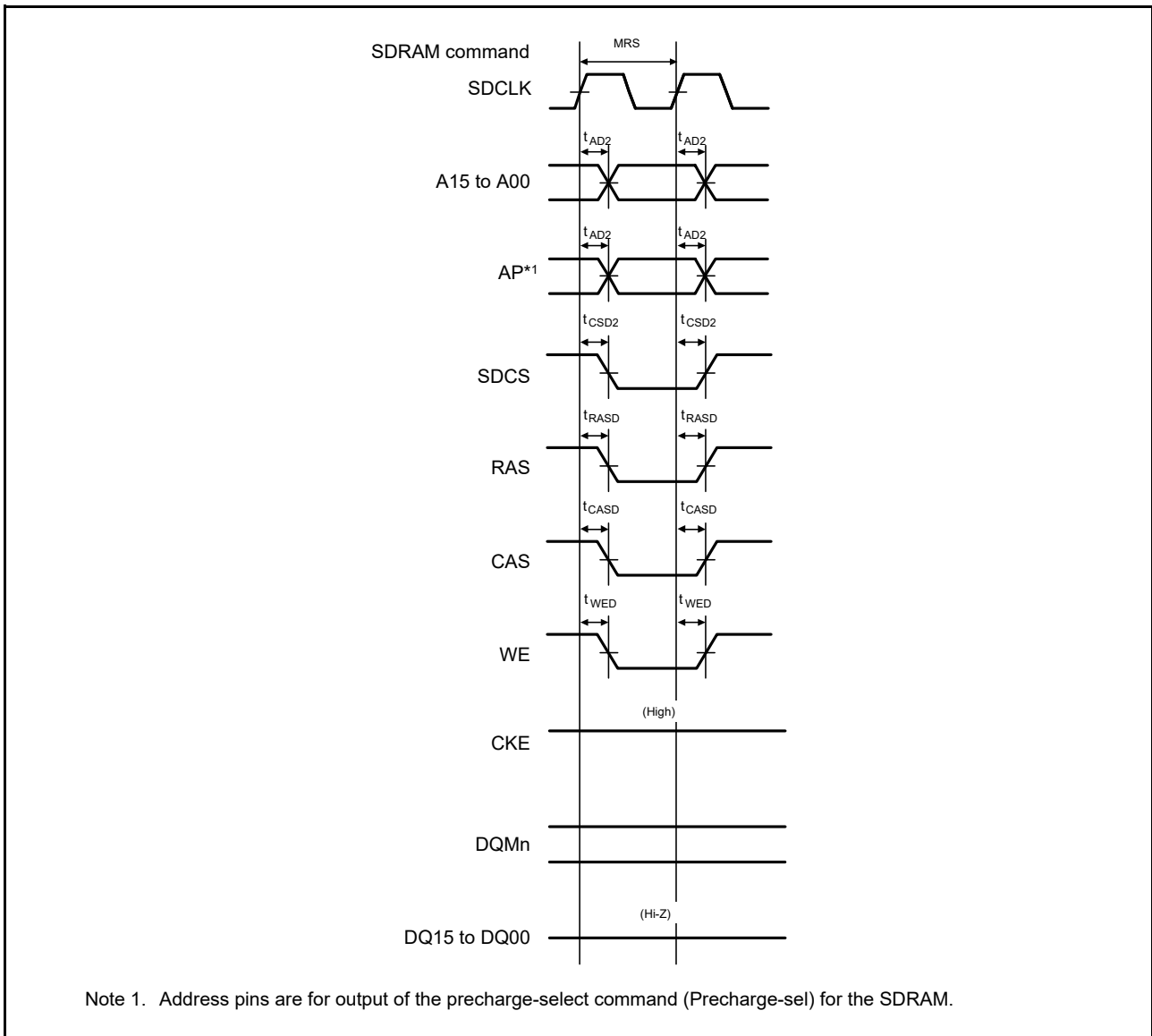


Figure 2.29 SDRAM mode register set timing

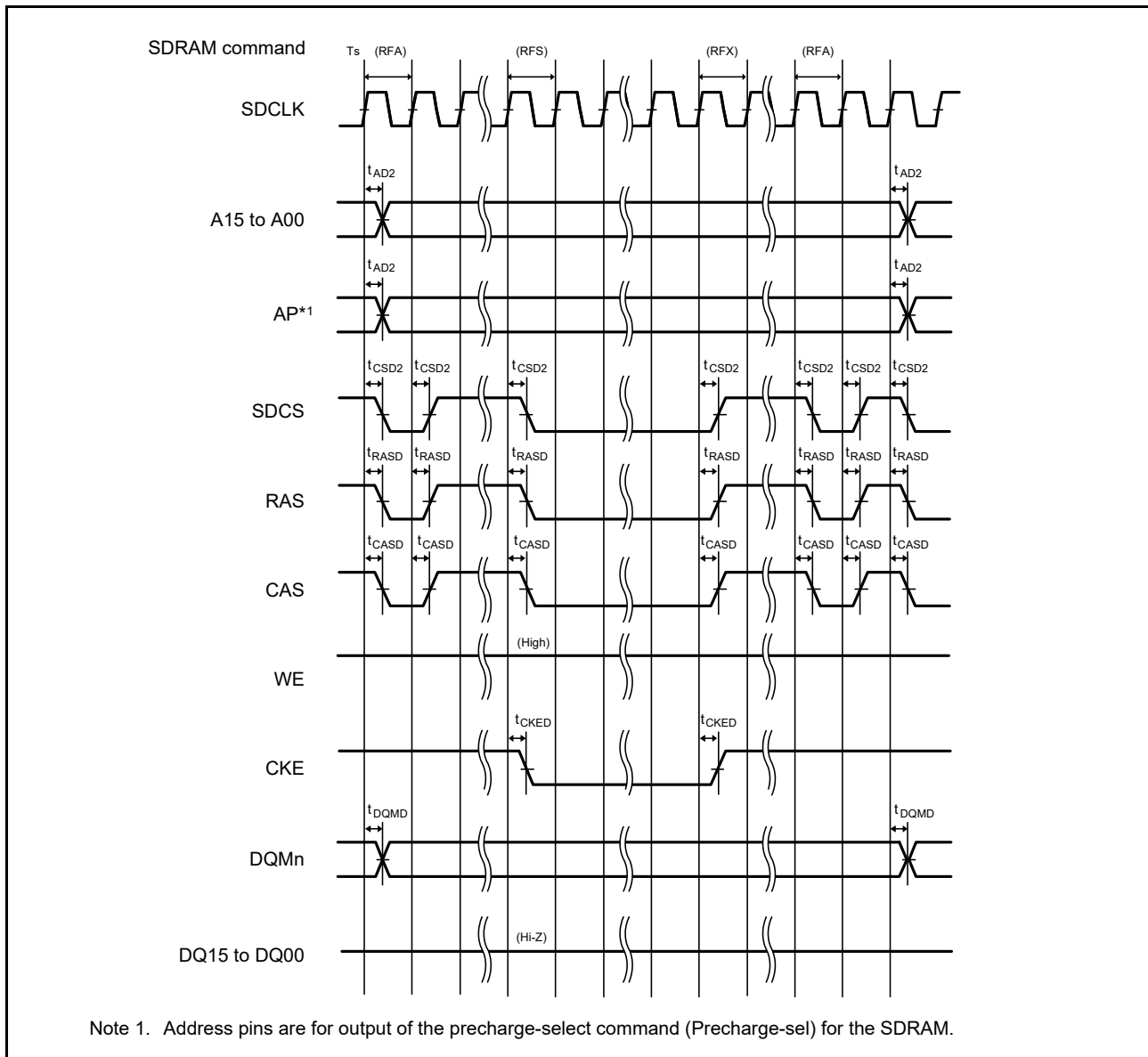


Figure 2.30 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:

Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	$t_{PRW}$	1.5	-	$t_{Pcyc}$	Figure 2.31
POEG	POEG input trigger pulse width	$t_{POEW}$	3	-	$t_{Pcyc}$	Figure 2.32

**Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)**

GPT32 Conditions:

High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

AGT Conditions:

Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions	
GPT32	Input capture pulse width	Single edge	1.5	-	$t_{PDcyc}$	Figure 2.33
		Dual edge	2.5	-		
GPT32	GTIOCxY output skew (x = 0 to 7, Y = A or B)	Middle drive buffer	-	4	ns	Figure 2.34
		High drive buffer	-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer	-	4		
		High drive buffer	-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer	-	6		
		High drive buffer	-	6		
OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO	$t_{GTOSK}$	-	5	ns	Figure 2.35	
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)	$t_{HRSK}^{*2}$	-	2.0	ns	Figure 2.36
AGT	AGTIO, AGTEE input cycle	$t_{ACYC}^{*3}$	100	-	ns	Figure 2.37
	AGTIO, AGTEE input high width, low width	$t_{ACKWH}$ , $t_{ACKWL}$	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	$t_{ACYC2}$	62.5	-	ns	
ADC12	ADC12 trigger input pulse width	$t_{TRGW}$	1.5	-	$t_{Pcyc}$	Figure 2.38
KINT	KRn (n = 00 to 07) pulse width	$t_{KR}$	250	-	ns	Figure 2.39

Note:  $t_{Pcyc}$ : PCLKB cycle,  $t_{PDcyc}$ : PCLKD cycle.

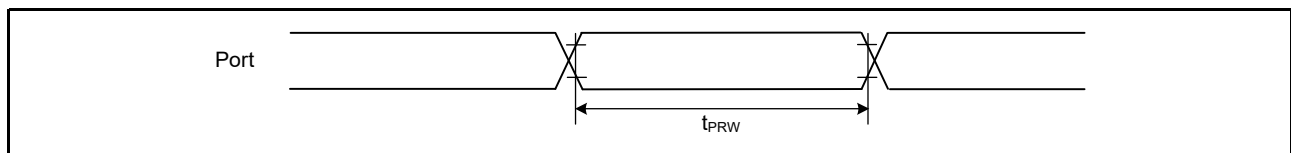
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.

Note 2. The load is 30 pF.

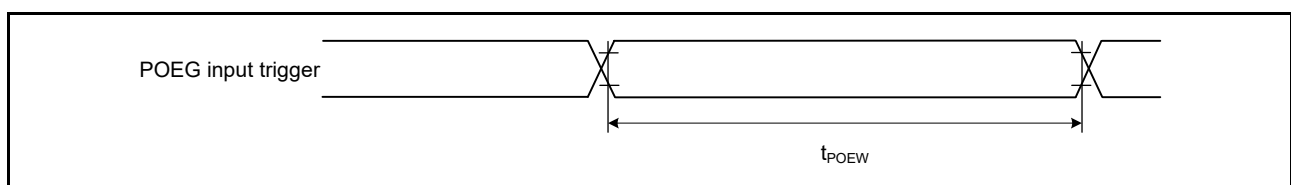
Note 3. Constraints on input cycle:

When not switching the source clock:  $t_{Pcyc} \times 2 < t_{ACYC}$  should be satisfied.

When switching the source clock:  $t_{Pcyc} \times 6 < t_{ACYC}$  should be satisfied.



**Figure 2.31 I/O ports input timing**



**Figure 2.32 POEG input trigger timing**

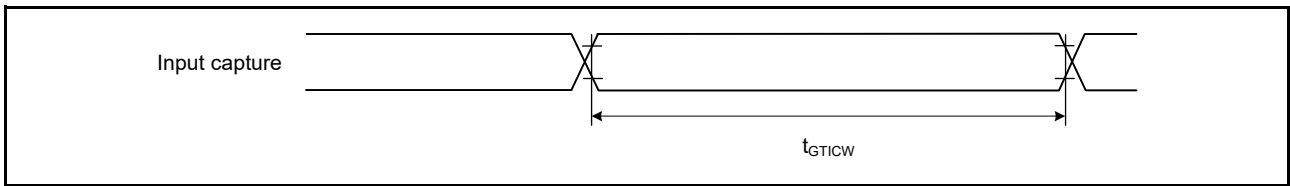


Figure 2.33 GPT32 input capture timing

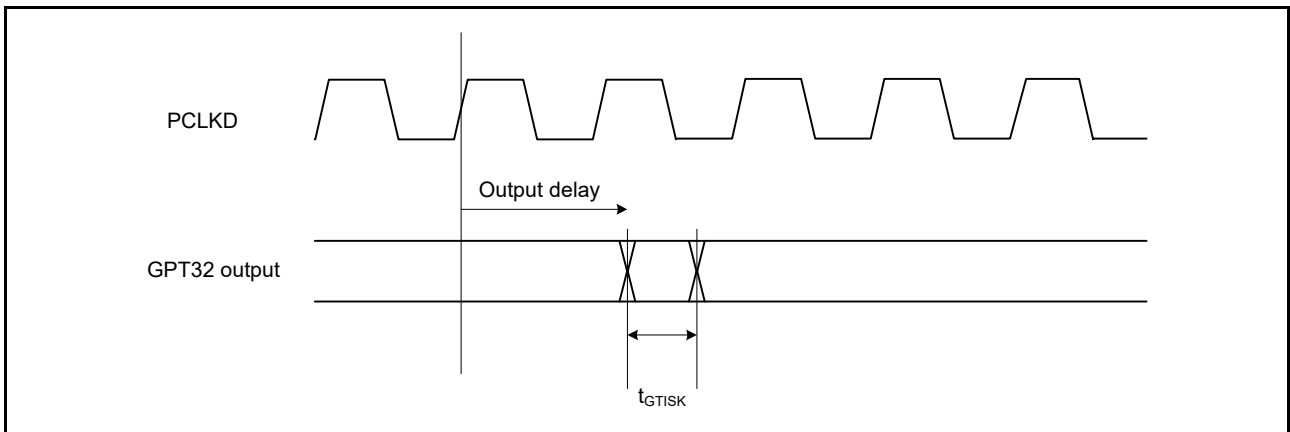


Figure 2.34 GPT32 output delay skew

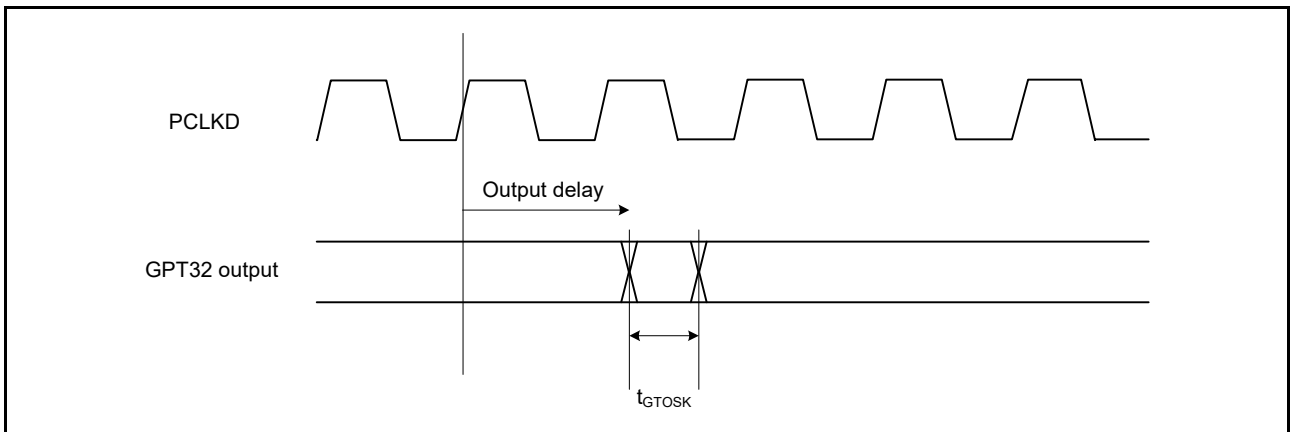


Figure 2.35 GPT32 output delay skew for OPS

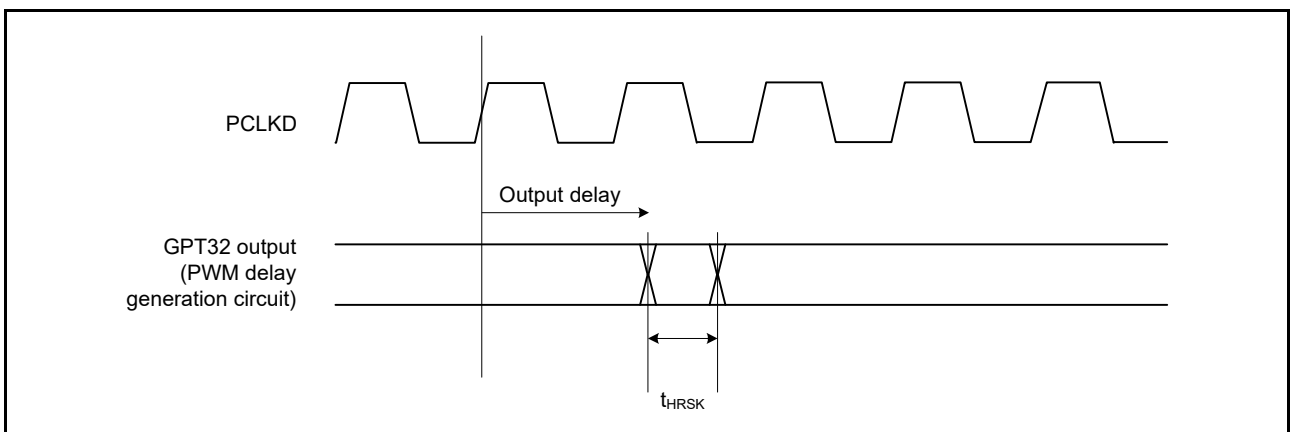


Figure 2.36 GPT32 (PWM Delay Generation Circuit) output delay skew

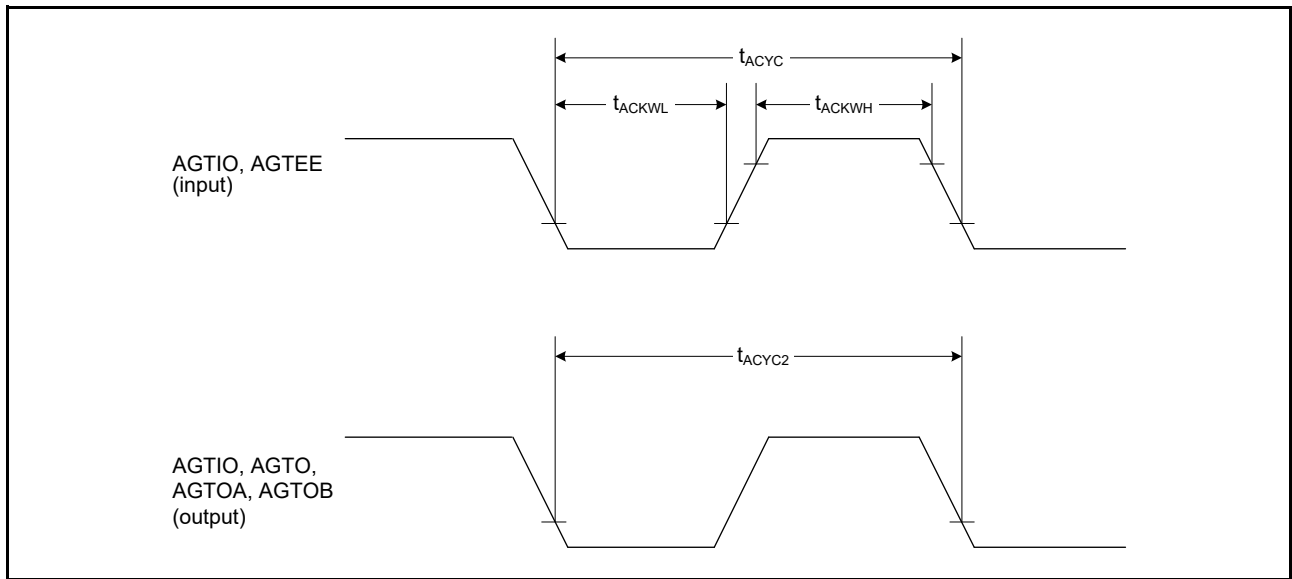


Figure 2.37 AGT input/output timing

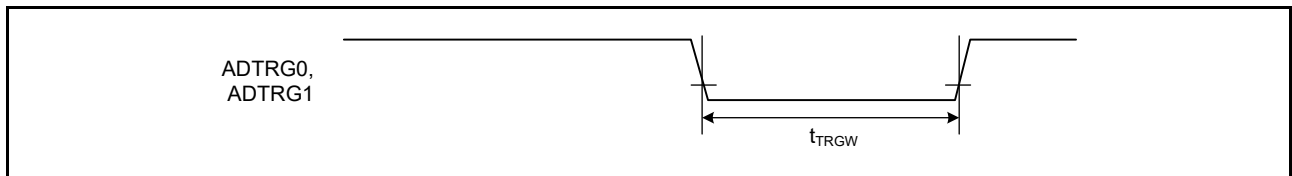


Figure 2.38 ADC12 trigger input timing

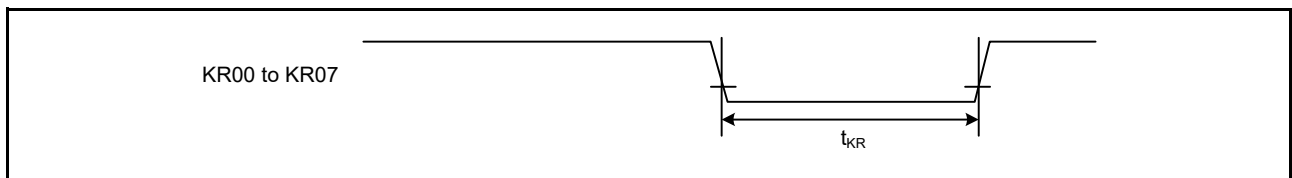


Figure 2.39 Key interrupt input timing

### 2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

### 2.3.9 CAC Timing

Table 2.21 CAC timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{CACREF}$	$t_{PBcyc} \leq t_{cac} \times 2$	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns
			$t_{PBcyc} > t_{cac} \times 2$	$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns

Note 1.  $t_{pBcyc}$ : PCLKB cycle.

Note 2.  $t_{cac}$ : CAC count clock source cycle.

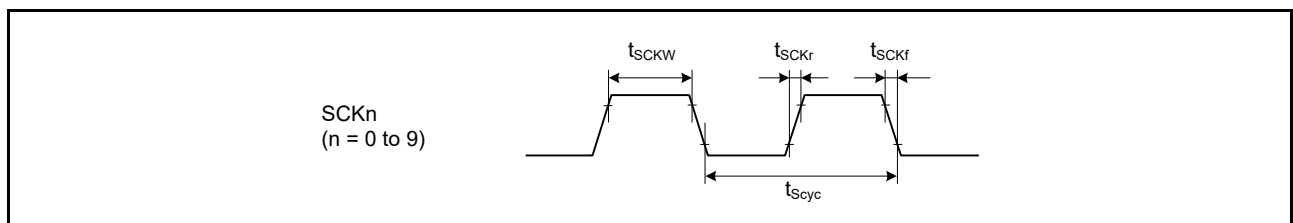
### 2.3.10 SCI Timing

**Table 2.22 SCI timing (1)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK9. For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit*1	Test conditions	
SCI	Input clock cycle	Asynchronous	$t_{Scyc}$	4	-	$t_{Pcyc}$	Figure 2.40
		Clock synchronous		6	-		
Input clock pulse width		$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
Input clock rise time		$t_{SCKr}$	-	5	ns		
Input clock fall time		$t_{SCKf}$	-	5	ns		
Output clock cycle	Asynchronous	$t_{Scyc}$	6	-	$t_{Pcyc}$		
	Clock synchronous		4	-			
Output clock pulse width		$t_{SCKW}$	0.4	0.6	$t_{Scyc}$		
Output clock rise time		$t_{SCKr}$	-	5	ns		
Output clock fall time		$t_{SCKf}$	-	5	ns		
Transmit data delay	Clock synchronous	$t_{TXD}$	-	25	ns	Figure 2.41	
Receive data setup time	Clock synchronous	$t_{RXS}$	15	-	ns		
Receive data hold time	Clock synchronous	$t_{RXH}$	5	-	ns		

Note 1.  $t_{Pcyc}$ : PCLKA cycle.



**Figure 2.40 SCK clock input/output timing**



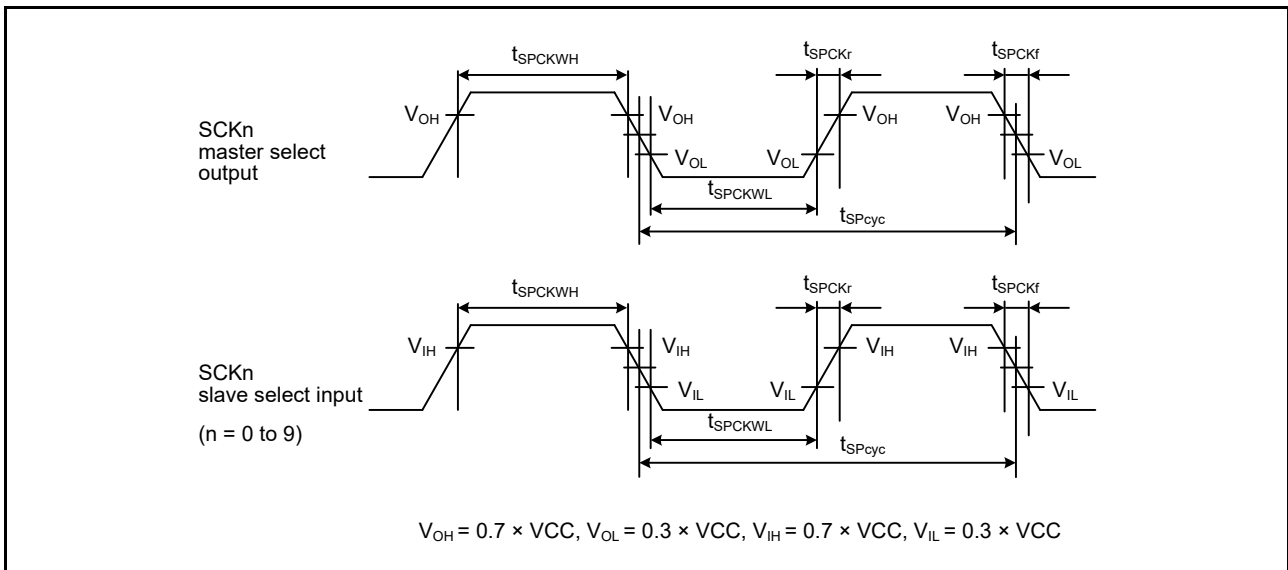


Figure 2.42 SCI simple SPI mode clock timing

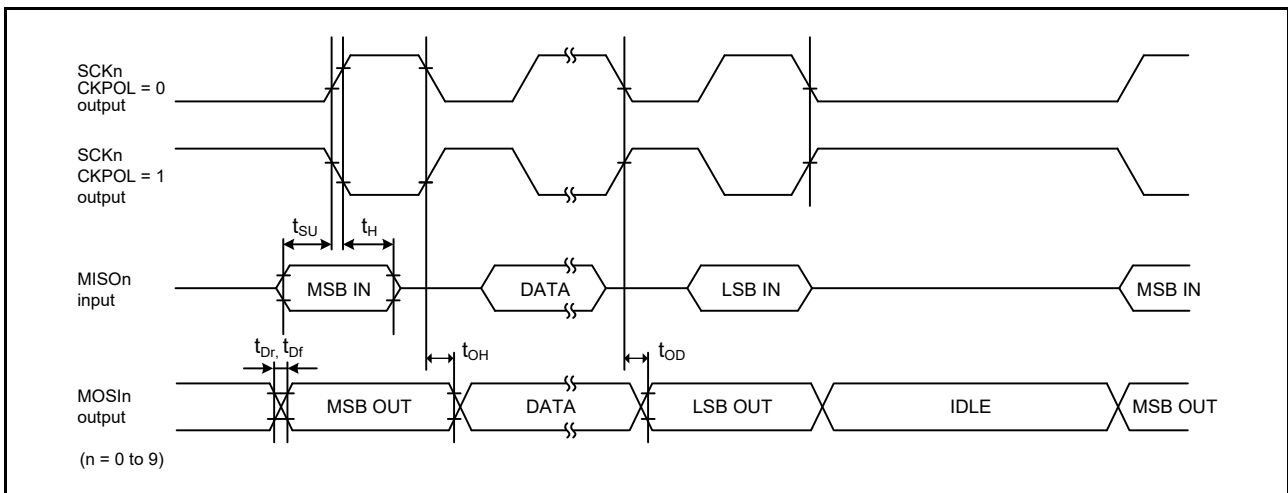


Figure 2.43 SCI simple SPI mode timing for master when CKPH = 1

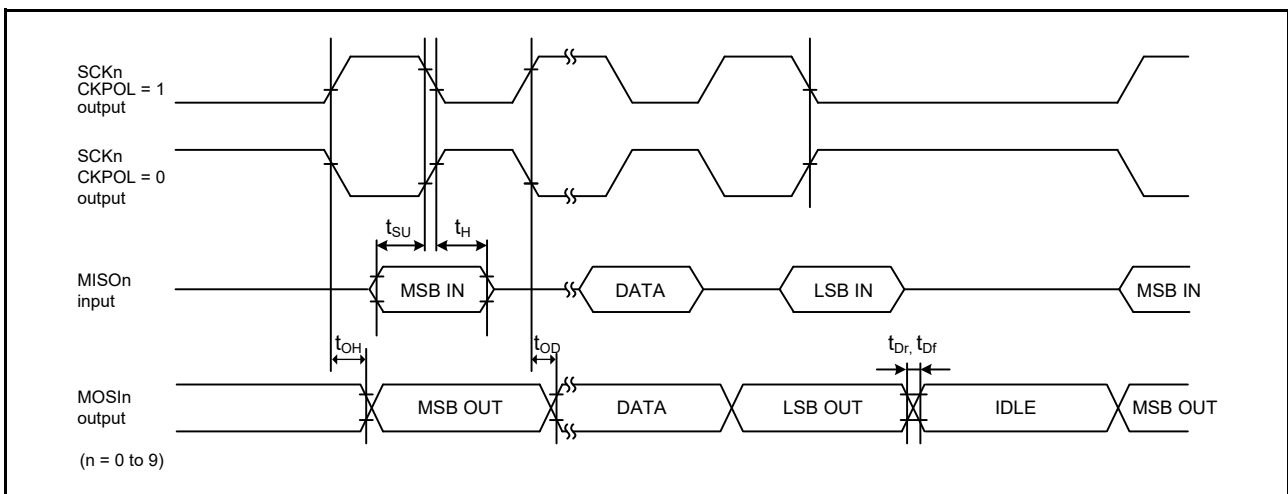


Figure 2.44 SCI simple SPI mode timing for master when CKPH = 0

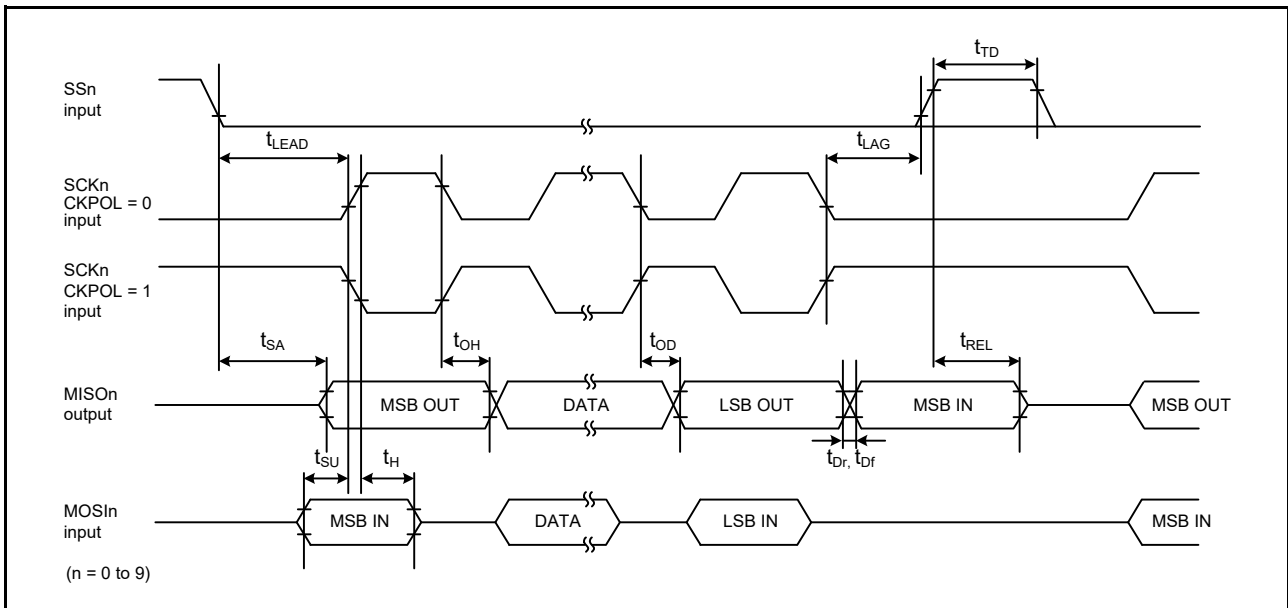


Figure 2.45 SCI simple SPI mode timing for slave when CKPH = 1

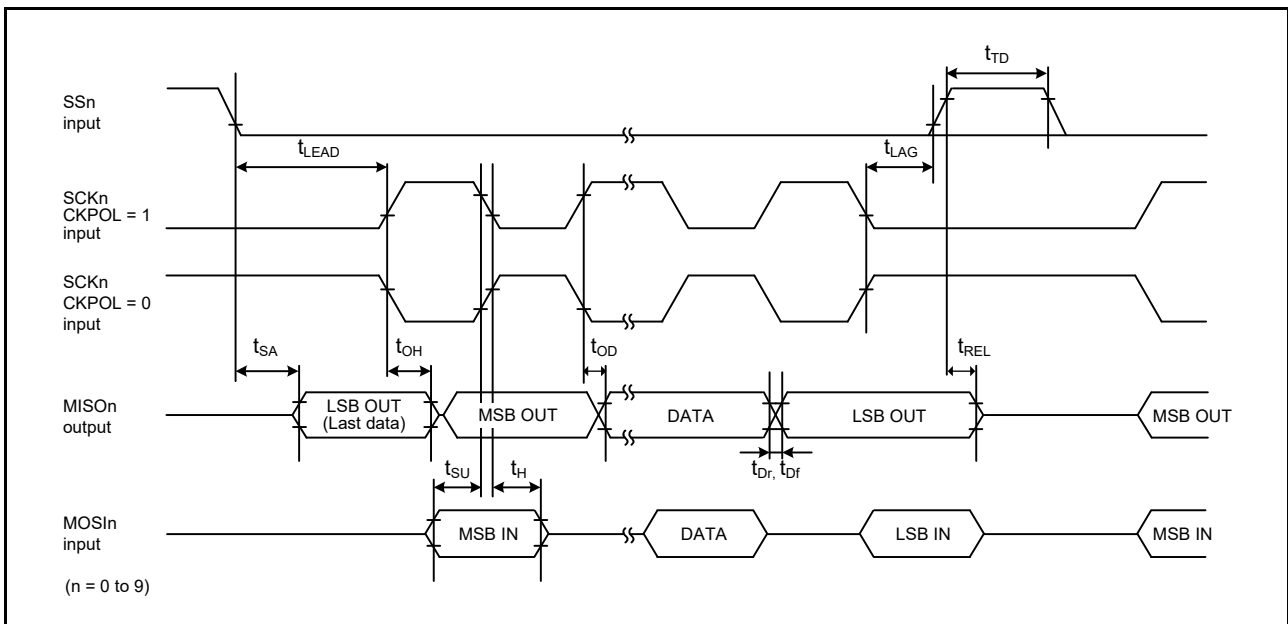


Figure 2.46 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Standard mode)	SDA input rise time	$t_{Sr}$	-	1000	ns	Figure 2.47
	SDA input fall time	$t_{Sf}$	-	300	ns	
	SDA input spike pulse removal time	$t_{SP}$	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	$t_{SDAS}$	250	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b^{*1}$	-	400	pF	

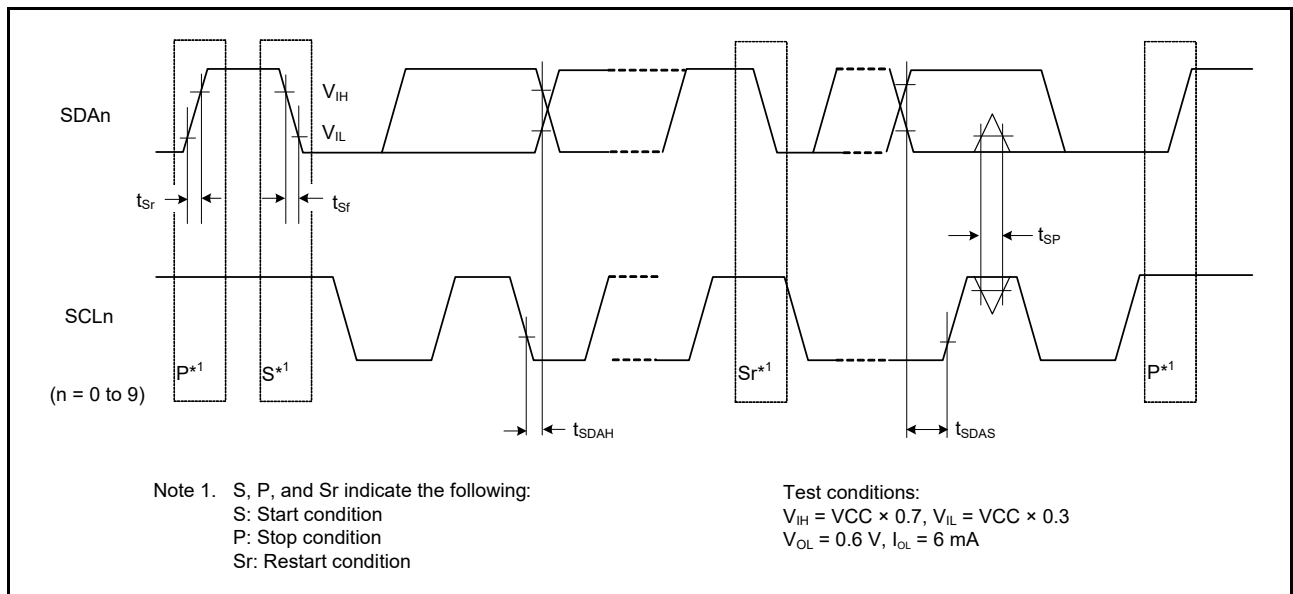
**Table 2.24 SCI timing (3) (2 of 2)**

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Fast mode)	SDA input rise time	$t_{Sr}$	-	300	ns	Figure 2.47
	SDA input fall time	$t_{Sf}$	-	300	ns	
	SDA input spike pulse removal time	$t_{SP}$	0	$4 \times t_{IICyc}$	ns	
	Data input setup time	$t_{SDAS}$	100	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b^{*1}$	-	400	pF	

Note:  $t_{IICyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle.

Note 1.  $C_b$  indicates the total capacity of the bus line.



**Figure 2.47 SCI simple IIC mode timing**

## 2.3.11 SPI Timing

**Table 2.25 SPI timing**

Conditions:

For RSPCKA and RSPCKB pins, high drive output is selected with the Port Drive Capability bit in the PmnPFS register.

For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit*1	Test conditions*2		
SPI	RSPCK clock cycle	Master	$t_{SPCyc}$	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	$t_{PCyc}$	Figure 2.48 C = 30 pF	
		Slave		4	4096			
RSPCK clock high pulse width	Master	$t_{SPCKWH}$	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns			
	Slave			$2 \times t_{PCyc}$	-			
RSPCK clock low pulse width	Master	$t_{SPCKWL}$	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns			
	Slave			$2 \times t_{PCyc}$	-			
RSPCK clock rise and fall time	Master	$t_{SPCKr}$	-	5	ns			
	Slave	$t_{SPCKf}$	-	1	μs			
Data input setup time	Master	$t_{SU}$		4	-	ns		Figure 2.49 to Figure 2.54 C = 30 pF
	Slave			5	-			
Data input hold time	Master (PCLKA division ratio set to 1/2)	$t_{HF}$	0	-	ns			
	Master (PCLKA division ratio set to a value other than 1/2)	$t_H$	$t_{PCyc}$	-				
	Slave	$t_H$	20	-				
SSL setup time	Master	$t_{LEAD}$		$N \times t_{SPCyc} - 10^3$	$N \times t_{SPCyc} + 100^3$	ns		
	Slave			$6 \times t_{PCyc}$	-	ns		
SSL hold time	Master	$t_{LAG}$		$N \times t_{SPCyc} - 10^4$	$N \times t_{SPCyc} + 100^4$	ns		
	Slave			$6 \times t_{PCyc}$	-	ns		
Data output delay	Master	$t_{OD}$		-	6.3	ns		
	Slave			-	20			
Data output hold time	Master	$t_{OH}$		0	-	ns		
	Slave			0	-			
Successive transmission delay	Master	$t_{TD}$		$t_{SPCyc} + 2 \times t_{PCyc}$	$8 \times t_{SPCyc} + 2 \times t_{PCyc}$	ns		
	Slave			$6 \times t_{PCyc}$				
MOSI and MISO rise and fall time	Output	$t_{Dr}, t_{Df}$		-	5	ns		
	Input			-	1			μs
SSL rise and fall time	Output	$t_{SSLr}$	-	5	ns			
	Input	$t_{SSLf}$	-	1	μs			
Slave access time		$t_{SA}$	-	$2 \times t_{PCyc} + 28$	ns	Figure 2.53 and Figure 2.54 C = 30 pF		
Slave output release time		$t_{REL}$	-	$2 \times t_{PCyc} + 28$				

Note 1.  $t_{PCyc}$ : PCLKA cycle.

- Note 2. Must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
- Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
- Note 4. N is set to an integer from 1 to 8 by the SSLND register.

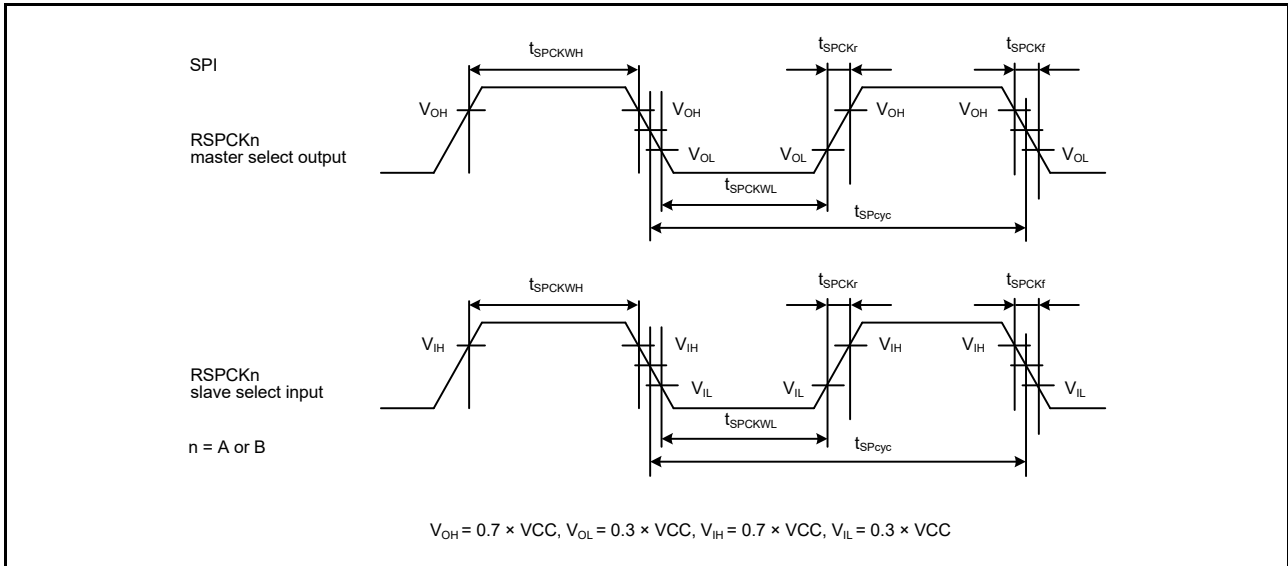


Figure 2.48 SPI clock timing

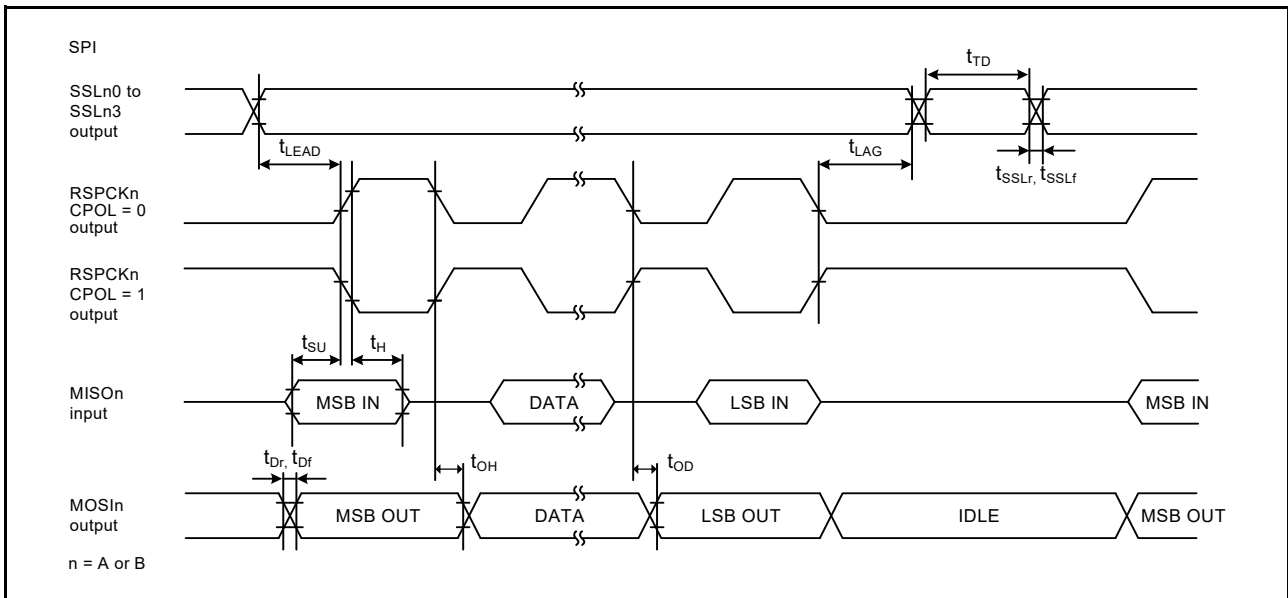
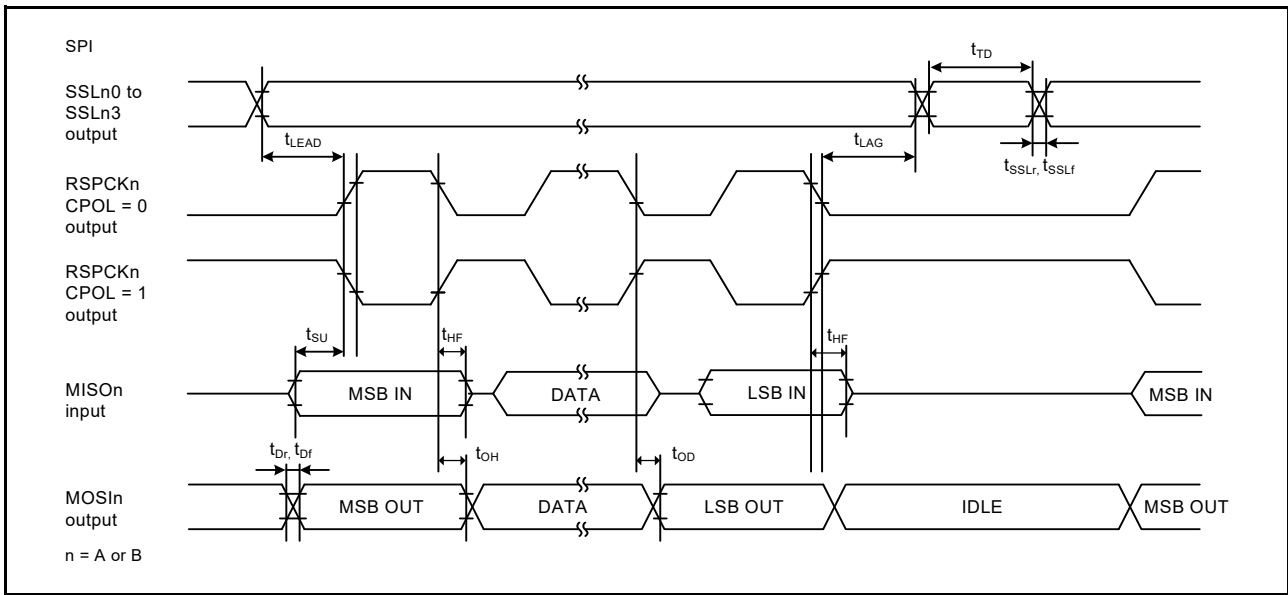
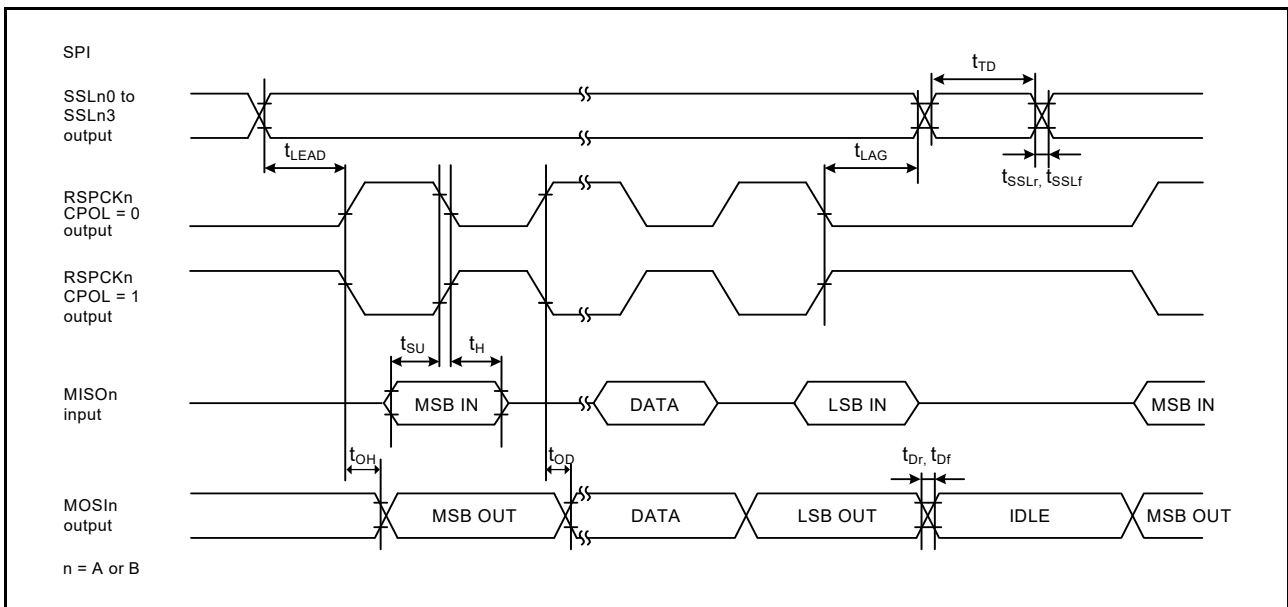


Figure 2.49 SPI timing for master when CPHA = 0



**Figure 2.50** SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



**Figure 2.51** SPI timing for master when CPHA = 1

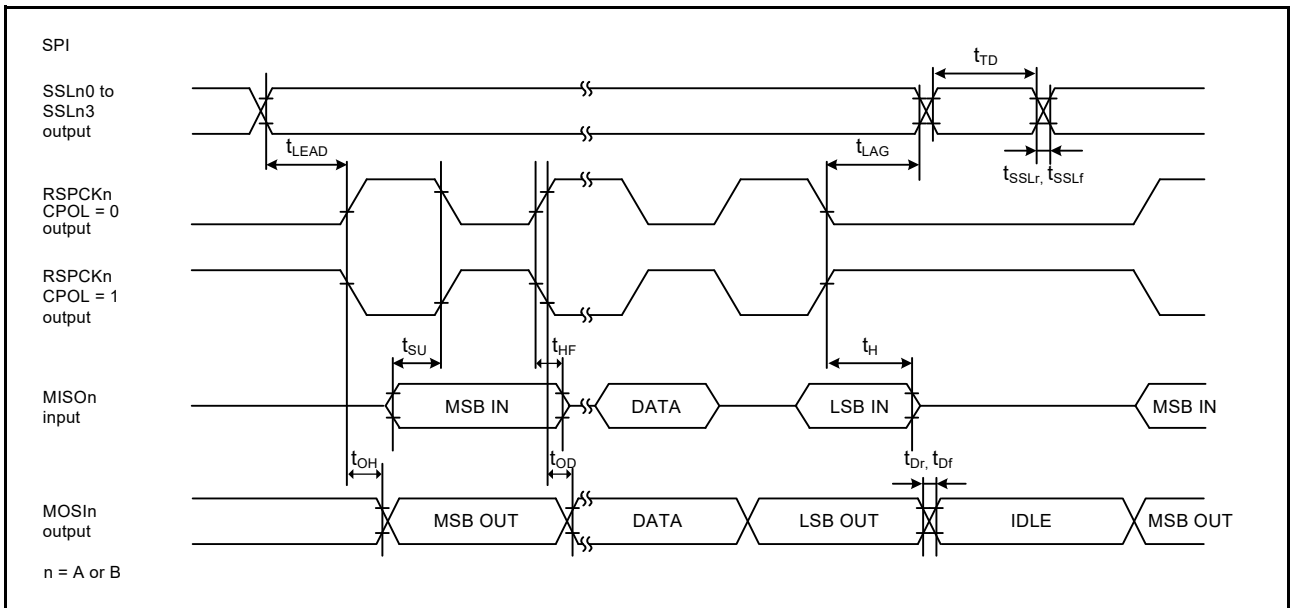


Figure 2.52 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

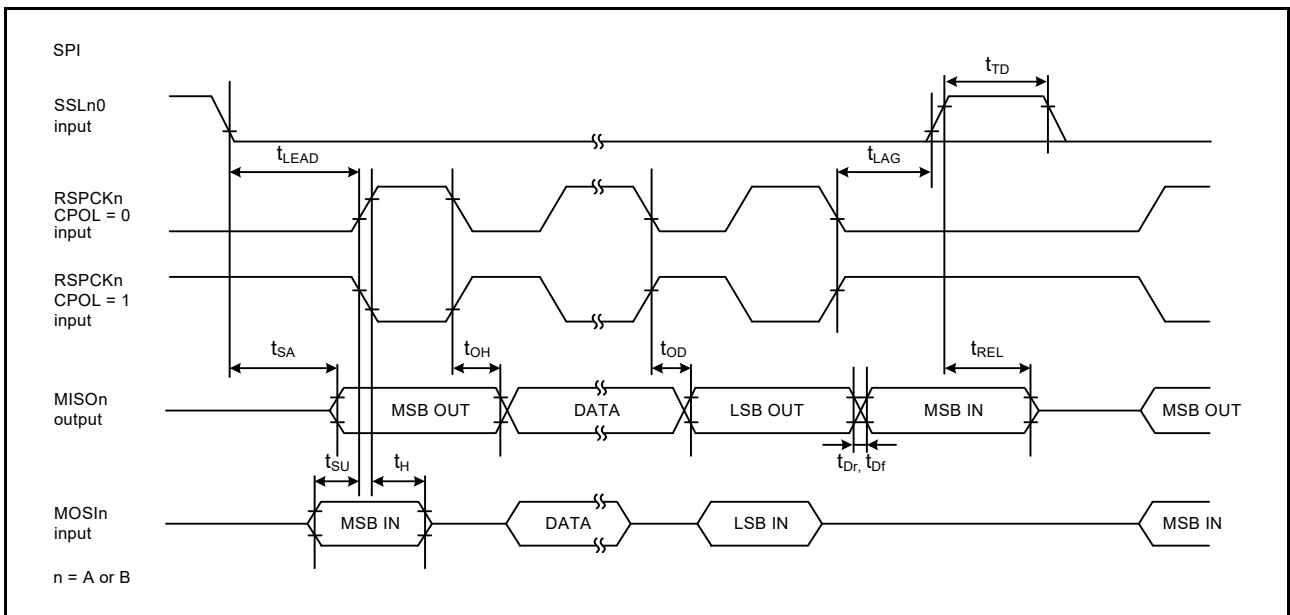


Figure 2.53 SPI timing for slave when CPHA = 0

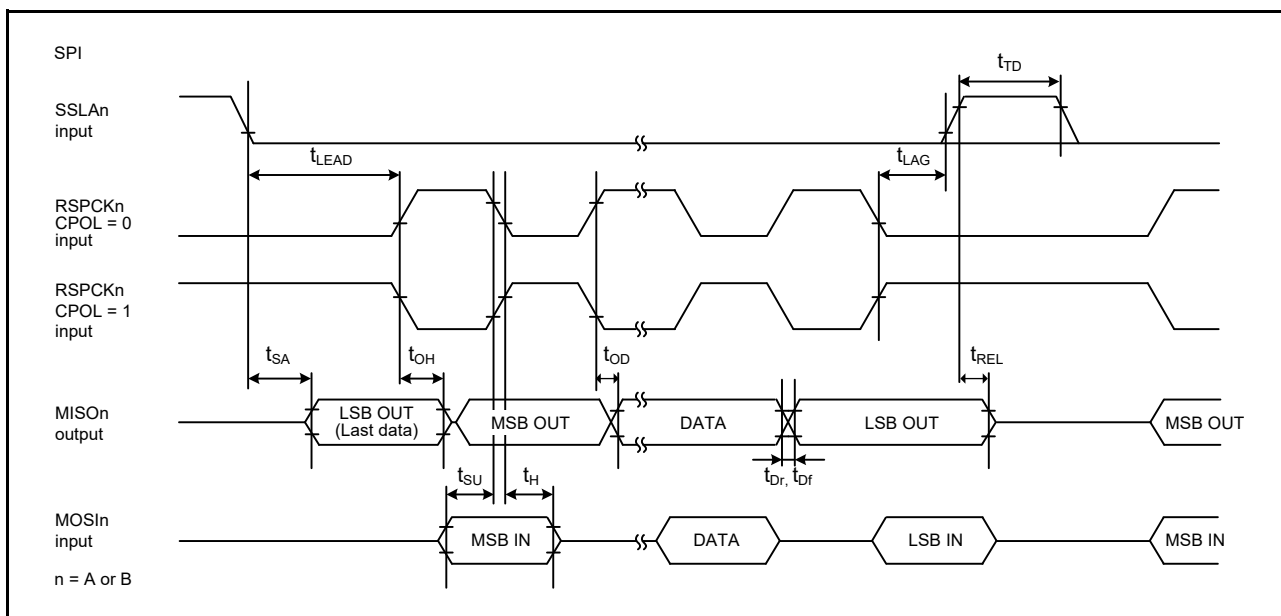


Figure 2.54 SPI timing for slave when CPHA = 1

### 2.3.12 QSPI Timing

Table 2.26 QSPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit*1	Test conditions
QSPI	QSPCK clock cycle	$t_{QScyc}$	48	$t_{Pcyc}$	Figure 2.55
	QSPCK clock high pulse width	$t_{QSWH}$	$t_{QScyc} \times 0.4$	ns	
	QSPCK clock low pulse width	$t_{QSWL}$	$t_{QScyc} \times 0.4$	ns	
	Data input setup time	$t_{Su}$	8	ns	Figure 2.56
	Data input hold time	$t_{IH}$	0	ns	
	QSSL setup time	$t_{LEAD}$	$(N+0.5) \times t_{QScyc} - 5^{*2}$	$(N+0.5) \times t_{QScyc} + 100^{*2}$	ns
	QSSL hold time	$t_{LAG}$	$(N+0.5) \times t_{QScyc} - 5^{*3}$	$(N+0.5) \times t_{QScyc} + 100^{*3}$	ns
	Data output delay	$t_{OD}$	-	4	ns
	Data output hold time	$t_{OH}$	-3.3	-	ns
	Successive transmission delay	$t_{TD}$	1	16	$t_{QScyc}$

Note 1.  $t_{Pcyc}$ : PCLKA cycle.

Note 2. N is set to 0 or 1 in SFMSLD.

Note 3. N is set to 0 or 1 in SFMSHD.

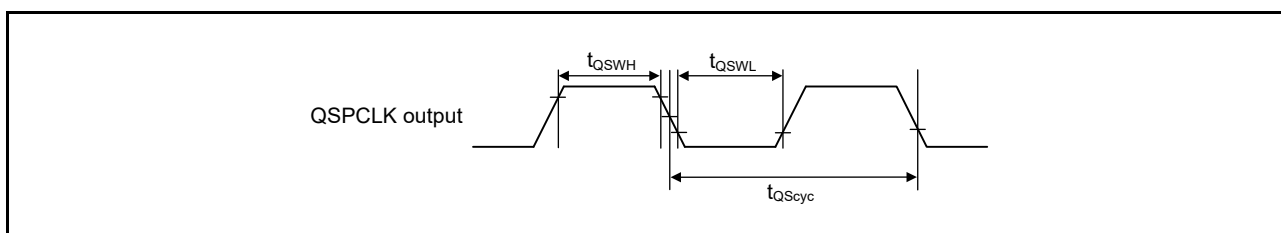


Figure 2.55 QSPI clock timing

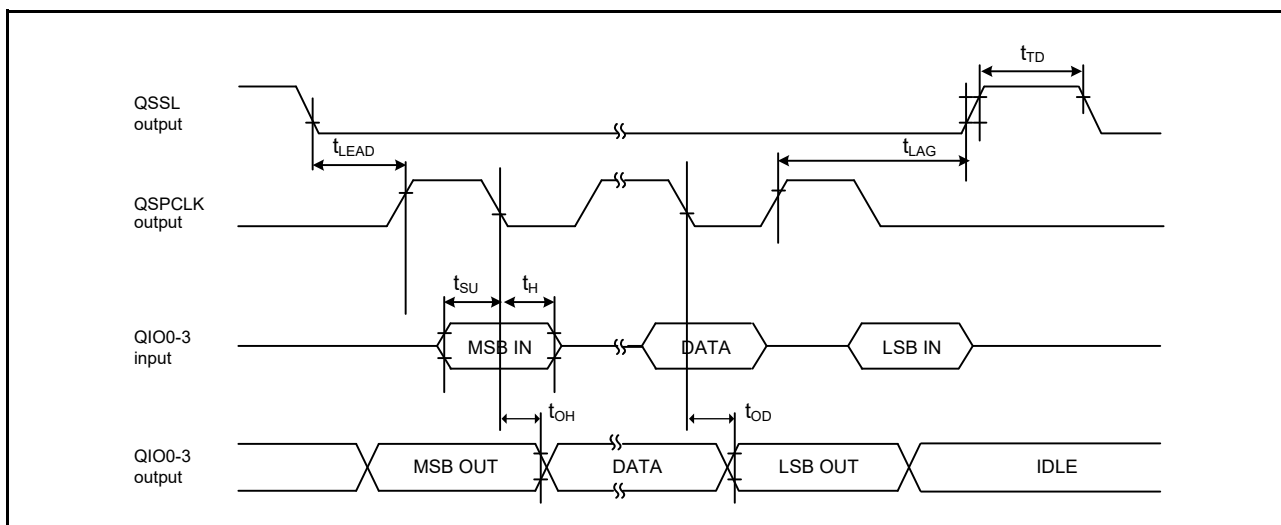


Figure 2.56 Transmit and receive timing

### 2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

- (1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_A, SCL1\_A, SDA1\_B, SCL1\_B.
- (2) The following pins do not require setting: SCL0\_A, SDA0\_A, SCL2, SDA2.
- (3) Use pins that have a letter appended to their names, for instance “\_A” or “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter	Symbol	Min*1	Max	Unit	Test conditions*3	
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	$t_{SCL}$	$6 (12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.57
	SCL input high pulse width	$t_{SCLH}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	$t_{SCLL}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	$t_{Sr}$	-	1000	ns	
	SCL, SDA input fall time	$t_{Sf}$	-	300	ns	
	SCL, SDA input spike pulse removal time	$t_{SP}$	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time when wakeup function is enabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is disabled	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is enabled	$t_{STAH}$	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	$t_{STAS}$	1000	-	ns	
	STOP condition input setup time	$t_{STOS}$	1000	-	ns	
	Data input setup time	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	400	pF	

**Table 2.27 IIC timing (1) (2 of 2)**

- (1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0\_B, SCL0\_B, SDA1\_A, SCL1\_A, SDA1\_B, SCL1\_B.  
 (2) The following pins do not require setting: SCL0\_A, SDA0\_A, SCL2, SDA2.  
 (3) Use pins that have a letter appended to their names, for instance “\_A” or “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter	Symbol	Min*1	Max	Unit	Test conditions*3	
IIC (Fast mode)	SCL input cycle time	$t_{SCL}$	$6 (12) \times t_{IICcyc} + 600$	-	ns	Figure 2.57
	SCL input high pulse width	$t_{SCLH}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	$t_{SCLL}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	$t_{Sr}$	$20 \times (\text{external pullup voltage}/5.5V)^2$	300	ns	
	SCL, SDA input fall time	$t_{Sf}$	$20 \times (\text{external pullup voltage}/5.5V)^2$	300	ns	
	SCL, SDA input spike pulse removal time	$t_{SP}$	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time when wakeup function is enabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is disabled	$t_{STAH}$	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is enabled	$t_{STAH}$	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	$t_{STAS}$	300	-	ns	
	STOP condition input setup time	$t_{STOS}$	300	-	ns	
	Data input setup time	$t_{SDAS}$	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
SCL, SDA capacitive load	$C_b$	-	400	pF		

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle,  $t_{Pcyc}$ : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0\_A, SDA0\_A, SCL2, and SDA2.

Note 3. Must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

**Table 2.28 IIC timing (2)**

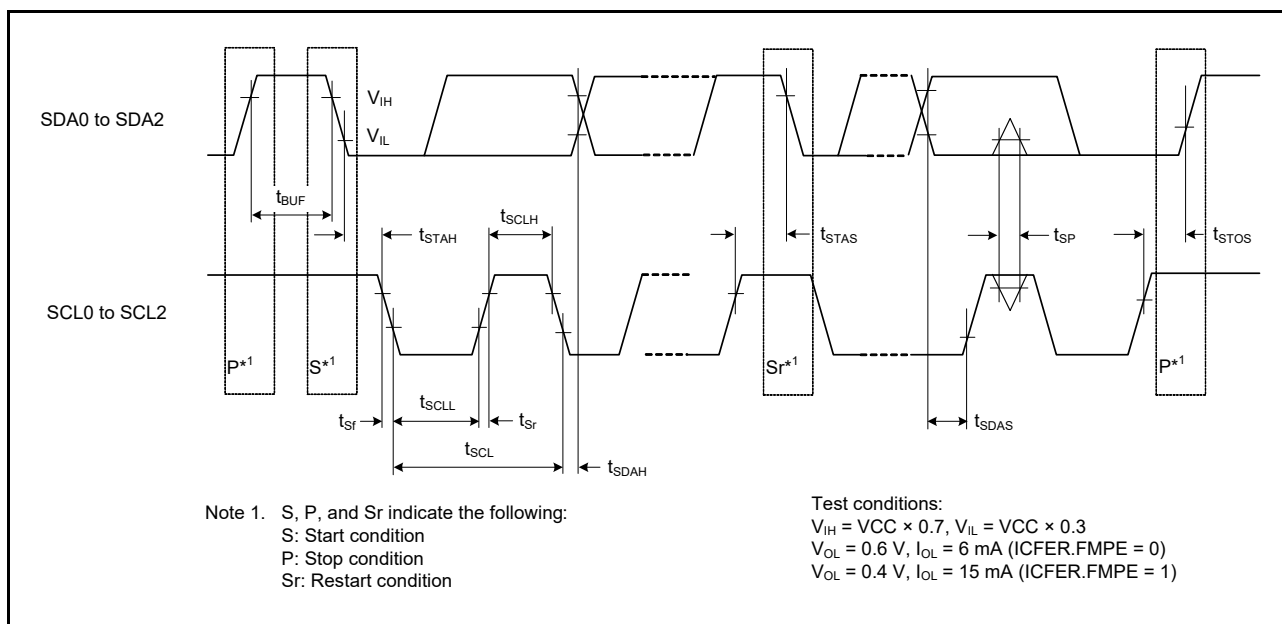
Setting of the SCL0\_A, SDA0\_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min <sup>*1,*2</sup>	Max	Unit	Test conditions	
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	$t_{SCL}$	$6 (12) \times t_{IICcyc} + 240$	-	ns	Figure 2.57
	SCL input high pulse width	$t_{SCLH}$	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SCL input low pulse width	$t_{SCLL}$	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SCL, SDA input rise time	$t_{Sr}$	-	120	ns	
	SCL, SDA input fall time	$t_{Sf}$	-	120	ns	
	SCL, SDA input spike pulse removal time	$t_{SP}$	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SDA input bus free time when wakeup function is enabled	$t_{BUF}$	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 120$	-	ns	
	Start condition input hold time when wakeup function is disabled	$t_{STAH}$	$t_{IICcyc} + 120$	-	ns	
	START condition input hold time when wakeup function is enabled	$t_{STAH}$	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 120$	-	ns	
	Restart condition input setup time	$t_{STAS}$	120	-	ns	
	Stop condition input setup time	$t_{STOS}$	120	-	ns	
	Data input setup time	$t_{SDAS}$	$t_{IICcyc} + 30$	-	ns	
	Data input hold time	$t_{SDAH}$	0	-	ns	
	SCL, SDA capacitive load	$C_b$	-	550	pF	

Note:  $t_{IICcyc}$ : IIC internal reference clock (IIC $\phi$ ) cycle,  $t_{Pcyc}$ : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2.  $C_b$  indicates the total capacity of the bus line.



**Figure 2.57 I2C bus interface input/output timing**

### 2.3.14 SSIE Timing

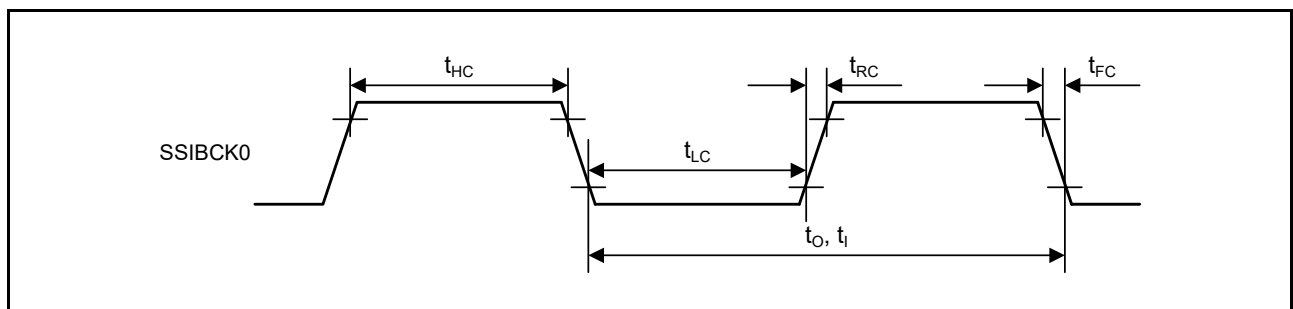
**Table 2.29 SSIE timing**

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance “\_A” or “\_B” to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK0	Cycle	Master	$t_O$	80	-	ns	Figure 2.58
		Slave	$t_I$	80	-	ns	
	High level/ low level	Master	$t_{HC}/t_{LC}$	0.35	-	$t_O$	
		Slave		0.35	-	$t_I$	
	Rising time/falling time	Master	$t_{RC}/t_{FC}$	-	0.15	$t_O / t_I$	
		Slave		-	0.15	$t_O / t_I$	
SSILRCK0/SSIFS0, SSITXD0, SSIRXD0, SSIDATA0	Input set up time	Master	$t_{SR}$	12	-	ns	Figure 2.60, Figure 2.61
		Slave		12	-	ns	
	Input hold time	Master	$t_{HR}$	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	$t_{DTR}$	-10	5	ns	Figure 2.60, Figure 2.61
		Slave		0	20	ns	
	Output delay time from SSILRCK0/SSIFS0 change	Slave	$t_{DTRW}$	-	20	ns	Figure 2.62*1
	GTIOC1A, AUDIO_CLK	Cycle		$t_{EXcyc}$	20	-	ns
High level/ low level			$t_{EXL}/t_{EXH}$	0.4	0.6	$t_{EXcyc}$	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA0 pin.



**Figure 2.58 SSIE clock input/output timing**

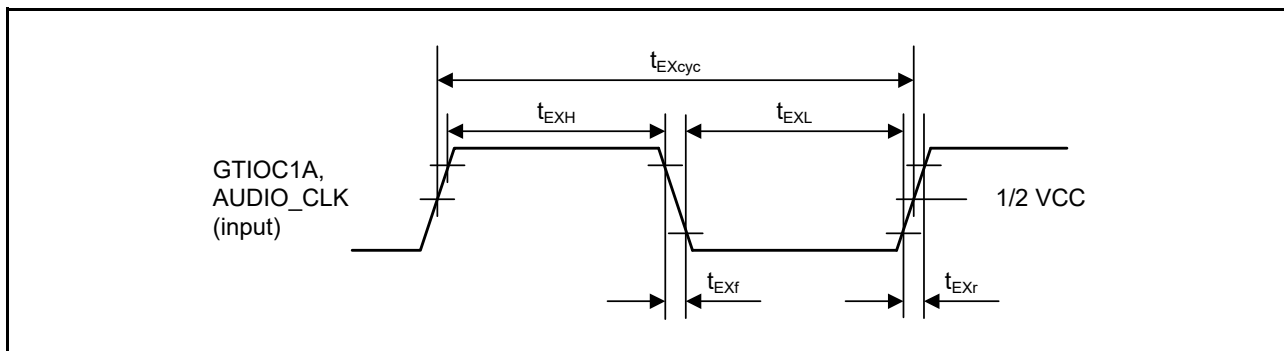


Figure 2.59 Clock input timing

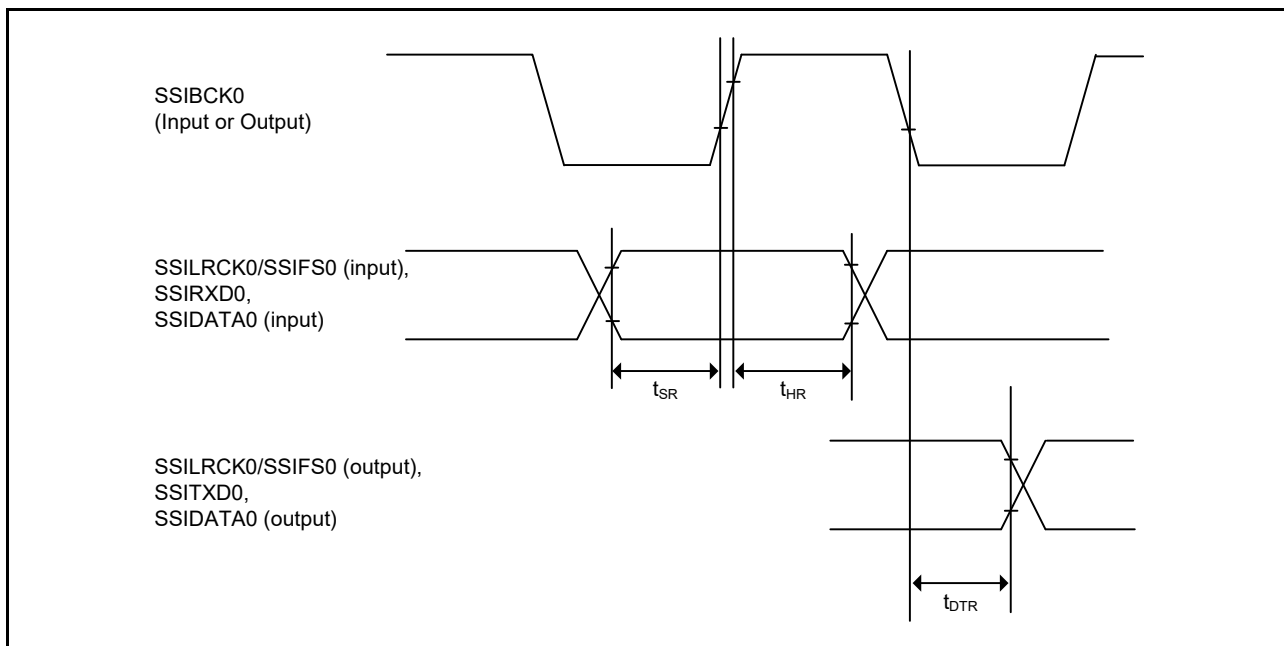


Figure 2.60 SSIE data transmit and receive timing when SSICR.BCKP = 0

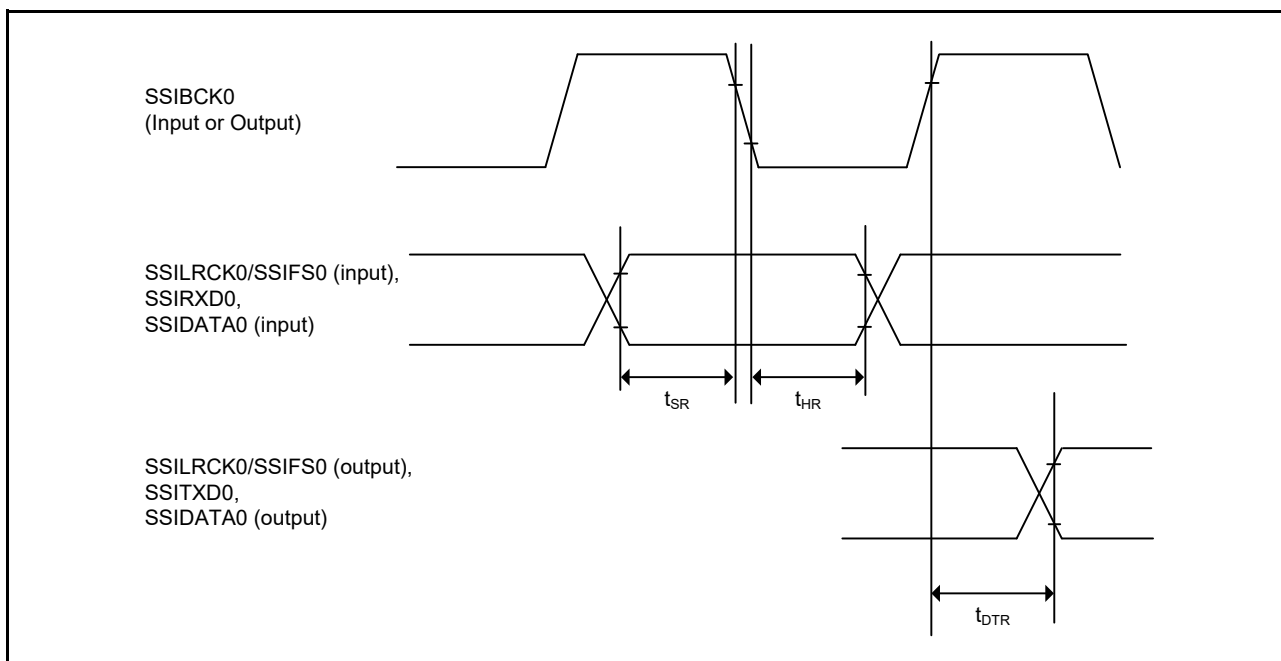


Figure 2.61 SSIE data transmit and receive timing when SSICR.BCKP = 1

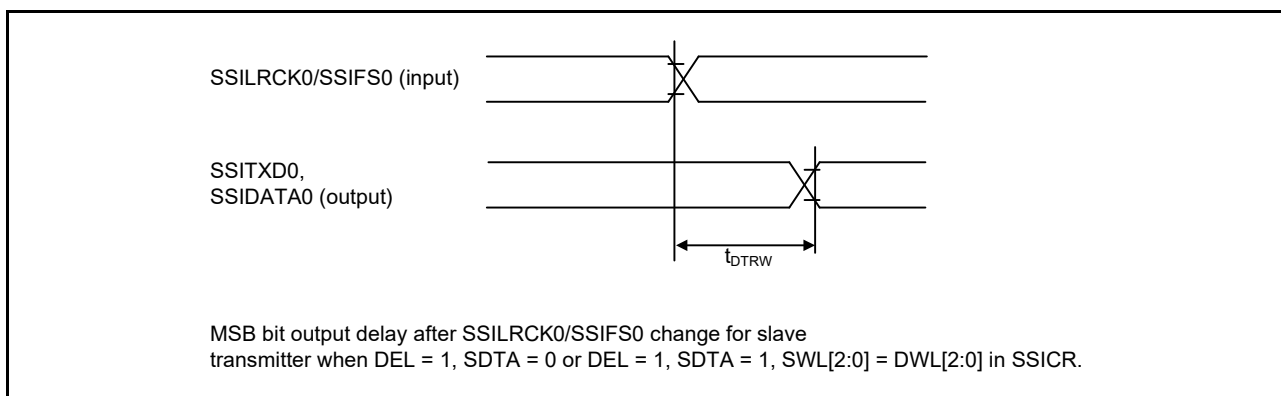


Figure 2.62 SSIE data output delay after SSILRCK0/SSIFS0 change

### 2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Clock duty ratio is 50%.

Parameter	Symbol	Min	Max	Unit	Test conditions*1
SDnCLK clock cycle	$T_{SDCYC}$	20	-	ns	Figure 2.63
SDnCLK clock high pulse width	$T_{SDWH}$	6.5	-	ns	
SDnCLK clock low pulse width	$T_{SDWL}$	6.5	-	ns	
SDnCLK clock rise time	$T_{SDLH}$	-	3	ns	
SDnCLK clock fall time	$T_{SDHL}$	-	3	ns	
SDnCMD/SDnDATm output data delay	$T_{SDODLY}$	-6	5	ns	
SDnCMD/SDnDATm input data setup	$T_{SDIS}$	4	-	ns	
SDnCMD/SDnDATm input data hold	$T_{SDIH}$	2	-	ns	

Note 1. Must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership.

For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

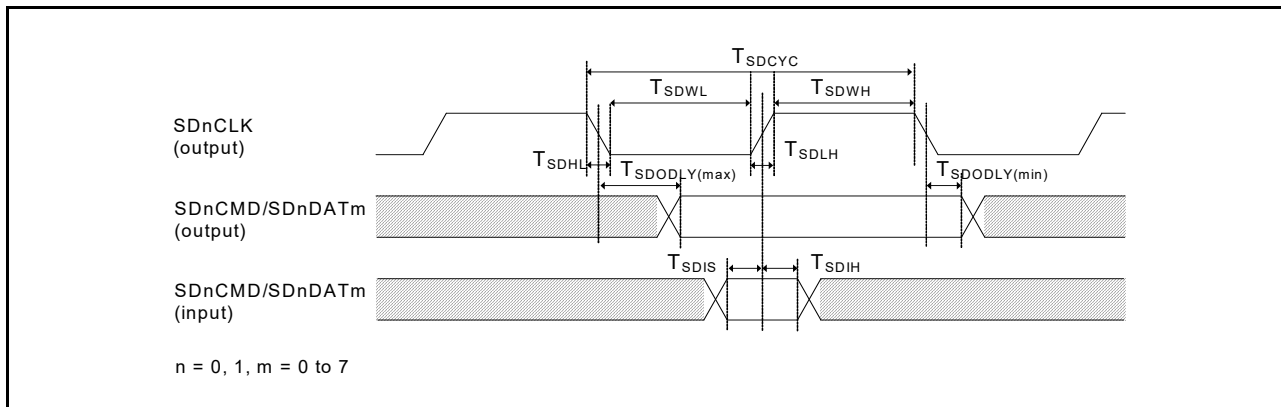


Figure 2.63 SD/MMC Host Interface signal timing

### 2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ET0\_MDC, ET0\_MDIO.

For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

ETHERC (MII): Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions*3	
ETHERC (RMII)	REF50CK0 cycle time	$T_{ck}$	20	-	ns	Figure 2.64 to Figure 2.67
	REF50CK0 frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK0 duty	-	35	65	%	
	REF50CK0 rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_XXXX*1 output delay	$T_{co}$	2.5	12.0	ns	
	RMII_XXXX*2 setup time	$T_{su}$	3	-	ns	
	RMII_XXXX*2 hold time	$T_{hd}$	1	-	ns	
	RMII_XXXX*1, *2 rise/fall time	$T_r/T_f$	0.5	4	ns	
	ET0_WOL output delay	$t_{WOLd}$	1	23.5	ns	Figure 2.68
ETHERC (MII)	ET0_TX_CLK cycle time	$t_{Tcyc}$	40	-	ns	-
	ET0_TX_EN output delay	$t_{TENd}$	1	20	ns	Figure 2.69
	ET0_ETXD0 to ET_ETXD3 output delay	$t_{MTDd}$	1	20	ns	
	ET0_CRS setup time	$t_{CRSs}$	10	-	ns	
	ET0_CRS hold time	$t_{CRSh}$	10	-	ns	
	ET0_COL setup time	$t_{COLs}$	10	-	ns	Figure 2.70
	ET0_COL hold time	$t_{COLh}$	10	-	ns	
	ET0_RX_CLK cycle time	$t_{TRcyc}$	40	-	ns	-
	ET0_RX_DV setup time	$t_{RDVs}$	10	-	ns	Figure 2.71
	ET0_RX_DV hold time	$t_{RDVh}$	10	-	ns	
	ET0_ERXD0 to ET_ERXD3 setup time	$t_{MRDs}$	10	-	ns	
	ET0_ERXD0 to ET_ERXD3 hold time	$t_{MRDh}$	10	-	ns	
	ET0_RX_ER setup time	$t_{RERs}$	10	-	ns	Figure 2.72
	ET0_RX_ER hold time	$t_{RESh}$	10	-	ns	
	ET0_WOL output delay	$t_{WOLd}$	1	23.5	ns	Figure 2.73

Note 1. RMII\_TXD\_EN, RMII\_TXD1, RMII\_TXD0.

Note 2. RMII\_CRS\_DV, RMII\_RXD1, RMII\_RXD0, RMII\_RX\_ER.

Note 3. The following pins must use pins that have a letter appended to their name, for instance “\_A”, “\_B”, to indicate group membership. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group.  
 REF50CK0\_A, REF50CK0\_B, RMII0\_xxxx\_A, RMII0\_xxxx\_B.

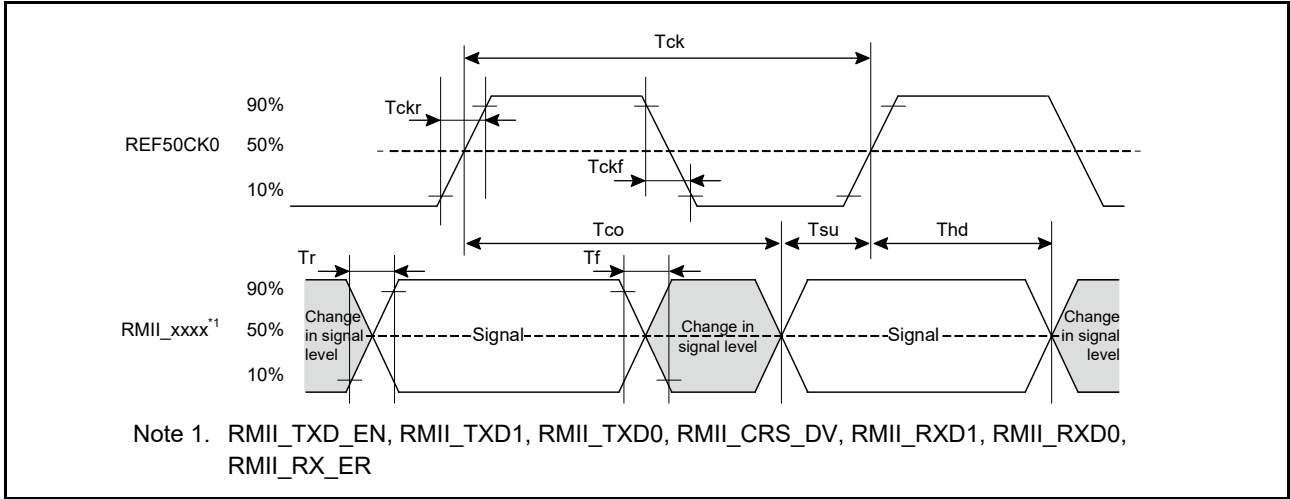


Figure 2.64 REF50CK0 and RMII signal timing

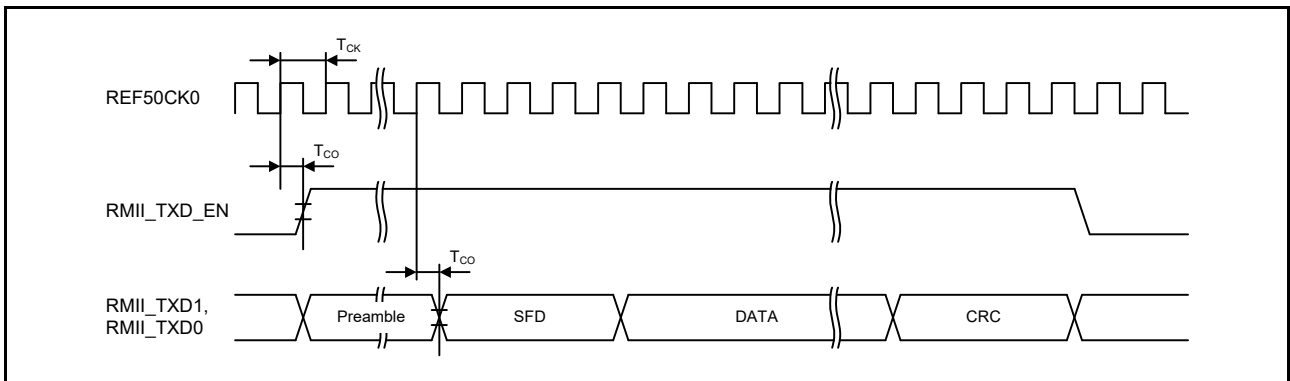


Figure 2.65 RMII transmission timing

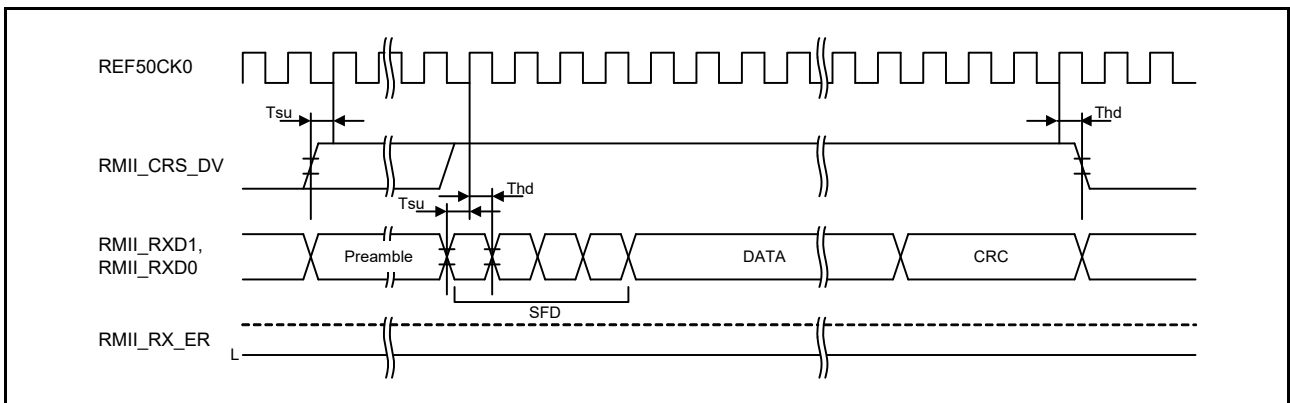


Figure 2.66 RMII reception timing in normal operation

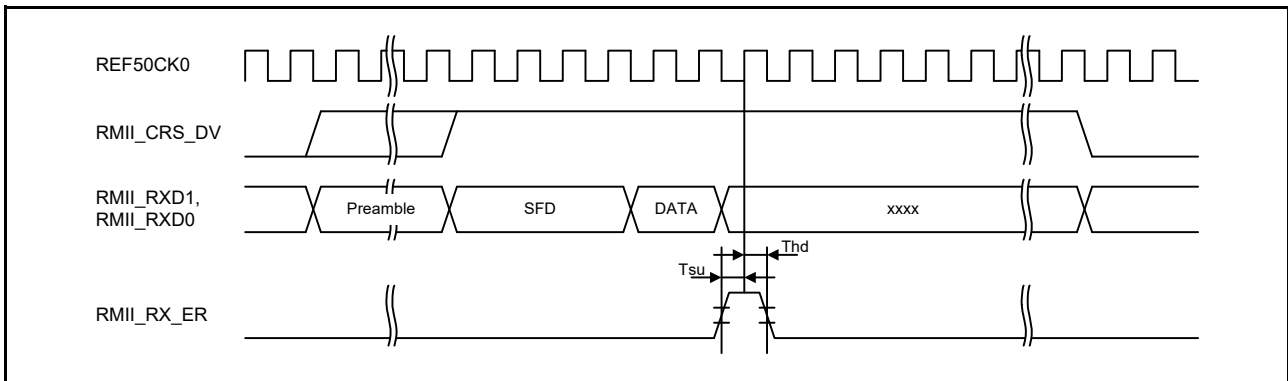


Figure 2.67 RMI reception timing when an error occurs

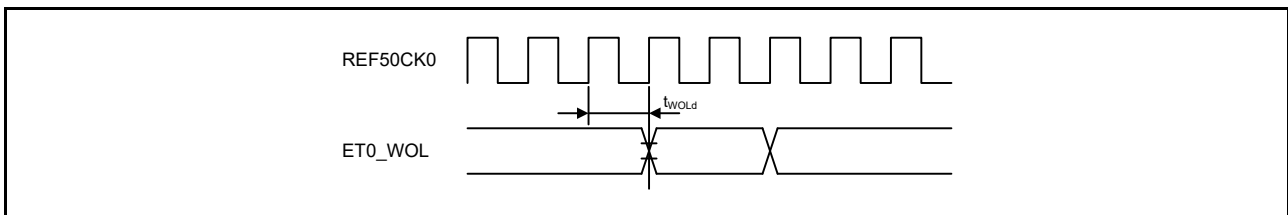


Figure 2.68 WOL output timing for RMI

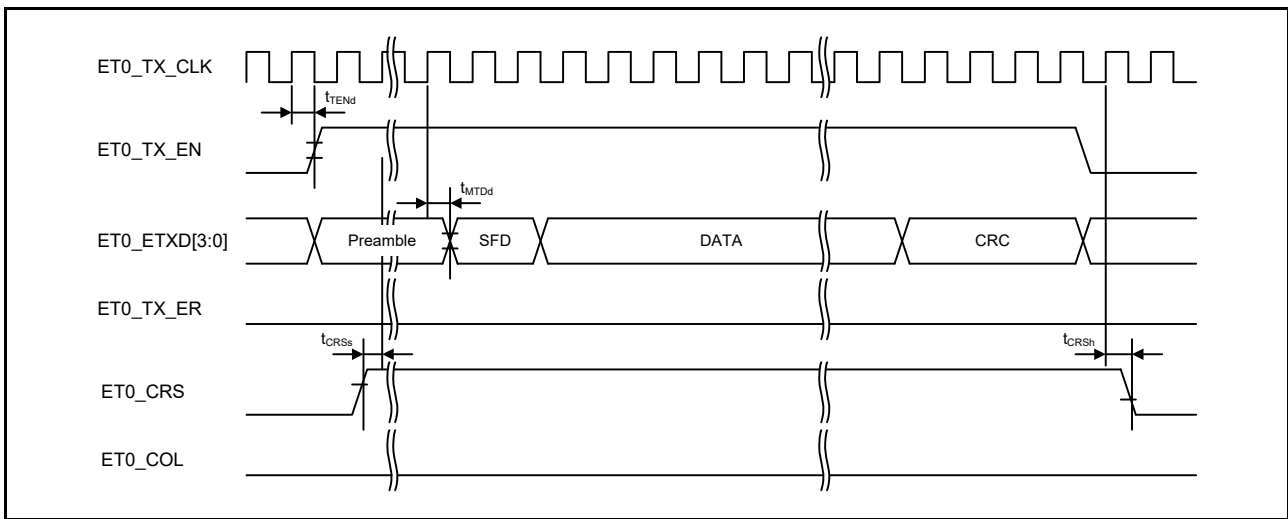


Figure 2.69 MII transmission timing in normal operation

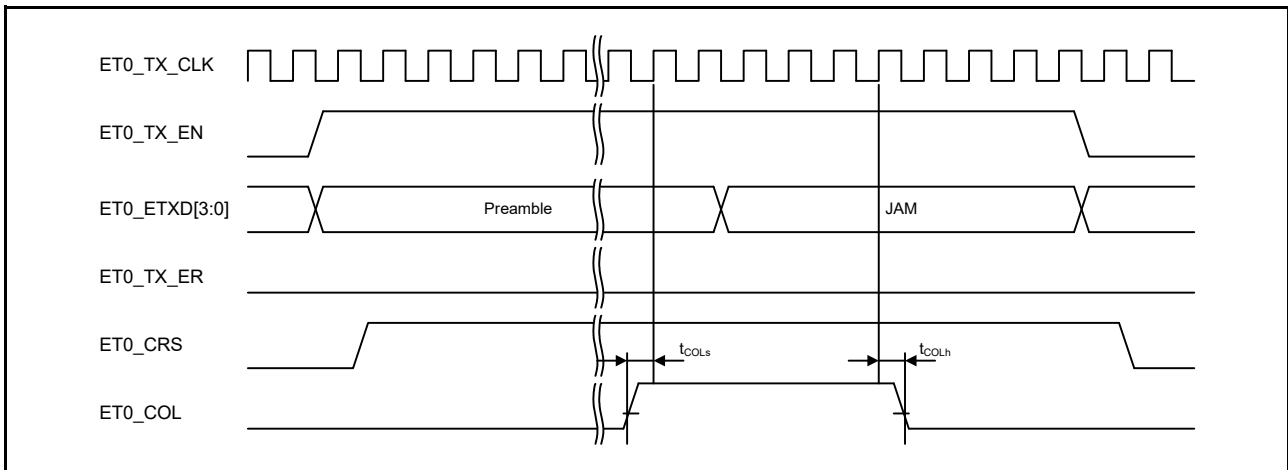


Figure 2.70 MII transmission timing when a conflict occurs

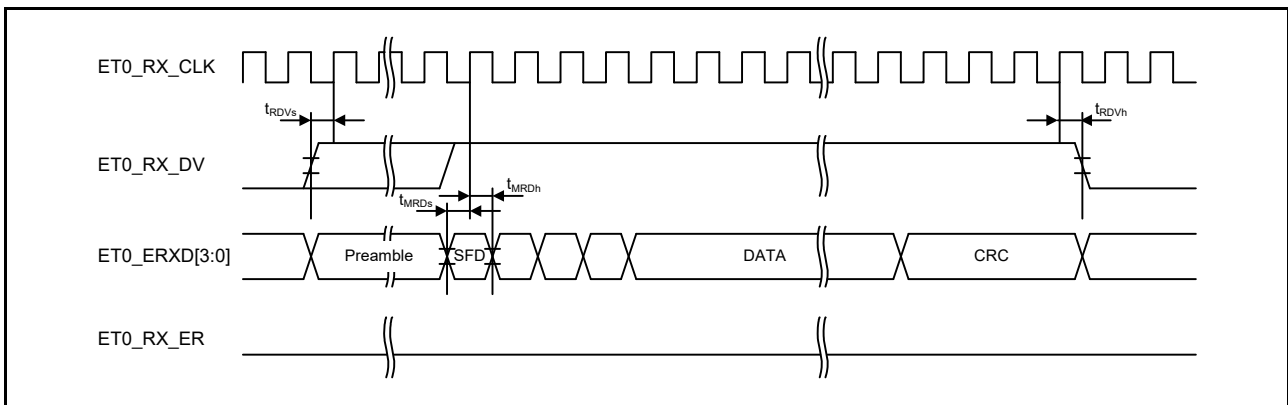


Figure 2.71 MII reception timing in normal operation

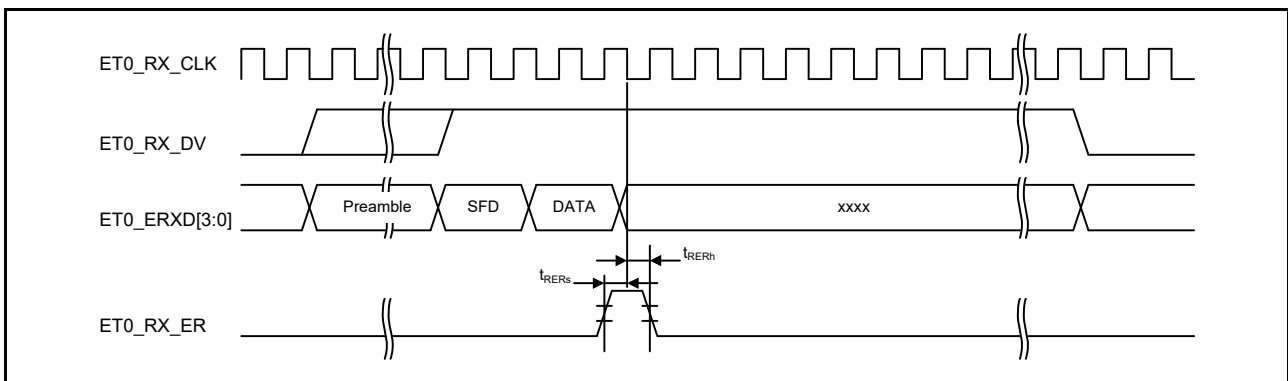


Figure 2.72 MII reception timing when an error occurs

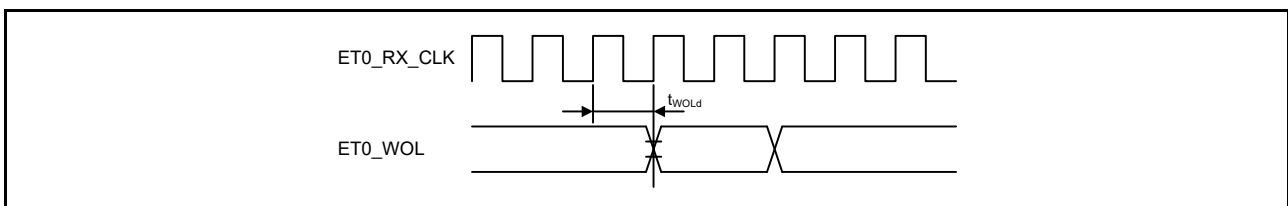


Figure 2.73 WOL output timing for MII

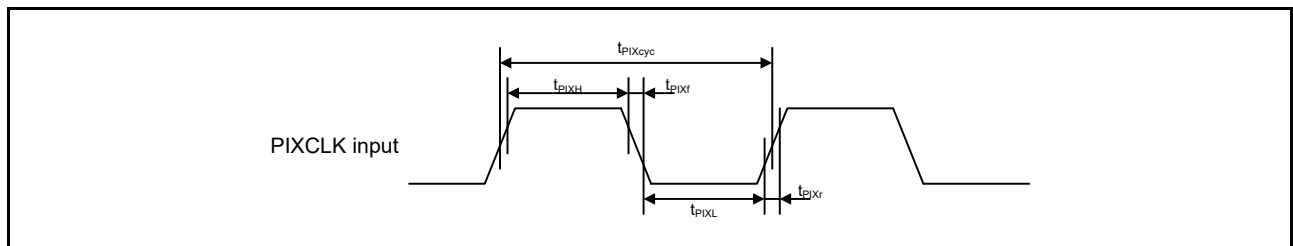
### 2.3.17 PDC Timing

**Table 2.32 PDC timing**

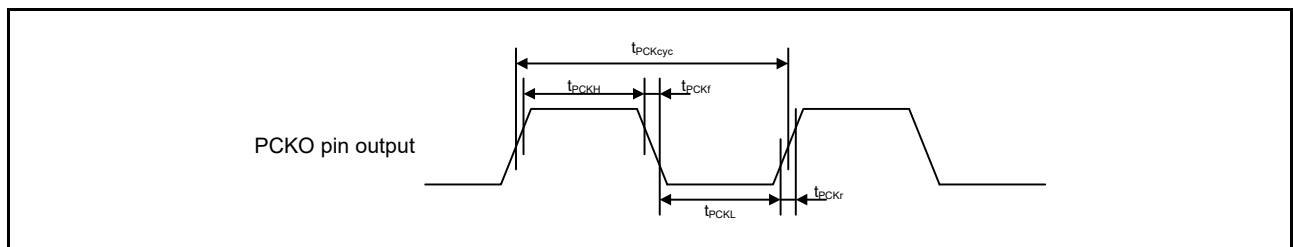
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.  
 Output load conditions:  $V_{OH} = V_{CC} \times 0.5$ ,  $V_{OL} = V_{CC} \times 0.5$ ,  $C = 30$  pF

Parameter	Symbol	Min	Max	Unit	Test conditions	
PDC	PIXCLK input cycle time	$t_{PIXcyc}$	37	-	ns	Figure 2.74
	PIXCLK input high pulse width	$t_{PIXH}$	10	-	ns	
	PIXCLK input low pulse width	$t_{PIXL}$	10	-	ns	
	PIXCLK rise time	$t_{PIXr}$	-	5	ns	
	PIXCLK fall time	$t_{PIXf}$	-	5	ns	
PDC	PCKO output cycle time	$t_{PCKcyc}$	$2 \times t_{PBcyc}$	-	ns	Figure 2.75
	PCKO output high pulse width	$t_{PCKH}$	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	-	ns	
	PCKO output low pulse width	$t_{PCKL}$	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	-	ns	
	PCKO rise time	$t_{PCKr}$	-	5	ns	
	PCKO fall time	$t_{PCKf}$	-	5	ns	
PDC	VSYNV/HSYNC input setup time	$t_{SYNCS}$	10	-	ns	Figure 2.76
	VSYNV/HSYNC input hold time	$t_{SYNCH}$	5	-	ns	
	PIXD input setup time	$t_{PIXDS}$	10	-	ns	
	PIXD input hold time	$t_{PIXDH}$	5	-	ns	

Note 1.  $t_{PBcyc}$ : PCLKB cycle.



**Figure 2.74 PDC input clock timing**



**Figure 2.75 PDC output clock timing**

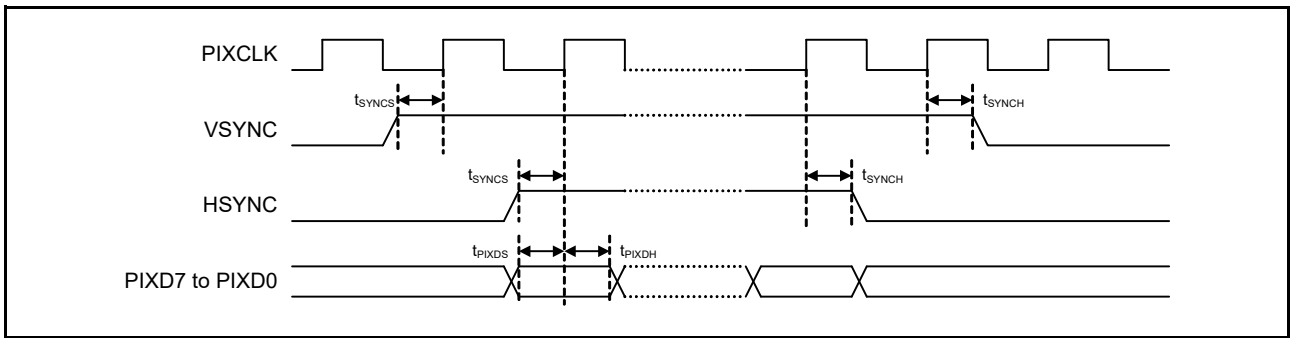


Figure 2.76 PDC AC timing

## 2.4 USB Characteristics

### 2.4.1 USBFS Timing

**Table 2.33 USBFS low-speed characteristics for host only (USB\_DP and USB\_DM pin characteristics)**  
 Conditions:  $V_{CC} = AV_{CC0} = V_{CC\_USB} = V_{BATT} = 3.0$  to  $3.6V$ ,  $2.7 \leq V_{REFH0}/V_{REFH} \leq AV_{CC0}$ ,  $U_{CLK} = 48$  MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	$V_{IH}$	2.0	-	-	V	-
	Input low voltage	$V_{IL}$	-	-	0.8	V	-
	Differential input sensitivity	$V_{DI}$	0.2	-	-	V	USB_DP - USB_DM
	Differential common-mode range	$V_{CM}$	0.8	-	2.5	V	-
Output characteristics	Output high voltage	$V_{OH}$	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	$V_{OL}$	0.0	-	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	$V_{CRS}$	1.3	-	2.0	V	Figure 2.77
	Rise time	$t_{LR}$	75	-	300	ns	$t_{LR}/t_{LF}$
	Fall time	$t_{LF}$	75	-	300	ns	
	Rise/fall time ratio	$t_{LR}/t_{LF}$	80	-	125	%	
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	$R_{pd}$	14.25	-	24.80	k $\Omega$	-

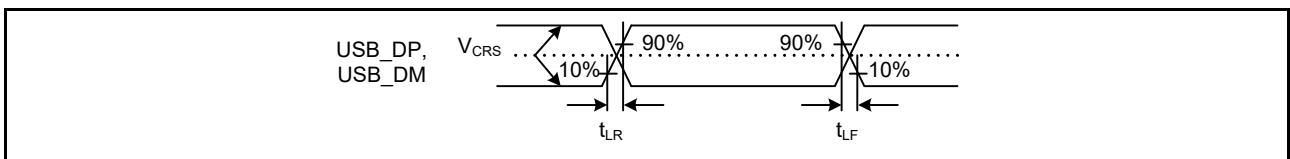


Figure 2.77 USB\_DP and USB\_DM output timing in low-speed mode

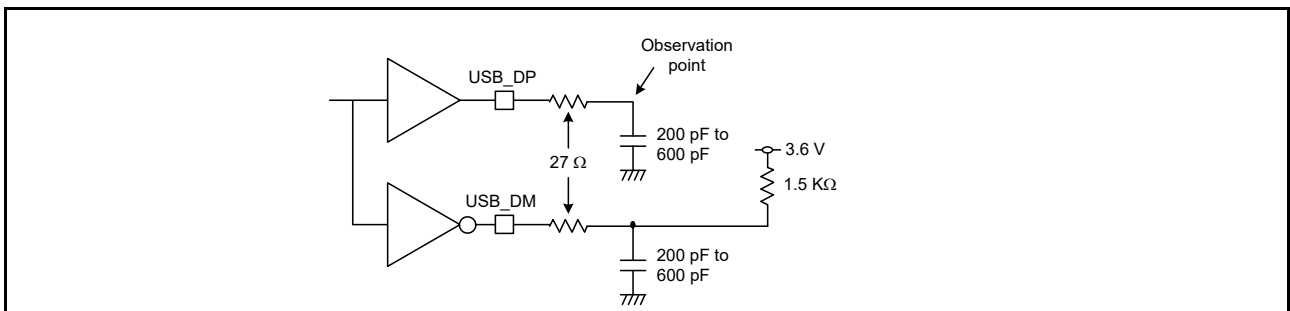
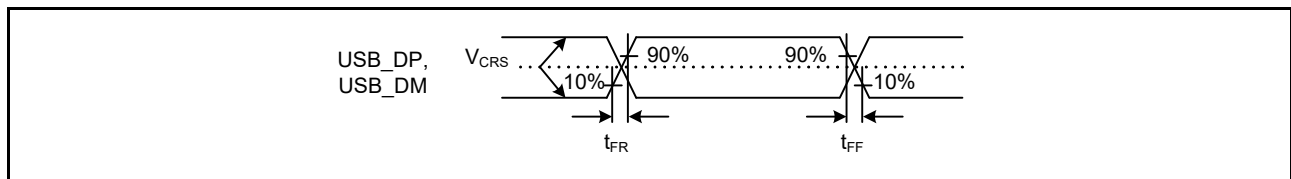


Figure 2.78 Test circuit in low-speed mode

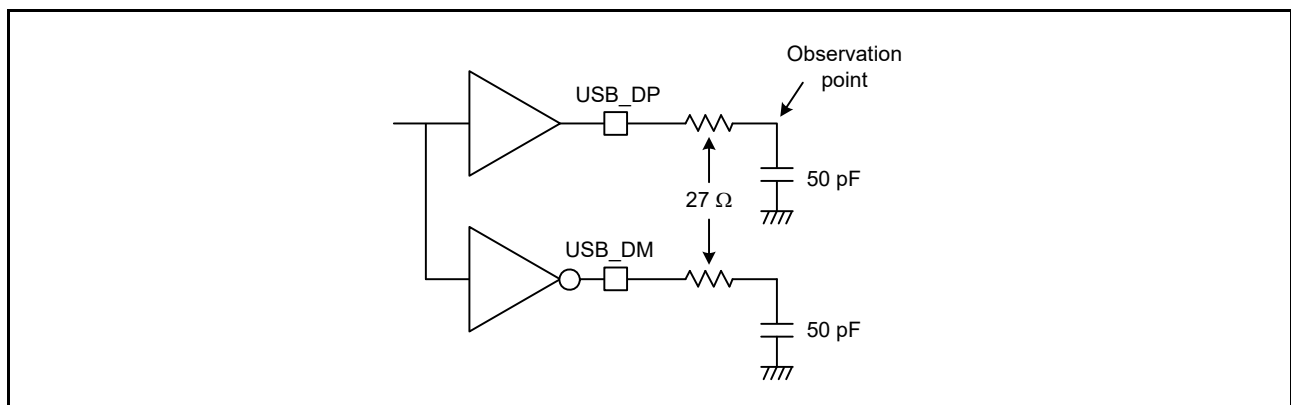
**Table 2.34 USBFS full-speed characteristics (USB\_DP and USB\_DM pin characteristics)**

Conditions:  $V_{CC} = AV_{CC0} = V_{CC\_USB} = V_{BATT} = 3.0$  to  $3.6$  V,  $2.7 \leq V_{REFH0}/V_{REFH} \leq AV_{CC0}$ ,  $U_{CLK} = 48$  MHz

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	$V_{IH}$	2.0	-	-	V	-
	Input low voltage	$V_{IL}$	-	-	0.8	V	-
	Differential input sensitivity	$V_{DI}$	0.2	-	-	V	$ USB\_DP - USB\_DM $
	Differential common-mode range	$V_{CM}$	0.8	-	2.5	V	-
Output characteristics	Output high voltage	$V_{OH}$	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	$V_{OL}$	0.0	-	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	$V_{CRS}$	1.3	-	2.0	V	Figure 2.79
	Rise time	$t_{LR}$	4	-	20	ns	
	Fall time	$t_{LF}$	4	-	20	ns	
	Rise/fall time ratio	$t_{LR} / t_{LF}$	90	-	111.11	%	$t_{FR} / t_{FF}$
	Output resistance	$Z_{DRV}$	28	-	44	$\Omega$	USBFS: $R_s = 27 \Omega$ included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	$R_{pu}$	0.900	-	1.575	k $\Omega$	During idle state
		$R_{pu}$	1.425	-	3.090	k $\Omega$	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	$R_{pd}$	14.25	-	24.80	k $\Omega$	-



**Figure 2.79 USB\_DP and USB\_DM output timing in full-speed mode**



**Figure 2.80 Test circuit in full-speed mode**

## 2.5 ADC12 Characteristics

**Table 2.35 A/D conversion characteristics for unit 0 (1 of 2)**

Conditions:  $P_{CLKC} = 1$  to 60 MHz

Parameter	Min	Typ	Max	Unit	Test conditions
Frequency	1	-	60	MHz	-
Analog input capacitance	-	-	30	pF	-

**Table 2.35 A/D conversion characteristics for unit 0 (2 of 2)**

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	<ul style="list-style-type: none"> <li>Sampling of channel-dedicated sample-and-hold circuits in 24 states</li> <li>Sampling in 15 states</li> </ul>
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
Dynamic range		0.25	-	VREFH0 - 0.25	V	-	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN003 to AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

The use of PORT0 as digital outputs is not allowed when the 12-bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see [Table 2.37](#).

**Table 2.36 A/D conversion characteristics for unit 1**

Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use*3 (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	<ul style="list-style-type: none"> <li>Sampling of channel-dedicated sample-and-hold circuits in 24 states</li> <li>Sampling in 15 states</li> </ul>
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
Dynamic range			0.25	-	VREFH - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN105 to AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116 to AN118)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

The use of PORT0 as digital outputs is not allowed when the 12-bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see [Table 2.37](#).

**Table 2.37 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit0 and unit1**

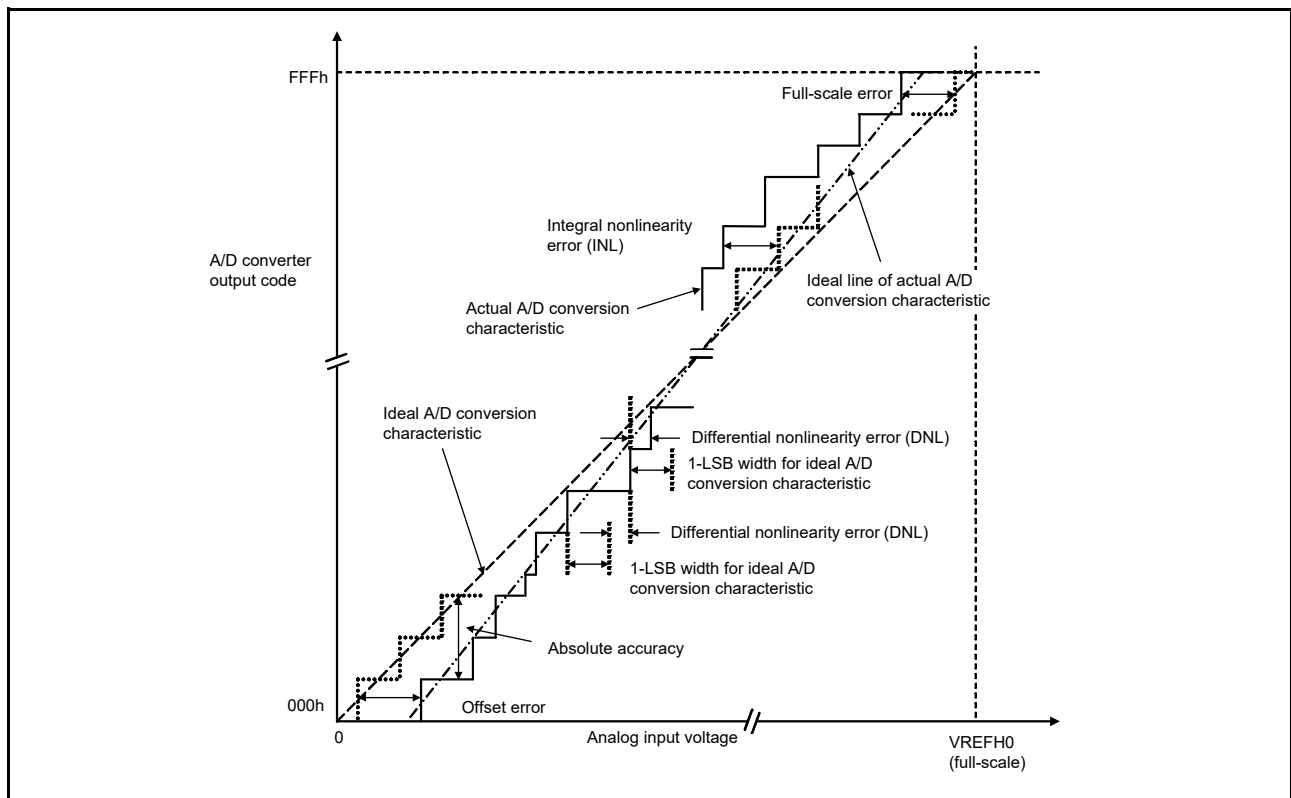
Conditions: PCLKC = 30/60 MHz

Parameter	Min	Typ	Max	Test conditions	
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	<ul style="list-style-type: none"> <li>• PCLKC = 60 MHz</li> <li>• Sampling in 15 states</li> </ul>
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	<ul style="list-style-type: none"> <li>• PCLKC = 30 MHz</li> <li>• Sampling in 7 states</li> </ul>
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit0 and unit1, setting the ADSHMSR.SHMD bit to 1 is recommended.

**Table 2.38 A/D internal reference voltage characteristics**

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	µs	-



**Figure 2.81 Illustration of ADC12 characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage  $V_{REFH0} = 3.072$  V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of  $\pm 5$  LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

## 2.6 DAC12 Characteristics

**Table 2.39 D/A conversion characteristics**

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	$\pm 24$	LSB	Resistive load 2 M $\Omega$
INL	-	$\pm 2.0$	$\pm 8.0$	LSB	Resistive load 2 M $\Omega$
DNL	-	$\pm 1.0$	$\pm 2.0$	LSB	-
Output impedance	-	8.5	-	k $\Omega$	-
Conversion time	-	-	3.0	$\mu$ s	Resistive load 2 M $\Omega$ , Capacitive load 20 pF
Output voltage range	0	-	$V_{REFH}$	V	-
With output amplifier					
INL	-	$\pm 2.0$	$\pm 4.0$	LSB	-
DNL	-	$\pm 1.0$	$\pm 2.0$	LSB	-
Conversion time	-	-	4.0	$\mu$ s	-
Resistive load	5	-	-	k $\Omega$	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	$V_{REFH} - 0.2$	V	-

## 2.7 TSN Characteristics

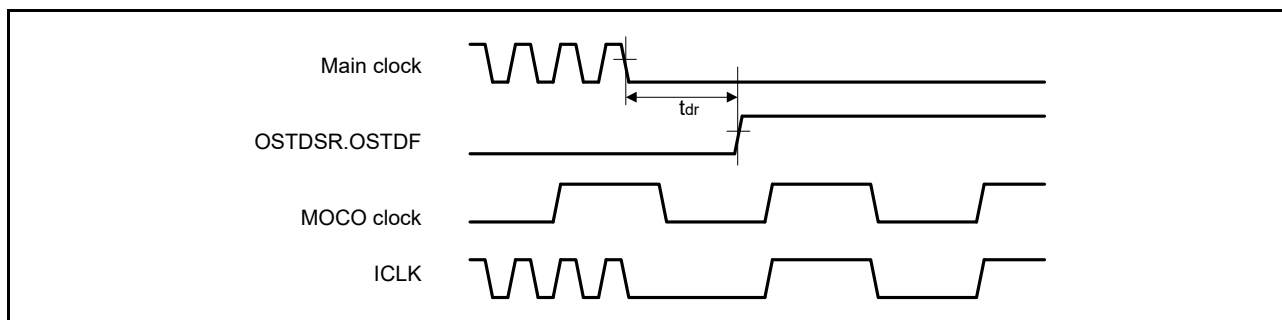
**Table 2.40 TSN characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t <sub>START</sub>	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

## 2.8 OSC Stop Detect Characteristics

**Table 2.41 Oscillation stop detection circuit characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t <sub>dr</sub>	-	-	1	ms	Figure 2.82



**Figure 2.82 Oscillation stop detection timing**

## 2.9 POR and LVD Characteristics

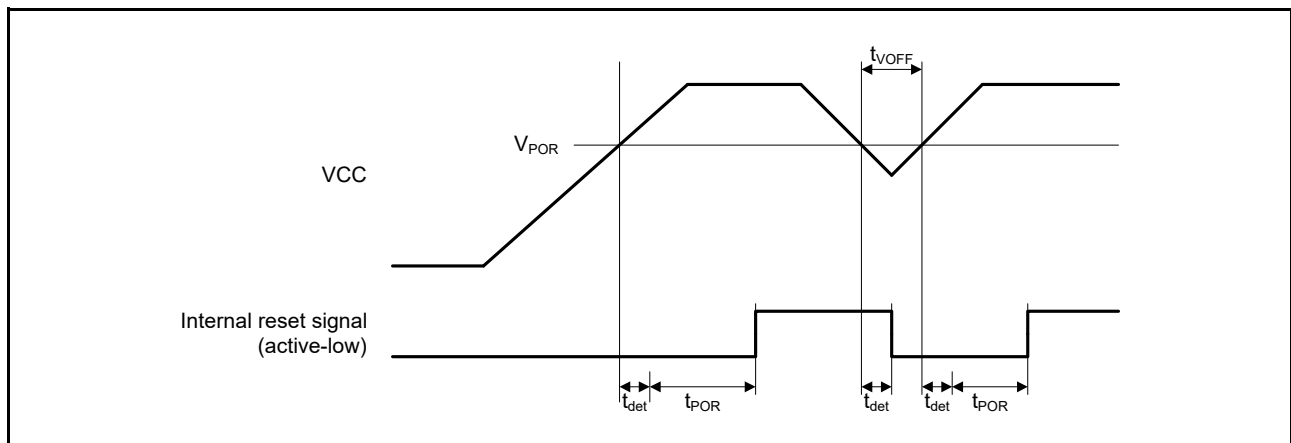
**Table 2.42 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)**

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCT[1:0] = 00b or 01b	V <sub>POR</sub>	2.5	2.6	2.7	V	Figure 2.83
		DPSBYCR.DEEPCT[1:0] = 11b		1.8	2.25	2.7		
Voltage detection circuit (LVD0)		V <sub>det0_1</sub>	2.84	2.94	3.04		Figure 2.84	
		V <sub>det0_2</sub>	2.77	2.87	2.97			
		V <sub>det0_3</sub>	2.70	2.80	2.90			
Voltage detection circuit (LVD1)		V <sub>det1_1</sub>	2.89	2.99	3.09		Figure 2.85	
		V <sub>det1_2</sub>	2.82	2.92	3.02			
		V <sub>det1_3</sub>	2.75	2.85	2.95			
Voltage detection circuit (LVD2)		V <sub>det2_1</sub>	2.89	2.99	3.09		Figure 2.86	
		V <sub>det2_2</sub>	2.82	2.92	3.02			
		V <sub>det2_3</sub>	2.75	2.85	2.95			

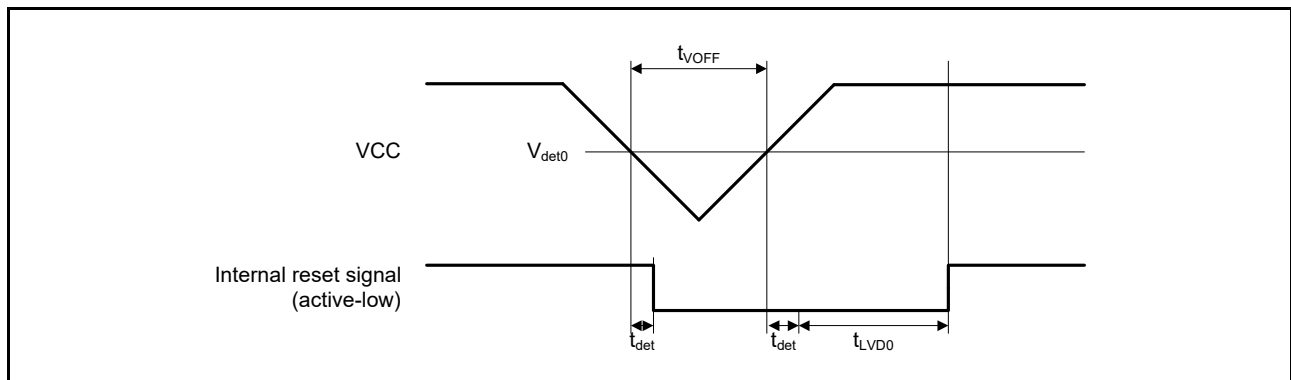
**Table 2.42 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Internal reset time	Power-on reset time	$t_{POR}$	-	4.5	-	ms
	LVD0 reset time	$t_{LVD0}$	-	0.51	-	
	LVD1 reset time	$t_{LVD1}$	-	0.38	-	
	LVD2 reset time	$t_{LVD2}$	-	0.38	-	
Minimum VCC down time*1	$t_{VOFF}$	200	-	-	$\mu$ s	Figure 2.83, Figure 2.84
Response delay	$t_{det}$	-	-	200	$\mu$ s	Figure 2.83 to Figure 2.86
LVD operation stabilization time (after LVD is enabled)	$t_{d(E-A)}$	-	-	10	$\mu$ s	Figure 2.85, Figure 2.86
Hysteresis width (LVD1 and LVD2)	$V_{LVH}$	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels  $V_{POR}$ ,  $V_{det1}$ , and  $V_{det2}$  for POR and LVD.



**Figure 2.83 Power-on reset timing**



**Figure 2.84 Voltage detection circuit timing ( $V_{det0}$ )**

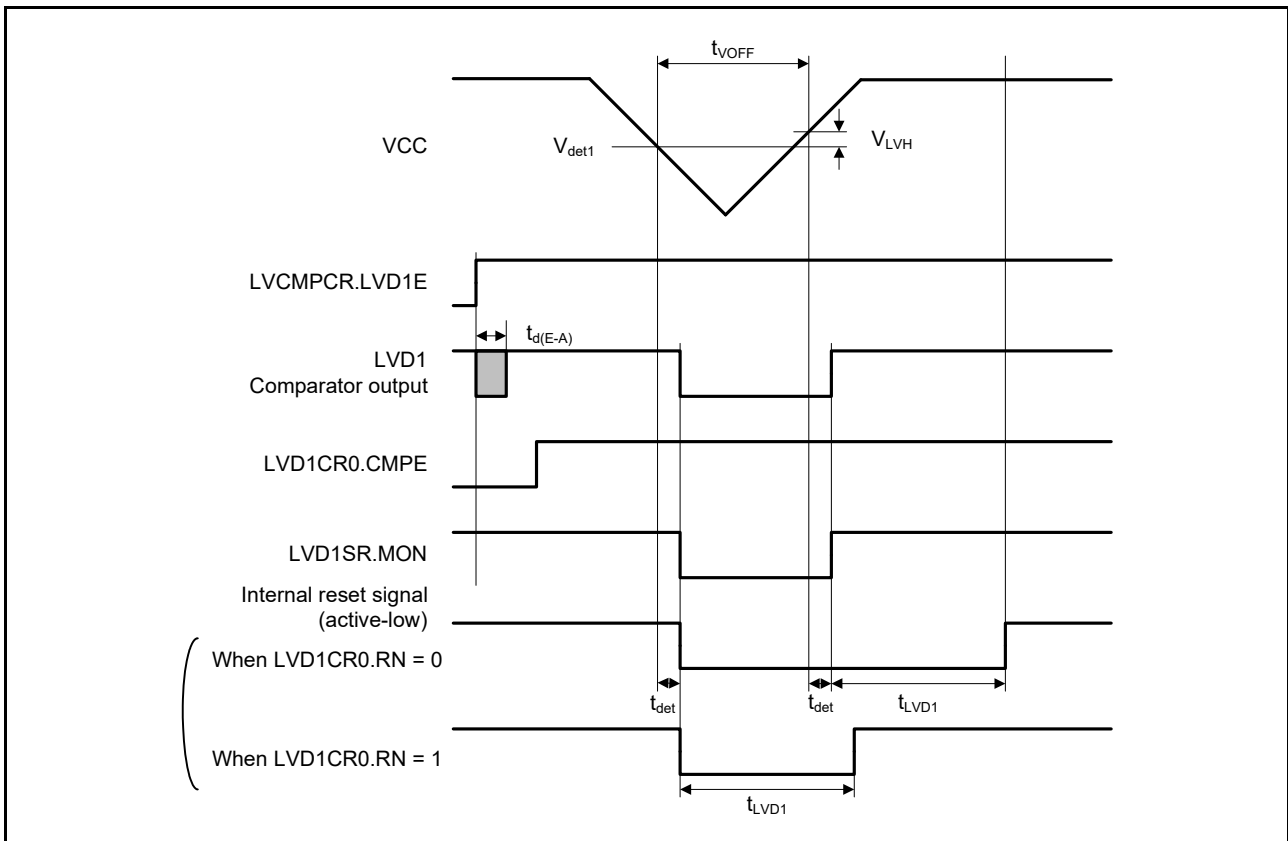


Figure 2.85 Voltage detection circuit timing ( $V_{det1}$ )

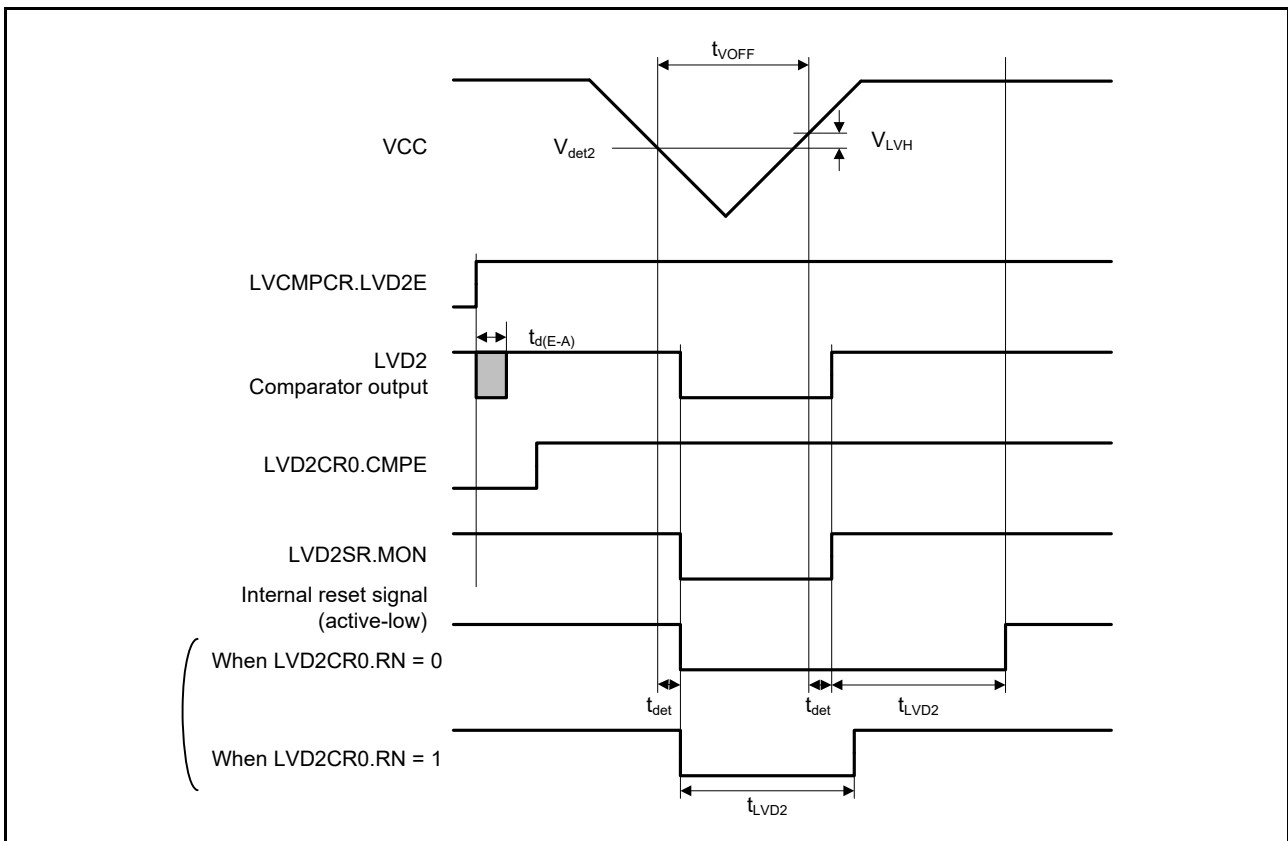


Figure 2.86 Voltage detection circuit timing ( $V_{det2}$ )

### 2.10 VBATT Characteristics

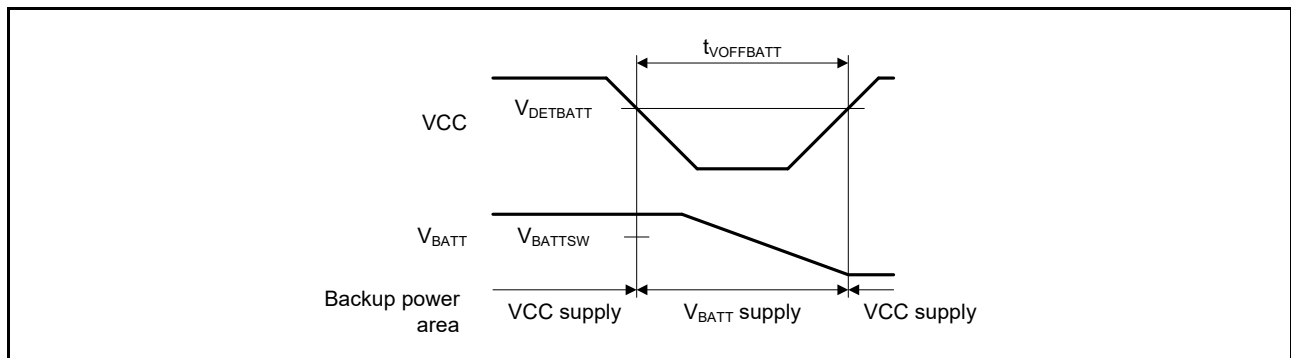
**Table 2.43 Battery backup function characteristics**

Conditions: VCC = AVCC0 = VCC\_USB = 2.7 to 3.6 V,  $2.7 \leq VREFH0/VREFH \leq AVCC0$ , VBATT = 1.65 to 3.6 V\*1

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	V <sub>DETBATT</sub>	2.50	2.60	2.70	V	Figure 2.87
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V <sub>BATTSW</sub>	2.70	-	-	V	
VCC-off period for starting power supply switching	t <sub>VOFFBATT</sub>	200	-	-	μs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup (V<sub>DETBATT</sub>).

Note 1. Low CL crystal cannot be used below VBATT = 1.8 V.



**Figure 2.87 Battery backup function characteristics**

### 2.11 CTSU Characteristics

**Table 2.44 CTSU characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C <sub>tscap</sub>	9	10	11	nF	-
TS pin capacitive load	C <sub>base</sub>	-	-	50	pF	-
Permissible output high current	ΣI <sub>oH</sub>	-	-	-40	mA	When the mutual capacitance method is applied

### 2.12 ACPHPS Characteristics

**Table 2.45 ACPHPS characteristics**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	V <sub>I</sub>	0	-	AVCC0	V	-
Output delay*1	T <sub>d</sub>	-	50	100	ns	V <sub>I</sub> = VREF ± 100 mV
Internal reference voltage	V <sub>ref</sub>	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

## 2.13 Flash Memory Characteristics

### 2.13.1 Code Flash Memory Characteristics

**Table 2.46 Code flash memory characteristics**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time $N_{PEC} \leq 100$ times	128-byte	$t_{P128}$	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	$t_{P8K}$	-	49	176	-	22	80	ms	
	32-KB	$t_{P32K}$	-	194	704	-	88	320	ms	
Programming time $N_{PEC} > 100$ times	128-byte	$t_{P128}$	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	$t_{P8K}$	-	60	212	-	27	96	ms	
	32-KB	$t_{P32K}$	-	234	848	-	106	384	ms	
Erasure time $N_{PEC} \leq 100$ times	8-KB	$t_{E8K}$	-	78	216	-	43	120	ms	
	32-KB	$t_{E32K}$	-	283	864	-	157	480	ms	
Erasure time $N_{PEC} > 100$ times	8-KB	$t_{E8K}$	-	94	260	-	52	144	ms	
	32-KB	$t_{E32K}$	-	341	1040	-	189	576	ms	
Reprogramming/erase cycle*4		$N_{PEC}$	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		$t_{SPD}$	-	-	264	-	-	120	μs	
First suspend delay during erasure in suspend priority mode		$t_{SESD1}$	-	-	216	-	-	120	μs	
Second suspend delay during erasure in suspend priority mode		$t_{SESD2}$	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		$t_{SEED}$	-	-	1.7	-	-	1.7	ms	
Forced stop command		$t_{FD}$	-	-	32	-	-	20	μs	
Data hold time*2		$t_{DRP}$	10*2, *3	-	-	10*2, *3	-	-	Years	Ta = +85°C
			30*2, *3	-	-	30*2, *3	-	-		

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

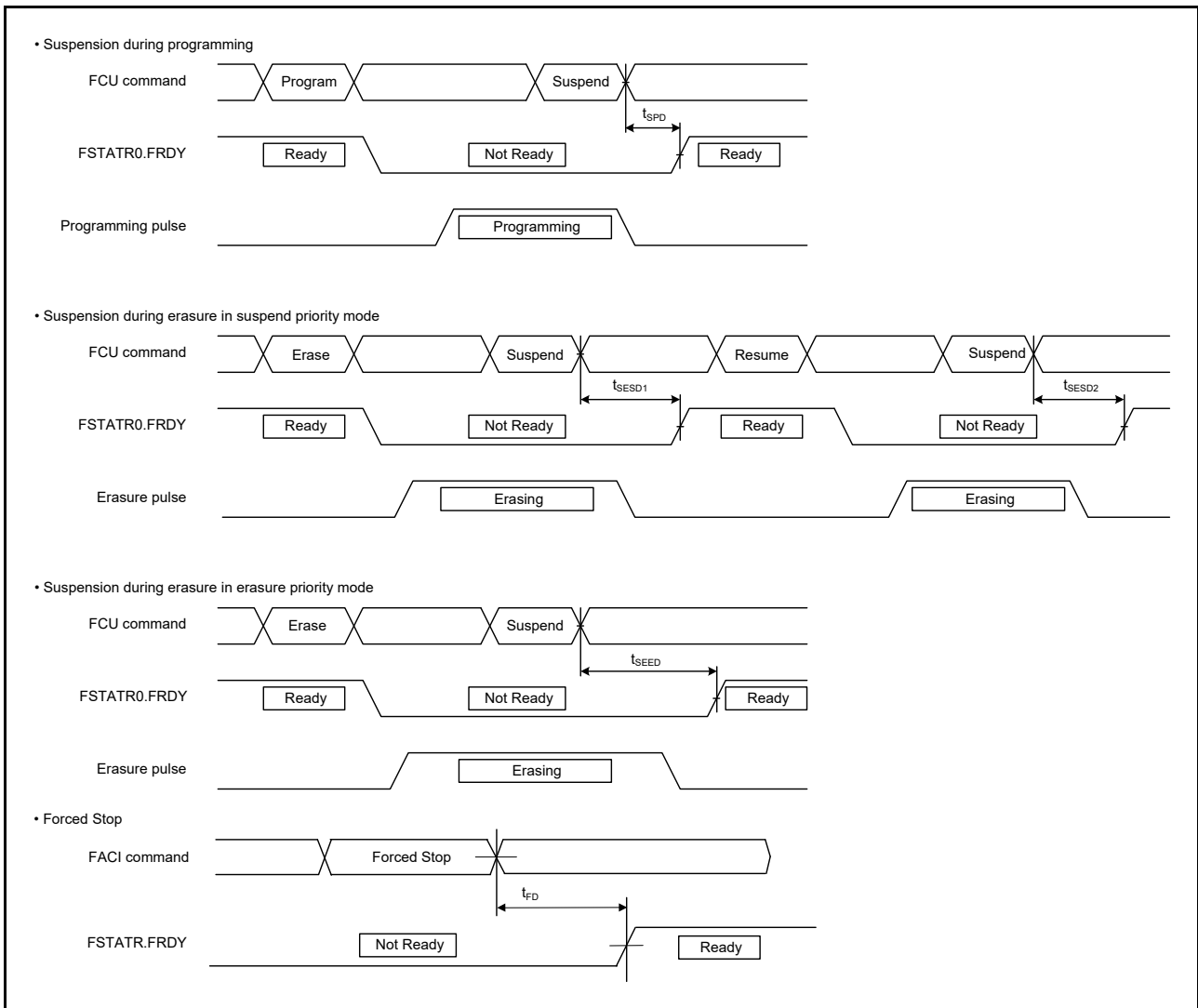


Figure 2.88 Suspension and forced stop timing for flash memory programming and erasure

## 2.13.2 Data Flash Memory Characteristics

**Table 2.47 Data flash memory characteristics**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t <sub>DP4</sub>	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t <sub>DP8</sub>	-	0.38	4.0	-	0.17	1.8		
	16-byte	t <sub>DP16</sub>	-	0.42	4.5	-	0.19	2.0		
Erasure time	64-byte	t <sub>DE64</sub>	-	3.1	18	-	1.7	10	ms	
	128-byte	t <sub>DE128</sub>	-	4.7	27	-	2.6	15		
	256-byte	t <sub>DE256</sub>	-	8.9	50	-	4.9	28		
Blank check time	4-byte	t <sub>DBC4</sub>	-	-	84	-	-	30	μs	
Reprogramming/erasure cycle*1		N <sub>DPEC</sub>	125000*2	-	-	125000*2	-	-	-	
Suspend delay during programming	4-byte	t <sub>DSPD</sub>	-	-	264	-	-	120	μs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t <sub>DSESD1</sub>	-	-	216	-	-	120	μs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t <sub>DSESD2</sub>	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t <sub>DSEED</sub>	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t <sub>FD</sub>	-	-	32	-	-	20	μs	
Data hold time*3		t <sub>DRP</sub>	10*3,*4	-	-	10*3,*4	-	-	Year	Ta = +85°C
			30*3,*4	-	-	30*3,*4	-	-		

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 4. This result is obtained from reliability testing.

## 2.14 Boundary Scan

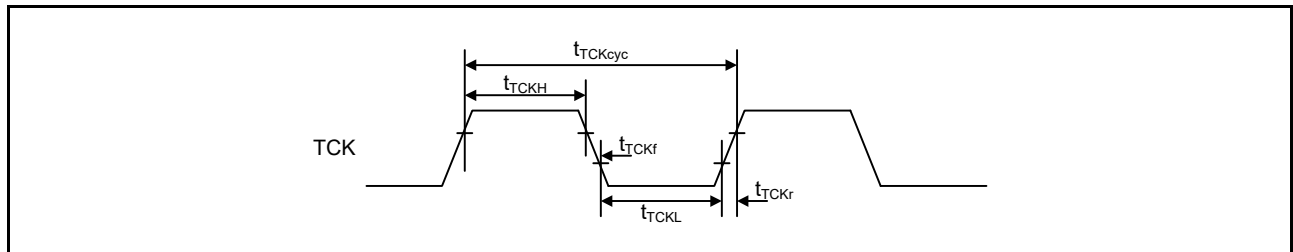
**Table 2.48 Boundary scan characteristics (1 of 2)**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t <sub>TCKcyc</sub>	100	-	-	ns	Figure 2.89
TCK clock high pulse width	t <sub>TCKH</sub>	45	-	-	ns	
TCK clock low pulse width	t <sub>TCKL</sub>	45	-	-	ns	
TCK clock rise time	t <sub>TCKr</sub>	-	-	5	ns	
TCK clock fall time	t <sub>TCKf</sub>	-	-	5	ns	

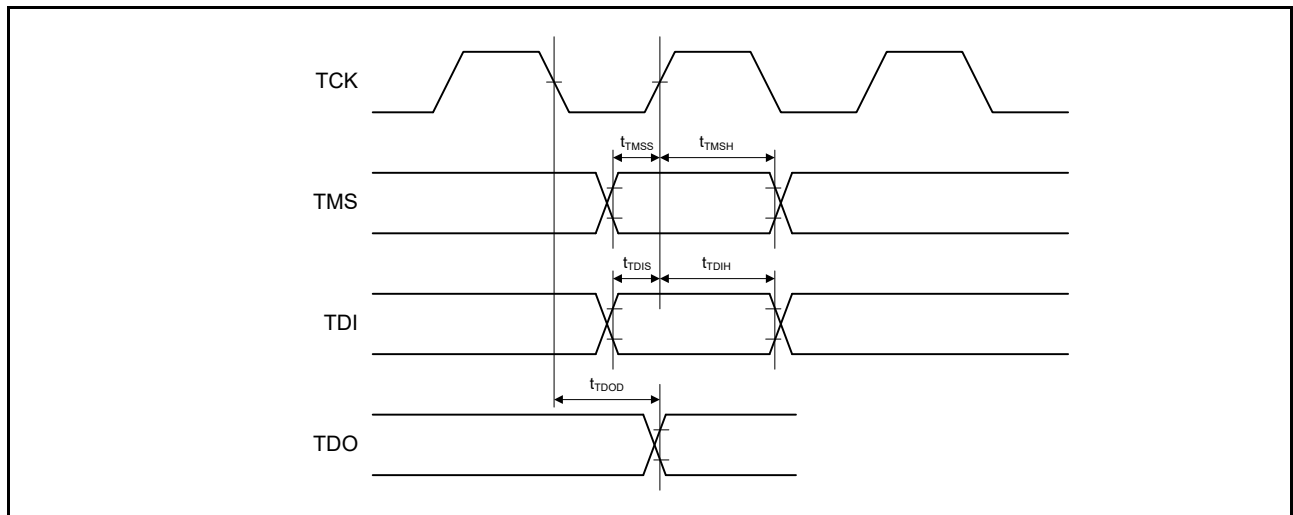
**Table 2.48 Boundary scan characteristics (2 of 2)**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	$t_{TMSS}$	20	-	-	ns	Figure 2.90
TMS hold time	$t_{TMSH}$	20	-	-	ns	
TDI setup time	$t_{TDIS}$	20	-	-	ns	
TDI hold time	$t_{TDIH}$	20	-	-	ns	
TDO data delay	$t_{TDOD}$	-	-	40	ns	
Boundary scan circuit startup time*1	$T_{BSSTUP}$	$t_{RESWP}$	-	-	-	Figure 2.91

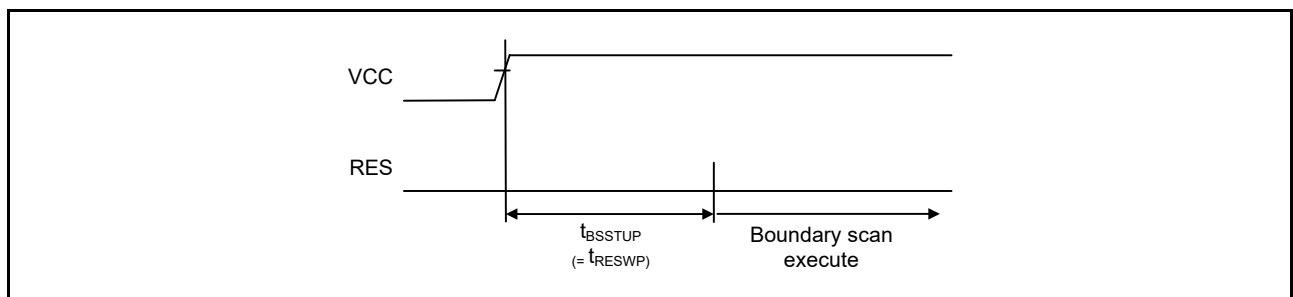
Note 1. Boundary scan does not function until the power-on reset becomes negative.



**Figure 2.89 Boundary scan TCK timing**



**Figure 2.90 Boundary scan input/output timing**

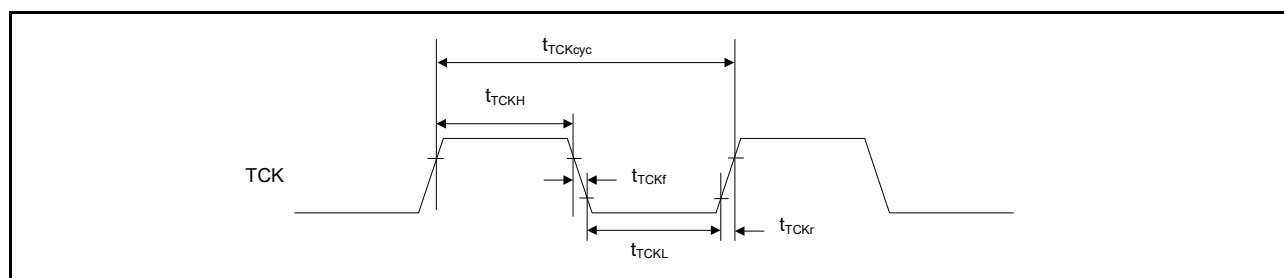


**Figure 2.91 Boundary scan circuit startup timing**

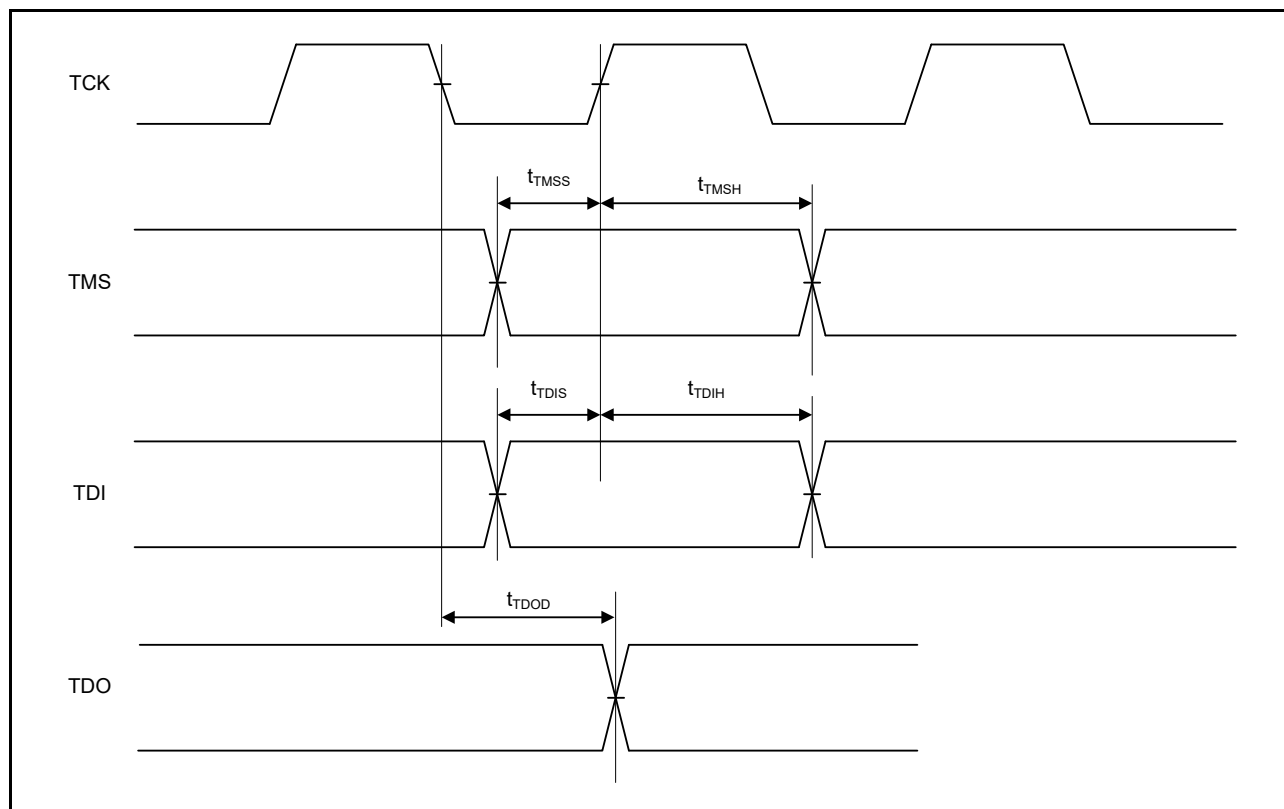
### 2.15 Joint Test Action Group (JTAG)

**Table 2.49 JTAG**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	$t_{TCKcyc}$	40	-	-	ns	Figure 2.89
TCK clock high pulse width	$t_{TCKH}$	15	-	-	ns	
TCK clock low pulse width	$t_{TCKL}$	15	-	-	ns	
TCK clock rise time	$t_{TCKr}$	-	-	5	ns	
TCK clock fall time	$t_{TCKf}$	-	-	5	ns	
TMS setup time	$t_{TMSS}$	8	-	-	ns	Figure 2.90
TMS hold time	$t_{TMSH}$	8	-	-	ns	
TDI setup time	$t_{TDIS}$	8	-	-	ns	
TDI hold time	$t_{TDIH}$	8	-	-	ns	
TDO data delay time	$t_{TDOD}$	-	-	20	ns	



**Figure 2.92 JTAG TCK timing**

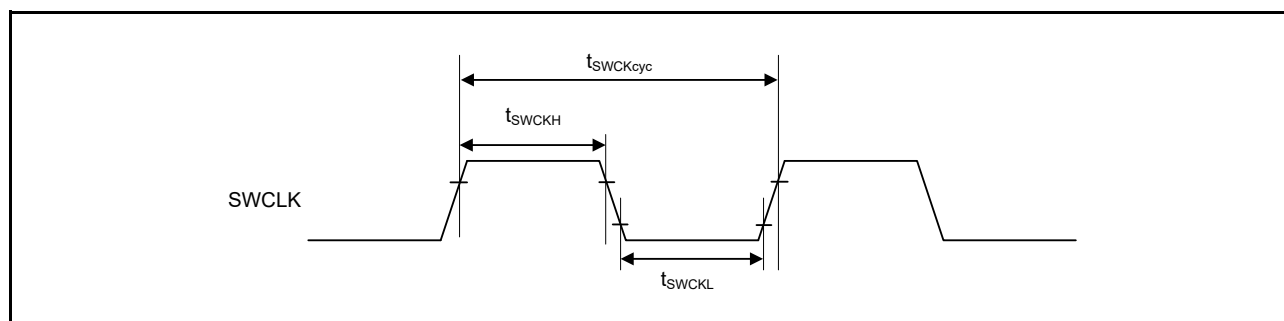


**Figure 2.93 JTAG input/output timing**

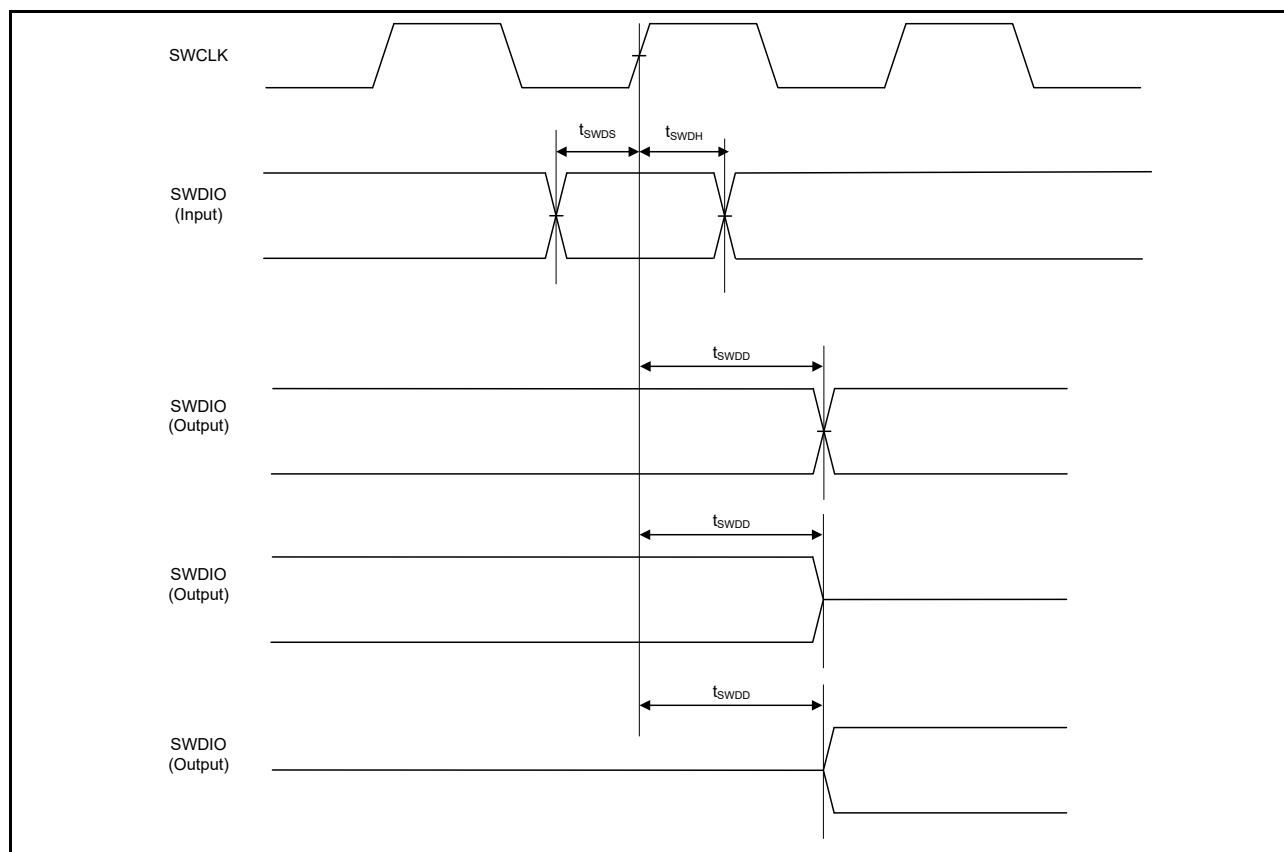
### 2.16 Serial Wire Debug (SWD)

**Table 2.50 SWD**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCLKcyc}$	40	-	-	ns	Figure 2.94
SWCLK clock high pulse width	$t_{SWCKH}$	15	-	-	ns	
SWCLK clock low pulse width	$t_{SWCKL}$	15	-	-	ns	
SWCLK clock rise time	$t_{SWCKr}$	-	-	5	ns	
SWCLK clock fall time	$t_{SWCKf}$	-	-	5	ns	
SWDIO setup time	$t_{SWDS}$	8	-	-	ns	Figure 2.95
SWDIO hold time	$t_{SWDH}$	8	-	-	ns	
SWDIO data delay time	$t_{SWDD}$	2	-	28	ns	



**Figure 2.94 SWD SWCLK timing**



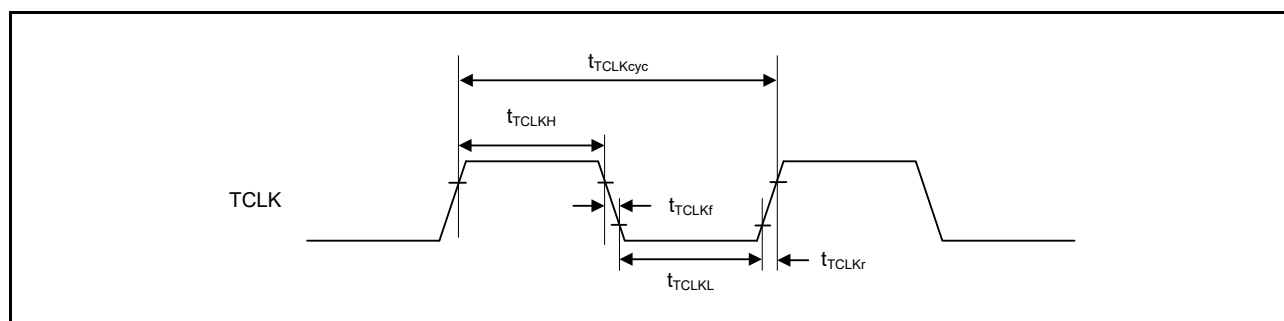
**Figure 2.95 SWD input/output timing**

### 2.17 Embedded Trace Macro Interface (ETM)

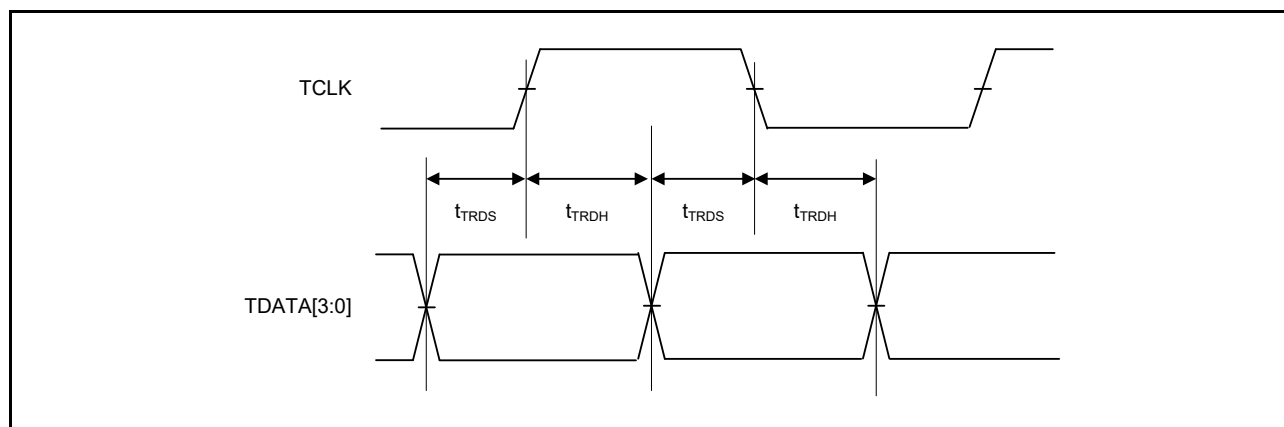
**Table 2.51 ETM**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLK_{cyc}}$	33.3	-	-	ns	Figure 2.96
TCLK clock high pulse width	$t_{TCLKH}$	13.6	-	-	ns	
TCLK clock low pulse width	$t_{TCLKL}$	13.6	-	-	ns	
TCLK clock rise time	$t_{TCLKr}$	-	-	3	ns	
TCLK clock fall time	$t_{TCLKf}$	-	-	3	ns	
TDATA[3:0] output setup time	$t_{TRDS}$	3.5	-	-	ns	Figure 2.97
TDATA[3:0] output hold time	$t_{TRDH}$	2.5	-	-	ns	



**Figure 2.96 ETM TCLK timing**



**Figure 2.97 ETM output timing**

## Appendix 1. Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

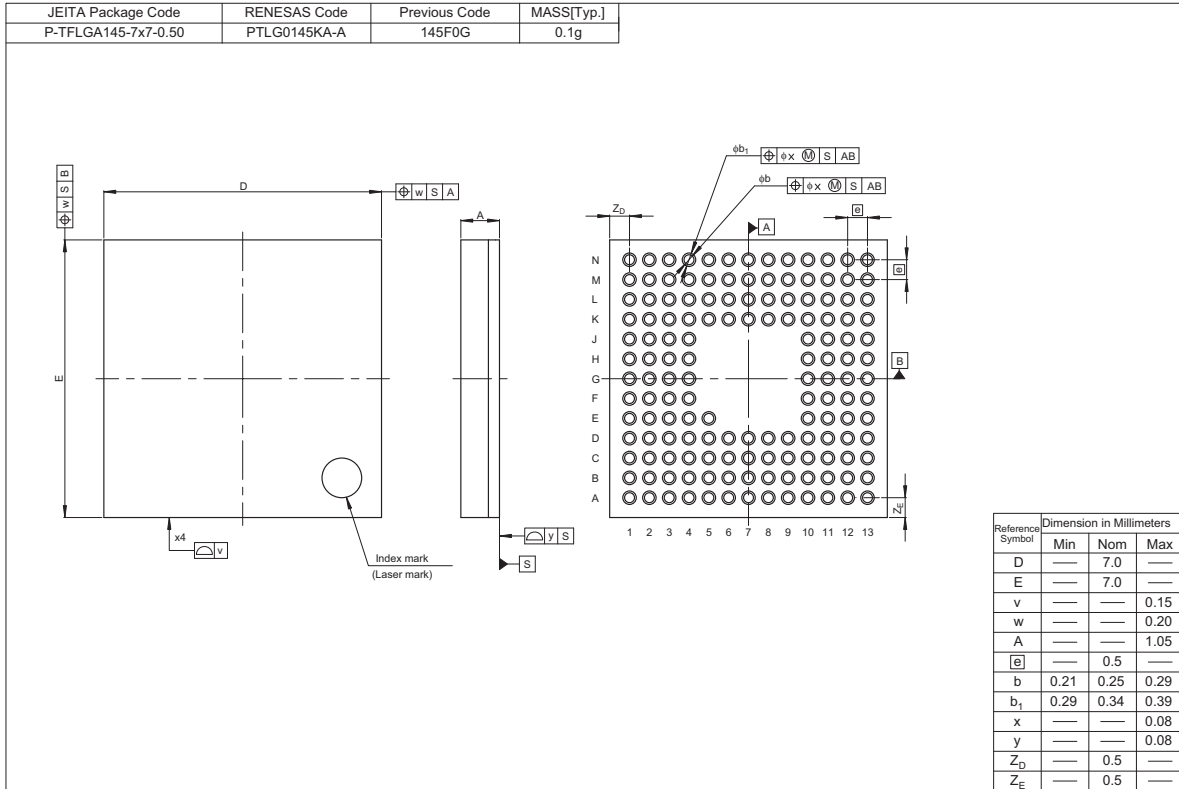


Figure 1.1 145-pin LGA

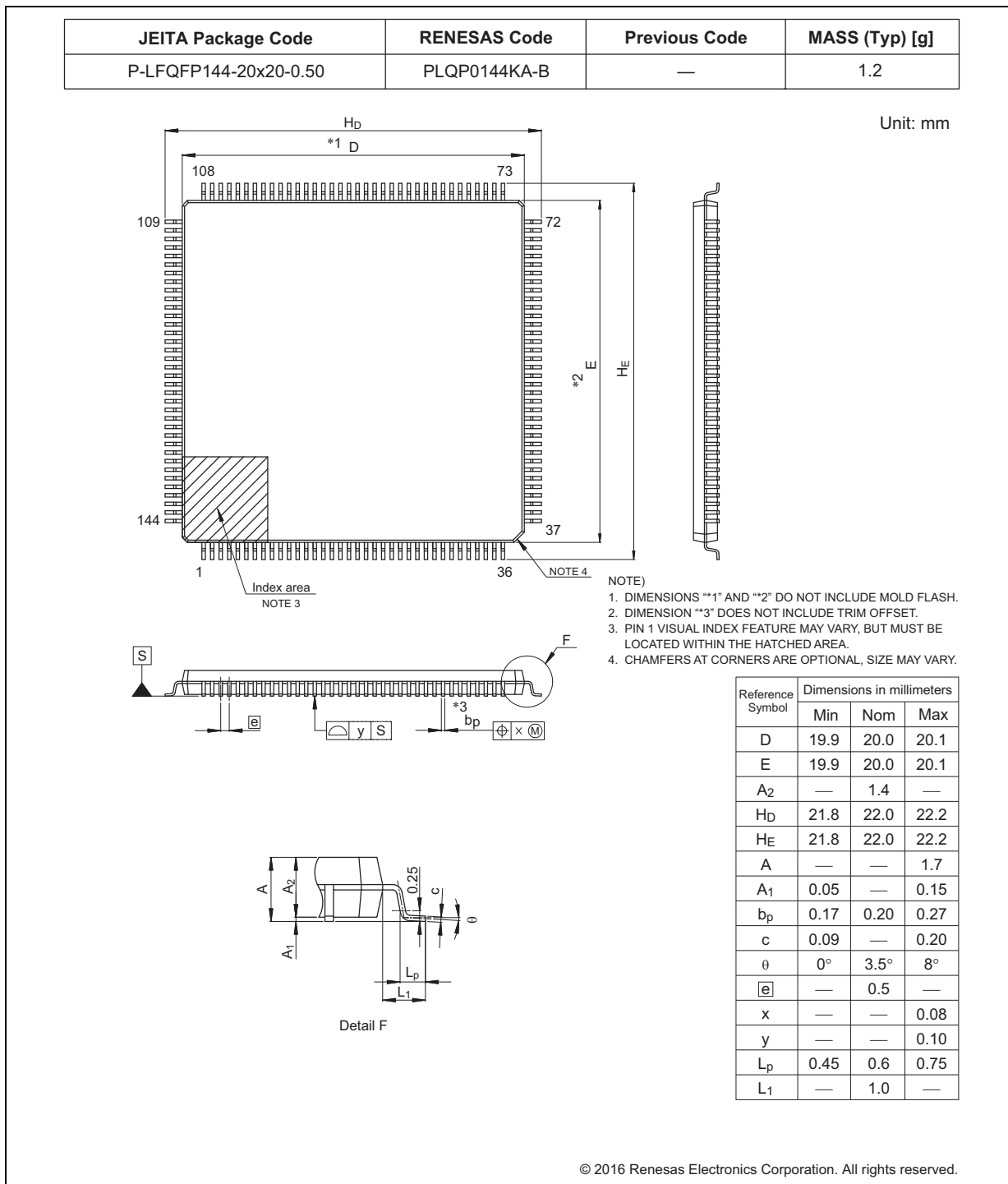
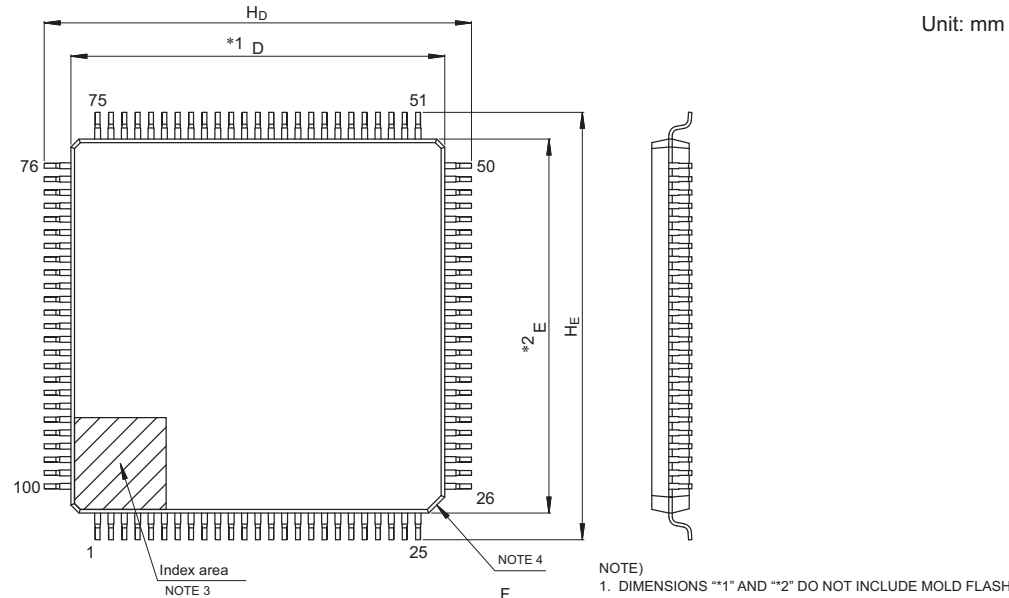


Figure 1.2 144-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6



- NOTE)
1. DIMENSIONS \*\*1" AND \*\*2" DO NOT INCLUDE MOLD FLASH.
  2. DIMENSION \*\*3" DOES NOT INCLUDE TRIM OFFSET.
  3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
  4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	15.8	16.0	16.2
H <sub>E</sub>	15.8	16.0	16.2
A	—	—	1.7
A <sub>1</sub>	0.05	—	0.15
b <sub>p</sub>	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
ⓔ	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L <sub>p</sub>	0.45	0.6	0.75
L <sub>1</sub>	—	1.0	—

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Figure 1.3 100-pin LQFP

Revision History	RA6M2 Group Datasheet
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Rev.	Date	Chapter	Summary
1.00	Oct 8, 2019	-	First Edition issued
1.10	May 14, 2021	-	Second Edition issued
1.20	Dec 23, 2022	-	Third Edition issued

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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