



# THE DATASHEET OF SI5325B-C-GMR

## µP-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

### Features

- Not recommended for new designs. For alternatives, see the Si533x family of products.
- Generates frequencies from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs with jitter generation as low as 0.5 ps rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 2 MHz)
- Dual clock inputs w/manual or automatically controlled switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- LOS, FOS alarm outputs
- I<sup>2</sup>C or SPI programmable
- On-chip voltage regulator for 1.8 ±5%, 2.5 or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

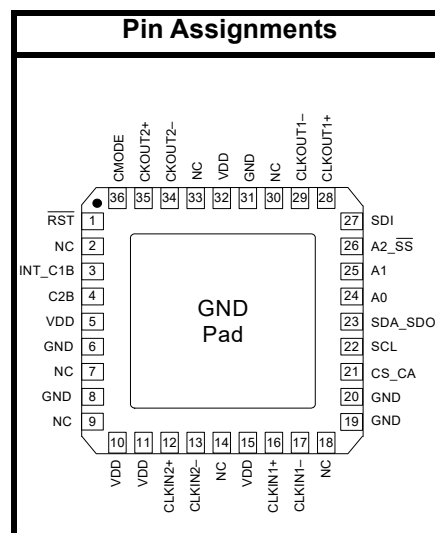
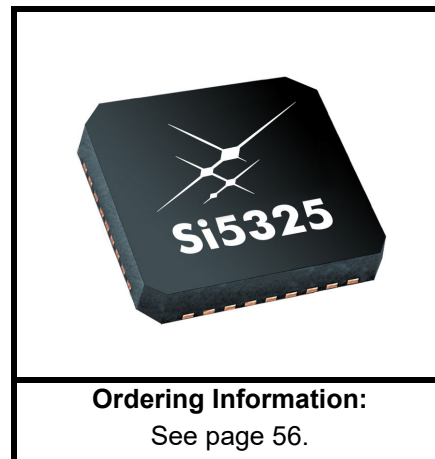
### Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Optical modules
- Wireless basestations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

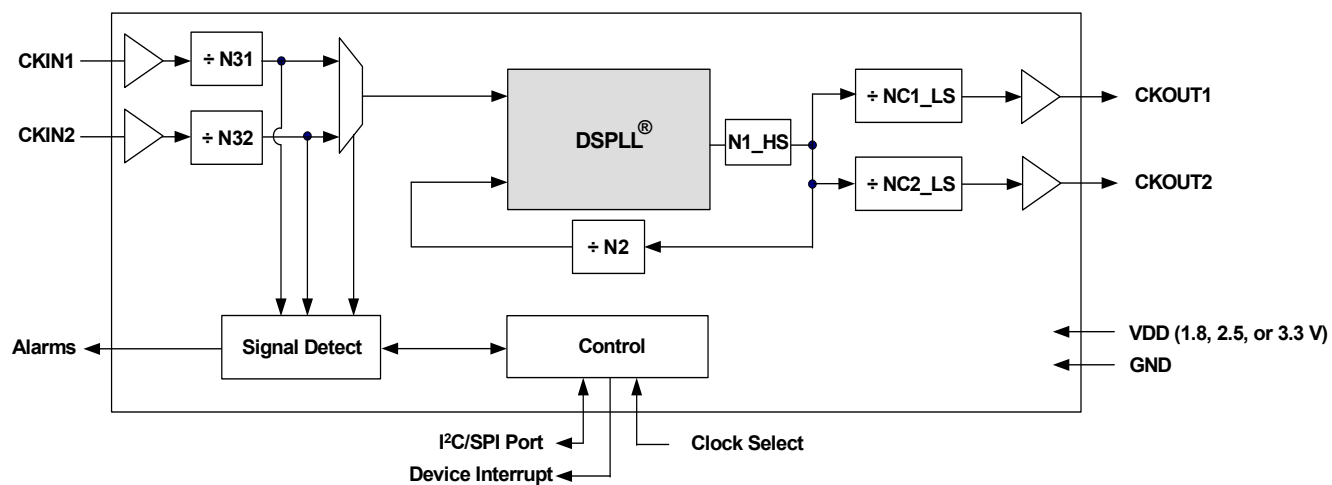
### Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The device provides frequency translation combinations across this operating range. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface.

The Si5325 is based on Skyworks Solutions' 3rd-generation DSPLL® technology, which provides frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5325 is ideal for providing clock multiplication in high performance timing applications.



## Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter                                                                                                                                                                                                                                | Symbol          | Test Condition | Min  | Typ | Max  | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------|------|-----|------|------|
| Ambient Temperature                                                                                                                                                                                                                      | T <sub>A</sub>  |                | −40  | 25  | 85   | C    |
| Supply Voltage during Normal Operation                                                                                                                                                                                                   | V <sub>DD</sub> | 3.3 V Nominal  | 2.97 | 3.3 | 3.63 | V    |
|                                                                                                                                                                                                                                          |                 | 2.5 V Nominal  | 2.25 | 2.5 | 2.75 | V    |
|                                                                                                                                                                                                                                          |                 | 1.8 V Nominal  | 1.71 | 1.8 | 1.89 | V    |
| <b>Note:</b> All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated. |                 |                |      |     |      |      |

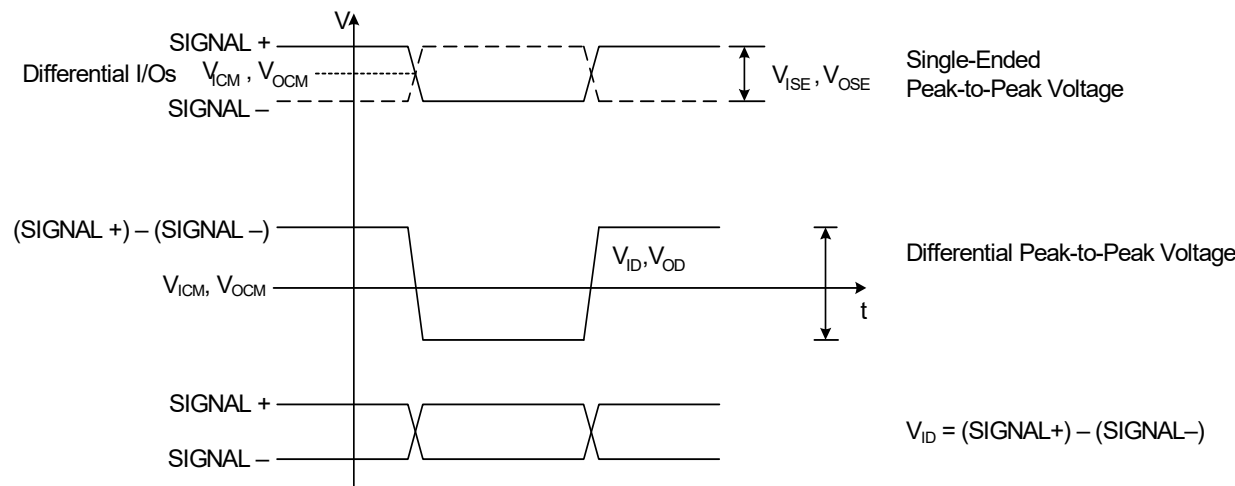


Figure 1. Differential Voltage Characteristics

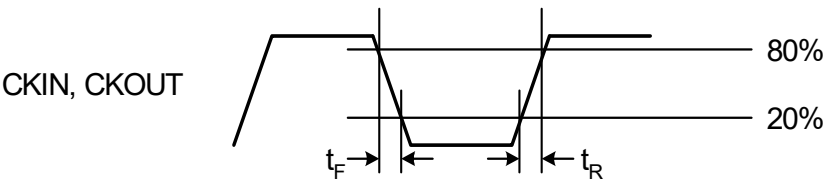


Figure 2. Rise/Fall Time Characteristics

**Table 2. DC Characteristics**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = –40 to 85 °C)

| Parameter                                                                                                                                           | Symbol             | Test Condition                                         | Min  | Typ | Max  | Unit            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------|------|-----|------|-----------------|
| Supply Current <sup>1</sup>                                                                                                                         | I <sub>DD</sub>    | LVPECL Format<br>622.08 MHz Out<br>Both CKOUTs Enabled | —    | 251 | 279  | mA              |
|                                                                                                                                                     |                    | LVPECL Format<br>622.08 MHz Out<br>1 CKOUT Enabled     | —    | 217 | 243  | mA              |
|                                                                                                                                                     |                    | CMOS Format<br>19.44 MHz Out<br>Both CKOUTs Enabled    | —    | 204 | 234  | mA              |
|                                                                                                                                                     |                    | CMOS Format<br>19.44 MHz Out<br>1 CKOUT Enabled        | —    | 194 | 220  | mA              |
|                                                                                                                                                     |                    | Disable Mode                                           | —    | 165 | —    | mA              |
| CKINn Input Pins <sup>2</sup>                                                                                                                       |                    |                                                        |      |     |      |                 |
| Input Common Mode<br>Voltage (Input Thresh-<br>old Voltage)                                                                                         | V <sub>ICM</sub>   | 1.8 V ± 5%                                             | 0.9  | —   | 1.4  | V               |
|                                                                                                                                                     |                    | 2.5 V ± 10%                                            | 1    | —   | 1.7  | V               |
|                                                                                                                                                     |                    | 3.3 V ± 10%                                            | 1.1  | —   | 1.95 | V               |
| Input Resistance                                                                                                                                    | CKN <sub>RIN</sub> | Single-ended                                           | 20   | 40  | 60   | kΩ              |
| Single-Ended Input<br>Voltage Swing<br>(See Absolute Specs)                                                                                         | V <sub>ISE</sub>   | f <sub>CKIN</sub> < 212.5 MHz<br>See Figure 1.         | 0.2  | —   | —    | V <sub>PP</sub> |
|                                                                                                                                                     |                    | f <sub>CKIN</sub> > 212.5 MHz<br>See Figure 1.         | 0.25 | —   | —    | V <sub>PP</sub> |
| Differential Input<br>Voltage Swing<br>(See Absolute Specs)                                                                                         | V <sub>ID</sub>    | f <sub>CKIN</sub> < 212.5 MHz<br>See Figure 1.         | 0.2  | —   | —    | V <sub>PP</sub> |
|                                                                                                                                                     |                    | f <sub>CKIN</sub> > 212.5 MHz<br>See Figure 1.         | 0.25 | —   | —    | V <sub>PP</sub> |
| <b>Notes:</b>                                                                                                                                       |                    |                                                        |      |     |      |                 |
| 1. Current draw is independent of supply voltage                                                                                                    |                    |                                                        |      |     |      |                 |
| 2. No under- or overshoot is allowed.                                                                                                               |                    |                                                        |      |     |      |                 |
| 3. LVPECL outputs require nominal VDD ≥ 2.5 V.                                                                                                      |                    |                                                        |      |     |      |                 |
| 4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details. |                    |                                                        |      |     |      |                 |
| 5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.                                                                              |                    |                                                        |      |     |      |                 |

**Table 2. DC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Symbol               | Test Condition                         | Min                   | Typ                   | Max                   | Unit             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------------------|-----------------------|-----------------------|-----------------------|------------------|
| <b>Output Clocks (CKOUTn)<sup>3</sup></b>                                                                                                                                                                                                                                                                                                                                                                                                                            |                      |                                        |                       |                       |                       |                  |
| Common Mode                                                                                                                                                                                                                                                                                                                                                                                                                                                          | CKO <sub>VCM</sub>   | LVPECL 100 Ω load line-to-line         | V <sub>DD</sub> -1.42 | —                     | V <sub>DD</sub> -1.25 | V                |
| Differential Output Swing <sup>5</sup>                                                                                                                                                                                                                                                                                                                                                                                                                               | CKO <sub>VD</sub>    | LVPECL 100 Ω load line-to-line         | 1.1                   | —                     | 1.9                   | V <sub>PP</sub>  |
| Single-Ended Output Swing <sup>5</sup>                                                                                                                                                                                                                                                                                                                                                                                                                               | CKO <sub>VSE</sub>   | LVPECL 100 Ω load line-to-line         | 0.5                   | —                     | 0.93                  | V <sub>PP</sub>  |
| Differential Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                          | CKO <sub>VD</sub>    | CML 100 Ω load line-to-line            | 350                   | 425                   | 500                   | mV <sub>PP</sub> |
| Common Mode Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                           | CKO <sub>VCM</sub>   | CML 100 Ω load line-to-line            | —                     | V <sub>DD</sub> -0.36 | —                     | V                |
| Differential Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                          | CKO <sub>VD</sub>    | LVDS 100 Ω load line-to-line           | 500                   | 700                   | 900                   | mV <sub>PP</sub> |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                      | Low Swing LVDS 100 Ω load line-to-line | 350                   | 425                   | 500                   | mV <sub>PP</sub> |
| Common Mode Output Voltage                                                                                                                                                                                                                                                                                                                                                                                                                                           | CKO <sub>VCM</sub>   | LVDS 100 Ω load line-to-line           | 1.125                 | 1.2                   | 1.275                 | V                |
| Differential Output Resistance                                                                                                                                                                                                                                                                                                                                                                                                                                       | CKO <sub>RD</sub>    | CML, LVPECL, LVDS                      | —                     | 200                   | —                     | Ω                |
| Output Voltage Low                                                                                                                                                                                                                                                                                                                                                                                                                                                   | CKO <sub>VOLLH</sub> | CMOS                                   | —                     | —                     | 0.4                   | V                |
| Output Voltage High                                                                                                                                                                                                                                                                                                                                                                                                                                                  | CKO <sub>VOHLH</sub> | V <sub>DD</sub> = 1.71 V<br>CMOS       | 0.8 x V <sub>DD</sub> | —                     | —                     | V                |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Current draw is independent of supply voltage</li> <li>2. No under- or overshoot is allowed.</li> <li>3. LVPECL outputs require nominal VDD ≥ 2.5 V.</li> <li>4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.</li> <li>5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.</li> </ol> |                      |                                        |                       |                       |                       |                  |

**Table 2. DC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = –40 to 85 °C)

| Parameter                                                                                                                                                                                                                                                                                                                                                                              | Symbol            | Test Condition                            | Min | Typ  | Max | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------------------------------------|-----|------|-----|------|
| Output Drive Current<br>(CMOS driving into<br>CKO <sub>VOL</sub> for output low<br>or CKO <sub>VOH</sub> for output<br>high. CKOUT+ and<br>CKOUT– shorted<br>externally)                                                                                                                                                                                                               | CKO <sub>IO</sub> | ICMOS[1:0] =11<br>V <sub>DD</sub> = 1.8 V | —   | 7.5  | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =10<br>V <sub>DD</sub> = 1.8 V | —   | 5.5  | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =01<br>V <sub>DD</sub> = 1.8 V | —   | 3.5  | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =00<br>V <sub>DD</sub> = 1.8 V | —   | 1.75 | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =11<br>V <sub>DD</sub> = 3.3 V | —   | 32   | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =10<br>V <sub>DD</sub> = 3.3 V | —   | 24   | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =01<br>V <sub>DD</sub> = 3.3 V | —   | 16   | —   | mA   |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | ICMOS[1:0] =00<br>V <sub>DD</sub> = 3.3 V | —   | 8    | —   | mA   |
| 2-Level LVCMOS Input Pins                                                                                                                                                                                                                                                                                                                                                              |                   |                                           |     |      |     |      |
| Input Voltage Low                                                                                                                                                                                                                                                                                                                                                                      | V <sub>IL</sub>   | V <sub>DD</sub> = 1.71 V                  | —   | —    | 0.5 | V    |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | V <sub>DD</sub> = 2.25 V                  | —   | —    | 0.7 | V    |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | V <sub>DD</sub> = 2.97 V                  | —   | —    | 0.8 | V    |
| Input Voltage High                                                                                                                                                                                                                                                                                                                                                                     | V <sub>IH</sub>   | V <sub>DD</sub> = 1.89 V                  | 1.4 | —    | —   | V    |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | V <sub>DD</sub> = 2.25 V                  | 1.8 | —    | —   | V    |
|                                                                                                                                                                                                                                                                                                                                                                                        |                   | V <sub>DD</sub> = 3.63 V                  | 2.5 | —    | —   | V    |
| Notes:<br>1. Current draw is independent of supply voltage<br>2. No under- or overshoot is allowed.<br>3. LVPECL outputs require nominal VDD ≥ 2.5 V.<br>4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.<br>5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz. |                   |                                           |     |      |     |      |

**Table 2. DC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = –40 to 85 °C)

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Symbol           | Test Condition                         | Min                    | Typ | Max                    | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|----------------------------------------|------------------------|-----|------------------------|------|
| <b>3-Level Input Pins<sup>4</sup></b>                                                                                                                                                                                                                                                                                                                                                                                                                                |                  |                                        |                        |     |                        |      |
| Input Voltage Low                                                                                                                                                                                                                                                                                                                                                                                                                                                    | V <sub>ILL</sub> |                                        | —                      | —   | 0.15 x V <sub>DD</sub> | V    |
| Input Voltage Mid                                                                                                                                                                                                                                                                                                                                                                                                                                                    | V <sub>IMM</sub> |                                        | 0.45 x V <sub>DD</sub> | —   | 0.55 x V <sub>DD</sub> | V    |
| Input Voltage High                                                                                                                                                                                                                                                                                                                                                                                                                                                   | V <sub>IHH</sub> |                                        | 0.85 x V <sub>DD</sub> | —   | —                      | V    |
| Input Low Current                                                                                                                                                                                                                                                                                                                                                                                                                                                    | I <sub>ILL</sub> | See Note 4                             | –20                    | —   | —                      | μA   |
| Input Mid Current                                                                                                                                                                                                                                                                                                                                                                                                                                                    | I <sub>IMM</sub> | See Note 4                             | –2                     | —   | +2                     | μA   |
| Input High Current                                                                                                                                                                                                                                                                                                                                                                                                                                                   | I <sub>IHH</sub> | See Note 4                             | —                      | —   | 20                     | μA   |
| <b>LVCMOS Output Pins</b>                                                                                                                                                                                                                                                                                                                                                                                                                                            |                  |                                        |                        |     |                        |      |
| Output Voltage Low                                                                                                                                                                                                                                                                                                                                                                                                                                                   | V <sub>OL</sub>  | IO = 2 mA<br>V <sub>DD</sub> = 1.71 V  | —                      | —   | 0.4                    | V    |
| Output Voltage Low                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                  | IO = 2 mA<br>V <sub>DD</sub> = 2.97 V  | —                      | —   | 0.4                    | V    |
| Output Voltage High                                                                                                                                                                                                                                                                                                                                                                                                                                                  | V <sub>OH</sub>  | IO = –2 mA<br>V <sub>DD</sub> = 1.71 V | V <sub>DD</sub> – 0.4  | —   | —                      | V    |
| Output Voltage High                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                  | IO = –2 mA<br>V <sub>DD</sub> = 2.97 V | V <sub>DD</sub> – 0.4  | —   | —                      | V    |
| Disabled Leakage Current                                                                                                                                                                                                                                                                                                                                                                                                                                             | I <sub>OZ</sub>  | RSTb = 0                               | –100                   | —   | 100                    | μA   |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. Current draw is independent of supply voltage</li> <li>2. No under- or overshoot is allowed.</li> <li>3. LVPECL outputs require nominal VDD ≥ 2.5 V.</li> <li>4. This is the amount of leakage that the 3-Level inputs can tolerate from an external driver. See Si53xx Family Reference Manual for more details.</li> <li>5. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.</li> </ol> |                  |                                        |                        |     |                        |      |

**Table 3. AC Characteristics**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

| Parameter                                                                | Symbol             | Test Condition                                                                                          | Min   | Typ | Max   | Unit |
|--------------------------------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------|-------|-----|-------|------|
| <b>CKINn Input Pins</b>                                                  |                    |                                                                                                         |       |     |       |      |
| Input Frequency                                                          | CKN <sub>F</sub>   |                                                                                                         | 10    | —   | 710   | MHz  |
| Input Duty Cycle<br>(Minimum Pulse Width)                                | CKN <sub>DC</sub>  | Whichever is smaller<br>(i.e., the 40% / 60%<br>limitation applies only<br>to high frequency<br>clocks) | 40    | —   | 60    | %    |
|                                                                          |                    |                                                                                                         | 2     | —   | —     | ns   |
| Input Capacitance                                                        | CKN <sub>CIN</sub> |                                                                                                         | —     | —   | 3     | pF   |
| Input Rise/Fall Time                                                     | CKN <sub>TRF</sub> | 20–80%<br>See Figure 2                                                                                  | —     | —   | 11    | ns   |
| <b>CKOUTn Output Pins</b>                                                |                    |                                                                                                         |       |     |       |      |
| (See ordering section for speed grade vs frequency limits)               |                    |                                                                                                         |       |     |       |      |
| Output Frequency<br>(Output not config-<br>ured for CMOS or<br>Disabled) | CKO <sub>F</sub>   | N1 ≥ 6                                                                                                  | 0.002 | —   | 945   | MHz  |
|                                                                          |                    | N1 = 5                                                                                                  | 970   | —   | 1134  | MHz  |
|                                                                          |                    | N1 = 4                                                                                                  | 1.213 | —   | 1.4   | GHz  |
| Maximum Output<br>Frequency in CMOS<br>Format                            | CKO <sub>F</sub>   |                                                                                                         | —     | —   | 212.5 | MHz  |
| Output Rise/Fall<br>(20–80 %) @<br>622.08 MHz output                     | CKO <sub>TRF</sub> | Output not configured for<br>CMOS or Disabled<br>See Figure 2                                           | —     | 230 | 350   | ps   |
| Output Rise/Fall<br>(20–80%) @<br>212.5 MHz output                       | CKO <sub>TRF</sub> | CMOS Output<br>V <sub>DD</sub> = 1.71<br>C <sub>LOAD</sub> = 5 pF                                       | —     | —   | 8     | ns   |
| Output Rise/Fall<br>(20–80%) @<br>212.5 MHz output                       | CKO <sub>TRF</sub> | CMOS Output<br>V <sub>DD</sub> = 2.97<br>C <sub>LOAD</sub> = 5 pF                                       | —     | —   | 2     | ns   |
| Output Duty Cycle<br>Uncertainty @<br>622.08 MHz                         | CKO <sub>DC</sub>  | 100 Ω Load<br>Line-to-Line<br>Measured at 50% Point<br>(Not for CMOS)                                   | —     | —   | +/-40 | ps   |

**Table 3. AC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = –40 to 85 °C)

| Parameter                                 | Symbol              | Test Condition                                                                                                                                                    | Min | Typ | Max      | Unit              |
|-------------------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|----------|-------------------|
| <b>LVC MOS Input Pins</b>                 |                     |                                                                                                                                                                   |     |     |          |                   |
| Minimum Reset Pulse Width                 | t <sub>RSTMN</sub>  |                                                                                                                                                                   | 1   | —   | —        | μs                |
| Reset to Microprocessor Access Ready      | t <sub>READY</sub>  |                                                                                                                                                                   | —   | —   | 10       | ms                |
| Input Capacitance                         | C <sub>in</sub>     |                                                                                                                                                                   | —   | —   | 3        | pF                |
| <b>LVC MOS Output Pins</b>                |                     |                                                                                                                                                                   |     |     |          |                   |
| Rise/Fall Times                           | t <sub>RF</sub>     | C <sub>LOAD</sub> = 20 pF<br>See Figure 2                                                                                                                         | —   | 25  | —        | ns                |
| LOSn Trigger Window                       | LOS <sub>TRIG</sub> | From last CKINn ↑ to ↓<br>Internal detection of LOSn<br>N3 ≠ 1                                                                                                    | —   | —   | 4.5 x N3 | T <sub>CKIN</sub> |
| Time to Clear LOL after LOS Cleared       | t <sub>CLRLOL</sub> | ↓LOS to ↓LOL<br>Fold = Fnew<br>Stable Xa/XB reference                                                                                                             | —   | 10  | —        | ms                |
| <b>Device Skew</b>                        |                     |                                                                                                                                                                   |     |     |          |                   |
| Output Clock Skew                         | t <sub>SKEW</sub>   | ↑ of CKOUTn to ↑ of CKOUT_m, CKOUTn and CKOUT_m at same frequency and signal format<br><u>PHASEOFFSET</u> = 0<br><u>CKOUT_ALWAYS_ON</u> = 1<br><u>SQ_ICAL</u> = 1 | —   | —   | 100      | ps                |
| Phase Change due to Temperature Variation | t <sub>TEMP</sub>   | Max phase changes from –40 to +85 °C                                                                                                                              | —   | 300 | 500      | ps                |

**Table 3. AC Characteristics (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

| Parameter                                                                                        | Symbol              | Test Condition                                 | Min     | Typ  | Max  | Unit     |
|--------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------|---------|------|------|----------|
| <b>PLL Performance</b><br>(f <sub>in</sub> = f <sub>out</sub> = 622.08 MHz; BW = 120 Hz; LVPECL) |                     |                                                |         |      |      |          |
| Lock Time                                                                                        | t <sub>LOCKMP</sub> | Start of ICAL to ↓ of LOL                      | —       | 35   | 1200 | ms       |
| Closed Loop Jitter Peaking                                                                       | J <sub>PK</sub>     |                                                | —       | 0.05 | 0.1  | dB       |
| Jitter Tolerance                                                                                 | J <sub>TOL</sub>    | Jitter Frequency ≥ Loop Bandwidth              | 5000/BW | —    | —    | ns pk-pk |
| Phase Noise<br>f <sub>out</sub> = 622.08 MHz                                                     | CKO <sub>PN</sub>   | 1 kHz Offset                                   | —       | -90  | —    | dBc/Hz   |
|                                                                                                  |                     | 10 kHz Offset                                  | —       | -113 | —    | dBc/Hz   |
|                                                                                                  |                     | 100 kHz Offset                                 | —       | -118 | —    | dBc/Hz   |
|                                                                                                  |                     | 1 MHz Offset                                   | —       | -132 | —    | dBc/Hz   |
| Subharmonic Noise                                                                                | SP <sub>SUBH</sub>  | Phase Noise @ 100 kHz Offset                   | —       | -88  | —    | dBc      |
| Spurious Noise                                                                                   | SP <sub>SPUR</sub>  | Max spur @ n x F3<br>(n ≥ 1, n x F3 < 100 MHz) | —       | -93  | —    | dBc      |

**Table 4. Microprocessor Control**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = -40 to 85 °C)

| Parameter                                  | Symbol                           | Test Condition                              | Min                    | Typ | Max                    | Unit |
|--------------------------------------------|----------------------------------|---------------------------------------------|------------------------|-----|------------------------|------|
| <b>I<sup>2</sup>C Bus Lines (SDA, SCL)</b> |                                  |                                             |                        |     |                        |      |
| Input Voltage Low                          | V <sub>IL</sub> I <sub>2C</sub>  |                                             | —                      | —   | 0.25 x V <sub>DD</sub> | V    |
| Input Voltage High                         | V <sub>IH</sub> I <sub>2C</sub>  |                                             | 0.7 x V <sub>DD</sub>  | —   | V <sub>DD</sub>        | V    |
| Hysteresis of Schmitt trigger inputs       | V <sub>HYS</sub> I <sub>2C</sub> | V <sub>DD</sub> = 1.8V                      | 0.1 x V <sub>DD</sub>  | —   | —                      | V    |
|                                            |                                  | V <sub>DD</sub> = 2.5 or 3.3 V              | 0.05 x V <sub>DD</sub> | —   | —                      | V    |
| Output Voltage Low                         | V <sub>OL</sub> I <sub>2C</sub>  | V <sub>DD</sub> = 1.8 V<br>IO = 3 mA        | —                      | —   | 0.2 x V <sub>DD</sub>  | V    |
|                                            |                                  | V <sub>DD</sub> = 2.5 or 3.3 V<br>IO = 3 mA | —                      | —   | 0.4                    | V    |

**Table 4. Microprocessor Control (Continued)**(V<sub>DD</sub> = 1.8 ± 5%, 2.5 ± 10%, or 3.3 V ± 10%, T<sub>A</sub> = –40 to 85 °C)

| Parameter                               | Symbol           | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------------|------------------|----------------|-----|-----|-----|------|
| <b>SPI Specifications</b>               |                  |                |     |     |     |      |
| Duty Cycle, SCLK                        | t <sub>DC</sub>  | SCLK = 10 MHz  | 40  | —   | 60  | %    |
| Cycle Time, SCLK                        | t <sub>c</sub>   |                | 100 | —   | —   | ns   |
| Rise Time, SCLK                         | t <sub>r</sub>   | 20–80%         | —   | —   | 25  | ns   |
| Fall Time, SCLK                         | t <sub>f</sub>   | 20–80%         | —   | —   | 25  | ns   |
| Low Time, SCLK                          | t <sub>lsc</sub> | 20–20%         | 30  | —   | —   | ns   |
| High Time, SCLK                         | t <sub>hsc</sub> | 80–80%         | 30  | —   | —   | ns   |
| Delay Time, SCLK Fall to SDO Active     | t <sub>d1</sub>  |                | —   | —   | 25  | ns   |
| Delay Time, SCLK Fall to SDO Transition | t <sub>d2</sub>  |                | —   | —   | 25  | ns   |
| Delay Time, SS Rise to SDO Tri-state    | t <sub>d3</sub>  |                | —   | —   | 25  | ns   |
| Setup Time, SS to SCLK Fall             | t <sub>su1</sub> |                | 25  | —   | —   | ns   |
| Hold Time, SS to SCLK Rise              | t <sub>h1</sub>  |                | 20  | —   | —   | ns   |
| Setup Time, SDI to SCLK Rise            | t <sub>su2</sub> |                | 25  | —   | —   | ns   |
| Hold Time, SDI to SCLK Rise             | t <sub>h2</sub>  |                | 20  | —   | —   | ns   |
| Delay Time between Slave Selects        | t <sub>cs</sub>  |                | 25  | —   | —   | ns   |

Table 5. Jitter Generation

| Parameter                                                                                                                                                                                         | Symbol | Test Condition*    | Min | Typ | Max | Unit              |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------|-----|-----|-----|-------------------|
|                                                                                                                                                                                                   |        | Measurement Filter |     |     |     |                   |
| Jitter Gen<br>OC-192                                                                                                                                                                              | JGEN   | 0.02–80 MHz        | —   | .49 | —   | ps <sub>rms</sub> |
|                                                                                                                                                                                                   |        | 4–80 MHz           | —   | .23 | —   | ps <sub>rms</sub> |
|                                                                                                                                                                                                   |        | 0.05–80 MHz        | —   | .47 | —   | ps <sub>rms</sub> |
| Jitter Gen<br>OC-48                                                                                                                                                                               | JGEN   | 0.12–20 MHz        | —   | .48 | —   | ps <sub>rms</sub> |
| <b>*Note:</b> Test conditions:<br>1. $f_{IN} = f_{OUT} = 622.08$ MHz<br>2. Clock input: LVPECL<br>3. Clock output: LVPECL<br>4. PLL bandwidth: 877 kHz<br>5. $V_{DD} = 2.5$ V<br>6. $T_A = 85$ °C |        |                    |     |     |     |                   |

Table 6. Thermal Characteristics

( $V_{DD} = 1.8 \pm 5\%$ ,  $2.5 \pm 10\%$ , or  $3.3$  V  $\pm 10\%$ ,  $T_A = -40$  to  $85$  °C)

| Parameter                              | Symbol        | Test Condition | Value | Unit |
|----------------------------------------|---------------|----------------|-------|------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air      | 32    | °C/W |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ | Still Air      | 14    | °C/W |

Table 7. Absolute Maximum Ratings

| Parameter                                                                                                                                                                                                                                                                                                                      | Symbol             | Value                           | Unit |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------|------|
| DC Supply Voltage                                                                                                                                                                                                                                                                                                              | V <sub>DD</sub>    | −0.5 to 3.8                     | V    |
| LVC MOS Input Voltage                                                                                                                                                                                                                                                                                                          | V <sub>DIG</sub>   | −0.3 to (V <sub>DD</sub> + 0.3) | V    |
| CKINn Voltage Level Limits                                                                                                                                                                                                                                                                                                     | CKN <sub>VIN</sub> | 0 to V <sub>DD</sub>            | V    |
| XA/XB Voltage Level Limits                                                                                                                                                                                                                                                                                                     | XA <sub>VIN</sub>  | 0 to 1.2                        | V    |
| Operating Junction Temperature                                                                                                                                                                                                                                                                                                 | T <sub>JCT</sub>   | −55 to 150                      | C    |
| Storage Temperature Range                                                                                                                                                                                                                                                                                                      | T <sub>STG</sub>   | −55 to 150                      | C    |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN−                                                                                                                                                                                                                                                                |                    | 2                               | kV   |
| ESD MM Tolerance; All pins except CKIN+/CKIN−                                                                                                                                                                                                                                                                                  |                    | 150                             | V    |
| ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN−                                                                                                                                                                                                                                                                                |                    | 750                             | V    |
| ESD MM Tolerance; CKIN+/CKIN−                                                                                                                                                                                                                                                                                                  |                    | 100                             | V    |
| Latch-Up Tolerance                                                                                                                                                                                                                                                                                                             |                    | JESD78 Compliant                |      |
| <b>Note:</b> Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. |                    |                                 |      |

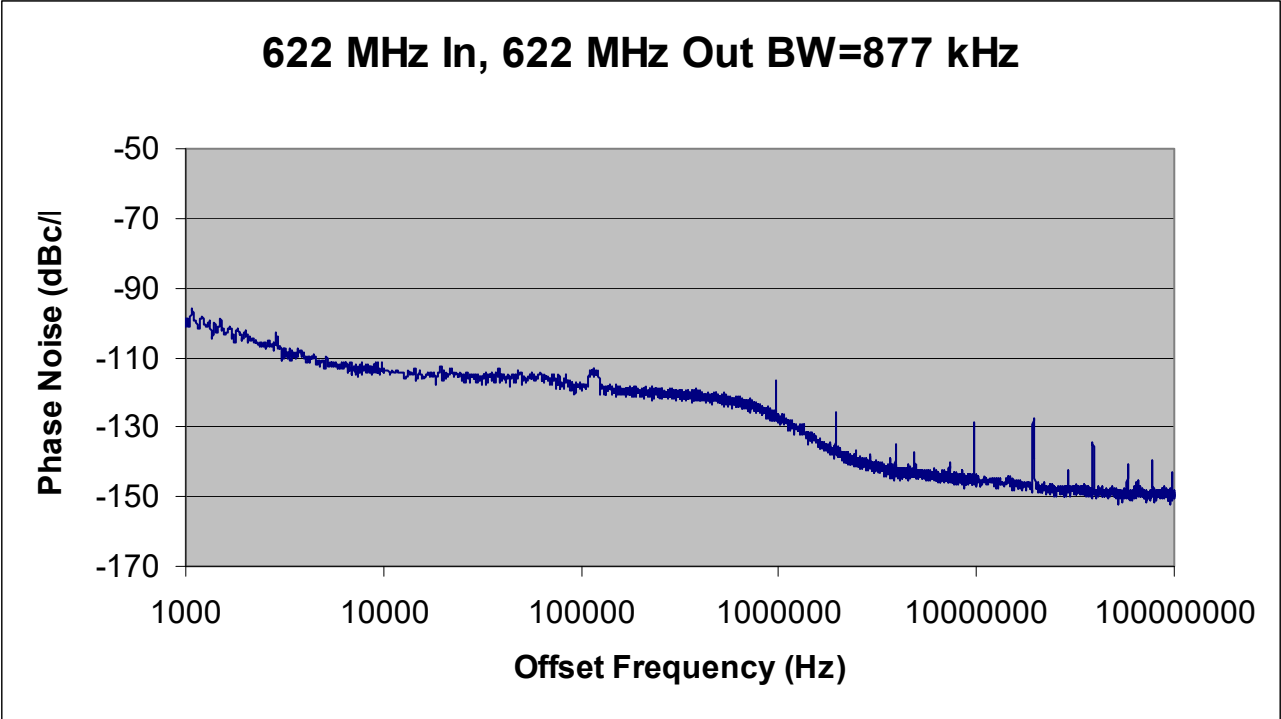


Table 8. Typical RMS Jitter Values

| Jitter Bandwidth            | RMS Jitter (fs) |
|-----------------------------|-----------------|
| OC-48, 12 kHz to 20 MHz     | 374             |
| OC-192, 20 kHz to 80 MHz    | 388             |
| OC-192, 4 MHz to 80 MHz     | 181             |
| OC-192, 50 kHz to 80 MHz    | 377             |
| Broadband, 800 Hz to 80 MHz | 420             |

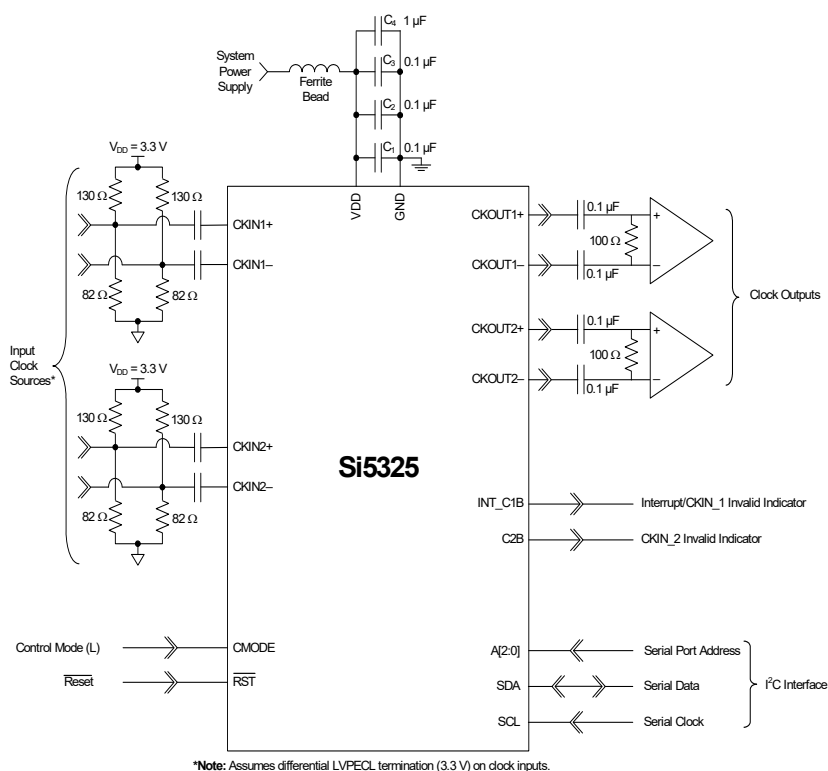
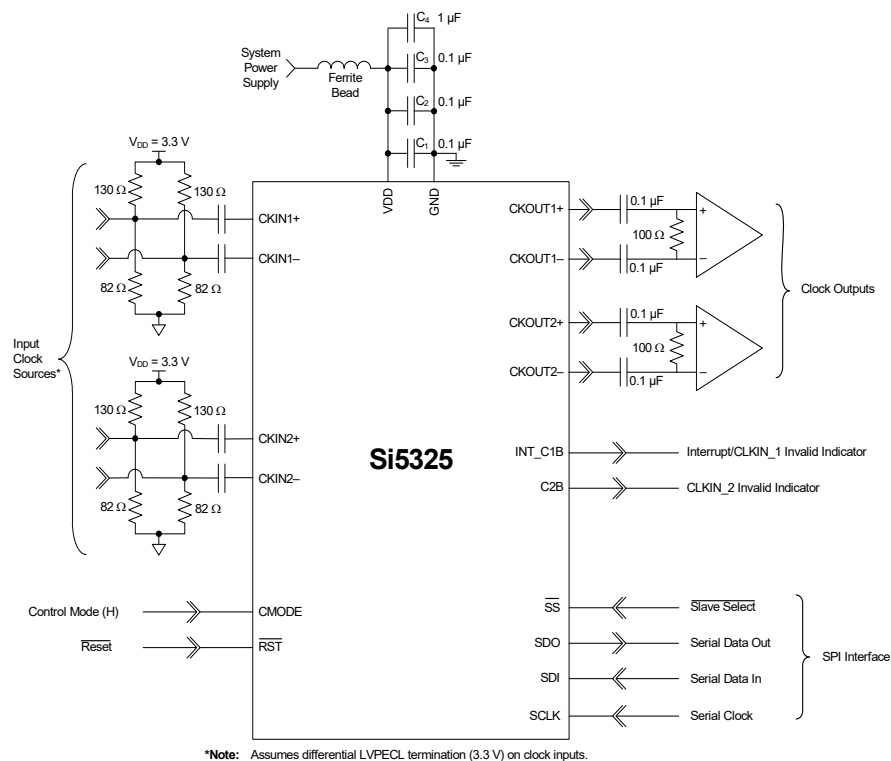
Figure 4. Si5325 Typical Application Circuit (I<sup>2</sup>C Control Mode)

Figure 5. Si5325 Typical Application Circuit (SPI Control Mode)

## 2. Functional Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two synchronous clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The device provides frequency translation across this operating range. Independent dividers are available for each input clock and output clock, so the Si5325 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I<sup>2</sup>C or SPI interface. Skyworks Solutions offers a PC-based software utility, *DSPLLsim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption.

This utility can be downloaded from <https://www.skyworksinc.com/en/Products/Timing>.

The Si5325 is based on Skyworks Solutions' third-generation DSPLL<sup>®</sup> technology, which provides frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5325 PLL loop bandwidth is digitally programmable and supports a range from 150 kHz to 1.3 MHz. The *DSPLLsim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5325 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption.

For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

### 2.1. Further Documentation

Consult the Skyworks Solutions Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5325. Additional design support is available from Skyworks Solutions through your distributor.

Skyworks Solutions has developed a PC-based software utility called *DSPLLsim* to simplify device configuration, including frequency planning and loop bandwidth selection.

The FRM and this utility can be downloaded from <https://www.skyworksinc.com/en/Products/Timing>.

### 3. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

| Register | D7               | D6           | D5              | D4           | D3             | D2              | D1            | D0           |
|----------|------------------|--------------|-----------------|--------------|----------------|-----------------|---------------|--------------|
| 0        |                  |              | CKOUT_ALWAYS_ON |              |                |                 | BYPASS_REG    |              |
| 1        |                  |              |                 |              | CK_PRIOR2[1:0] |                 | CK_PRIOR[1:0] |              |
| 2        | BWSEL_REG[3:0]   |              |                 |              |                |                 |               |              |
| 3        | CKSEL_REG[1:0]   |              |                 | SQ_ICAL      |                |                 |               |              |
| 4        | AUTOSEL_REG[1:0] |              |                 |              |                |                 |               |              |
| 5        | ICMOS[1:0]       |              |                 |              |                |                 |               |              |
| 6        |                  |              | SFOUT2_REG[2:0] |              |                | SFOUT1_REG[2:0] |               |              |
| 7        |                  |              |                 |              |                | FOSREFSEL[2:0]  |               |              |
| 8        | HLOG_2[1:0]      |              | HLOG_1[1:0]     |              |                |                 |               |              |
| 10       |                  |              |                 |              | DSBL2_REG      | DSBL1_REG       |               |              |
| 11       |                  |              |                 |              |                |                 | PD_CK2        | PD_CK1       |
| 19       | FOS_EN           | FOS_THR[1:0] |                 | VALTIME[1:0] |                |                 |               |              |
| 20       |                  |              |                 |              | CK2_BAD_PIN    | CK1_BAD_PIN     |               | INT_PIN      |
| 21       |                  |              |                 |              |                |                 | CK1_ACTV_PIN  | CKSEL_PIN    |
| 22       |                  |              |                 |              | CK_ACTV_POL    | CK_BAD_POL      |               | INT_POL      |
| 23       |                  |              |                 |              |                | LOS2_MSK        | LOS1_MSK      |              |
| 24       |                  |              |                 |              |                | FOS2_MSK        | FOS1_MSK      |              |
| 25       | N1_HS[2:0]       |              |                 |              |                |                 |               |              |
| 31       |                  |              |                 |              | NC1_LS[19:16]  |                 |               |              |
| 32       | NC1_LS[15:8]     |              |                 |              |                |                 |               |              |
| 33       | NC1_LS[7:0]      |              |                 |              |                |                 |               |              |
| 34       |                  |              |                 |              | NC2_LS[19:16]  |                 |               |              |
| 35       | NC2_LS[15:8]     |              |                 |              |                |                 |               |              |
| 36       | NC2_LS[7:0]      |              |                 |              |                |                 |               |              |
| 40       |                  |              |                 |              | N2_LS[19:16]   |                 |               |              |
| 41       | N2_LS[15:8]      |              |                 |              |                |                 |               |              |
| 42       | N2_LS[7:0]       |              |                 |              |                |                 |               |              |
| 43       |                  |              |                 |              |                | N31[18:16]      |               |              |
| 44       | N31[15:8]        |              |                 |              |                |                 |               |              |
| 45       | N31[7:0]         |              |                 |              |                |                 |               |              |
| 46       |                  |              |                 |              |                | N32[18:16]      |               |              |
| 47       | N32[15:8]        |              |                 |              |                |                 |               |              |
| 48       | N32[7:0]         |              |                 |              |                |                 |               |              |
| 55       |                  |              | CLKIN2RATE[2:0] |              |                | CLKIN1RATE[2:0] |               |              |
| 128      |                  |              |                 |              |                |                 | CK2_ACTV_REG  | CK1_ACTV_REG |

| Register | D7                    | D6   | D5           | D4           | D3            | D2       | D1            | D0            |
|----------|-----------------------|------|--------------|--------------|---------------|----------|---------------|---------------|
| 129      |                       |      |              |              |               | LOS2_INT | LOS1_INT      |               |
| 130      |                       |      |              |              |               | FOS2_INT | FOS1_INT      |               |
| 131      |                       |      |              |              |               | LOS2_FLG | LOS1_FLG      |               |
| 132      |                       |      |              |              | FOS2_FLG      | FOS1_FLG |               |               |
| 134      | PARTNUM_RO[11:4]      |      |              |              |               |          |               |               |
| 135      | PARTNUM_RO[3:0]       |      |              |              | REVID_RO[3:0] |          |               |               |
| 136      | RST_REG               | ICAL |              |              |               |          |               |               |
| 138      |                       |      |              |              |               |          | LOS2_EN [1:1] | LOS1_EN [1:1] |
| 139      |                       |      | LOS2_EN[0:0] | LOS1_EN[0:0] |               |          | FOS2_EN       | FOS1_EN       |
| 142      | INDEPENDENTSKEW1[7:0] |      |              |              |               |          |               |               |
| 143      | INDEPENDENTSKEW2[7:0] |      |              |              |               |          |               |               |

## 4. Register Descriptions

### Register 0.

| Bit  | D7 | D6 | D5              | D4 | D3 | D2 | D1         | D0 |
|------|----|----|-----------------|----|----|----|------------|----|
| Name |    |    | CKOUT_ALWAYS_ON |    |    |    | BYPASS_REG |    |
| Type | R  | R  | R/W             | R  | R  | R  | R/W        | R  |

Reset value = 0001 0100

| Bit | Name            | Function                                                                                                                                                                                                                                                                                                                                                          |
|-----|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved        |                                                                                                                                                                                                                                                                                                                                                                   |
| 5   | CKOUT_ALWAYS_ON | <b>CKOUT Always On.</b><br>This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 9 on page 51.<br>0: Squelch output until part is calibrated (ICAL).<br>1: Provide an output. Note: The frequency may be significantly off until the part is calibrated.                        |
| 4:2 | Reserved        |                                                                                                                                                                                                                                                                                                                                                                   |
| 1   | BYPASS_REG      | <b>Bypass Register.</b><br>This bit enables or disables the PLL bypass mode. Use only when the device is in VCO freeze or before the first ICAL. Bypass mode is not supported for CMOS output clocks.<br>0: Normal operation<br>1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL. Bypass mode is not supported for CMOS outputs. |
| 0   | Reserved        |                                                                                                                                                                                                                                                                                                                                                                   |

## Register 1.

| Bit  | D7 | D6 | D5 | D4 | D3              | D2 | D1              | D0 |
|------|----|----|----|----|-----------------|----|-----------------|----|
| Name |    |    |    |    | CK_PRIOR2 [1:0] |    | CK_PRIOR1 [1:0] |    |
| Type | R  | R  | R  | R  | R/W             |    | R/W             |    |

Reset value = 1110 0100

| Bit | Name            | Function                                                                                                                                                                                                     |
|-----|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved        |                                                                                                                                                                                                              |
| 3:2 | CK_PRIOR2 [1:0] | <b>CK_PRIOR 2.</b><br>Selects which of the input clocks will be 2nd priority in the autoselection state machine.<br>00: CKIN1 is 2nd priority.<br>01: CKIN2 is 2nd priority.<br>10: Reserved<br>11: Reserved |
| 1:0 | CK_PRIOR1 [1:0] | <b>CK_PRIOR 1.</b><br>Selects which of the input clocks will be 1st priority in the autoselection state machine.<br>00: CKIN1 is 1st priority.<br>01: CKIN2 is 1st priority.<br>10: Reserved<br>11: Reserved |

## Register 2.

| Bit  | D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|----|----|----|----|----|----|----|
| Name | BWSEL_REG [3:0] |    |    |    |    |    |    |    |
| Type | R/W             |    |    |    | R  | R  | R  | R  |

Reset value = 0100 0010

| Bit | Name            | Function                                                                                                                                                                                    |
|-----|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | BWSEL_REG [3:0] | <b>BWSEL_REG.</b><br>Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect. |
| 3:0 | Reserved        |                                                                                                                                                                                             |

**Register 3.**

| Bit         | D7              | D6 | D5 | D4      | D3 | D2 | D1 | D0 |
|-------------|-----------------|----|----|---------|----|----|----|----|
| <b>Name</b> | CKSEL_REG [1:0] |    |    | SQ_ICAL |    |    |    |    |
| <b>Type</b> | R/W             |    | R  | R/W     | R  | R  | R  | R  |

Reset value = 0000 0101

| Bit | Name            | Function                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | CKSEL_REG [1:0] | <b>CKSEL_REG.</b><br>If the device is operating in register-based manual clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1 and AUTOSEL_REG = 00, the CS_CA input pin continues to control clock selection and CKSEL_REG is of no consequence.<br>00: CKIN_1 selected.<br>01: CKIN_2 selected.<br>10: Reserved<br>11: Reserved |
| 5   | Reserved        |                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 4   | SQ_ICAL         | <b>SQ_ICAL.</b><br>This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 9 on page 51.<br>0: Output clocks enabled during ICAL.<br>1: Output clocks disabled during ICAL.                                                                                                                                                                             |
| 3:0 | Reserved        |                                                                                                                                                                                                                                                                                                                                                                                                                                   |

## Register 4.

| Bit  | D7                | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | AUTOSEL_REG [1:0] |    |    |    |    |    |    |    |
| Type | R/W               |    | R  | R  | R  | R  | R  | R  |

Reset value = 0001 0010

| Bit | Name              | Function                                                                                                                                                                                                                    |
|-----|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | AUTOSEL_REG [1:0] | <b>AUTOSEL_REG [1:0].</b><br>Selects method of input clock selection to be used.<br>00: Manual (either register or pin controlled, see CKSEL_PIN)<br>01: Automatic Non-Revertive<br>10: Automatic Revertive<br>11: Reserved |
| 5:0 | Reserved          |                                                                                                                                                                                                                             |

## Register 5.

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | ICMOS [1:0] |    |    |    |    |    |    |    |
| Type | R/W         |    | R  | R  | R  | R  | R  | R  |

Reset value = 1110 1101

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                                         |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | ICMOS [1:0] | <b>ICMOS [1:0].</b><br>When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-.<br>00: 8 mA/2 mA.<br>01: 16 mA/4 mA<br>10: 24 mA/6 mA<br>11: 32 mA/8 mA |
| 5:0 | Reserved    |                                                                                                                                                                                                                                                                                                                                  |

**Register 6.**

| Bit  | D7 | D6 | D5               | D4 | D3 | D2               | D1 | D0 |
|------|----|----|------------------|----|----|------------------|----|----|
| Name |    |    | SFOUT2_REG [2:0] |    |    | SFOUT1_REG [2:0] |    |    |
| Type | R  | R  | R/W              |    |    | R/W              |    |    |

Reset value = 0010 1101

| Bit | Name             | Function                                                                                                                                                                                                                                                                                                                           |
|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved         |                                                                                                                                                                                                                                                                                                                                    |
| 5:3 | SFOUT2_REG [2:0] | <b>SFOUT2_REG [2:0].</b><br>Controls output signal format and disable for CKOUT2 output buffer. Bypass mode is not supported for CMOS output clocks.<br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode is not supported for CMOS outputs)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |
| 2:0 | SFOUT1_REG [2:0] | <b>SFOUT1_REG [2:0].</b><br>Controls output signal format and disable for CKOUT1 output buffer. Bypass mode is not supported for CMOS output clocks.<br>000: Reserved<br>001: Disable<br>010: CMOS (Bypass mode is not supported for CMOS outputs)<br>011: Low swing LVDS<br>100: Reserved<br>101: LVPECL<br>110: CML<br>111: LVDS |

## Register 7.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2              | D1 | D0 |
|------|----|----|----|----|----|-----------------|----|----|
| Name |    |    |    |    |    | FOSREFSEL [2:0] |    |    |
| Type | R  | R  | R  | R  | R  | R/W             |    |    |

Reset value = 0010 1010

| Bit | Name            | Function                                                                                                                                                                                                                                                                        |
|-----|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved        |                                                                                                                                                                                                                                                                                 |
| 2:0 | FOSREFSEL [2:0] | <b>FOSREFSEL [2:0].</b><br>Selects which input clock is used as the reference frequency for Frequency Off-Set (FOS) alarms.<br>000: XA/XB (External reference)<br>001: CKIN1<br>010: CKIN2<br>011: Reserved<br>100: Reserved<br>101: Reserved<br>110: Reserved<br>111: Reserved |

**Register 8.**

| Bit  | D7          | D6 | D5          | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|-------------|----|----|----|----|----|
| Name | HLOG_2[1:0] |    | HLOG_1[1:0] |    |    |    |    |    |
| Type | R/W         |    | R/W         |    | R  | R  | R  | R  |

Reset value = 0000 0000

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                             |
|-----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | HLOG_2 [1:0] | <b>HLOG_2 [1:0].</b><br>00: Normal operation<br>01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.<br>10: Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.<br>11: Reserved |
| 5:4 |              | <b>HLOG_1 [1:0].</b><br>00: Normal operation<br>01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses.<br>10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses.<br>11: Reserved |
| 3:0 | Reserved     |                                                                                                                                                                                                                                                                                                                      |

## Register 10.

| Bit  | D7 | D6 | D5 | D4 | D3        | D2        | D1       | D0       |
|------|----|----|----|----|-----------|-----------|----------|----------|
| Name |    |    |    |    | DSBL2_REG | DSBL1_REG | Reserved | Reserved |
| Type | R  | R  | R  | R  | R/W       | R/W       | R        | R        |

Reset value = 0000 0000

| Bit | Name      | Function                                                                                                                                                                                               |
|-----|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved  |                                                                                                                                                                                                        |
| 3   | DSBL2_REG | <b>DSBL2_REG.</b><br>This bit controls the powerdown of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down.<br>0: CKOUT2 enabled<br>1: CKOUT2 disabled |
| 2   | DSBL1_REG | <b>DSBL1_REG.</b><br>This bit controls the powerdown of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down.<br>0: CKOUT1 enabled<br>1: CKOUT1 disabled |
| 1:0 | Reserved  |                                                                                                                                                                                                        |

## Register 11.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2 | D1     | D0     |
|------|----|----|----|----|----|----|--------|--------|
| Name |    |    |    |    |    |    | PD_CK2 | PD_CK1 |
| Type | R  | R  | R  | R  | R  | R  | R/W    | R/W    |

Reset value = 0100 0000

| Bit | Name     | Function                                                                                                              |
|-----|----------|-----------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved |                                                                                                                       |
| 1   | PD_CK2   | <b>PD_CK2.</b><br>This bit controls the powerdown of the CKIN2 input buffer.<br>0: CKIN2 enabled<br>1: CKIN2 disabled |
| 0   | PD_CK1   | <b>PD_CK1.</b><br>This bit controls the powerdown of the CKIN1 input buffer.<br>0: CKIN1 enabled<br>1: CKIN1 disabled |

**Register 12.**

| Bit  | D7     | D6            | D5 | D4            | D3 | D2 | D1 | D0 |
|------|--------|---------------|----|---------------|----|----|----|----|
| Name | FOS_EN | FOS_THR [1:0] |    | VALTIME [1:0] |    |    |    |    |
| Type | R/W    | R/W           |    | R/W           |    | R  | R  | R  |

Reset value = 0010 1100

| Bit | Name          | Function                                                                                                                                                                                                                                                                                              |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | FOS_EN        | <b>FOS_EN.</b><br>Frequency Offset Enable globally disables FOS. See the individual FOS enables (FOSX_EN, register 139).<br>0: FOS disable<br>1: FOS enabled by FOSx_EN                                                                                                                               |
| 6:5 | FOS_THR [1:0] | <b>FOS_THR [1:0].</b><br>Frequency Offset at which FOS is declared:<br>00: $\pm 11$ to 12 ppm (Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK)<br>01: $\pm 48$ to 49 ppm (SMC)<br>10: $\pm 30$ ppm (SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK.<br>11: $\pm 200$ ppm |
| 4:3 | VALTIME [1:0] | <b>VALTIME [1:0].</b><br>Sets amount of time for input clock to be valid before the associated alarm is removed.<br>00: 2 ms<br>01: 100 ms<br>10: 200 ms<br>11: 13 seconds                                                                                                                            |
| 2:0 | Reserved      |                                                                                                                                                                                                                                                                                                       |

## Register 13.

| Bit  | D7 | D6 | D5 | D4 | D3          | D2          | D1 | D0      |
|------|----|----|----|----|-------------|-------------|----|---------|
| Name |    |    |    |    | CK2_BAD_PIN | CK1_BAD_PIN |    | INT_PIN |
| Type | R  | R  | R  | R  | R/W         | R/W         | R  | R/W     |

Reset value = 0011 1110

| Bit | Name        | Function                                                                                                                                                                                                                                                                                           |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved    |                                                                                                                                                                                                                                                                                                    |
| 3   | CK2_BAD_PIN | <b>CK2_BAD_PIN.</b><br>The CK2_BAD status can be reflected on the C2B output pin.<br>0: C2B output pin tristated<br>1: C2B status reflected to output pin                                                                                                                                          |
| 2   | CK1_BAD_PIN | <b>CK1_BAD_PIN.</b><br>The CK1_BAD status can be reflected on the C1B output pin.<br>0: C1B output pin tristated<br>1: C1B status reflected to output pin                                                                                                                                          |
| 1   | Reserved    |                                                                                                                                                                                                                                                                                                    |
| 0   | INT_PIN     | <b>INT_PIN.</b><br>Reflects the interrupt status on the INT_C1B output pin.<br>0: Interrupt status not displayed on INT_C1B output pin. If CK1_BAD_PIN = 0, INT_C1B output pin is tristated.<br>1: Interrupt status reflected to output pin. Instead, the INT_C1B pin indicates when CKIN1 is bad. |

**Register 14.**

| Bit  | D7 | D6      | D5 | D4 | D3 | D2 | D1           | D0        |
|------|----|---------|----|----|----|----|--------------|-----------|
| Name |    |         |    |    |    |    | CK1_ACTV_PIN | CKSEL_PIN |
| Type | R  | Force 1 | R  | R  | R  | R  | R/W          | R/W       |

Reset value = 1111 1111

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                                                          |
|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved     |                                                                                                                                                                                                                                                                                                                                                   |
| 1   | CK1_ACTV_PIN | <b>CK1_ACTV_PIN.</b><br>The CK1_ACTV_REG status bit can be reflected to the CS_CA output pin using the CK1_ACTV_PIN enable function. CK1_ACTV_PIN is of consequence only when pin controlled clock selection is not being used.<br>0: CS_CA output pin tristated.<br>1: Clock Active status reflected to output pin.                              |
| 0   | CKSEL_PIN    | <b>CKSEL_PIN.</b><br>If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CS_CA input pin. This bit is only active when AUTOSEL_REG = Manual.<br>0: CS_CA pin is ignored. CKSEL_REG[1:0] register bits control clock selection.<br>1: CS_CA input pin controls clock selection. |

## Register 15.

| Bit  | D7 | D6 | D5 | D4 | D3          | D2         | D1 | D0      |
|------|----|----|----|----|-------------|------------|----|---------|
| Name |    |    |    |    | CK_ACTV_POL | CK_BAD_POL |    | INT_POL |
| Type | R  | R  | R  | R  | R/W         | R/W        | R  | R/W     |

Reset value = 1101 1111

| Bit | Name        | Function                                                                                                                                          |
|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved    |                                                                                                                                                   |
| 3   | CK_ACTV_POL | <b>CK_ACTV_POL.</b><br>Sets the active polarity for the CS_CA signals when reflected on an output pin.<br>0: Active low<br>1: Active high         |
| 2   | CK_BAD_POL  | <b>CK_BAD_POL.</b><br>Sets the active polarity for the INT_C1B and C2B signals when reflected on output pins.<br>0: Active low<br>1: Active high  |
| 1   | Reserved    |                                                                                                                                                   |
| 0   | INT_POL     | <b>INT_POL.</b><br>Sets the active polarity for the interrupt status when reflected on the INT_C1B output pin.<br>0: Active low<br>1: Active high |

**Register 16.**

| Bit  | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0       |
|------|----|----|----|----|----|----------|----------|----------|
| Name |    |    |    |    |    | LOS2_MSK | LOS1_MSK | Reserved |
| Type | R  | R  | R  | R  | R  | R/W      | R/W      | R        |

Reset value = 0001 1111

| Bit | Name     | Function                                                                                                                                                                                                                                                                                                                  |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved |                                                                                                                                                                                                                                                                                                                           |
| 2   | LOS2_MSK | <b>LOS2_MSK.</b><br>Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register.<br>0: LOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1).<br>1: LOS2_FLG ignored in generating interrupt output. |
| 1   | LOS1_MSK | <b>LOS1_MSK.</b><br>Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register.<br>0: LOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1).<br>1: LOS1_FLG ignored in generating interrupt output. |
| 0   | Reserved |                                                                                                                                                                                                                                                                                                                           |

## Register 17.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0 |
|------|----|----|----|----|----|----------|----------|----|
| Name |    |    |    |    |    | FOS2_MSK | FOS1_MSK |    |
| Type | R  | R  | R  | R  | R  | R/W      | R/W      | R  |

Reset value = 0011 1111

| Bit | Name     | Function                                                                                                                                                                                                                                                                                                        |
|-----|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved |                                                                                                                                                                                                                                                                                                                 |
| 2   | FOS2_MSK | <b>FOS2_MSK.</b><br>Determines if the FOS2_FLG is used to in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register.<br>0: FOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1).<br>1: FOS2_FLG ignored in generating interrupt output. |
| 1   | FOS1_MSK | <b>FOS1_MSK.</b><br>Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register.<br>0: FOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1).<br>1: FOS1_FLG ignored in generating interrupt output.    |
| 0   | Reserved |                                                                                                                                                                                                                                                                                                                 |

**Register 18.**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | N1_HS [2:0] |    |    |    |    |    |    |    |
| Type | R/W         |    |    | R  | R  | R  | R  | R  |

Reset value = 0010 0000

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                             |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | N1_HS [2:0] | <b>N1_HS [2:0].</b><br>Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 2) low-speed divider.<br>000: N1 = 4 Note: Changing the coarse skew via the INC pin is disabled for this value.<br>001: N1 = 5<br>010: N1 = 6<br>011: N1 = 7<br>100: N1 = 8<br>101: N1 = 9<br>110: N1 = 10<br>111: N1 = 11 |
| 4:0 | Reserved    |                                                                                                                                                                                                                                                                                                                      |

**Register 31.**

| Bit  | D7 | D6 | D5 | D4 | D3             | D2 | D1 | D0 |
|------|----|----|----|----|----------------|----|----|----|
| Name |    |    |    |    | NC1_LS [19:16] |    |    |    |
| Type | R  | R  | R  | R  | R/W            |    |    |    |

Reset value = 0000 0000

| Bit | Name           | Function                                                                                                                                                                                                                                                                                                                       |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved       |                                                                                                                                                                                                                                                                                                                                |
| 3:0 | NC1_LS [19:16] | <b>NC1_LS [19:16].</b><br>Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

## Register 32.

| Bit  | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | NC1_LS [15:8] |    |    |    |    |    |    |    |
| Type | R/W           |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                      |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | NC1_LS [15:8] | <b>NC1_LS [15:8].</b><br>Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

## Register 33.

| Bit  | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | NC1_LS [7:0] |    |    |    |    |    |    |    |
| Type | R/W          |    |    |    |    |    |    |    |

Reset value = 0011 0001

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                     |
|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | NC1_LS [19:0] | <b>NC1_LS [7:0].</b><br>Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

**Register 34.**

| Bit  | D7 | D6 | D5 | D4 | D3             | D2 | D1 | D0 |
|------|----|----|----|----|----------------|----|----|----|
| Name |    |    |    |    | NC2_LS [19:16] |    |    |    |
| Type | R  | R  | R  | R  | R/W            |    |    |    |

Reset value = 0000 0000

| Bit | Name           | Function                                                                                                                                                                                                                                                                                                                       |
|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved       |                                                                                                                                                                                                                                                                                                                                |
| 3:0 | NC2_LS [19:16] | <b>NC2_LS [19:16].</b><br>Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

**Register 35.**

| Bit  | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | NC2_LS [15:8] |    |    |    |    |    |    |    |
| Type | R/W           |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                      |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | NC2_LS [15:8] | <b>NC2_LS [15:8].</b><br>Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

## Register 36.

| Bit  | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | NC2_LS [7:0] |    |    |    |    |    |    |    |
| Type | R/W          |    |    |    |    |    |    |    |

Reset value = 0011 0001

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                                     |
|-----|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | NC2_LS [7:0] | <b>NC2_LS [7:0].</b><br>Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000011 = 4<br>00000000000000000101 = 6<br>...<br>11111111111111111111 = $2^{20}$<br>Valid divider values = [1, 2, 4, 6, ..., $2^{20}$ ] |

## Register 40.

| Bit  | D7 | D6 | D5 | D4 | D3            | D2 | D1 | D0 |
|------|----|----|----|----|---------------|----|----|----|
| Name |    |    |    |    | N2_LS [19:16] |    |    |    |
| Type | R  |    |    |    | R/W           |    |    |    |

Reset value = 1100 0000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                       |
|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved      |                                                                                                                                                                                                                                                                                                                                                |
| 3:0 | N2_LS [19:16] | <b>N2_LS [19:16].</b><br>Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive).<br><br>00000000000000100000 = 32<br>00000000000000100010 = 34<br>00000000000000100100 = 36<br>...<br>00000000001000000000 = 512<br>Valid divider values = [32, 34, 36...512] |

**Register 41.**

| Bit         | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|----|----|----|----|----|----|----|
| <b>Name</b> | N2_LS [15:8] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W          |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N2_LS [15:8] | <p><b>N2_LS [15:8].</b><br/>Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive).</p> <p>00000000000000100000 = 32<br/> 00000000000000100010 = 34<br/> 00000000000000100100 = 36<br/> ...<br/> 00000000001000000000 = 512</p> <p>Valid divider values = [32, 34, 36...512]</p> |

**Register 42.**

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | N2_LS [7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 1111 1001

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N2_LS [7:0] | <p><b>N2_LS [7:0].</b><br/>Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive).</p> <p>00000000000000100000 = 32<br/> 00000000000000100010 = 34<br/> 00000000000000100100 = 36<br/> ...<br/> 00000000001000000000 = 512</p> <p>Valid divider values = [32, 34, 36...512]</p> |

## Register 43.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2          | D1 | D0 |
|------|----|----|----|----|----|-------------|----|----|
| Name |    |    |    |    |    | N31 [18:16] |    |    |
| Type | R  | R  | R  | R  | R  | R/W         |    |    |

Reset value = 0000 0000

| Bit | Name        | Function                                                                                                                                                                                                                                         |
|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved    |                                                                                                                                                                                                                                                  |
| 2:0 | N31 [18:16] | <b>N31 [18:16].</b><br>Sets value for input divider for CKIN1.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values = [1, 2, 3, ..., $2^{19}$ ] |

## Register 44.

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | N31_[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name       | Function                                                                                                                                                                                                                                        |
|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N31_[15:8] | <b>N31_[15:8].</b><br>Sets value for input divider for CKIN1.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values = [1, 2, 3, ..., $2^{19}$ ] |

**Register 45.**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | N31_[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 0000 1001

| Bit | Name      | Function                                                                                                                                                                                                                                     |
|-----|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N31_[7:0] | <b>N31_[7:0].</b><br>Sets value for input divider for CKIN1.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values=[1, 2, 3, ..., $2^{19}$ ] |

**Register 46.**

| Bit  | D7 | D6 | D5 | D4 | D3 | D2          | D1 | D0 |
|------|----|----|----|----|----|-------------|----|----|
| Name |    |    |    |    |    | N32_[18:16] |    |    |
| Type | R  | R  | R  | R  | R  | R/W         |    |    |

Reset value = 0000 0000

| Bit | Name        | Function                                                                                                                                                                                                                                         |
|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved    |                                                                                                                                                                                                                                                  |
| 2:0 | N32_[18:16] | <b>N32_[18:16].</b><br>Sets value for input divider for CKIN2.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values = [1, 2, 3, ..., $2^{19}$ ] |

## Register 47.

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | N32_[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name       | Function                                                                                                                                                                                                                                      |
|-----|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N32_[15:8] | <b>N32_[15:8].</b><br>Sets value for input divider for CKIN2.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values=[1, 2, 3, ..., $2^{19}$ ] |

## Register 48.

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | N32_[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 0000 1001

| Bit | Name      | Function                                                                                                                                                                                                                                       |
|-----|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | N32_[7:0] | <b>N32_[7:0].</b><br>Sets value for input divider for CKIN2.<br>00000000000000000000 = 1<br>00000000000000000001 = 2<br>00000000000000000010 = 3<br>...<br>11111111111111111111 = $2^{19}$<br>Valid divider values = [1, 2, 3, ..., $2^{19}$ ] |

**Register 55h.**

| Bit  | D7 | D6 | D5               | D4 | D3 | D2              | D1 | D0 |
|------|----|----|------------------|----|----|-----------------|----|----|
| Name |    |    | CLKIN2RATE_[2:0] |    |    | CLKIN1RATE[2:0] |    |    |
| Type | R  | R  | R/W              |    |    | R/W             |    |    |

Reset value = 0000 0000

| Bit | Name             | Function                                                                                                                                                                                                                           |
|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved         |                                                                                                                                                                                                                                    |
| 5:3 | CLKIN2RATE[2:0]  | <b>CLKIN2RATE[2:0].</b><br>CKINn frequency selection for FOS alarm monitoring.<br>000: 10–27 MHz<br>001: 25–54 MHz<br>002: 50–105 MHz<br>003: 95–215 MHz<br>004: 190–435 MHz<br>005: 375–710 MHz<br>006: Reserved<br>007: Reserved |
| 2:0 | CLKIN1RATE [2:0] | <b>CLKIN1RATE[2:0].</b><br>CKINn frequency selection for FOS alarm monitoring.<br>000: 10–27 MHz<br>001: 25–54 MHz<br>002: 50–105 MHz<br>003: 95–215 MHz<br>004: 190–435 MHz<br>005: 375–710 MHz<br>006: Reserved<br>007: Reserved |

## Register 128.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2 | D1           | D0           |
|------|----|----|----|----|----|----|--------------|--------------|
| Name |    |    |    |    |    |    | CK2_ACTV_REG | CK1_ACTV_REG |
| Type | R  | R  | R  | R  | R  | R  | R            | R            |

Reset value = 0010 0000

| Bit | Name         | Function                                                                                                                                                                                                                  |
|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved     |                                                                                                                                                                                                                           |
| 1   | CK2_ACTV_REG | <b>CK2_ACTV_REG.</b><br>Indicates if CKIN2 is currently the active clock for the PLL input.<br>0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1.<br>1: CKIN2 is the active input clock. |
| 0   | CK1_ACTV_REG | <b>CK1_ACTV_REG.</b><br>Indicates if CKIN1 is currently the active clock for the PLL input.<br>0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1.<br>1: CKIN1 is the active input clock. |

## Register 129.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0 |
|------|----|----|----|----|----|----------|----------|----|
| Name |    |    |    |    |    | LOS2_INT | LOS1_INT |    |
| Type | R  | R  | R  | R  | R  | R        | R        | R  |

Reset value = 0000 0110

| Bit | Name     | Function                                                                                                                           |
|-----|----------|------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved |                                                                                                                                    |
| 2   | LOS2_INT | <b>LOS2_INT.</b><br>Indicates the LOS status on CKIN2.<br>0: Normal operation.<br>1: Internal loss-of-signal alarm on CKIN2 input. |
| 1   | LOS1_INT | <b>LOS1_INT.</b><br>Indicates the LOS status on CKIN1.<br>0: Normal operation.<br>1: Internal loss-of-signal alarm on CKIN1 input. |
| 0   | Reserved |                                                                                                                                    |

**Register 130.**

| Bit  | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0 |
|------|----|----|----|----|----|----------|----------|----|
| Name |    |    |    |    |    | FOS2_INT | FOS1_INT |    |
| Type | R  | R  | R  | R  | R  | R        | R        | R  |

Reset value = 0000 0001

| Bit | Name     | Function                                                                                                            |
|-----|----------|---------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved |                                                                                                                     |
| 2   | FOS2_INT | <b>CKIN2 Frequency Offset Status.</b><br>0: Normal operation.<br>1: Internal frequency offset alarm on CKIN2 input. |
| 1   | FOS1_INT | <b>CKIN1 Frequency Offset Status.</b><br>0: Normal operation.<br>1: Internal frequency offset alarm on CKIN1 input. |
| 0   | Reserved |                                                                                                                     |

## Register 131.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0 |
|------|----|----|----|----|----|----------|----------|----|
| Name |    |    |    |    |    | LOS2_FLG | LOS1_FLG |    |
| Type | R  | R  | R  | R  | R  | R/W      | R/W      | R  |

Reset value = 0001 1111

| Bit | Name     | Function                                                                                                                                                                                                                                               |
|-----|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved |                                                                                                                                                                                                                                                        |
| 2   | LOS2_FLG | <b>CKIN2 Loss-of-Signal Flag.</b><br>0: Normal operation.<br>1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing 0 to this bit. |
| 1   | LOS1_FLG | <b>CKIN1 Loss-of-Signal Flag.</b><br>0: Normal operation<br>1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing 0 to this bit.  |
| 0   | Reserved |                                                                                                                                                                                                                                                        |

**Register 132.**

| Bit  | D7 | D6 | D5 | D4 | D3       | D2       | D1 | D0 |
|------|----|----|----|----|----------|----------|----|----|
| Name |    |    |    |    | FOS2_FLG | FOS1_FLG |    |    |
| Type | R  | R  | R  | R  | R/W      | R/W      | R  | R  |

Reset value = 0000 0010

| Bit    | Name     | Function                                                                                                                                                                                                                                                   |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4, 0 | Reserved |                                                                                                                                                                                                                                                            |
| 3      | FOS2_FLG | <b>CLKIN_2 Frequency Offset Flag.</b><br>0: Normal operation.<br>1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing 0 to this bit. |
| 2      | FOS1_FLG | <b>CLKIN_1 Frequency Offset Flag.</b><br>0: Normal operation<br>1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing 0 to this bit.  |
| 1      | Reserved |                                                                                                                                                                                                                                                            |

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**Register 134.**

---

| Bit  | D7                | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|----|----|----|----|----|----|----|
| Name | PARTNUM_RO [11:4] |    |    |    |    |    |    |    |
| Type | R                 |    |    |    |    |    |    |    |

Reset value = 0000 0001

| Bit | Name              | Function                                             |
|-----|-------------------|------------------------------------------------------|
| 7:0 | PARTNUM_RO [11:0] | <b>Device ID (1 of 2).</b><br>0000 0001 1001: Si5325 |

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**Register 135.**

---

| Bit  | D7               | D6 | D5 | D4 | D3             | D2 | D1 | D0 |
|------|------------------|----|----|----|----------------|----|----|----|
| Name | PARTNUM_RO [3:0] |    |    |    | REVID_RO [3:0] |    |    |    |
| Type | R                |    |    |    | R              |    |    |    |

Reset value = 1010 0010

| Bit | Name              | Function                                                                                                                    |
|-----|-------------------|-----------------------------------------------------------------------------------------------------------------------------|
| 7:4 | PARTNUM_RO [11:0] | <b>Device ID (2 of 2).</b><br>0000 0001 1001: Si5325                                                                        |
| 3:0 | REVID_RO [3:0]    | <b>Indicates Revision Number of Device.</b><br>0000: Revision A<br>0001: Revision B<br>0010: Revision C<br>Others: Reserved |

**Register 136.**

| Bit  | D7      | D6   | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|------|----|----|----|----|----|----|
| Name | RST_REG | ICAL |    |    |    |    |    |    |
| Type | R/W     | R/W  | R  | R  | R  | R  | R  | R  |

Reset value = 0000 0000

| Bit | Name     | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RST_REG  | <b>Internal Reset (Same as Pin Reset).</b><br><b>Note:</b> The I2C (or SPI) port may not be accessed until 10 ms after RST_REG is asserted.<br>0: Normal operation.<br>1: Reset of all internal logic. Outputs disabled or tristated during reset.                                                                                                                                                                                                                                                                                                                                              |
| 6   | ICAL     | <b>Start an Internal Calibration Sequence.</b><br>For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL.<br><b>Note:</b> Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect.<br>0: Normal operation.<br>1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low. |
| 5:0 | Reserved |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## Register 138.

| Bit  | D7 | D6 | D5 | D4 | D3 | D2 | D1            | D0            |
|------|----|----|----|----|----|----|---------------|---------------|
| Name |    |    |    |    |    |    | LOS2_EN [1:1] | LOS1_EN [1:1] |
| Type | R  | R  | R  | R  | R  | R  | R/W           | R/W           |

Reset value = 0000 1111

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                     |
|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved      |                                                                                                                                                                                                                                                                                                                                              |
| 1   | LOS2_EN [1:0] | <b>Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).</b><br><b>Note:</b> LOS2_EN is split between two registers.<br>00: Disable LOS monitoring.<br>01: Reserved.<br>10: Enable LOSA monitoring.<br>11: Enable LOS monitoring.<br>LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details. |
| 0   | LOS1_EN [1:0] | <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b><br><b>Note:</b> LOS1_EN is split between two registers.<br>00: Disable LOS monitoring.<br>01: Reserved.<br>10: Enable LOSA monitoring.<br>11: Enable LOS monitoring.<br>LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details. |

**Register 139.**

| Bit  | D7 | D6 | D5            | D4            | D3 | D2 | D1      | D0      |
|------|----|----|---------------|---------------|----|----|---------|---------|
| Name |    |    | LOS2_EN [0:0] | LOS1_EN [0:0] |    |    | FOS2_EN | FOS1_EN |
| Type | R  | R  | R/W           | R/W           | R  | R  | R/W     | R/W     |

Reset value = 1111 1111

| Bit         | Name          | Function                                                                                                                                                                                                                                                                                                                                     |
|-------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6,<br>3:2 | Reserved      |                                                                                                                                                                                                                                                                                                                                              |
| 5           | LOS2_EN [1:0] | <b>Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).</b><br><b>Note:</b> LOS2_EN is split between two registers.<br>00: Disable LOS monitoring.<br>01: Reserved.<br>10: Enable LOSA monitoring.<br>11: Enable LOS monitoring.<br>LOSA is a slower and less sensitive version of LOS. See the family reference manual for details  |
| 4           | LOS1_EN [1:0] | <b>Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).</b><br><b>Note:</b> LOS1_EN is split between two registers.<br>00: Disable LOS monitoring.<br>01: Reserved.<br>10: Enable LOSA monitoring.<br>11: Enable LOS monitoring.<br>LOSA is a slower and less sensitive version of LOS. See the family reference manual for details. |
| 1           | FOS2_EN       | <b>Enables FOS on a Per Channel Basis.</b><br>0: Disable FOS monitoring.<br>1: Enable FOS monitoring.                                                                                                                                                                                                                                        |
| 0           | FOS1_EN       | <b>Enables FOS on a Per Channel Basis.</b><br>0: Disable FOS monitoring.<br>1: Enable FOS monitoring.                                                                                                                                                                                                                                        |

---

**Register 142.**

---

| Bit  | D7                     | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW1 [7:0] |    |    |    |    |    |    |    |
| Type | R/W                    |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name                   | Function                                                                                                                                                          |
|-----|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | INDEPENDENTSKEW1 [7:0] | <b>INDEPENDENTSKEW1.</b><br>8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. Default = 0. |

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**Register 143.**

---

| Bit  | D7                     | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------|----|----|----|----|----|----|----|
| Name | INDEPENDENTSKEW2 [7:0] |    |    |    |    |    |    |    |
| Type | R/W                    |    |    |    |    |    |    |    |

Reset value = 0000 0000

| Bit | Name                    | Function                                                                                                                                                          |
|-----|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | INDEPEND-ENTSKEW2 [7:0] | <b>INDEPENDENTSKEW2.</b><br>8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. Default = 0. |

**Table 9. CKOUT\_ALWAYS\_ON and SQICAL Truth Table**

| CKOUT_ALWAYS_ON | SQICAL | Results                                                                 | Output to Output Skew Preserved? |
|-----------------|--------|-------------------------------------------------------------------------|----------------------------------|
| 0               | 0      | CKOUT OFF until after the first ICAL                                    | N                                |
| 0               | 1      | CKOUT OFF until after the first successful ICAL (i.e., when LOL is low) | Y                                |
| 1               | 0      | CKOUT always ON, including during an ICAL                               | N                                |
| 1               | 1      | CKOUT always ON, including during an ICAL                               | Y                                |

Table 10 lists all of the register locations that should be followed by an ICAL after their contents are changed.

**Table 10. Register Locations Requiring ICAL**

| Addr | Register        |
|------|-----------------|
| 0    | BYPASS_REG      |
| 0    | CKOUT_ALWAYS_ON |
| 1    | CK_PRIOR2       |
| 1    | CK_PRIOR1       |
| 2    | BWSEL_REG       |
| 4    | HIST_DEL        |
| 5    | ICMOS           |
| 7    | FOSREFSEL       |
| 9    | HIST_AVG        |
| 10   | DSBL2_REG       |
| 10   | DSBL1_REG       |
| 11   | PD_CK2          |
| 11   | PD_CK1          |
| 19   | FOS_EN          |
| 19   | FOS_THR         |
| 19   | VALTIME         |
| 19   | LOCKT           |
| 25   | N1_HS           |
| 31   | NC1_LS          |
| 34   | NC2_LS          |
| 40   | N2_HS           |
| 40   | N2_LS           |
| 43   | N31             |
| 46   | N32             |
| 55   | CLKIN2RATE      |
| 55   | CLKIN1RATE      |

## 5. Pin Descriptions: Si5325

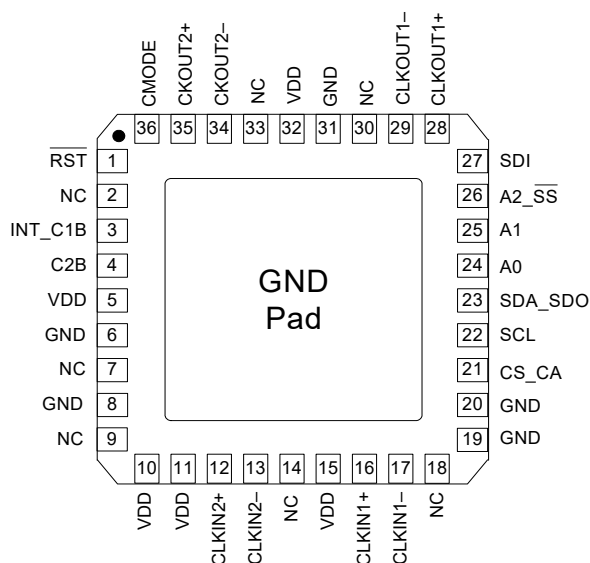


**Table 11. Si5325 Pin Descriptions**

| Pin #                                                                                                                     | Pin Name                | I/O | Signal Level | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------------------------------------------------------------------------------|-------------------------|-----|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                                                                                         | $\overline{\text{RST}}$ | I   | LVC MOS      | <b>External Reset.</b><br>Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details.<br>This pin has a weak pull-up.                                                                                                                                                                                                                                            |
| 2, 7, 9, 14, 18, 30, 33                                                                                                   | NC                      |     |              | <b>No Connect.</b><br>This pin must be left unconnected for normal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 3                                                                                                                         | INT_C1B                 | O   | LVC MOS      | <b>Interrupt/CKIN1 Invalid Indicator.</b><br>This pin functions as a device interrupt output or an alarm output for CKIN1. If used as an interrupt output, <i>INT_PIN</i> must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the <i>INT_POL</i> register bit.<br>If used as an alarm output, the pin functions as a LOS (and optionally FOS) alarm indicator for CKIN1. Set <i>CK1_BAD_PIN</i> = 1 and <i>INT_PIN</i> = 0.<br>0 = CKIN1 present.<br>1 = LOS (FOS) on CKIN1.<br>The active polarity is controlled by <i>CK_BAD_POL</i> . If no function is selected, the pin tristates. |
| <b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i> . See Si5325 Register Map. |                         |     |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

Table 11. Si5325 Pin Descriptions (Continued)

| Pin #                                                                                                                     | Pin Name         | I/O             | Signal Level | Description                                                                                                                                                                                                                                                                                                    |
|---------------------------------------------------------------------------------------------------------------------------|------------------|-----------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4                                                                                                                         | C2B              | O               | LVC MOS      | <b>CKIN2 Invalid Indicator.</b><br>This pin functions as a LOS (and optionally FOS) alarm indicator for CKIN2 if <i>CK2_BAD_PIN</i> = 1.<br>0 = CKIN2 present.<br>1 = LOS (FOS) on CKIN2.<br>The active polarity can be changed by <i>CK_BAD_POL</i> . If <i>CK2_BAD_PIN</i> = 0, the pin tristates.           |
| 5, 10, 11,<br>15, 32                                                                                                      | V <sub>DD</sub>  | V <sub>DD</sub> | Supply       | <b>Supply.</b><br>The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following VDD pins:<br>5                    0.1 µF<br>10                   0.1 µF<br>32                   0.1 µF<br>A 1.0 µF should also be placed as close to device as is practical. |
| 6, 8, 19,<br>20 31                                                                                                        | GND              | GND             | Supply       | <b>Ground.</b><br>Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.                                                                                                                                                                               |
| 12<br>13                                                                                                                  | CKIN2+<br>CKIN2– | I               | Multi        | <b>Clock Input 2.</b><br>Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.                                                                                                                                                           |
| 16<br>17                                                                                                                  | CKIN1+<br>CKIN1– | I               | Multi        | <b>Clock Input 1.</b><br>Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.                                                                                                                                                           |
| <b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i> . See Si5325 Register Map. |                  |                 |              |                                                                                                                                                                                                                                                                                                                |

Table 11. Si5325 Pin Descriptions (Continued)

| Pin #                                                                                                                           | Pin Name | I/O | Signal Level | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------------------------------------------------------------------------------------|----------|-----|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 21                                                                                                                              | CS_CA    | I/O | LVC MOS      | <p><b>Input Clock Select/Active Clock Indicator.</b></p> <p><b>Input:</b> In manual clock selection mode, this pin functions as the manual input clock selector if the <i>CKSEL_PIN</i> is set to 1.<br/> 0 = Select CKIN1.<br/> 1 = Select CKIN2.<br/> If <i>CKSEL_PIN</i> = 0, the <i>CKSEL_REG</i> register bit controls this function. If configured as input, must be set high or low.</p> <p><b>Output:</b> In automatic clock selection mode, this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both clocks, CA will indicate the last active clock that was used before entering the VCO freeze state. The <i>CK_ACTV_PIN</i> register bit must be set to 1 to reflect the active clock status to the CA output pin.<br/> 0 = CKIN1 active input clock.<br/> 1 = CKIN2 active input clock.<br/> If <i>CK_ACTV_PIN</i> = 0, this pin will tristate. The CA status will always be reflected in the <i>CK_ACT-V_REG</i> read only register bit.</p> |
| 22                                                                                                                              | SCL      | I   | LVC MOS      | <p><b>Serial Clock/Serial Clock.</b></p> <p>This pin functions as the serial clock input for both SPI and I<sup>2</sup>C modes.<br/> This pin has a weak pulldown.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 23                                                                                                                              | SDA_SDO  | I/O | LVC MOS      | <p><b>Serial Data.</b></p> <p>In I<sup>2</sup>C control mode (CMODE = 0), this pin functions as the bidirectional serial data port.<br/> In SPI control mode (CMODE = 1), this pin functions as the serial data output.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 25<br>24                                                                                                                        | A1<br>A0 | I   | LVC MOS      | <p><b>Serial Port Address.</b></p> <p>In I<sup>2</sup>C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I<sup>2</sup>C address is 1101 [A2] [A1] [A0].<br/> In SPI control mode (CMODE = 1), these pins are ignored.<br/> This pin has a weak pulldown.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 26                                                                                                                              | A2_SS    | I   | LVC MOS      | <p><b>Serial Port Address/Slave Select.</b></p> <p>In I<sup>2</sup>C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2].<br/> In SPI control mode (CMODE = 1), this pin functions as the slave select input.<br/> This pin has a weak pulldown.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <p><b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i>. See Si5325 Register Map.</p> |          |     |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

Table 11. Si5325 Pin Descriptions (Continued)

| Pin #                                                                                                                     | Pin Name           | I/O | Signal Level | Description                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------------------------------------------------------------------------------|--------------------|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27                                                                                                                        | SDI                | I   | LVCMOS       | <b>Serial Data In.</b><br>In I <sup>2</sup> C control mode (CMODE = 0), this pin is ignored.<br>In SPI control mode (CMODE = 1), this pin functions as the serial data input.<br>This pin has a weak pulldown.                                                                                                            |
| 29<br>28                                                                                                                  | CKOUT1–<br>CKOUT1+ | O   | Multi        | <b>Output Clock 1.</b><br>Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by <i>SFOUT1_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 34<br>35                                                                                                                  | CKOUT2–<br>CKOUT2+ | O   | Multi        | <b>Output Clock 2.</b><br>Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by <i>SFOUT2_REG</i> register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs. |
| 36                                                                                                                        | CMODE              | I   | LVCMOS       | <b>Control Mode.</b><br>Selects I <sup>2</sup> C or SPI control mode for the Si5325.<br>0 = I <sup>2</sup> C Control Mode.<br>1 = SPI Control Mode.<br>Must not float.                                                                                                                                                    |
| GND PAD                                                                                                                   | GND                | GND | Supply       | <b>Ground Pad.</b><br>The ground pad must provide a low thermal and electrical impedance to a ground plane.                                                                                                                                                                                                               |
| <b>Note:</b> Internal register names are indicated by underlined italics, e.g., <i>INT_PIN</i> . See Si5325 Register Map. |                    |     |              |                                                                                                                                                                                                                                                                                                                           |

## 6. Ordering Guide

| Ordering Part Number | Output Clock Frequency Range                  | Package              | ROHS6, Pb-Free | Temperature Range |
|----------------------|-----------------------------------------------|----------------------|----------------|-------------------|
| Si5325A-C-GM*        | .002–945 MHz<br>970–1134 MHz<br>1.213–1.4 GHz | 36-Lead 6 x 6 mm QFN | Yes            | –40 to 85 °C      |
| Si5325B-C-GM*        | .002–808 MHz                                  | 36-Lead 6 x 6 mm QFN | Yes            | –40 to 85 °C      |
| Si5325C-C-GM*        | .002–346 MHz                                  | 36-Lead 6 x 6 mm QFN | Yes            | –40 to 85 °C      |

**\*Note:** Not recommended for new designs. For alternatives, see the Si533x family.

## 7. Package Outline: 36-Pin QFN

Figure 6 illustrates the package details for the Si5325. Table 12 lists the values for the dimensions shown in the illustration.

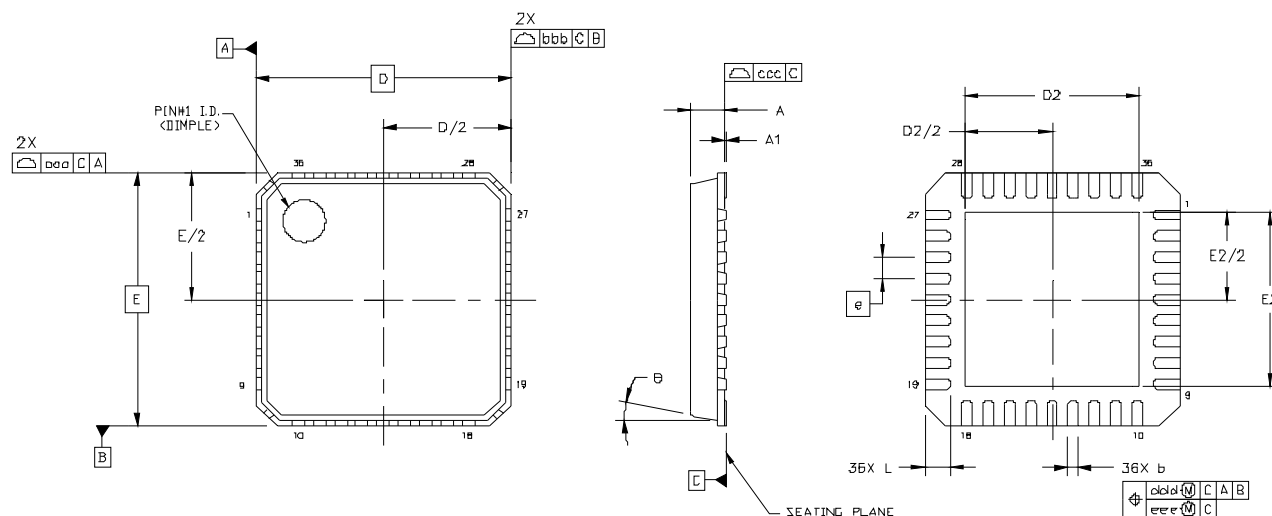


Figure 6. 36-Pin Quad Flat No-lead (QFN)

Table 12. Package Dimensions

| Symbol | Millimeters |      |      |
|--------|-------------|------|------|
|        | Min         | Nom  | Max  |
| A      | 0.80        | 0.85 | 0.90 |
| A1     | 0.00        | 0.02 | 0.05 |
| b      | 0.18        | 0.25 | 0.30 |
| D      | 6.00 BSC    |      |      |
| D2     | 3.95        | 4.10 | 4.25 |
| e      | 0.50 BSC    |      |      |
| E      | 6.00 BSC    |      |      |
| E2     | 3.95        | 4.10 | 4.25 |
| L      | 0.50        | 0.60 | 0.70 |
| θ      | —           | —    | 12°  |
| aaa    | —           | —    | 0.10 |
| bbb    | —           | —    | 0.10 |
| ccc    | —           | —    | 0.08 |
| ddd    | —           | —    | 0.10 |
| eee    | —           | —    | 0.05 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 8. Land Pattern: 36-Pin QFN

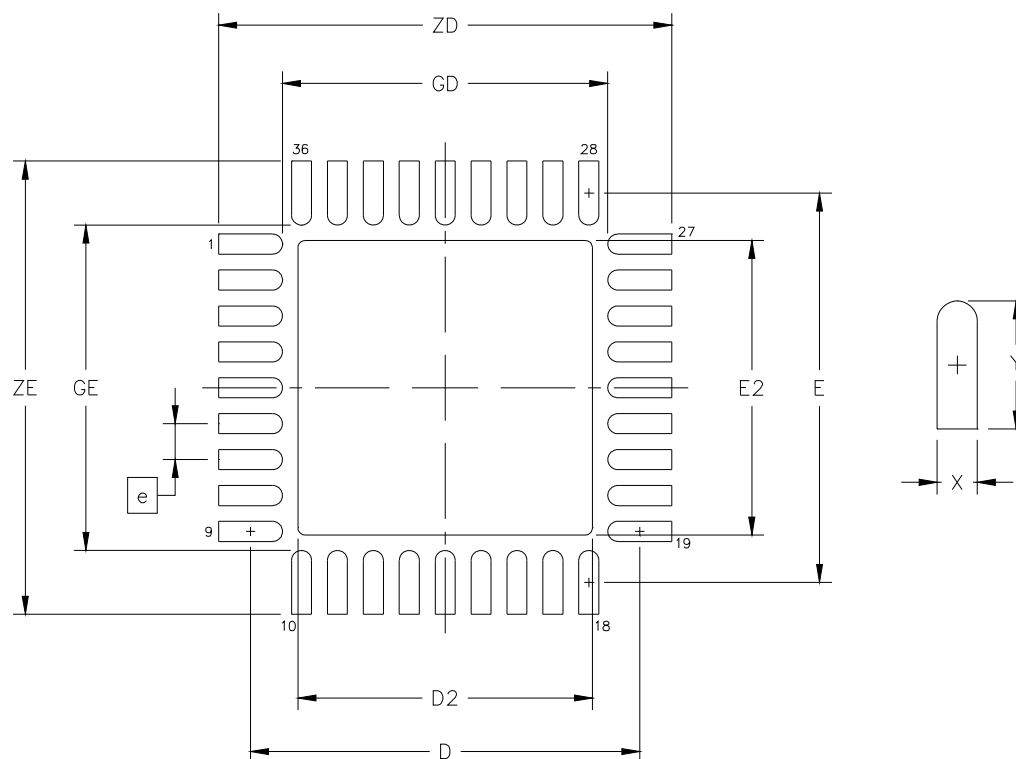


**Figure 7. 36-Pin QFN Land Pattern**

Table 13. PCB Land Pattern Dimensions

| Dimension | MIN       | MAX  |
|-----------|-----------|------|
| e         | 0.50 BSC. |      |
| E         | 5.42 REF. |      |
| D         | 5.42 REF. |      |
| E2        | 4.00      | 4.20 |
| D2        | 4.00      | 4.20 |
| GE        | 4.53      | —    |
| GD        | 4.53      | —    |
| X         | —         | 0.28 |
| Y         | 0.89 REF. |      |
| ZE        | —         | 6.31 |
| ZD        | —         | 6.31 |

**Notes:****General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

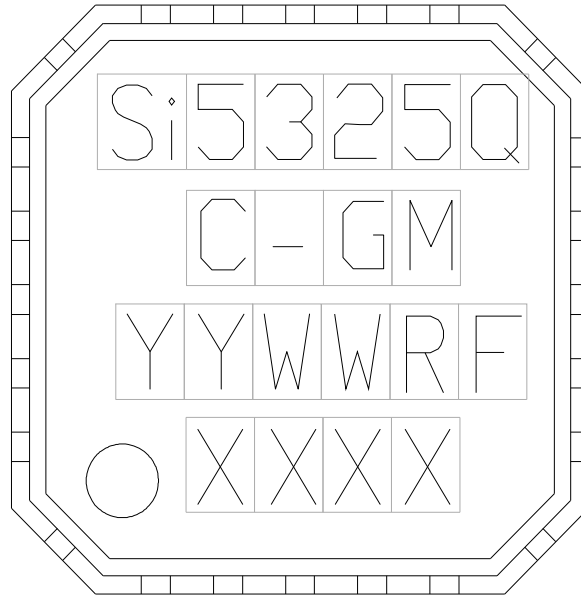
**Card Assembly**

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# Si5325

## 9. Top Marking

### 9.1. Si5325 Top Marking (QFN)



### 9.2. Top Marking Explanation

|                        |                            |                                                                                                                                                                 |
|------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Mark Method:</b>    | Laser                      |                                                                                                                                                                 |
| <b>Font Size:</b>      | 0.80 mm<br>Right-Justified |                                                                                                                                                                 |
| <b>Line 1 Marking:</b> | Si5325Q                    | Customer Part Number<br>Q = Speed Code: A, B, C<br>See Ordering Guide for options.                                                                              |
| <b>Line 2 Marking:</b> | C-GM                       | C = Product Revision<br>G = Temperature Range –40 to 85 °C (RoHS6)<br>M = QFN Package                                                                           |
| <b>Line 3 Marking:</b> | YYWWRF                     | YY = Year<br>WW = Work Week<br>R = Die Revision<br>F = Internal code<br>Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| <b>Line 4 Marking:</b> | Pin 1 Identifier           | Circle = 0.75 mm Diameter<br>Lower-Left Justified                                                                                                               |
|                        | XXXX                       | Internal Code                                                                                                                                                   |

## DOCUMENT CHANGE LIST

### Revision 0.23 to Revision 0.24

- Clarified that the two outputs have a common, higher frequency source on page 1.
- Changed LVTTTL to LVCMOS in Table 2, "Absolute Maximum Ratings," on page 5.
- Added Figure 1, "Typical Phase Noise Plot," on page 4.
- Updated "5. Pin Descriptions: Si5325".
  - Removed references to latency control, INC, and DEC.
  - Changed font for register names to underlined italics.
- Updated "6. Ordering Guide" on page 56.
- Added "8. Land Pattern: 36-Pin QFN".

### Revision 0.24 to Revision 0.25

- Updated Section "5. Pin Descriptions: Si5325" on page 52.

### Revision 0.25 to Revision 0.26

- Removed Figure 1. "Typical Phase Noise Plot."
- Changed pins 11 and 15 from NC to VDD in "5. Pin Descriptions: Si5325".

### Revision 0.26 to Revision 0.3

- Changed 1.8 V operating range to  $\pm 5\%$ .
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Added page 14.
- Updated "2. Functional Description" on page 16.
- Clarified "5. Pin Descriptions: Si5325" on page 52 including pull-up/pull-down.

### Revision 0.3 to Revision 0.4

- Added register map
- Lowered minimum CKOUT frequency
- Updated spec tables
  - ESD tolerance, Table 2 on page 5
  - Minimum input and output clock frequencies, Table 1 on page 4
  - Absolute maximum VDD voltage, Table 2 on page 5
- Added to spec table
  - CKIN voltage limits, Table 2 on page 5
  - Typical jitter and phase noise values, Table 1 on page 4
- No bypass mode with CMOS outputs

### Revision 0.4 to Revision 0.5

- Expanded electrical specification tables 1 through 7.
- Removed support for CMOS outputs in Bypass mode.
- Corrected minor errors in register map section.
- Updated "Features" on page 1".
  - Added "not recommended for new designs" language.
- Updated Table 5 on page 52.
- Updated "6. Ordering Guide" on page 56.
- Removed note from "5. Pin Descriptions: Si5325" on page 52.

### Revision 0.5 to Revision 1.0

- Updated logo.
- Transitioned to full production.



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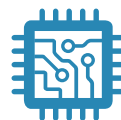
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