THE DATASHEET OF

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Si5347/46 Rev D Data Sheet

Dual/Quad DSPLL™ Any-Frequency, Any-Output Jitter Attenuators

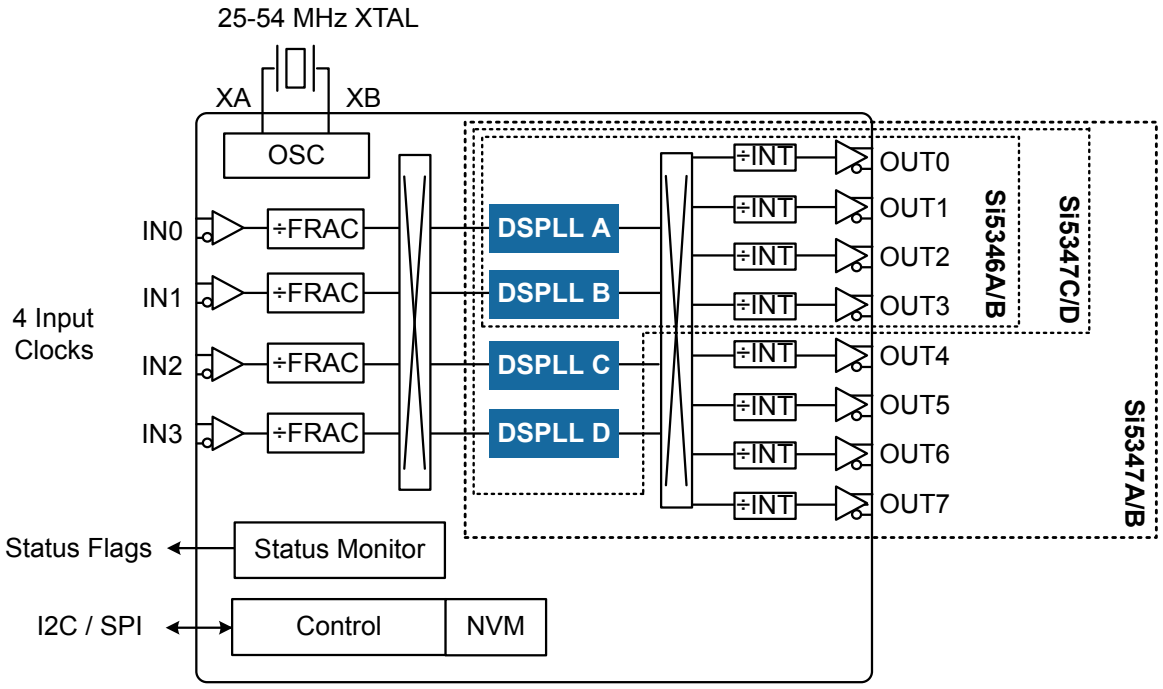
The Si5347 is a high-performance, jitter-attenuating clock multiplier which integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5346 is a dual DSPLL version in a smaller package. Each DSPLL has access to any of the four inputs and can provide low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency conversion with typical jitter performance under 100 fs. Each DSPLL supports independent free-run, holdover modes of operation, as well as automatic and hitless input clock switching. The Si5347/46 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up in a known configuration. Programming the Si5347/46 is easy with Skyworks' ClockBuilder Pro™ software. Factory preprogrammed devices are also available.

KEY FEATURES

- Four or two independent DSPLLs, any output frequency from any input frequency
- Ultra-low jitter of 95 fs rms
- Input frequency range:
  - External Crystal: 25–54 MHz
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 720 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Status Monitoring
- Hitless switching
- Si5347: 4 input, 8 output, 64-QFN 9×9 mm
- Si5346: 4 input, 4 output, 44-QFN 7×7 mm

Applications

- OTN Muxponders and Transponders
- 10/40/100G network line cards
- GbE/10 GbE/100 GbE Synchronous Ethernet (ITU-T G.8262)
- Carrier Ethernet switches
- Broadcast video



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1. Feature List

The Si5347/46-D features are listed below:

- Four or two DSPLLs to synchronize to multiple inputs
- Generates any combination of output frequencies from any input frequency
- Ultra low jitter:
  - 95 fs typ (12 kHz – 20 MHz)
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: up to 720 MHz
  - LVCMOS: up to 250 MHz
- Flexible crosspoints route any input to any output clock
- Programmable jitter attenuation bandwidth per DSPLL: 0.1 Hz to 4 kHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Hitless input clock switching: automatic or manual
- Locks to gapped clock inputs
- Automatic free-run and holdover modes
- Fastlock feature for low nominal bandwidths
- Glitchless on-the-fly DSPLL frequency changes
- DCO mode: as low as 0.01 ppb steps per DSPLL
- Core voltage:
  - V_{DD}: 1.8 V ±5%
  - V_{DDA}: 3.3 V ±5%
- Independent output clock supply pins: 3.3, 2.5, or 1.8 V
- Output-output skew:
  - Using same DSPLL: 65 ps (Max)
- Serial interface: I^2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder Pro software simplifies device configuration
- Si5347: Quad DSPLL, 64-QFN 9×9 mm
- Si5346: Dual DSPLL, 44-QFN 7×7 mm
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Table 2.1. Si5347/46 Ordering Guide

Ordering Part Number	Number Of DSPLLs	Number of Outputs	Output Clock Frequency Range	Package	RoHS-6, Pb-Free	Temp Range
Si5347A-D-GM[1,2]	4	8	0.0001 to 720 MHz	64-Lead 9x9 QFN	Yes	–40 to 85 °C
Si5347B-D-GM[1,2]			0.0001 to 350 MHz			
Si5347C-D-GM[1,2]		4	0.0001 to 720 MHz			
Si5347D-D-GM[1,2]			0.0001 to 350 MHz			
Si5346A-D-GM[1,2]	2	4	0.0001 to 720 MHz	44-Lead 7x7 QFN		
Si5346B-D-GM[1,2]			0.0001 to 350 MHz			
Si5347-D-EVB	—	—	—	Evaluation Board	—	—
Si5346-D-EVB	—	—	—		—	—

Notes:

1. Add an R at the end of the device part number to denote tape and reel ordering options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by the ClockBuilder Pro software. Part number format is: Si5347A-Dxxxxx-GM or Si5346A-Dxxxxx-GM, where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.

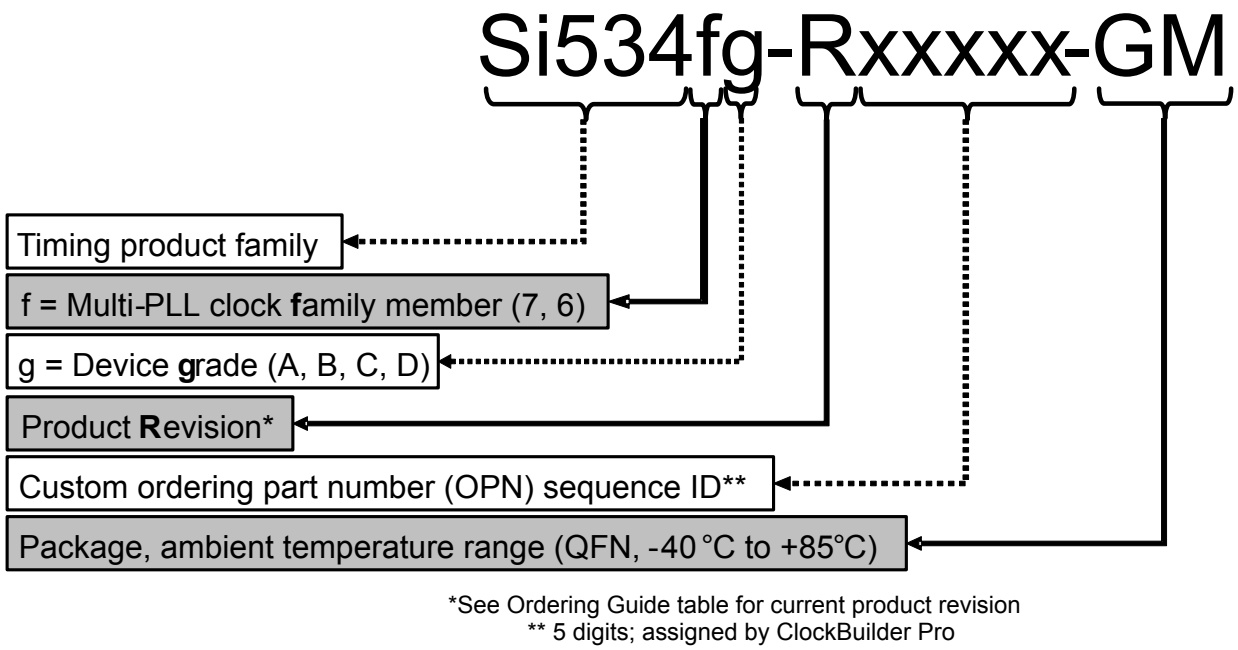


Figure 2.1. Ordering Part Number Fields

3. Functional Description

The Si5347 takes advantage of Skyworks' 4th generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. Each DSPLL has access to any of the four inputs (IN0 to IN3) with manual or automatic input selection. Any of the output clocks (OUT0 to OUT7) can be configured to any of the DSPLLs using a flexible crosspoint connection. The Si5346 is a smaller form factor dual DSPLL version with four inputs and four outputs.

3.1 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (P_n/P_d), fractional frequency multiplication (M_n/M_d), and integer output division (R_n) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro software.

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register-configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

3.2.1 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting, as described in Section 3.2 DSPLL Loop Bandwidth. The fastlock feature can be enabled or disabled independently for each of the DSPLLs.

3.3 Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 3.1 Modes of Operation on page 7. The following sections describe each of these modes in greater detail.

3.3.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard register reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can either affect all or each DSPLL individually.

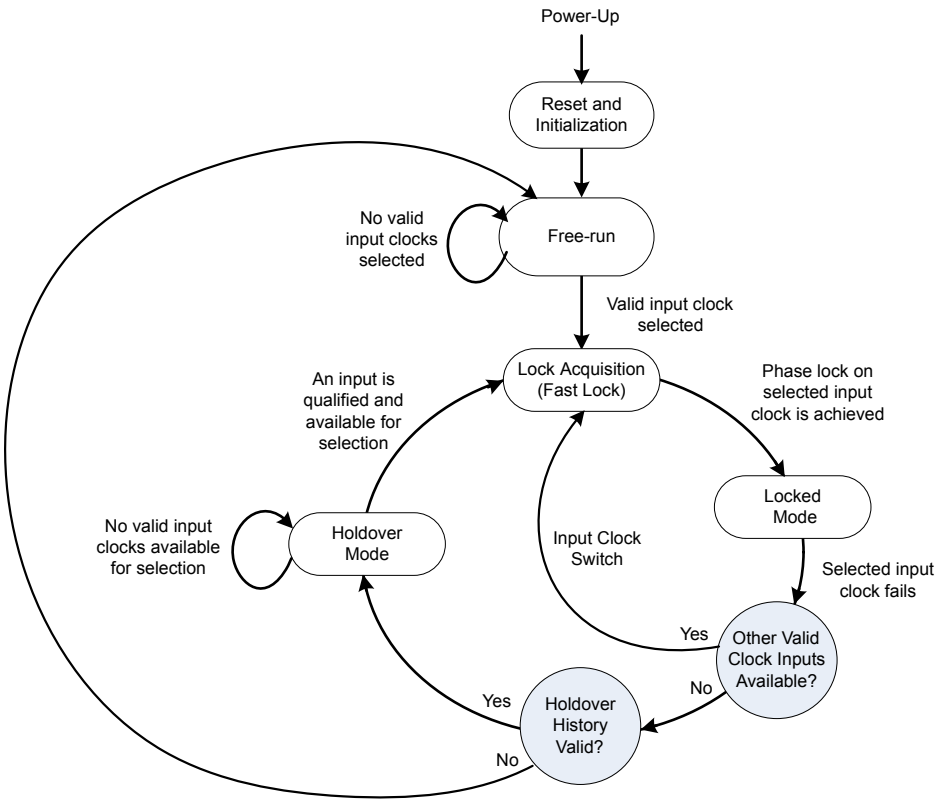


Figure 3.1. Modes of Operation

3.3.2 Free-run Mode

Once power is applied to the Si5347 and initialization is complete, all four DSPLLs will automatically enter Free-run Mode. The frequency accuracy of the generated output clocks in Free-run Mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in Free-run Mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in Free-run Mode or Holdover Mode.

3.3.3 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.

If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

3.3.4 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own LOLb pin and status bit to indicate when lock is achieved. See 3.7.4 LOL Detection for more details on the operation of the loss of lock circuit.

3.3.5 Holdover Mode

Any of the DSPLLs will automatically enter Holdover Mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable, as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

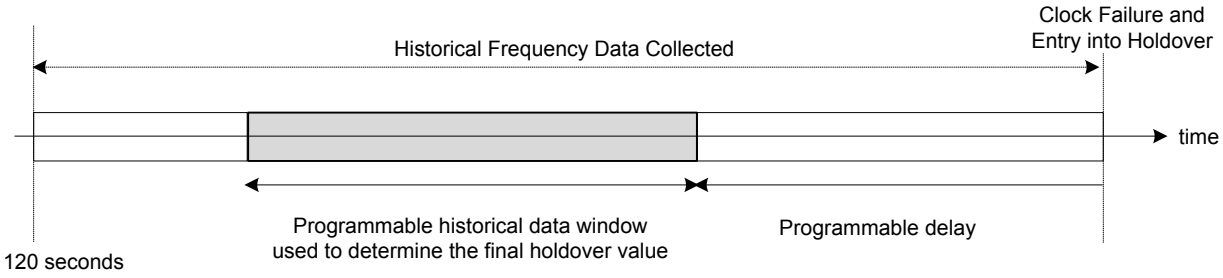


Figure 3.2. Programmable Holdover Window

When entering Holdover Mode, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in Holdover Mode, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, a DSPLL will automatically exit the Holdover Mode and reacquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless, and its rate is controlled by the DSPLL bandwidth or the fastlock bandwidth. These options are register programmable.

Add new section The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 3.6.6 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

3.4 Digitally-Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW).The frequency adjustments are controlled through the serial interface or by pin control using frequency increment (FINC) or decrement (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in either Free-run or Locked Mode.

3.5 External Reference (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra-low jitter reference clock for the DSPLLs and for providing a stable reference for the Free-run and Holdover Modes. A simplified diagram is shown in the figure below. The device includes internal XTAL loading capacitors, which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 5.12 Crystal Specifications[1] on page 36 for crystal specifications. A crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. The Si5347-46 Rev D Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. For SyncE line card PLL applications (e.g. loop bandwidth set to 0.1 Hz), a TCXO is required on the XA/XB reference to minimize wander and to provide a stable holdover reference. See the Si5347-46 Rev D Reference Manual for more information. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (C_L) are disabled in the REFCLK mode. Refer to Table 5.3 Input Clock Specifications on page 27 for REFCLK requirements when using this mode. The Si5347-46 Rev D Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. A P_{REF} divider is available to accommodate external clock frequencies higher than 54 MHz. Although the REFCLK frequency range of 25 MHz to 54 MHz is supported, frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.

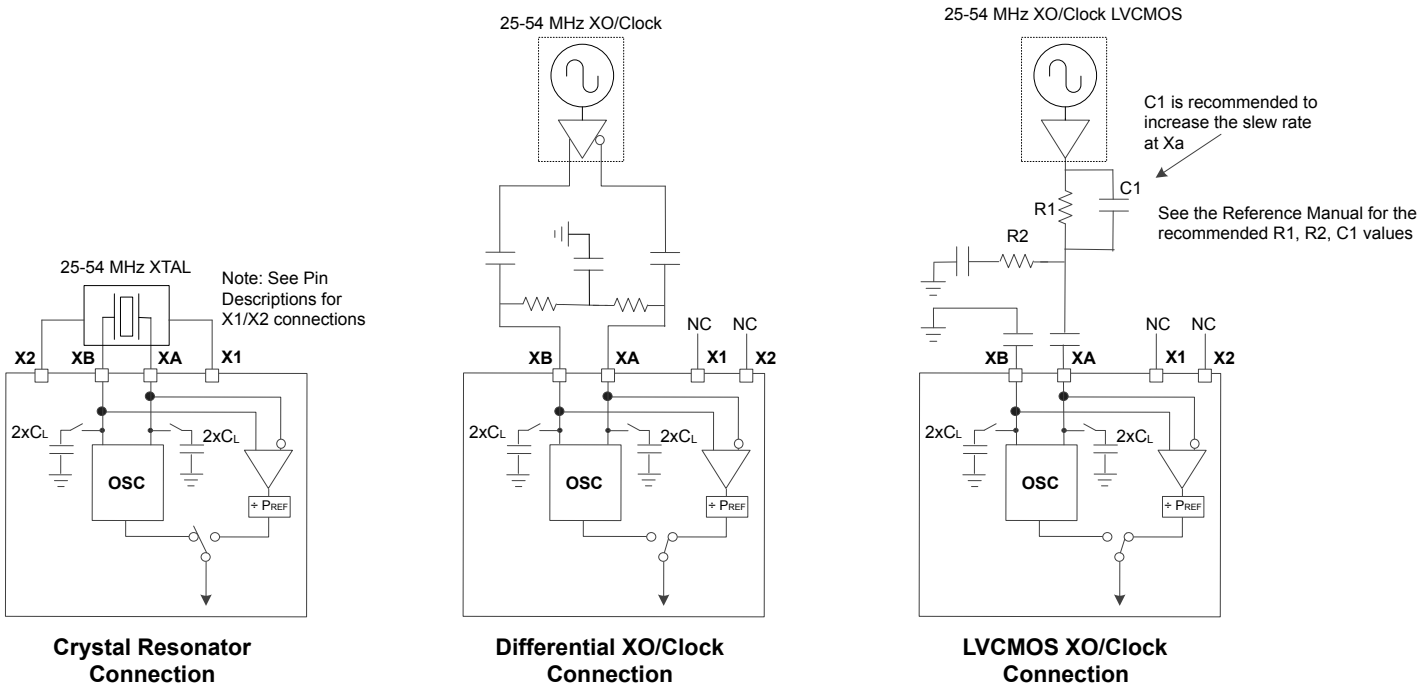


Figure 3.3. Crystal Resonator and External Reference Clock Connection Options

Note: See Table 5.3 Input Clock Specifications on page 27 and the Si5347-46 Rev D Reference Manual for more information.

3.6 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs, as shown in the figure below.

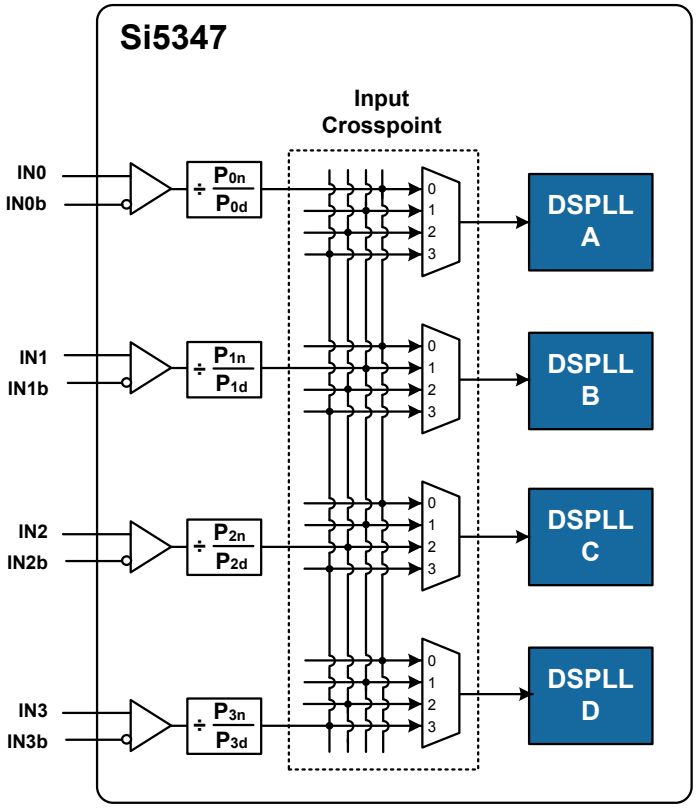


Figure 3.4. DSPLL Input Selection Crosspoint

3.6.1 Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

3.6.2 Manual Input Selection

In Manual Mode, the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter Holdover Mode.

3.6.3 Automatic Input Selection

When configured in this mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection.

All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter the Holdover mode if there are no valid inputs available.

3.6.4 Input Configuration and Terminations

Each of the inputs can be configured as differential or single-ended LVCMOS. The recommended input termination schemes are shown in the figure below. Standard 50% duty cycle signals must be ac-coupled, while low duty cycle Pulsed CMOS signals can be dc-coupled. Unused inputs can be disabled and left unconnected when not in use.

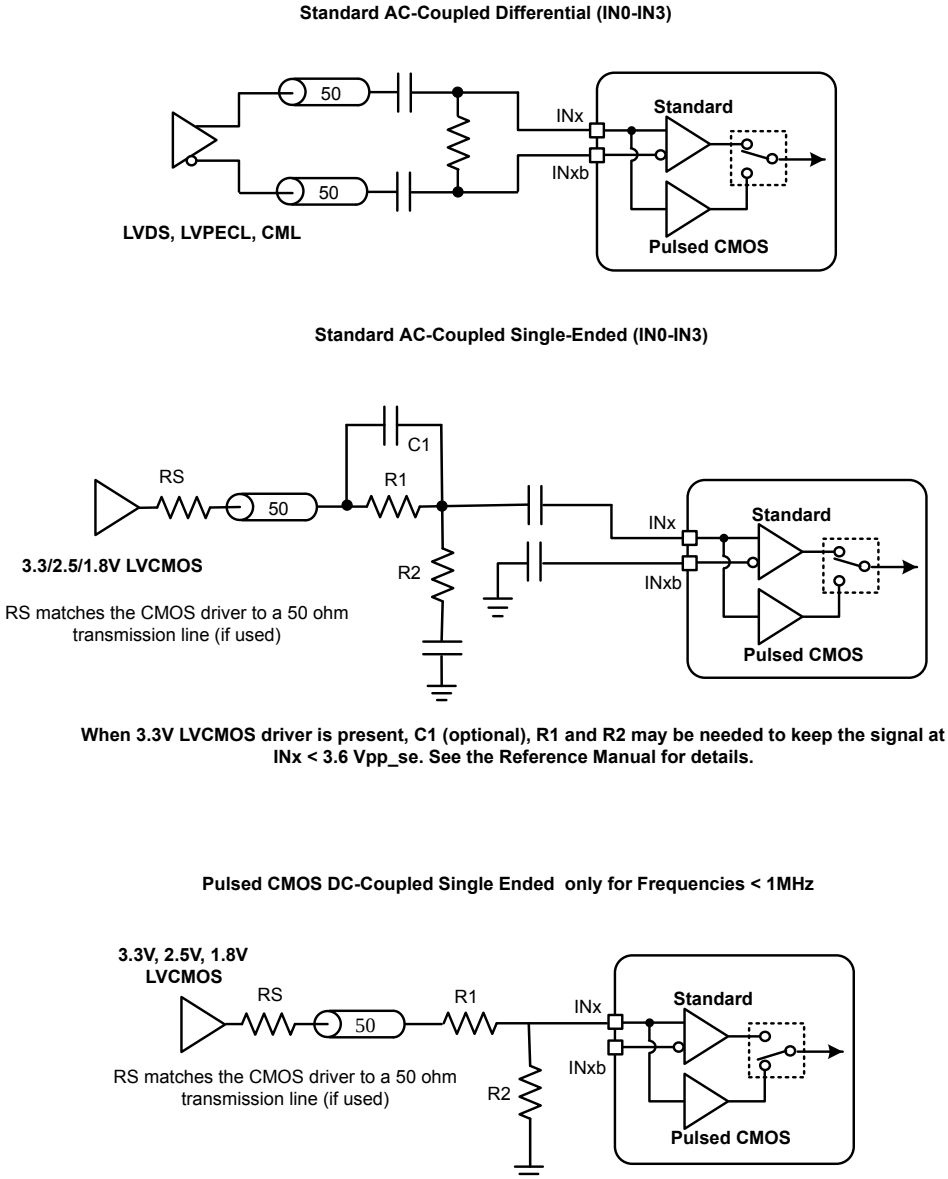


Figure 3.5. Termination of Differential and LVCMOS Input Signals

Note: See Table 5.3 Input Clock Specifications on page 27 and the Si5347-46 Rev D Reference Manual for more information.

3.6.5 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis.

3.6.6 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see 3.3.5 Holdover Mode.

3.6.7 Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition.

3.6.8 Synchronizing to Gapped Input Clocks

Each of the DSPLLs support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter, so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. This is shown in the figure below.

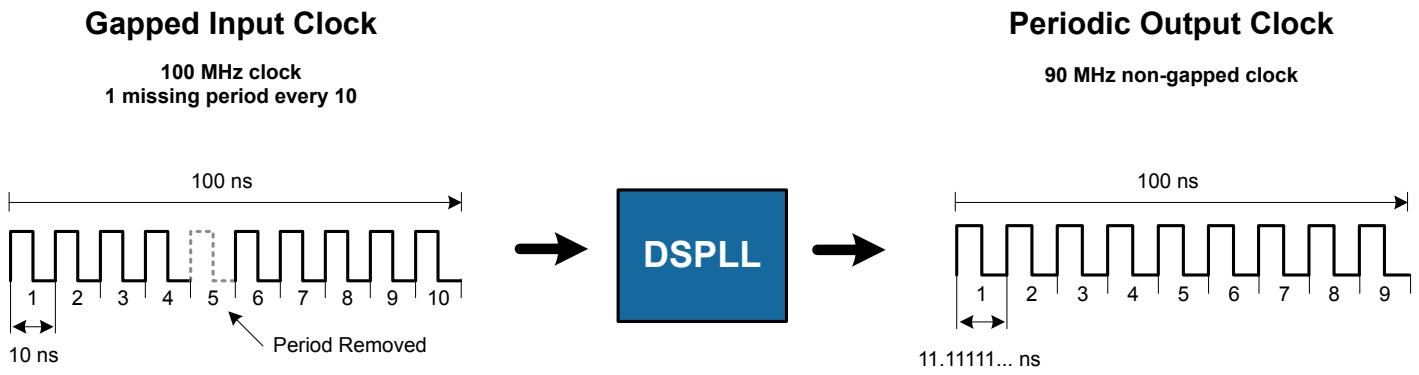


Figure 3.6. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every 8. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 5.8 Performance Characteristics on page 32 when the switch occurs during a gap in either input clock.

3.7 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for LOS and OOF, as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has an LOL indicator, which is asserted when synchronization is lost with their selected input clock.

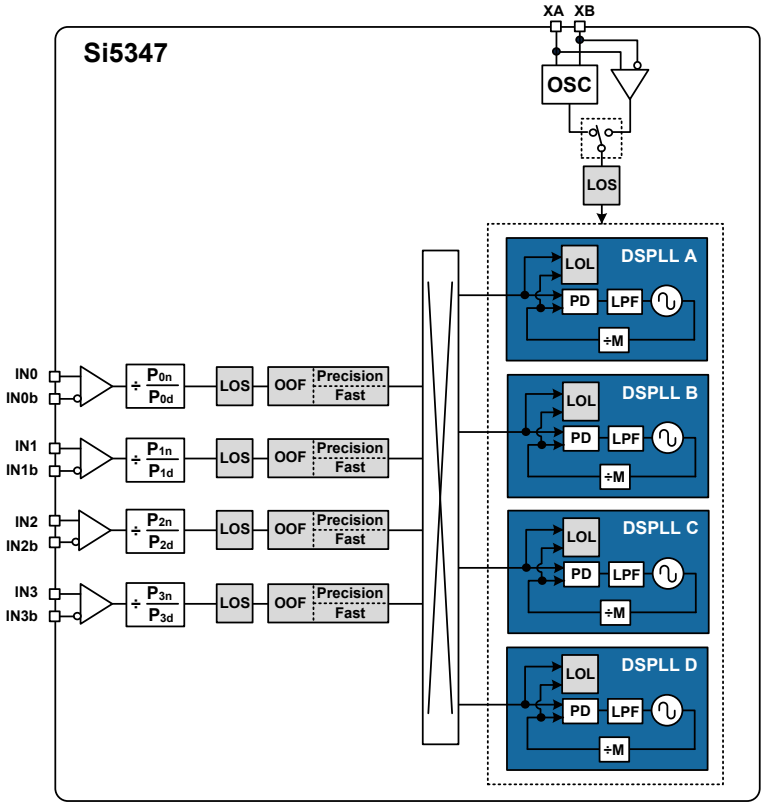


Figure 3.7. Si5347 Fault Monitors

3.7.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro software. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

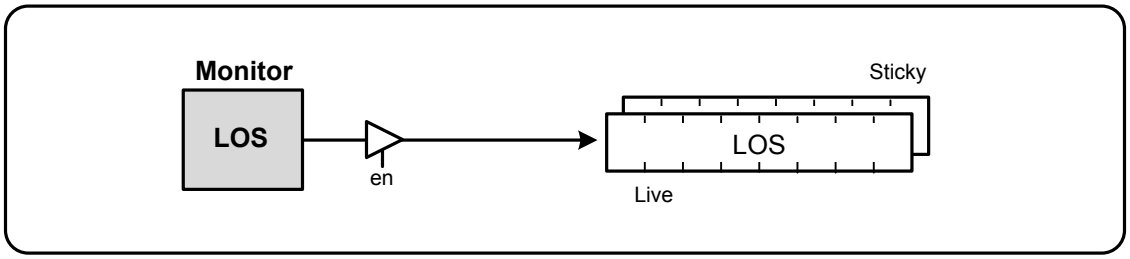


Figure 3.8. LOS Status Indicators

3.7.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.7.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference, which it considers as its “0_ppm” reference.

This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor, as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

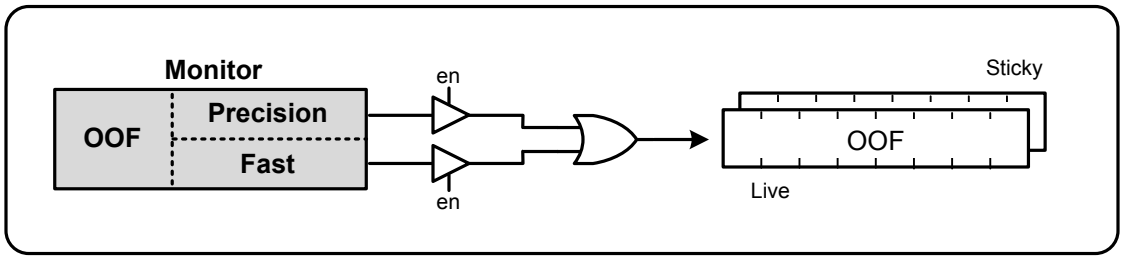


Figure 3.9. OOF Status Indicator

Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within 1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range, which is register configurable up to ±500 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 – IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register-configurable.

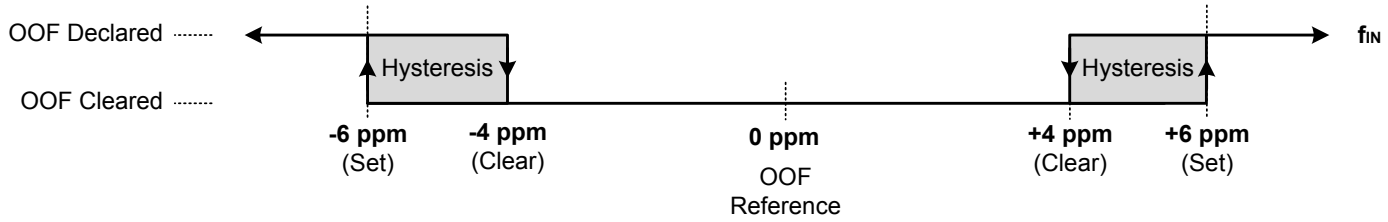


Figure 3.10. Example of Precise OOF Monitor Assertion and De-assertion Triggers

Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

3.7.4 LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts an LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Bb, LOL_Cb, LOL_Db). The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

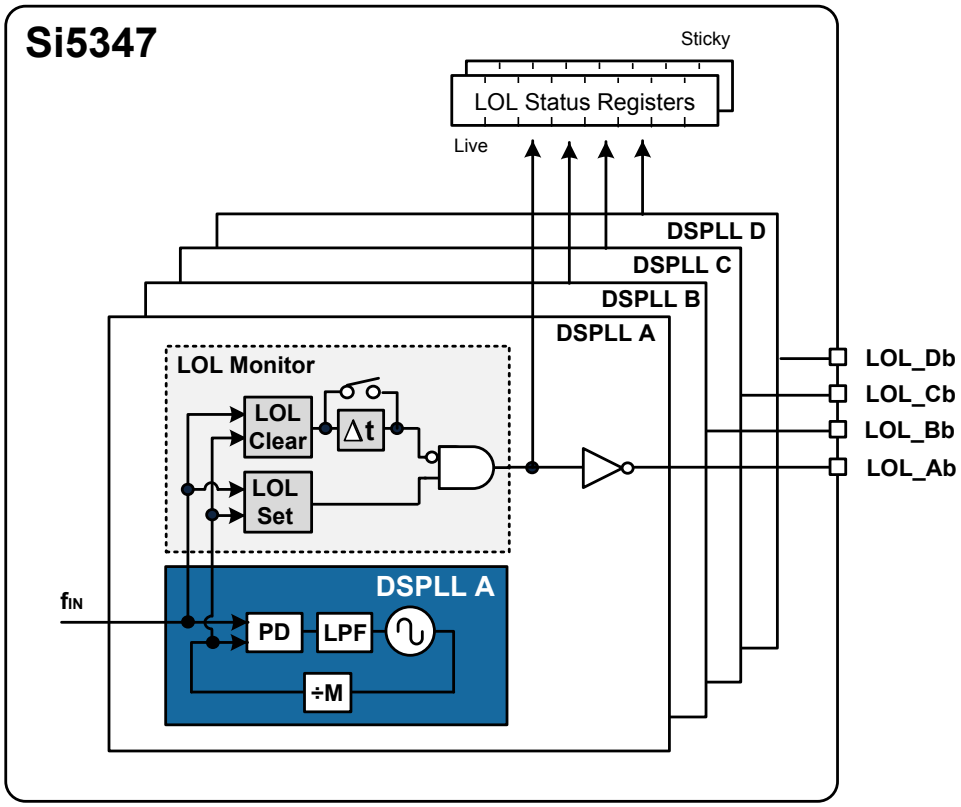


Figure 3.11. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity, which is register-configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference is shown in the figure below.

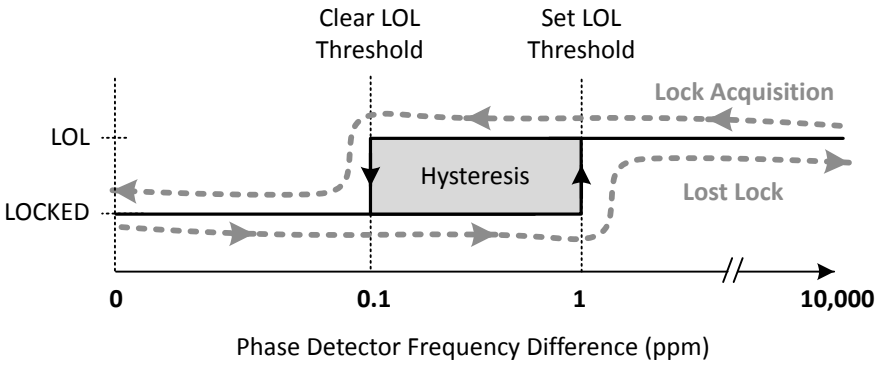


Figure 3.12. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro software.

3.7.5 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

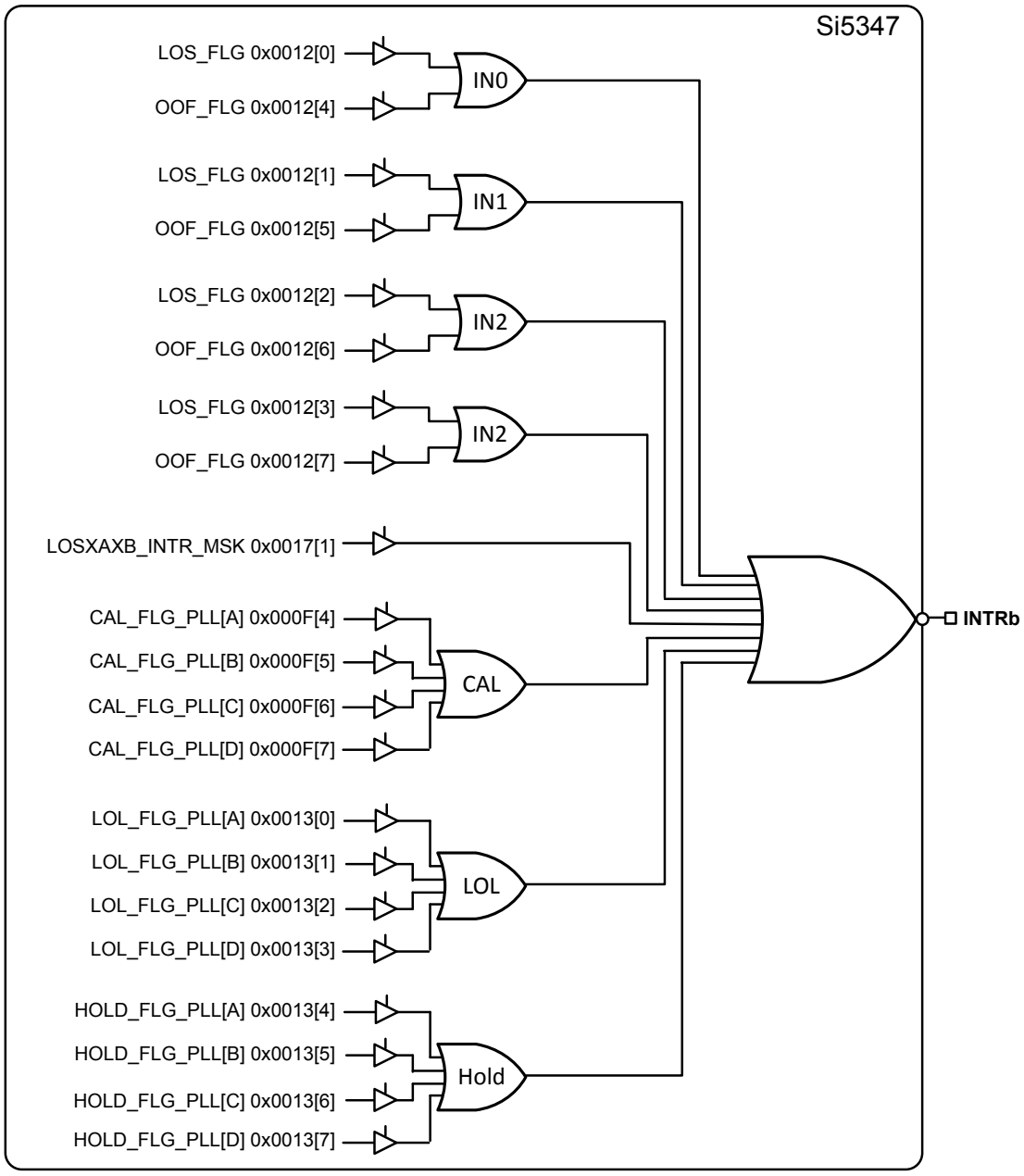


Figure 3.13. Interrupt Triggers and Masks

3.8 Outputs

The Si5347 supports up to eight differential output drivers and the Si5346 supports four. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 16 single-ended outputs, or any combination of differential and single-ended outputs.

3.8.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs, as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.

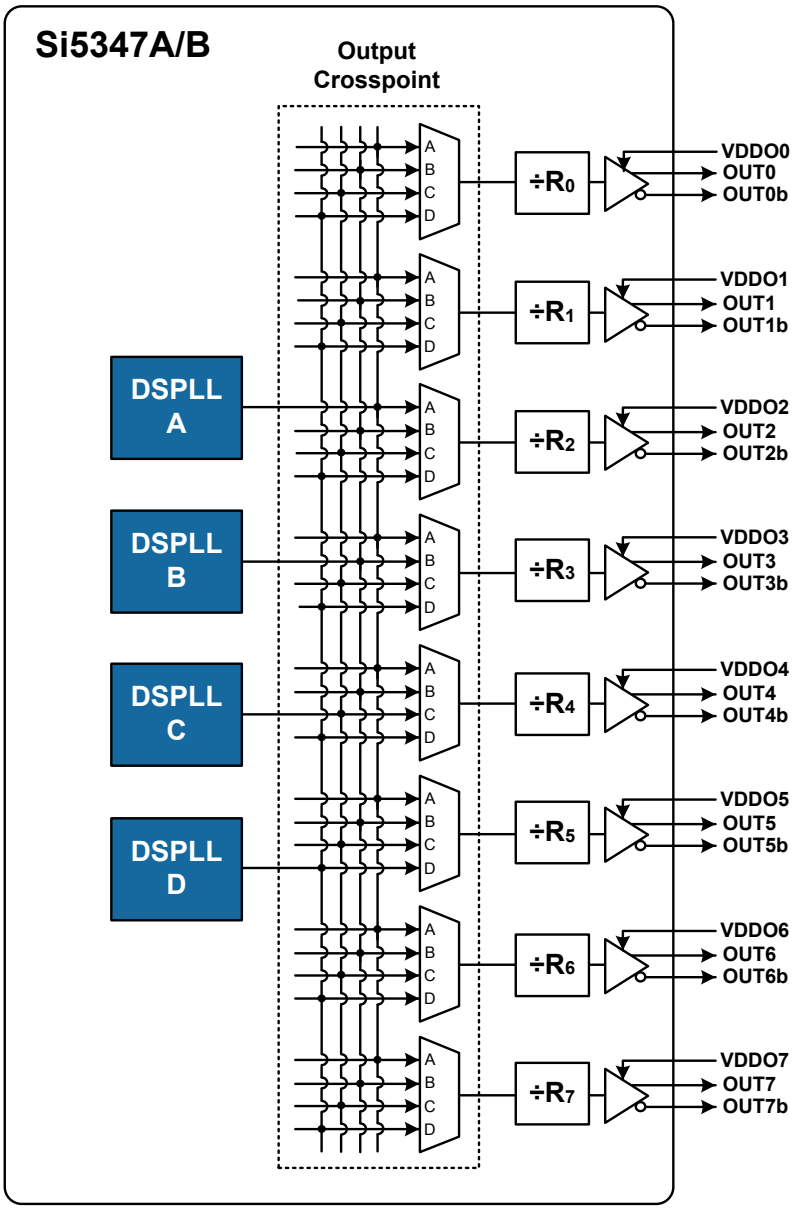


Figure 3.14. Si5347A/B DSPLL to Output Driver Crosspoint

3.8.2 Differential Output Terminations

Note: In this document, the terms "LVDS" and "LVPECL" refer to driver formats that are compatible with these signaling standards.

The differential output drivers support both ac-coupled and dc-coupled terminations, as shown in the figure below.

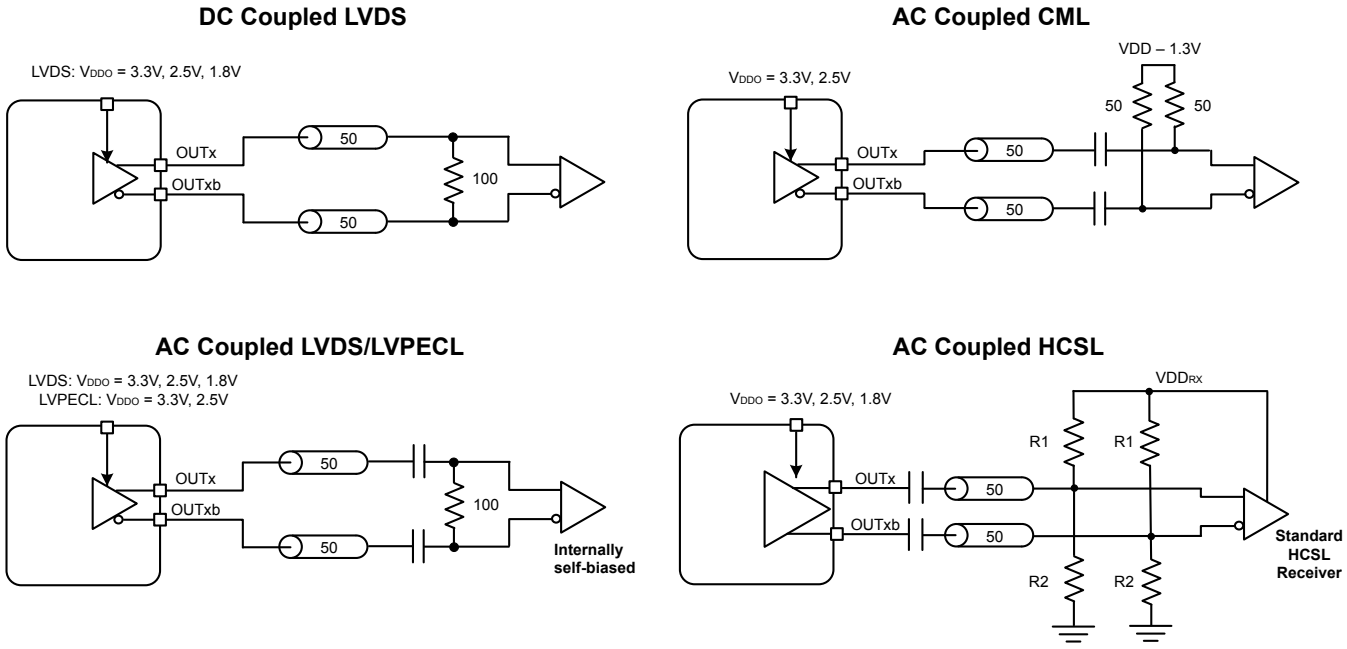


Figure 3.15. Supported Differential Output Terminations

Note: See the Si5347/46 Rev D Family Reference Manual for resistor values.

3.8.3 LVCMOS Output Terminations

LVCMOS outputs are dc-coupled, as shown in the figure below.

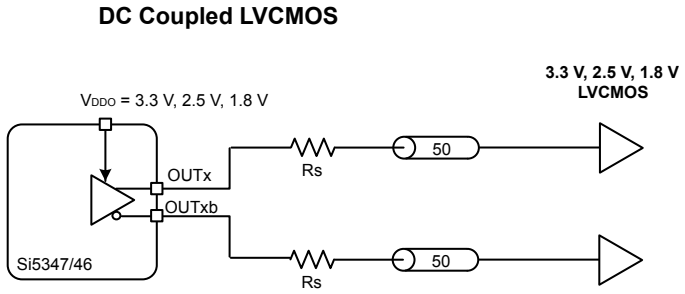


Figure 3.16. LVCMOS Output Terminations

3.8.4 Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 16 single-ended outputs or any combination of differential and single-ended outputs.

3.8.5 Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential modes is programmable and depends on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

3.8.6 LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO option, as shown in the table below. Note that selecting a lower source impedance may result in higher output power consumption.

Table 3.1. Typical Output Impedance (Z_S)

VDDO	CMOS_DRIVE_Selection		
	OUTx_CMOS_DRV = 1	OUTx_CMOS_DRV = 2	OUTx_CMOS_DRV = 3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

3.8.7 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

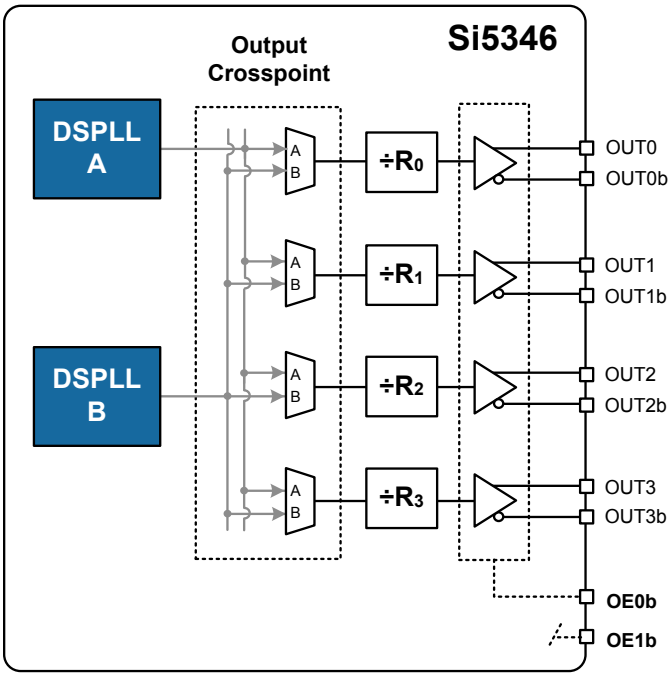
3.8.8 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable, which enables complementary clock generation and/or inverted polarity with respect to other output drivers.

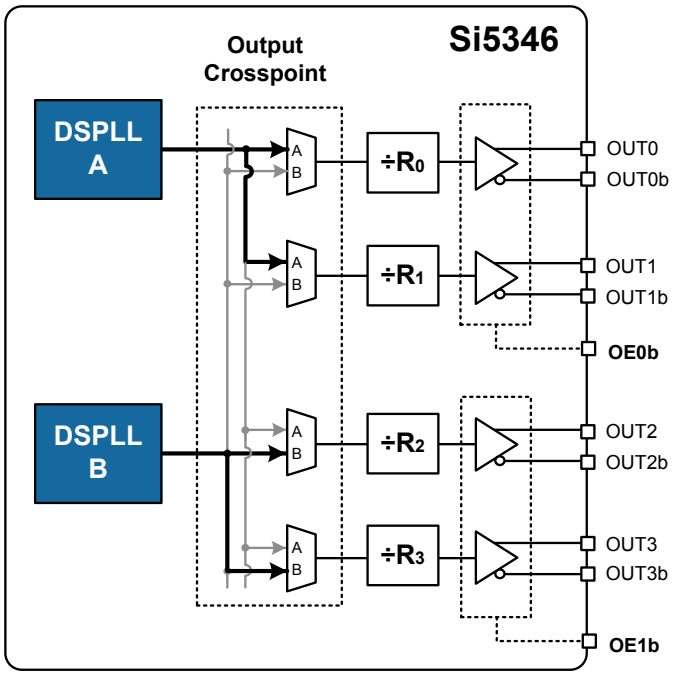
3.8.9 Output Enable/Disable

The Si5347/46 allows enabling/disabling outputs by pin or register control, or a combination of both. Two output enable pins are available (OE0b, OE1b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b remains unmapped and has no effect until configured. The figure below shows an example of an output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OEb pin(s) has them enabled. By default the output enable register settings are configured to allow the OEb pins to have full control.



In its default state the OE0b pin enables/disables all outputs. The OE1b pin is not mapped and has no effect on outputs.



An example of a configurable output enable scheme. In this case OE0b controls the outputs associated with DSPLL A, while OE1b controls the outputs of DSPLL B.

Figure 3.17. Example of Configuring Output Enable Pins

3.8.10 Output Disable During LOL

By default a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.8.11 Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

3.8.12 Output Driver State When Disabled

The disabled state of an output driver is register configurable as disable low or disable high.

3.8.13 Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

3.8.14 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.9 Power Management

Unused inputs, output drivers, and DSPLLs can be powered down when unused. Consult the Si5347-46 Rev D Reference Manual and the ClockBuilder Pro software for details.

3.10 In-Circuit Programming

The Si5347/46 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5347-46 Rev D Reference Manual for a detailed procedure for writing registers to NVM.

3.11 Serial Interface

Configuration and operation of the Si5347/46 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire mode. See the Si5347-46 Rev D Reference Manual for details.

3.12 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory pre-programmed part will generate clocks at power-up. Custom, factory-pre-programmed devices are available. Use the ClockBuilder Pro custom part number wizard to quickly and easily request and generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your pre-programmed device will typically ship in about two weeks.

3.13 Enabling Features and/or Configuration Settings Not Available in ClockBuilder Pro for Factory Pre-programmed Devices

As with essentially all modern software utilities, the ClockBuilder Pro software is continuously updated and enhanced. By registering at www.skyworksinc.com, you will be notified whenever changes are made and what the impact of those changes are. This update process will ultimately enable ClockBuilder Pro software users to access all features and register setting values documented in this data sheet and the Si5347-46 Rev D Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact Skyworks for assistance. One example of this type of feature or custom setting is the customizable output amplitude and common voltages for the clock outputs. After careful review of your project file and requirements, the Skyworks applications engineer will email back your CBPro project file with your specific features and register settings enabled using what is referred to as the manual "settings override" feature of CBPro. "Override" settings to match your request(s) will be listed in your design report file. Examples of setting "overrides" in a CBPro design report are shown in the table below.

Table 3.2. Setting Overrides

Location	Name	Type	Target	Dec Value	Hex Value
0x0535[0]	FORCE_HOLD_PLLB	No NVM	N/A	1	0x1
0x0B48[4:0]	OOF_DIV_CLK_DIS	User	OPN and EVB	31	0x1F

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the figure below.

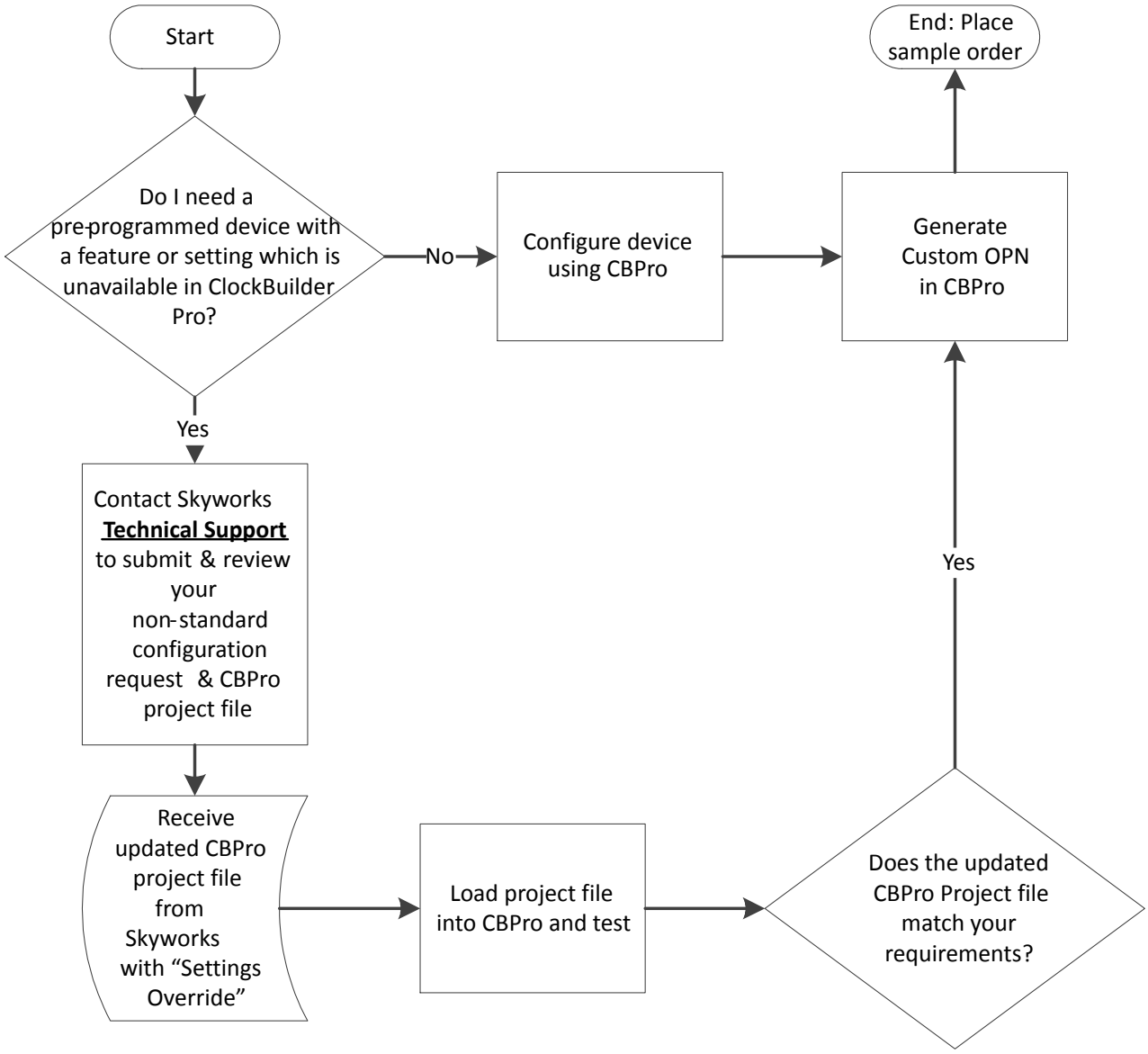


Figure 3.18. Process for Requesting Non-Standard CBPro Features

Note: Contact Skyworks at https://www.skyworksinc.com/en/Support.

4. Register Map

Refer to the Si5347-46 Rev D Reference Manual for a complete list of register descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%,T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	25	85	°C
Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status Pin Supply Voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

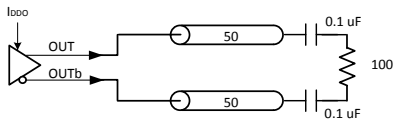
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1, 2]	I_{DD}	Si5347, 4 DSPLLs	—	300	450	mA
		S5347, 1 DSPLL	—	190	340	mA
		Si5346	—	185	280	mA
	I_{DDA}	Si5347, 4 DSPLLs	—	125	140	mA
		Si5347, 1 DSPLL	—	125	140	mA
		Si5346	—	125	140	mA
Output Buffer Supply Current	I_{DDO}	LVPECL Output[3] @ 156.25 MHz	—	22	26	mA
		LVDS Output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] Output @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS[4] Output @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS[4] Output @ 156.25 MHz	—	12	16	mA
Total Power Dissipation[5]	P_d	Si5347, 4 DSPLLs[1]	—	1200	1600	mW
		Si5347, 1 DSPLL[1]	—	1050	1420	mW
		Si5346[2]	—	880	1100	mW

Notes:

1. Si5347 test configuration: 7×2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5346 test configuration: 4×2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 4.7 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. Refer to the Si5347-46 Rev D Reference Manual for more details on register settings.
5. Detailed power consumption for any configuration can be estimated using the ClockBuilder Pro software when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

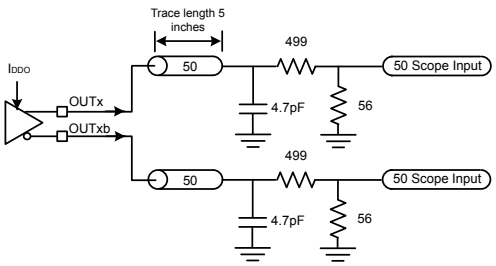


Table 5.3. Input Clock Specifications

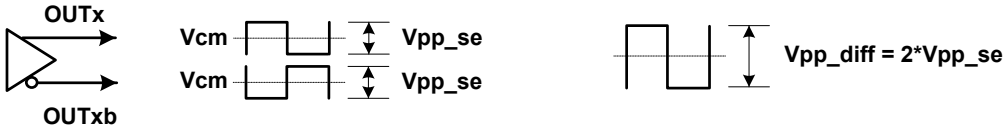
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard AC-Coupled Differential or Single-Ended (IN0/IN0b, IN1/IN1b, IN2/IN2b, IN3/IN3b)						
Input Frequency Range	f_{IN}	Differential	0.008	—	750	MHz
		All Single-ended signals (including LVCMOS)	0.008	—	250	MHz
Voltage Swing[1]	V_{IN}	Differential AC-coupled f_{IN} < 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled 250 MHz < f_{IN} < 750 MHz	225	—	1800	mVpp_se
		Single-ended AC-coupled f_{IN}< 250 MHz	100	—	3600	mVpp_se
Slew Rate[2,3]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		—	2.4	—	pF
Input Resistance Differential	R_{IN_DIFF}		—	16	—	kΩ
Input Resistance Single-ended	R_{IN_SE}		—	8	—	kΩ
LVCMOS / Pulsed CMOS, DC-Coupled, Single-Ended (IN0, IN1, IN2, IN3)[4]						
Input Frequency	f_{IN_LVCMOS}		0.008	—	250	MHz
	$f_{IN_PULSED_CMOS}$		0.008	—	1.0	MHz
Input Voltage	V_{IL}		–0.2	—	0.4	V
	V_{IH}		0.8	—	—	V
Slew Rate[2,3]	SR		400	—	—	V/µs
Minimum Pulse Width	PW	Pulse Input	1.6	—	—	ns
Input Resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK Frequency	f_{IN_REF}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
Input Voltage Swing	V_{IN_DIFF}		365	—	2500	mVpp_diff
	V_{IN_SE}		365	—	2000	mVpp_se
Slew rate[2,3]	SR	Imposed for best jitter performance	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Notes:

1. Voltage swing is specified as single-ended mVpp.



2. Recommended for specified jitter performance. Jitter performance can degrade if the minimum slew rate specification is not met (see Si5347-46 Rev D Reference Manual).
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 - 0.2) \times V_{IN_Vpp_se}) / SR$.
4. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks < 1 MHz, which must be dc-coupled because they have a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. Since the input thresholds (VIL, VIH) of this buffer are non-standard (0.4 and 0.8 V, respectively), refer to the input attenuator circuit for DC-coupled Pulsed LVCMOS in the Si5347-46 Rev D Reference Manual. Otherwise, for standard LVCMOS input clocks, use the Standard AC-coupled, Single-ended input mode.

Table 5.4. Serial and Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5347 Serial and Control Input Pins (I2C_SEL, RSTb, OE0b, A1/SDO, SCLK, A0/CSb, FINC, A0/CSb, SDA/SDIO, DSPLL_SEL[1:0])						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, FINC	100	—	—	ns
Update Rate	F_{UR}	FINC	—	—	1	MHz
Si5347 Control Input Pins (FDEC, OE1b)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDS}	V
	V_{IH}		0.7 x V_{DDS}	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Minimum Pulse Width	PW	FDEC	100	—	—	ns
Update Rate	F_{UR}	FDEC	—	—	1	MHz
Si5346 Serial and Control Input Pins (I2C_SEL, RSTb, OE0b, OE1b, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	1.5	—	pF
Input Resistance	R_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

Table 5.5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	720	MHz
Duty Cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} < 720 MHz		45	—	55	%
Output-Output Skew Using Same DSPLL	T_{SKS}	Outputs on same DSPLL (Measured at 720 MHz)		—	0	75	ps
OUT-OUTb Skew	T_{SK_OUT}	Measured from positive to negative output pins		—	0	50	ps
Output Voltage Amplitude[1]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	430	510	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	640	750	900	
Common Mode Voltage[1,2]	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.10	1.20	1.30	V
			LVPECL	1.90	2.00	2.10	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.10	1.20	1.30	
		V_{DDO} = 1.8 V	sub-LVDS	0.80	0.90	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F			—	100	150	ps
Differential Output Impedance	Z_O			—	100	—	Ω
Power Supply Noise Rejection[2]	PSRR	10 kHz sinusoidal noise		—	–101	—	dBc
		100 kHz sinusoidal noise		—	–96	—	dBc
		500 kHz sinusoidal noise		—	–99	—	dBc
		1 MHz sinusoidal noise		—	–97	—	dBc
Output-output Crosstalk[3]	XTALK	Si5347		—	–72	—	dB
		Si5346		—	–88	—	dB

Notes:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5347-46 Rev D Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.
2. Measured for 156.25 MHz carrier frequency. 100 mVpp of sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.

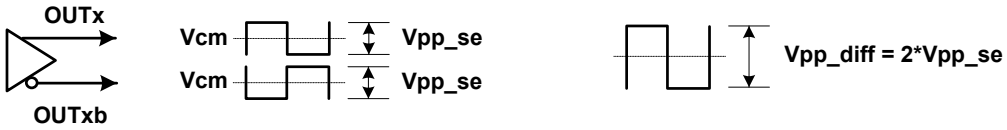


Table 5.6. LVCMOS Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		45	—	55	
Output Voltage High[1,2,3]	V_{OH}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –12 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –17 mA		—	—	
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=2	I_{OH} = –8 mA		—	—	
		OUTx_CMOS_DRV=3	I_{OH} = –11 mA		—	—	
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV=3	I_{OH} = –5 mA		—	—	
Output Voltage Low[1,2,3]	V_{OL}	V_{DDO} = 3.3 V					
		OUTx_CMOS_DRV=1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 12 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 17 mA	—	—		
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV=1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=2	I_{OL} = 8 mA	—	—		
		OUTx_CMOS_DRV=3	I_{OL} = 11 mA	—	—		
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV=2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV=3	I_{OL} = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3V		—	400	600	ps
		VDDO = 2.5 V		—	450	600	ps
		VDDO = 1.8 V		—	550	750	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5347-46 Rev D Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the dc test configuration.
3. A 5 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, at 156.25 MHz.

LVCMOS Output Test Configuration

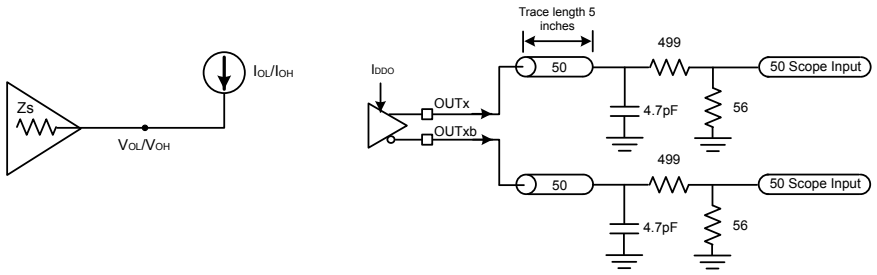


Table 5.7. Output Serial and Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5347 Serial and Status Output Pins (LOL_Ab, LOL_Bb, LOL_Cb, LOL_Db, INTRb, LOS_XAXBb, SDA/SDIO[1], A1/SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5346 Status Output Pins (INTRb, LOS_XAXBb, SDA/SDIO[1], A1/SDO)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5346 Serial and Status Output Pins (LOL_Ab, LOL_Bb)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

Notes:

1. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I2C_SEL pulled high. V_{OL} remains valid in all cases.
2. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5347-46 Rev D Reference Manual for more details on register settings.

Table 5.8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Loop Bandwidth Programming Range[1]	f_{BW}		0.1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL Lock Time[2]	t_{ACQ}	With Fastlock enabled, f_{IN} = 19.44 MHz	—	280	300	ms
POR to Serial Interface Ready[3]	t_{RDY}		—	—	15	ms
Jitter Peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1&2 Carrier Frequency = 10.3125 GHz Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Manual or automatic switch between two input clocks at same frequency[5]	—	—	2.4	ns
Pull-in Range	ω_P		—	500	—	ppm
RMS Phase Jitter[4]	J_{GEN}	12 kHz to 20 MHz	—	95	140	fs rms

Notes:

1. Actual loop bandwidth might be lower; please refer to CBPro for actual value on your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths, both set to 100 Hz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
3. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Jitter generation test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz. Does not include jitter from input reference.
5. For input frequency configurations, which have Fpfd > 1 MHz. Consult your CBPro Design report for the Fpfd frequency of your configuration.

Table 5.9. I²C Timing Specifications (SCL, SDA)

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

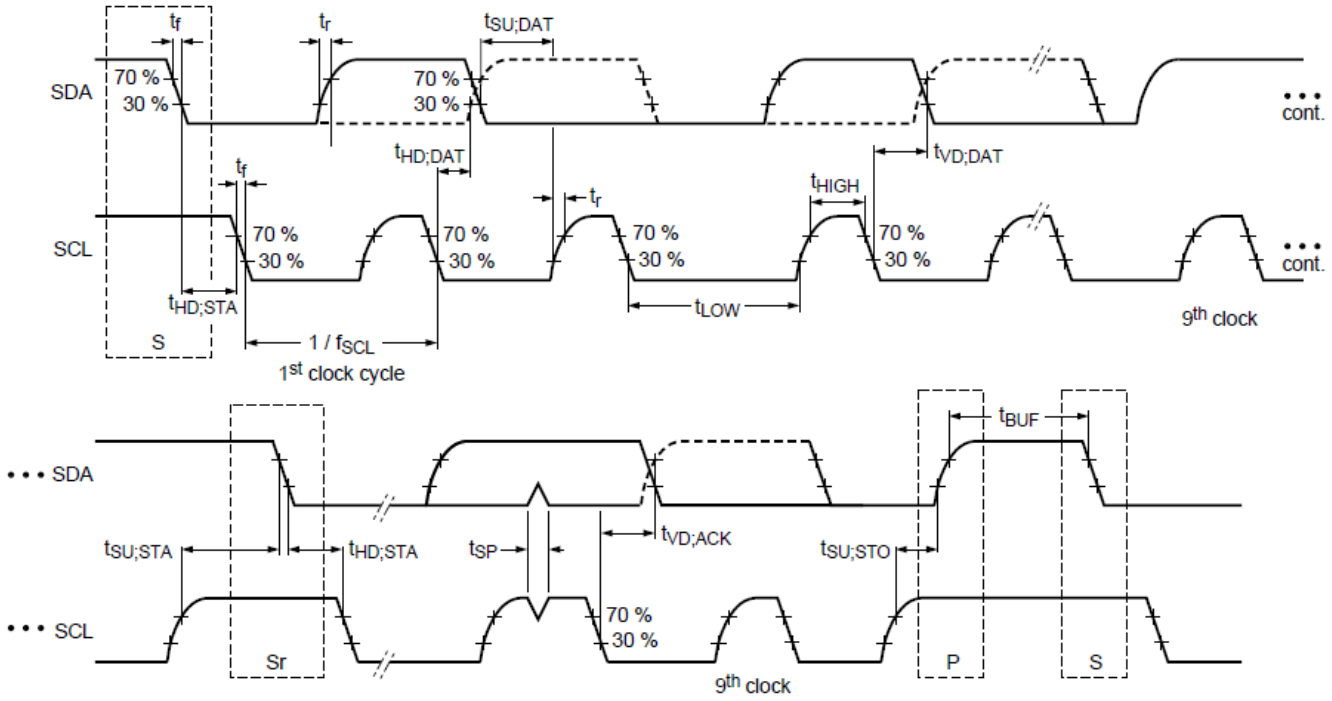


Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

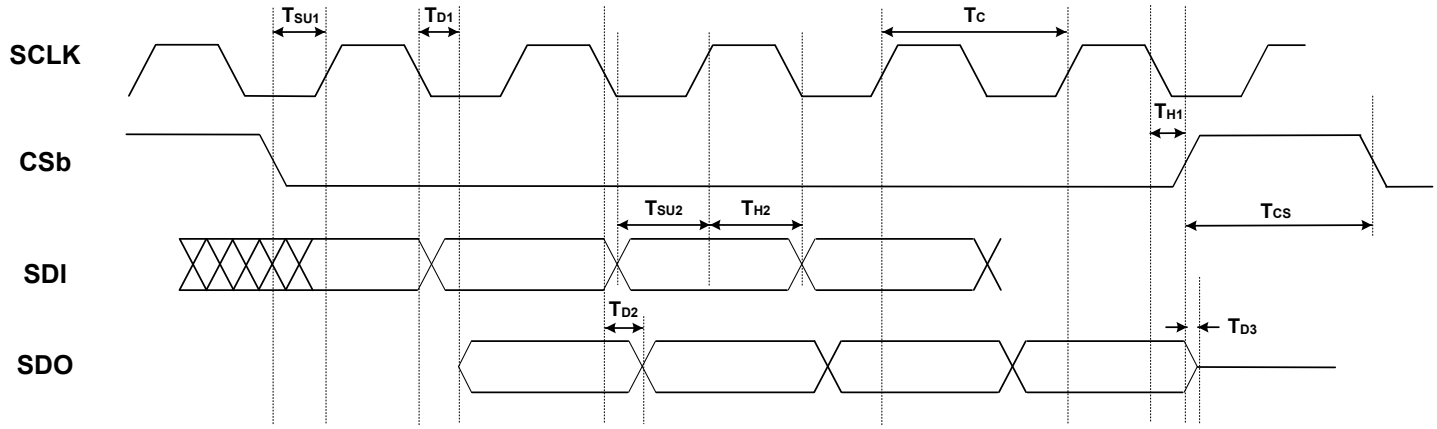


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	2	—	—	T_C

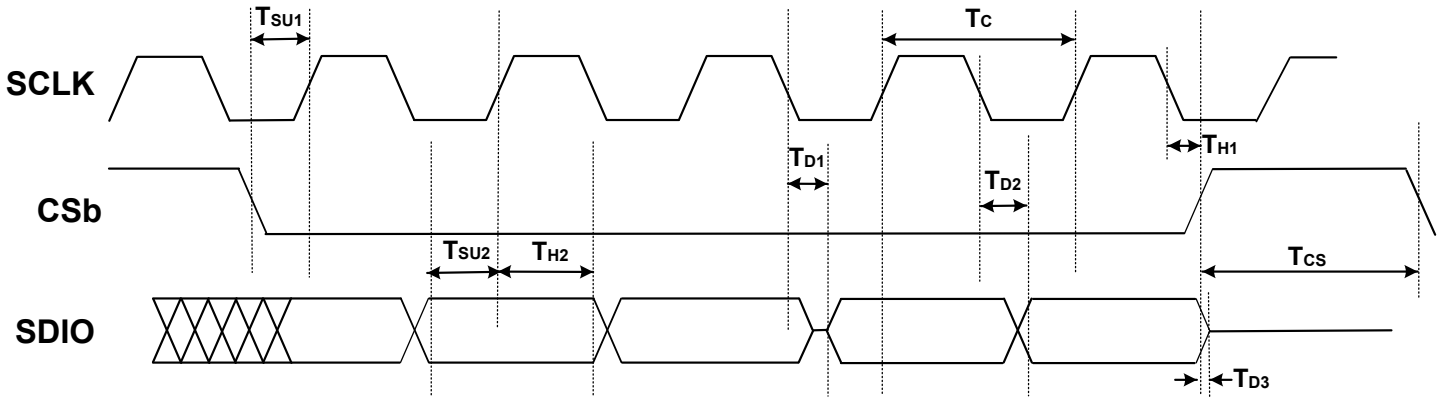


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. Crystal Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency Range	f_{XTAL}	Full operating range. Jitter performance may be reduced.	24.97	—	54.06	MHz
		Range for best jitter.	48	—	54	MHz
Load Capacitance	C_L		—	8	—	pF
Crystal Drive Level	d_L		—	—	200	µW
Equivalent Series Resistance Shunt Capacitance	r_{ESR} C_O	Refer to the Si5347-46 Rev D Reference Manual to determine ESR and shunt capacitance.				

Notes:

1. Refer to the Si534x/8x Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 48 to 54 MHz crystals. The Si5348 is designed to only work with crystals that meet these specifications and not with XOs.

Table 5.13. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Unit
Si5347–64QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	θ_{JC}		9.5	
Thermal Resistance Junction to Board	θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	
Si5346–44QFN				
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	22.3	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.4	
Thermal Resistance Junction to Case	θ_{JC}		10.9	
Thermal Resistance Junction to Board	θ_{JB}		9.3	
	Ψ_{JB}		9.2	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.23	

Note:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.14. Absolute Maximum Ratings[1, 2, 3, 4]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input Voltage Range	V_{I1}[5]	IN0 – IN3	–1.0 to 3.8	V
	V_{I2}	RSTb, OE0b, OE1b, I2C_SEL, FINC, FDEC, PLL_SEL[1:0] SDA/SDIO, A1/SDO, SCLK, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Max Junction Temperature in Operation	T_{JCT}		125	°C
Storage Temperature Range	T_{STG}		–55 to 150	°C
Soldering Temperature (Pb-free profile)[3]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P		20–40	s

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN and 44-QFN packages are RoHS-6 compliant.
3. For detailed MSL and packaging information, go to https://www.skyworksinc.com/Product_Certificate.aspx.
4. The device is compliant with JEDEC J-STD-020.
5. The minimum voltage at these pins can be as low as –1.0 V when an AC input signal of 10 MHz or greater is applied. See Table 5.3 Input Clock Specifications on page 27 spec for Single-ended AC Coupled f_{IN} < 250 MHz.

6. Typical Application Schematic

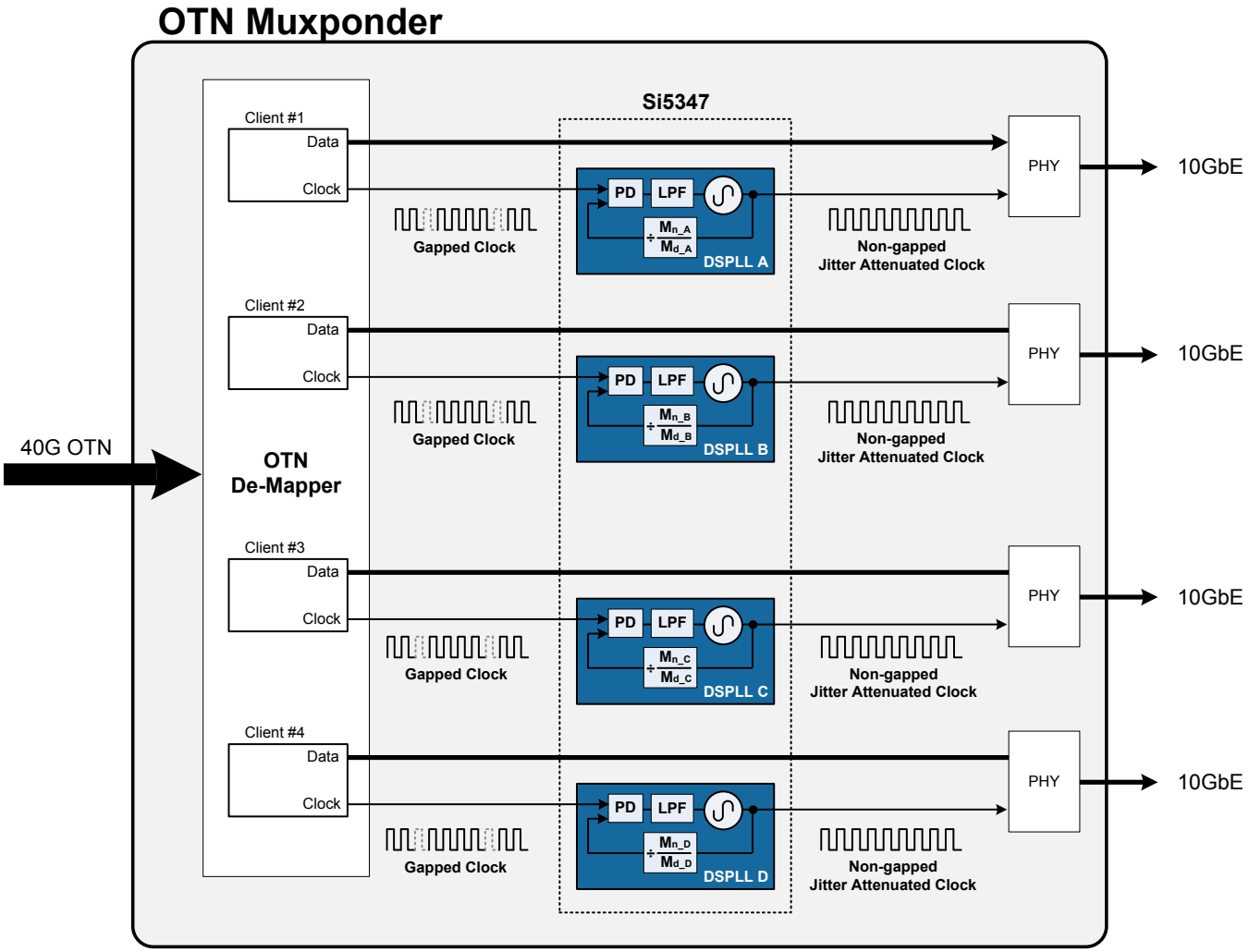


Figure 6.1. Using the Si5347 to Clean Gapped Clocks in an OTN Application

7. Detailed Block Diagrams

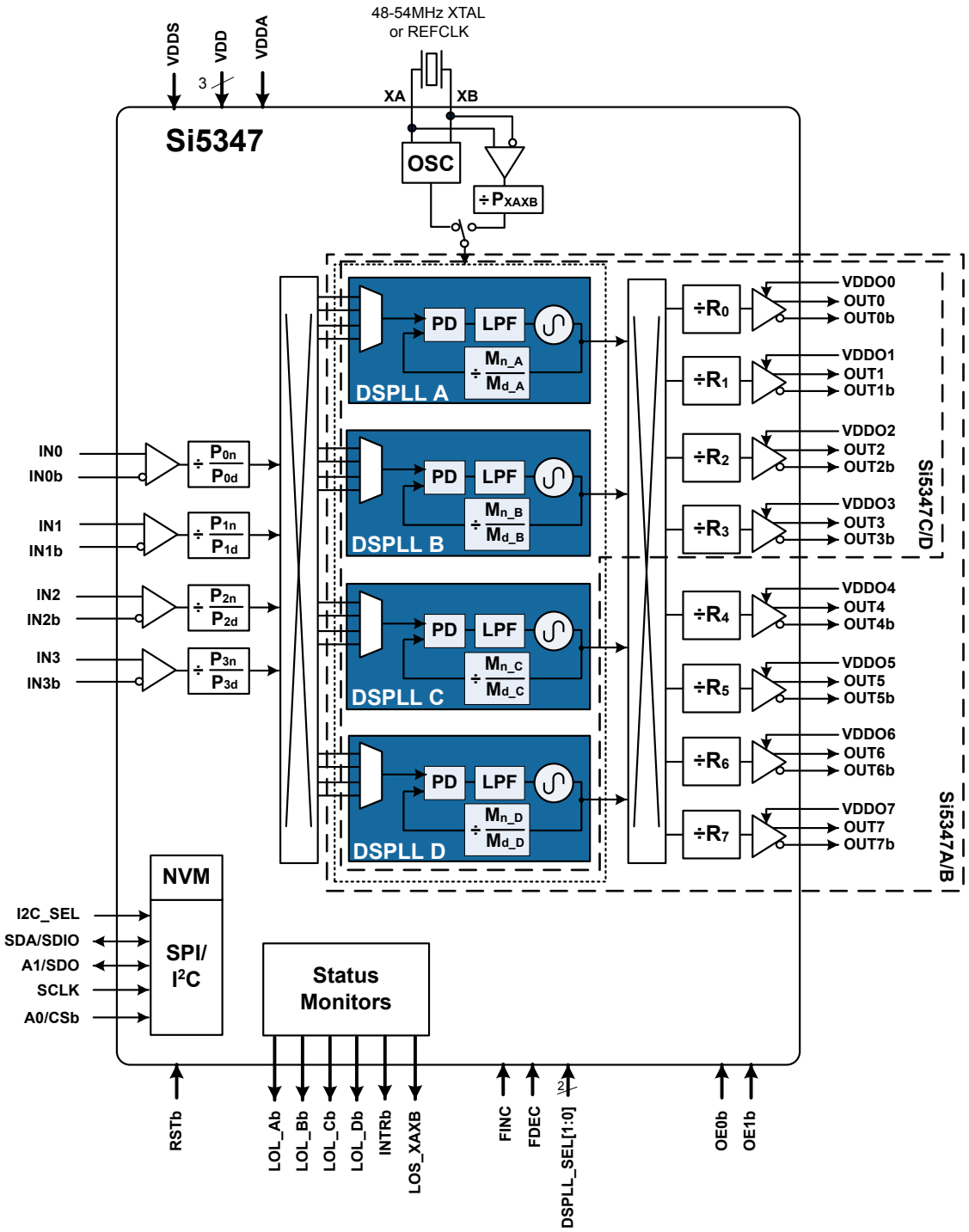


Figure 7.1. Si5347 Block Diagram

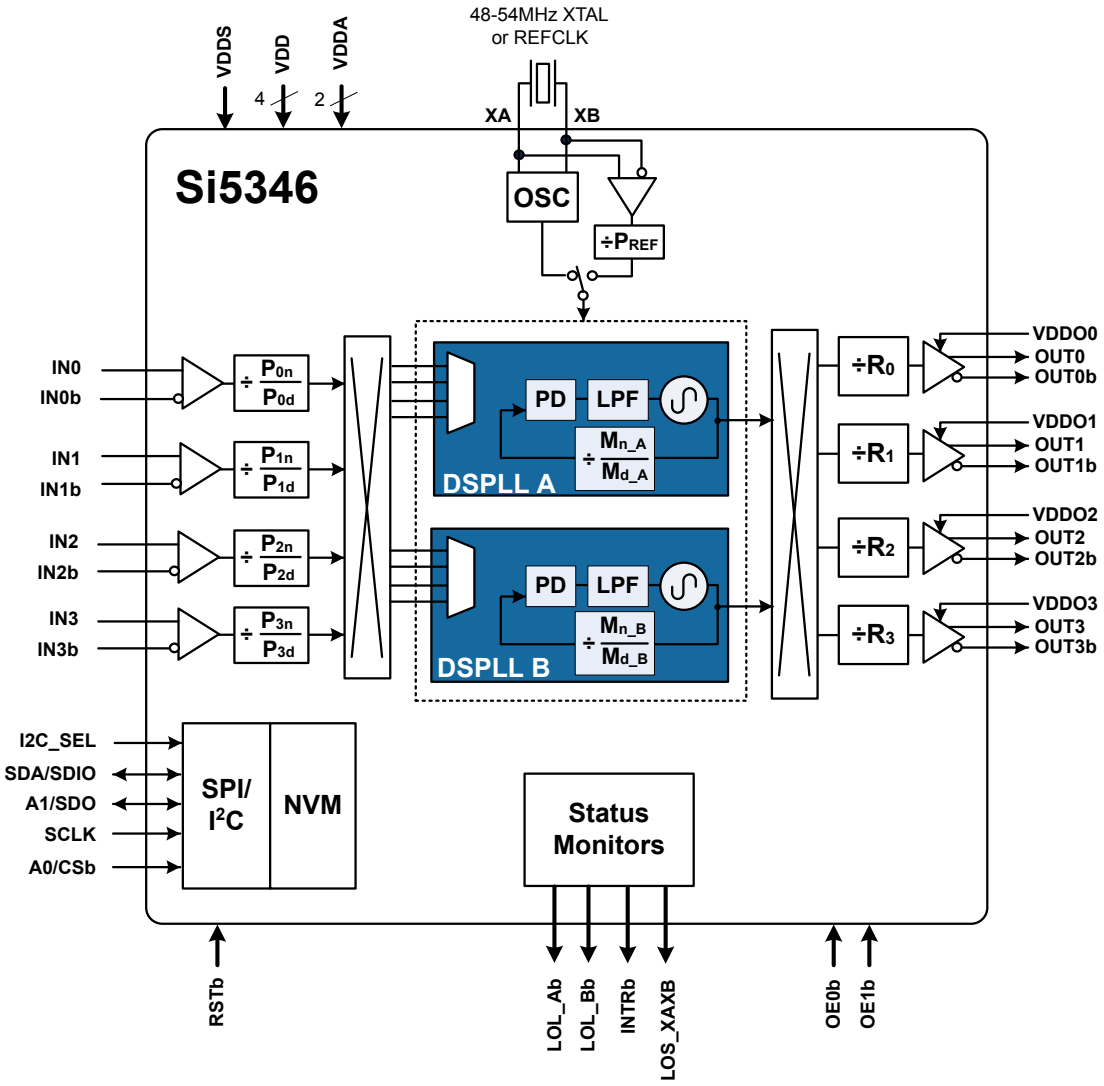


Figure 7.2. Si5346 Block Diagram

8. Typical Operating Characteristics (Jitter and Phase Noise)

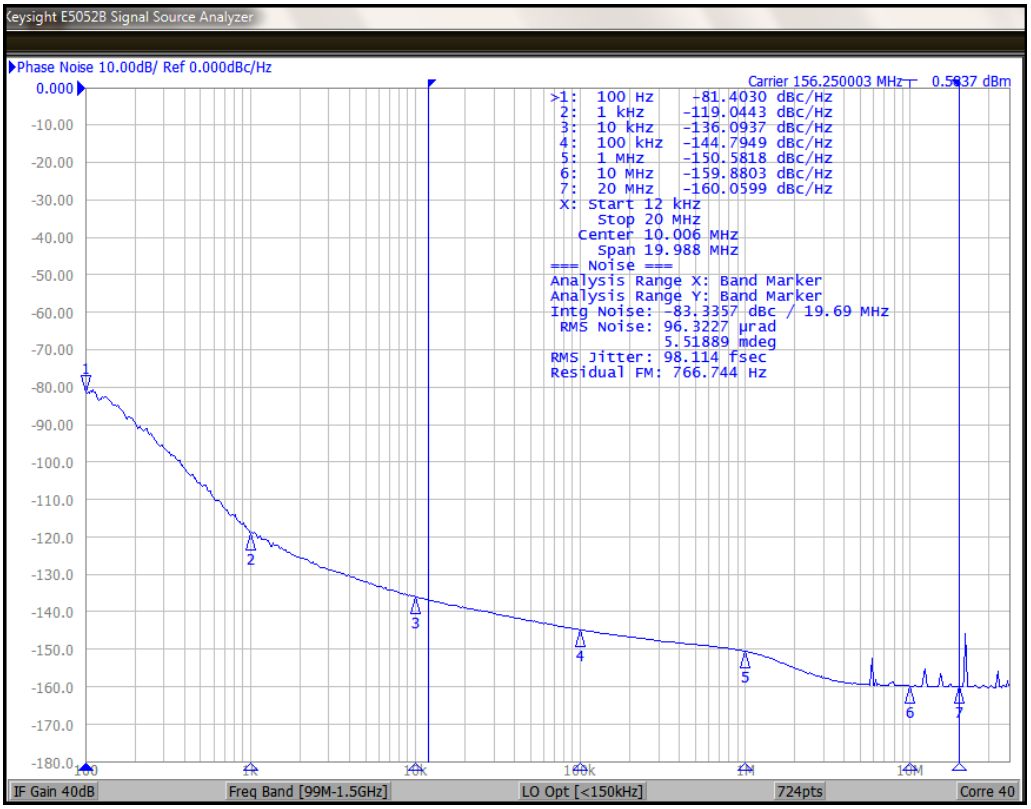


Figure 8.1. Input = 25 MHz; Output = 156.25 MHz, 2.5 V LVDS

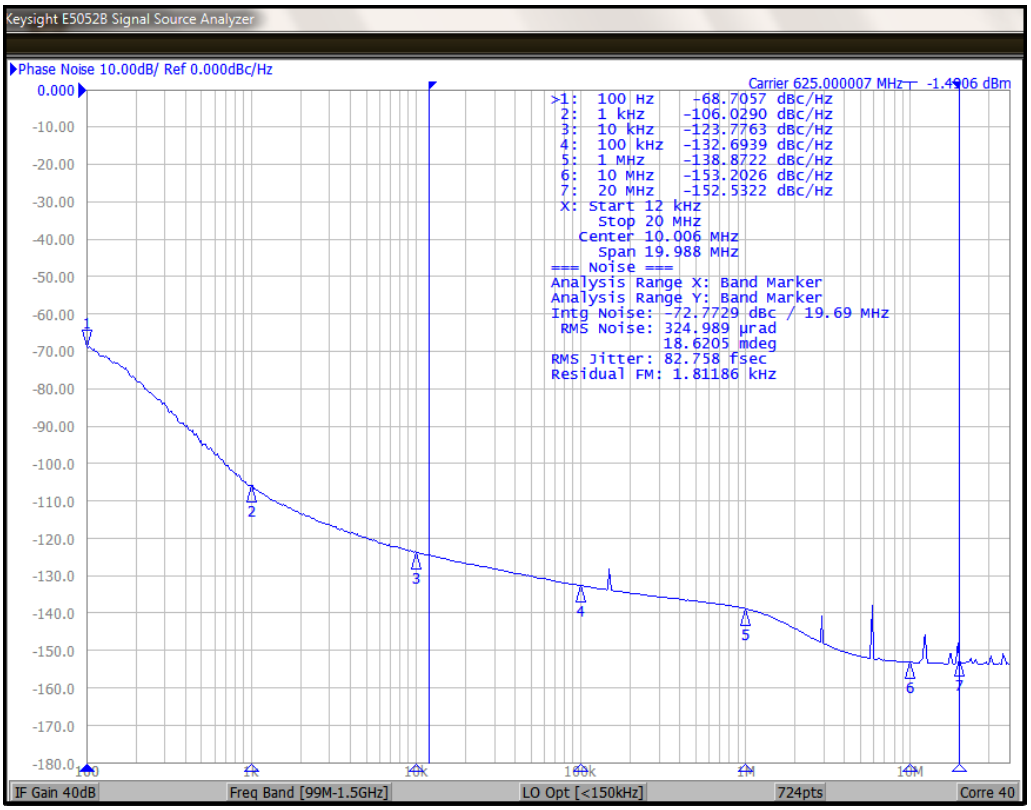


Figure 8.2. Input = 25 MHz; Output = 625 MHz, 2.5 V LVDS

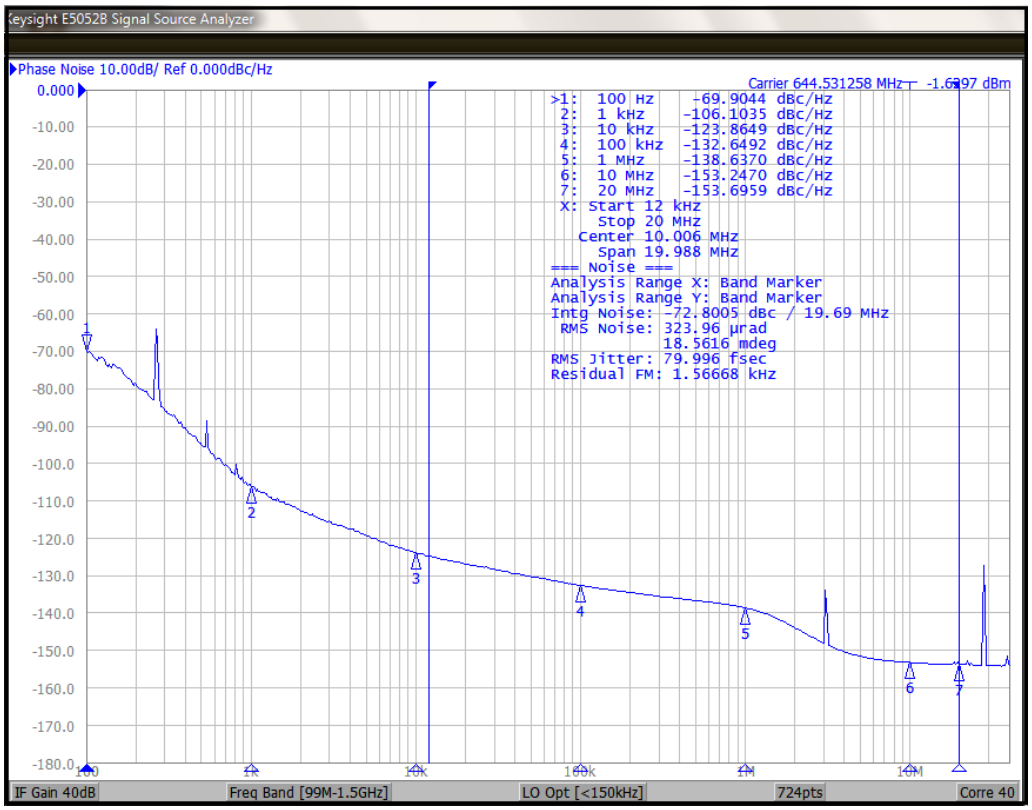


Figure 8.3. Input = 19.44 MHz; Output = 644.53125 MHz, 2.5 V LVDS

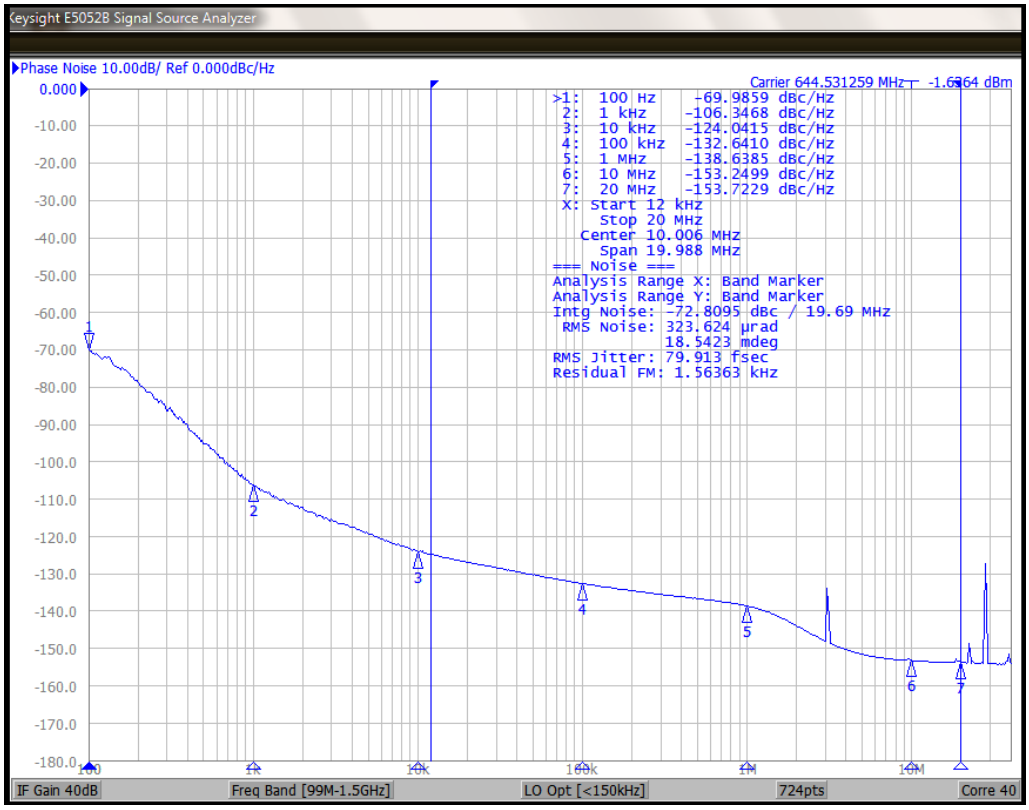


Figure 8.4. Input = 25 MHz; Output = 644.53125 MHz, 2.5 V LVDS

9. Pin Descriptions

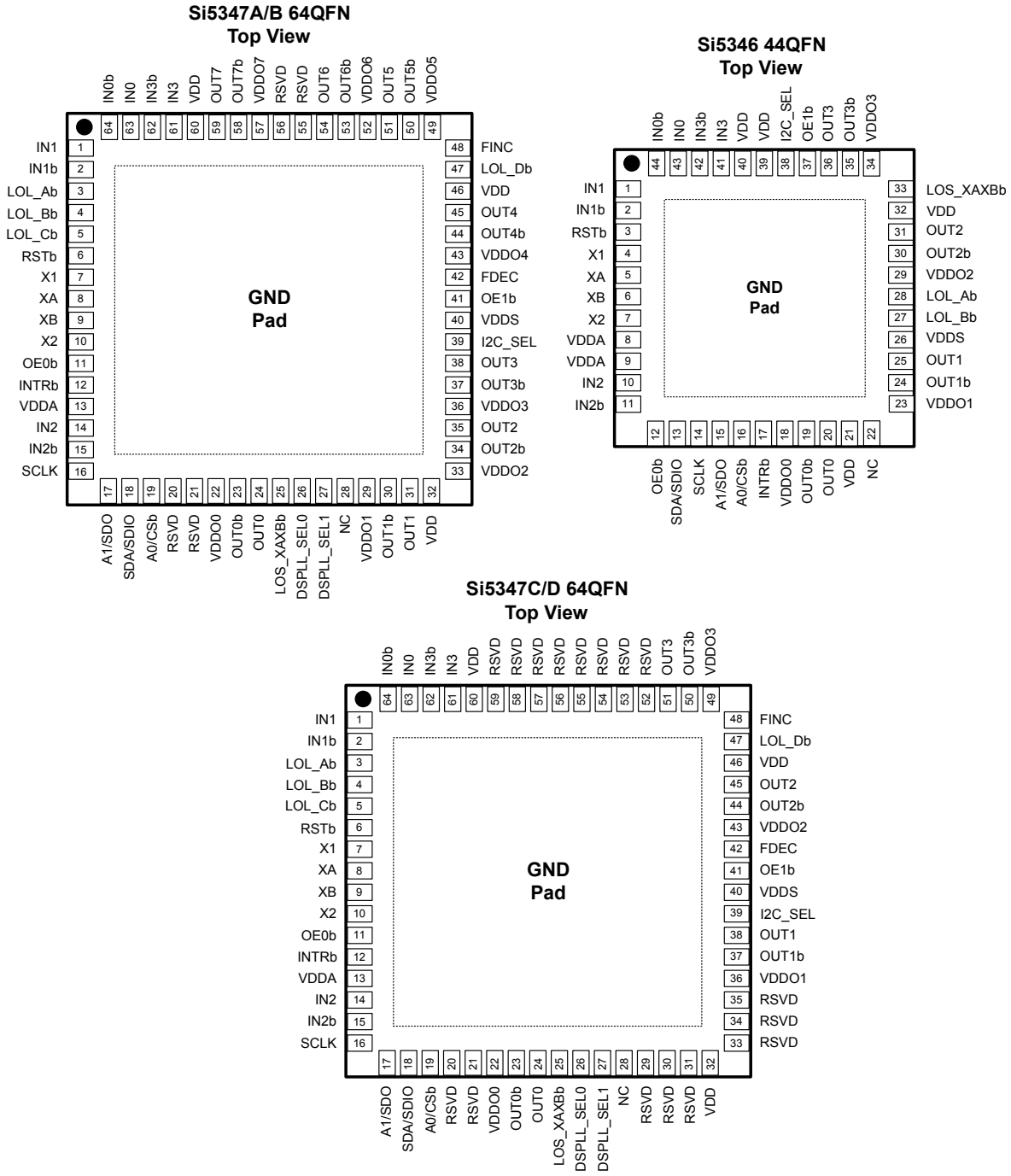


Figure 9.1. Si5347/46 Pin Descriptions

Table 9.1. Si5347/46 Pin Descriptions[1]

Pin Name	Pin Number			Pin Type[2]	Function
	Si5347A/B	Si5347C/D	Si5346		
Inputs					
XA	8	8	5	I	**Crystal Input.** Input pin for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.
XB	9	9	6	I	
X1	7	7	4	I	**XTAL Ground.** Connect these pins directly to the XTAL ground pins. X1, X2, and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5347-46 Rev D Reference Manual for layout guidelines. These pins should be left disconnected when connecting XA/XB pins to an external reference clock (REFCLK).
X2	10	10	7	I	
IN0	63	63	43	I	**Clock Inputs.** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to 3.6.4 Input Configuration and Terminations for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded when accepting a single-ended clock.
IN0b	64	64	44	I	
IN1	1	1	1	I	
IN1b	2	2	2	I	
IN2	14	14	10	I	
IN2b	15	15	11	I	
IN3	61	61	41	I	
IN3b	62	62	42	I	
Outputs					
OUT0	24	24	20	O	**Output Clocks.** These output clocks support a programmable signal amplitude and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in 3.8.2 Differential Output Terminations and 3.8.3 LVCMOS Output Terminations. Unused outputs should be left unconnected.
OUT0b	23	23	19	O	
OUT1	31	38	25	O	
OUT1b	30	37	24	O	
OUT2	35	45	31	O	
OUT2b	34	44	30	O	
OUT3	38	51	36	O	
OUT3b	37	50	35	O	
OUT4	45	—	—	O	
OUT4b	44	—	—	O	
OUT5	51	—	—	O	
OUT5b	50	—	—	O	
OUT6	54	—	—	O	
OUT6b	53	—	—	O	
OUT7	59	—	—	O	
OUT7b	58	—	—	O	

Pin Name	Pin Number			Pin Type[2]	Function
	Si5347A/B	Si5347C/D	Si5346		
Serial Interface					
I2C_SEL	39	39	38	I	**I2C Select.**[3] This pin selects the serial interface mode as I^2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.
SDA/SDIO	18	18	13	I/O	**Serial Data Interface.**[3] This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of > 1 kΩ. No pull-up resistor is needed when in SPI mode.
A1/SDO	17	17	15	I/O	**Address Select 1/Serial Data Output.**[3] In I^2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode this is the serial data output (SDO) pin.
SCLK	16	16	14	I	**Serial Clock Input.**[3] This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of > 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	19	19	16	I	**Address Select 0/Chip Select.**[3] This pin functions as the hardware controlled address A0 in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up.
Control/Status					
INTRb	12	12	17	O	**Interrupt.**[3] This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	6	6	3	I	**Device Reset.**[3] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up.
OE0b	11	11	12	I	**Output Enable 0.**[3] This pin is used to enable (when held low) and disable (when held high) the output clocks. By default this pin controls all outputs. It can also be configured to control a subset of outputs. See 3.8.9 Output Enable/Disable for details. This pin is internally pulled-down.
OE1b	41	41	—		**Output Enable 1. (Si5347)**[4] This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See 3.8.9 Output Enable/Disable for details. There is no internal pull-up/pull-down for this pin. This pin must be pulled up or down externally (do not leave floating when not in use).
	—	—	37		**Output Enable 1. (Si5346)**[3] This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See 3.8.9 Output Enable/Disable for details. This pin is internally pulled-down.

Pin Name	Pin Number			Pin Type[2]	Function
	Si5347A/B	Si5347C/D	Si5346		
LOL_Ab	3	3	28	O	**Loss Of Lock_A/B/C/D.[3, 4]** These output pins indicate when DSPLL A, B, C, D is out-of-lock (low) or locked (high). They can be left unconnected when not in use. Si5347: See Note 3, Si5346: See Note 4.
LOL_Bb	4	4	27	O	
LOL_Cb	5	5	—	O	
LOL_Db	47	47	—	O	
LOS_XAXBb	25	25	33	O	**Status Pins.[3]** This pin indicates a loss of signal alarm on the XA/XB pins. This either indicates a XTAL failure or a loss of external signal on the XA/XB pins. This pin can be left unconnected when unused.
DSPLL_SEL 0	26	26	—	I	**DSPLL Select Pins (Si5347 only).[3]** These pins are used in conjunction with the FINC and FDEC pins. The DSPLL_SEL[1:0] pins determine which DSPLL is affected by a frequency change using the FINC and FDEC pins. See 3.4 Digitally-Controlled Oscillator (DCO) Mode for details. These pins are internally pulled-down.
DSPLL_SEL 1	27	27	—	I	
FDEC	42	42	—	I	**Frequency Decrement Pin (Si5347 only).[4]** This pin is used to step-down the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_SEL[1:0] pins. This pin must be pulled up or down externally (do not leave floating when not in use).
FINC	48	48	—	I	**Frequency Increment Pin (Si5347 only).[3]** This pin is used to step-up the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_SEL[1:0] pins. This pin is pulled low internally and can be left unconnected when not in use.
RSVD	20	20	—	—	**Reserved.** These pins are connected to the die. Leave disconnected.
	21	21	—	—	
	—	29	—	—	
	—	30	—	—	
	—	31	—	—	
	—	33	—	—	
	—	34	—	—	
	—	35	—	—	
	—	52	—	—	
	—	53	—	—	
	—	54	—	—	
	55	55	—	—	
	56	56	—	—	
	—	57	—	—	
	—	58	—	—	
	—	59	—	—	

Pin Name	Pin Number			Pin Type[2]	Function
	Si5347A/B	Si5347C/D	Si5346		
NC	28	28	22	—	**No Connect.** These pins are not connected to the die. Leave disconnected.
Power					
VDD	32	32	21	P	**Core Supply Voltage.** The device core operates from a 1.8 V supply. See the Si5347-46 Rev D Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	46	46	32		
	60	60	39		
	—	—	40		
VDDA	13	13	8	P	**Core Supply Voltage 3.3 V.** This core supply pin requires a 3.3 V power source. See the Si5347-46 Rev D Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	—	—	9	P	
VDDS	40	40	26	P	**Status Output Voltage.** The voltage on this pin determines VOL/VOH on the Si5346 LOL_Ab and LOL_Bb outputs. On the Si5347, this pin determines VIL/VIH for the FDEC and OE1b inputs. Connect to either 3.3 V or 1.8 V. A 0.1 µF bypass capacitor should be placed very close to this pin.
VDDO0	22	22	18	P	**Output Clock Supply Voltage 0–7.** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTnb outputs. A 0.1 uF bypass capacitor should be placed very close to this pin. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins.
VDDO1	29	36	23	P	
VDDO2	33	43	29	P	
VDDO3	36	49	34	P	
VDDO4	43	—	—	P	
VDDO5	49	—	—	P	
VDDO6	52	—	—	P	
VDDO7	57	—	—	P	
GND PAD	—	—	—	P	**Ground Pad.** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plan as short as possible.

Notes:

1. Refer to the Si5347-46 Rev D Reference Manual for more information on register setting names.
2. I = Input, O = Output, P = Power.
3. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
4. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.
5. All status pins except I2C and SPI are push-pull.

10. Package Outlines

10.1 Si5347 9x9 mm 64-QFN Package Diagram

The figure below illustrates the package details for the Si5347. The table below lists the values for the dimensions shown in the illustration.

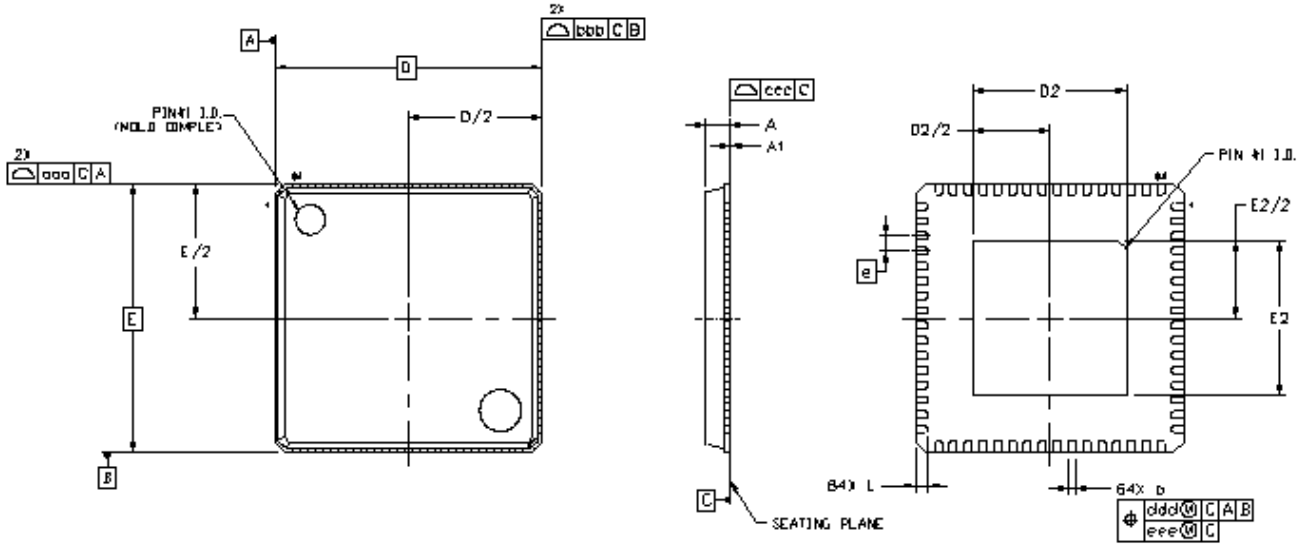


Figure 10.1. 64-Pin Quad Flat No-Lead (QFN)

Table 10.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.2 Si5346 7x7 mm 44-QFN Package Diagram

The figure below illustrates the package details for the Si5346. The table below lists the values for the dimensions shown in the illustration.

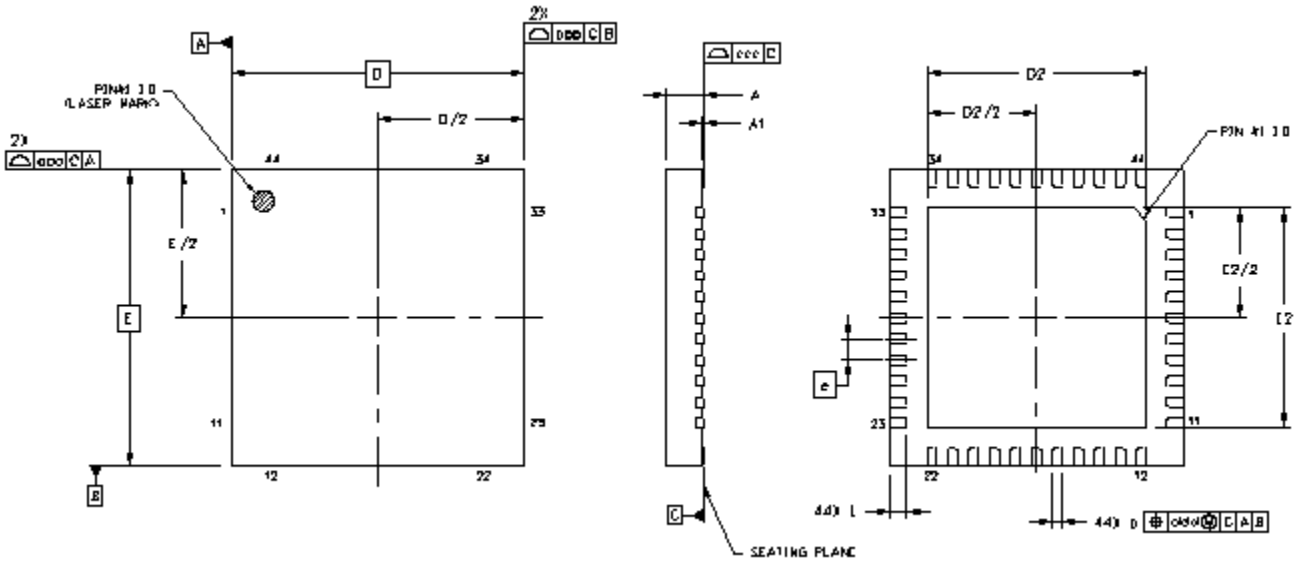


Figure 10.2. 44-Pin Quad Flat No-Lead (QFN)

Table 10.2. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

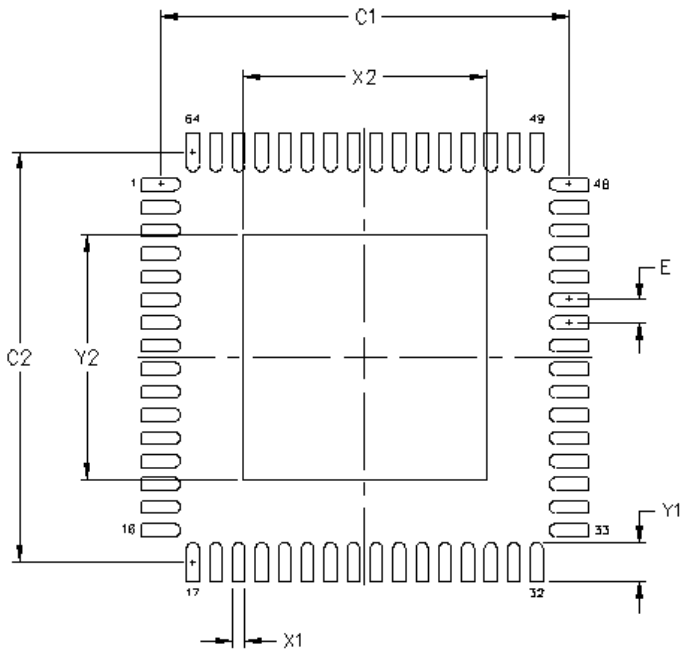
Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration. Refer to the Si5347-46 Rev D Reference Manual for information about thermal via recommendations.

Si5347



Si5346

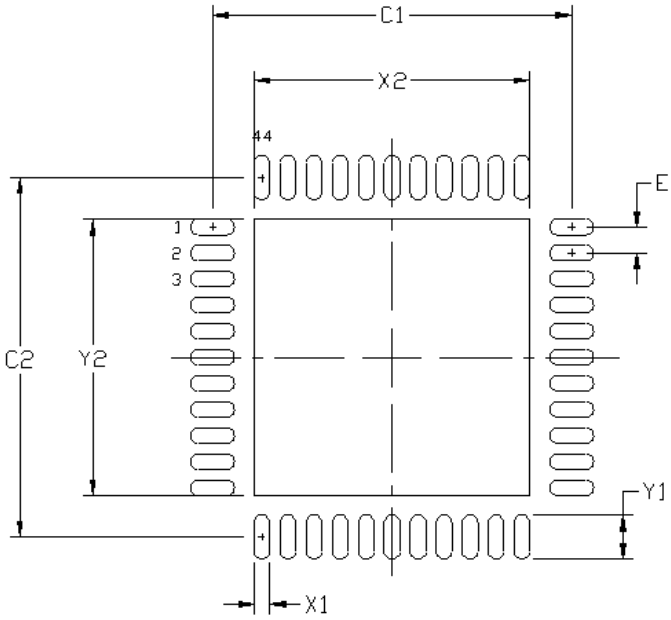


Figure 11.1. PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5347 (Max)	Si5346 (Max)
C1	8.90	6.90
C2	8.90	6.90
E	0.50	0.50
X1	0.30	0.30
Y1	0.85	0.85
X2	5.30	5.30
Y2	5.30	5.30

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 3x3 array of 1.25 mm square openings on 1.80 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

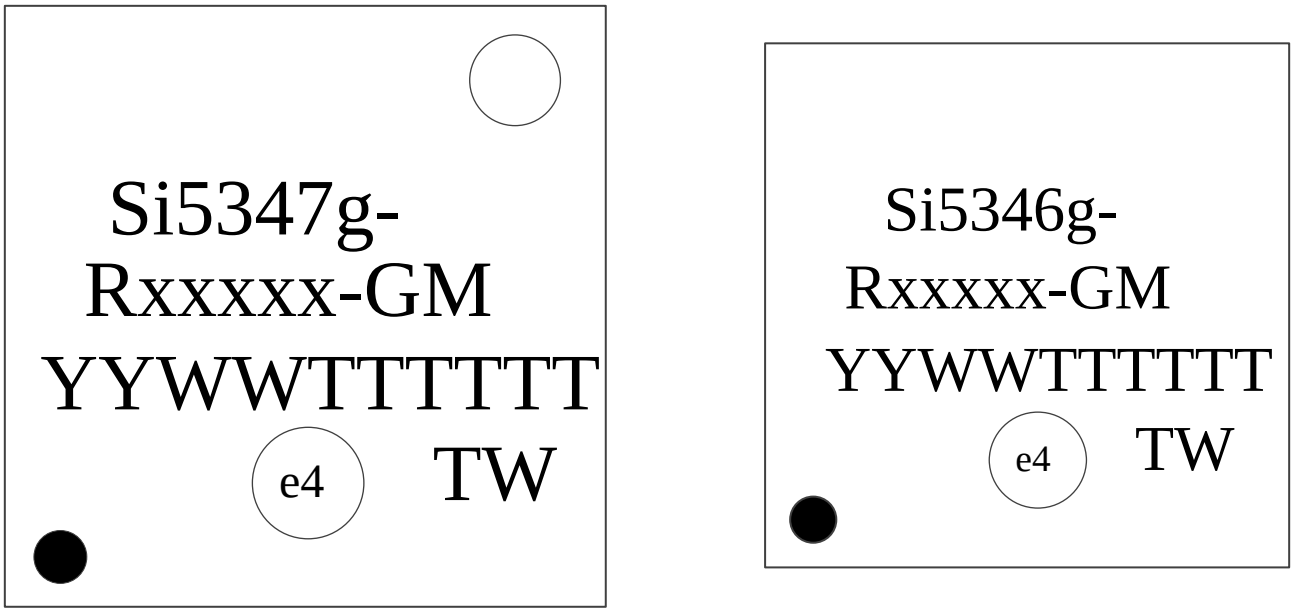


Figure 12.1. Si5347/46 Top Marking

Table 12.1. Si5347/46 Top Marking Explanation

Line	Characters	Description
1	Si5347g- Si5346g-	Base part number and Device Grade. Si5347: Quad PLL; 64-QFN Si5346: Dual PLL; 44-QFN g = Device Grade. See Section 2. Ordering Guide for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (See Section 2. Ordering Guide for current revision.) xxxxx = Customer specific NVM sequence number. (Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices). See Section 2. Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C).
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) or 1.4 mm (44-QFN) diameter	Pin 1 indicator; left-justified
	e4	Pb-free symbol; Center-Justified
	TW	TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

Log in or register at http://www.skyworksinc.com to access the device errata document.

14. Revision History

Revision 1.1

September, 2018

- Updated Figure 3.3 Crystal Resonator and External Reference Clock Connection Options on page 9.
- Updated Figure 3.5 Termination of Differential and LVCMOS Input Signals on page 11.
- Updated Figure 3.15 Supported Differential Output Terminations on page 19.
- Updated .
  - Updated Note 4 and LVCMOS Output Test Configuration circuit.
- Updated Table 5.3 Input Clock Specifications on page 27.
- Updated .
  - Updated Input Capacitance values.
- Updated Output-to-Output Skew specification in Table 5.5 Differential Clock Output Specifications on page 29.
- Removed Output-to-Output Skew specification in Table 5.6 LVCMOS Clock Output Specifications on page 30.
  - Updated LVCMOS Output Test Configuration under Note 3.
- Removed Input-to-Output Delay Variation specification in Table 5.8 Performance Characteristics on page 32.
  - Updated Note 2 and Removed Note 6.

Revision 1.0

July, 2016

- Initial release.

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