



# ADC322x

## Dual-Channel, 12-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters

### 1 Features

- Dual channel
- 12-Bit resolution
- Single supply: 1.8 V
- Serial LVDS interface (SLVDS)
- Flexible input clock buffer with divide-by-1, -2, -4
- SNR = 70.2 dBFS, SFDR = 87 dBc at  $f_{IN} = 70$  MHz
- Ultra-low power consumption:
  - 116 mW/Ch at 125 MSPS
- Channel isolation: 105 dB
- Internal dither and chopper
- Support for multi-chip synchronization
- Pin-to-pin compatible with 14-Bit version
- Package: VQFN-48 (7 mm × 7 mm)

### 2 Applications

- [Multi-carrier, multi-mode cellular base stations](#)
- [Radar and smart antenna arrays](#)
- [Munitions guidance](#)
- [Motor control feedback](#)
- [Network and vector analyzers](#)
- Communications test equipment
- Nondestructive testing
- [Microwave receivers](#)
- Software-defined radios (SDRs)
- Quadrature and diversity radio receivers
- [Handheld radio and instrumentation](#)

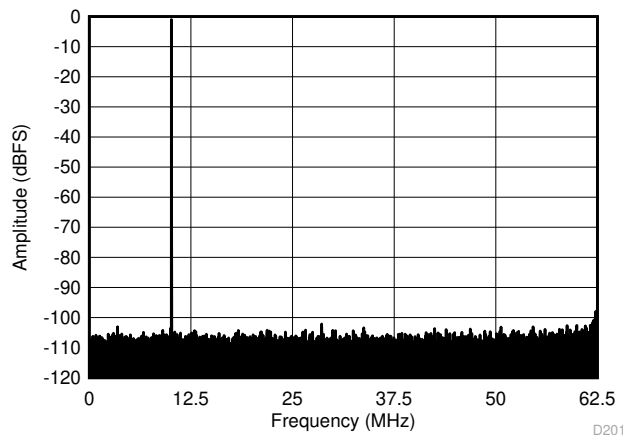
### 3 Description

The ADC322x are a high-linearity, ultra-low power, dual-channel, 12-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC322x family supports serial low-voltage differential signaling (LVDS) in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. Optionally, a one-wire serial LVDS interface is available. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

#### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|-------------|------------------------|-------------------|
| ADC322x     | VQFN (48)              | 7.00 mm × 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Performance at  $f_s = 125$  MSPS,  $f_{IN} = 10$  MHz  
(SNR = 70.6 dBFS, SFDR = 100 dBc)**



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## 4 Revision History

### Changes from Revision D (August 2019) to Revision E (June 2022) Page

|  |   |
|--|---|
| • Changed the device number from: ADC3241 to: ADC3221 and ADC3242 to: ADC3222 in <i>Electrical Characteristics: ADC3221, ADC3222</i> ..... | 8 |
| • Changed the device number from: ADC3243 to: ADC3223 and ADC3244 to: ADC3224 in <i>Electrical Characteristics: ADC3223, ADC3224</i> ..... | 8 |

### Changes from Revision C (July 2019) to Revision D (August 2019) Page

|   |    |
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| • Deleted Graphs: Histogram, Integral Nonlinearity, and Differential Nonlinearity ..... | 19 |
| • Deleted Graphs: Histogram, Integral Nonlinearity, and Differential Nonlinearity ..... | 24 |
| • Deleted Graphs: Histogram, Integral Nonlinearity, and Differential Nonlinearity ..... | 30 |
| • Deleted Graphs: Histogram, Integral Nonlinearity, and Differential Nonlinearity ..... | 35 |

### Changes from Revision B (March 2016) to Revision C (July 2019) Page

|   |   |
|---|---|
| • Added text to the <i>Description</i> : Optionally, a one-wire serial LVDS interface is available. ....                                    | 1 |
| • Changed the description of pin AVDD, DVDD, GND, and PDN pins in the <i>Pin Functions</i> table .....                                      | 4 |
| • Changed the condition statement for <i>Electrical Characteristics: General</i> .....  | 7 |
| • Moved the location of <i>Electrical Characteristics: General</i> .....  | 7 |
| • Changed the parameter description of $E_{G(REF)}$ in <i>Electrical Characteristics: General</i> .....                                     | 7 |
| • Deleted $E_{G(CHAN)}$ from <i>Electrical Characteristics: General</i> .....   | 7 |
| • Changed the parameter description of $\alpha_{(EGCHAN)}$ in <i>Electrical Characteristics: General</i> .....                              | 7 |
| • Changed the condition statement for <i>Electrical Characteristics: ADC3221, ADC3222</i> .....   | 8 |
| • Changed ADC clock frequency (ADC3241) From: MAX = 125 MSPS To: MAX = 25 MSPS in <i>Electrical Characteristics: ADC3221, ADC3222</i> ..... | 8 |
| • Changed ADC clock frequency (ADC3242) From: MAX = 125 MSPS To: MAX = 50 MSPS in <i>Electrical Characteristics: ADC3221, ADC3222</i> ..... | 8 |

|  |    |
|--|----|
| • Changed the condition statement for <i>Electrical Characteristics: ADC3223, ADC3224</i> .....  | 8  |
| • Changed the condition statement for <i>Electrical Characteristics: ADC3221</i> .....           | 9  |
| • Changed the condition statement for <i>Electrical Characteristics: ADC3222</i> .....           | 11 |
| • Changed the condition statement for <i>Electrical Characteristics: ADC3223</i> .....           | 13 |
| • Changed the condition statement for <i>Electrical Characteristics: ADC3224</i> .....           | 15 |
| • Added Differential swing to <i>DIGITAL INPUTS (SYSREFP, SYSREFM)</i> .....                     | 17 |
| • Deleted $V_{IH}$ and $V_{IL}$ from <i>DIGITAL INPUTS (SYSREFP, SYSREFM)</i> .....              | 17 |
| • added table note: SYSREF is internally biased to 0.9 V.to <i>Digital Characteristics</i> ..... | 17 |
| • Added Graphs: Histogram, Integral Nonlinearity, and Differential Nonlinearity .....            | 19 |
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| • Added <i>Digital Inputs</i> section to Digital Characteristics table.....   | 17 |
| • Updated <a href="#">Figure 6-19</a> , <a href="#">Figure 6-20</a> , <a href="#">Figure 6-23</a> , <a href="#">Figure 6-24</a> , <a href="#">Figure 6-25</a> and, <a href="#">Figure 6-26</a> .....        | 19 |
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| • Updated <a href="#">Figure 6-79</a> , <a href="#">Figure 6-80</a> , <a href="#">Figure 6-83</a> , <a href="#">Figure 6-84</a> , <a href="#">Figure 6-85</a> , and <a href="#">Figure 6-86</a> .....       | 30 |
| • Updated <a href="#">Figure 6-109</a> , <a href="#">Figure 6-110</a> , <a href="#">Figure 6-113</a> , <a href="#">Figure 6-114</a> , <a href="#">Figure 6-115</a> , and <a href="#">Figure 6-116</a> ..... | 35 |
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| • Changed <a href="#">Figure 7-2</a> .....  | 42 |
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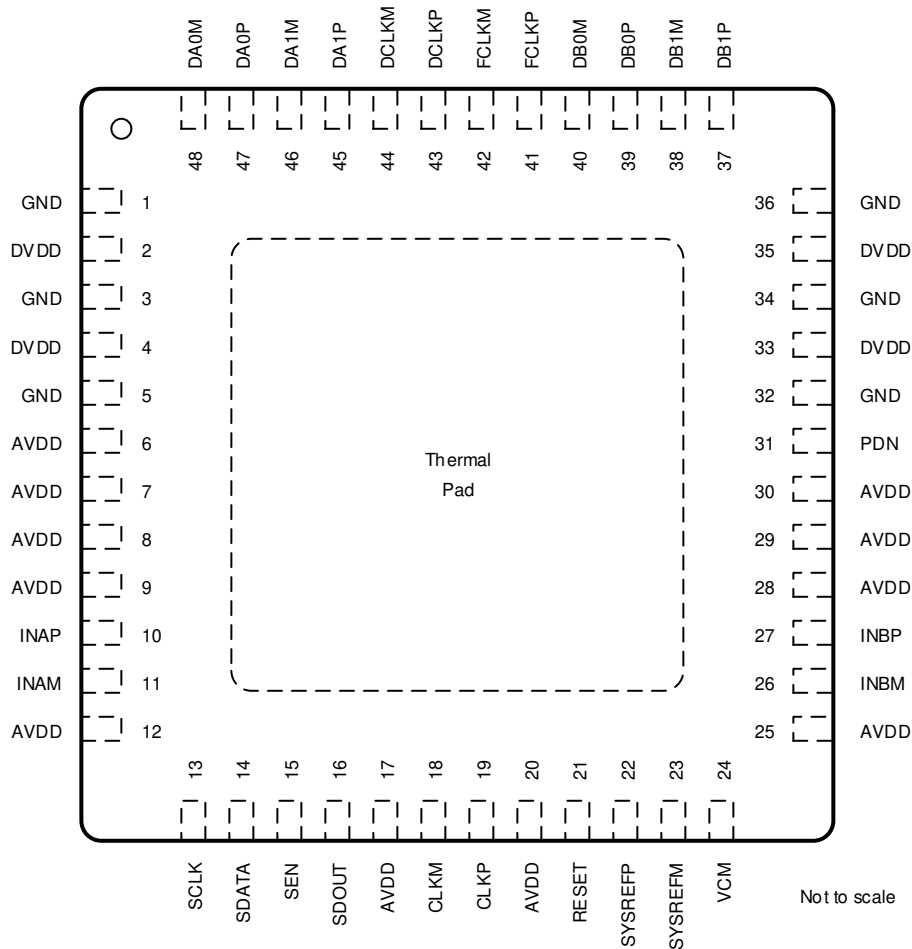
|                                    |   |
|------------------------------------|---|
| • Released to Production Data..... | 1 |
|------------------------------------|---|

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## Device Comparison Table

| INTERFACE   | RESOLUTION (Bits) | 25 MSPS | 50 MSPS  | 80 MSPS  | 125 MSPS | 160 MSPS  |
|-------------|-------------------|---------|----------|----------|----------|-----------|
| Serial LVDS | 12                | ADC3221 | ADC3222  | ADC3223  | ADC3224  | —         |
|             | 14                | ADC3241 | ADC3242  | ADC3243  | ADC3244  | —         |
| JESD204B    | 12                | —       | ADC32J22 | ADC32J23 | ADC32J24 | ADC32J2x5 |
|             | 14                | —       | ADC32J42 | ADC32J43 | ADC32J44 | ADC32J45  |

## 5 Pin Configuration and Functions



**Figure 5-1. RGZ Package, 48-Pin VQFN (Top View)**

**Table 5-1. Pin Functions**

| PIN  |  | I/O | DESCRIPTION   |
|------|--|-----|---|
| NAME | NO.                                    |     |   |
| AVDD | 6, 7, 8, 9, 12, 17, 20, 25, 28, 29, 30 | I   | Analog 1.8-V power supply, decoupled with capacitors. |
| CLKM | 18                                     | I   | Negative differential clock input for the ADC         |
| CLKP | 19                                     | I   | Positive differential clock input for the ADC         |
| DA0M | 48                                     | O   | Negative serial LVDS output for channel A0            |
| DA0P | 47                                     | O   | Positive serial LVDS output for channel A0            |
| DA1M | 46                                     | O   | Negative serial LVDS output for channel A1            |

**Table 5-1. Pin Functions (continued)**

| PIN     |                     | I/O | DESCRIPTION  |
|---------|---------------------|-----|--|
| NAME    | NO.                 |     |  |
| DA1P    | 45                  | O   | Positive serial LVDS output for channel A1   |
| DB0M    | 40                  | O   | Negative serial LVDS output for channel B0   |
| DB0P    | 39                  | O   | Positive serial LVDS output for channel B0   |
| DB1M    | 38                  | O   | Negative serial LVDS output for channel B1   |
| DB1P    | 37                  | O   | Positive serial LVDS output for channel B1   |
| DCLKM   | 44                  | O   | Negative bit clock output  |
| DCLKP   | 43                  | O   | Positive bit clock output  |
| DVDD    | 2, 4, 33, 35        | I   | Digital 1.8-V power supply, decoupled with capacitors.   |
| FCLKM   | 42                  | O   | Negative frame clock output  |
| FCLKP   | 41                  | O   | Positive frame clock output  |
| GND     | 1, 3, 5, 32, 34, 36 | I   | Ground, 0 V. Connect to the printed circuit board (PCB) ground plane. PowerPAD™  |
| INAM    | 11                  | I   | Negative differential analog input for channel A   |
| INAP    | 10                  | I   | Positive differential analog input for channel A   |
| INBM    | 26                  | I   | Negative differential analog input for channel B   |
| INBP    | 27                  | I   | Positive differential analog input for channel B   |
| PDN     | 31                  | I   | Power-down control; active high. This pin may be configured through the SPI. This pin has an internal 150-kΩ pull-down resistor. |
| RESET   | 21                  | I   | Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.   |
| SCLK    | 13                  | I   | Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.  |
| SDATA   | 14                  | I   | Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.   |
| SDOUT   | 16                  | O   | Serial interface data output   |
| SEN     | 15                  | I   | Serial interface enable; active low. This pin has an internal 150-kΩ pull-up resistor to AVDD.                                   |
| SYSREFM | 23                  | I   | Negative external SYSREF input   |
| SYSREFP | 22                  | I   | Positive external SYSREF input   |
| VCM     | 24                  | O   | Common-mode voltage for analog inputs  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                    |                                    | MIN  | MAX                   | UNIT |
|------------------------------------|------------------------------------|------|-----------------------|------|
| Analog supply voltage range, AVDD  |                                    | -0.3 | 2.1                   | V    |
| Digital supply voltage range, DVDD |                                    | -0.3 | 2.1                   | V    |
| Voltage applied to input pins      | INAP, INBP, INAM, INBM             | -0.3 | min (1.9, AVDD + 0.3) | V    |
|                                    | CLKP, CLKM                         | -0.3 | AVDD + 0.3            |      |
|                                    | SYSREFP, SYSREFM                   | -0.3 | AVDD + 0.3            |      |
|                                    | SCLK, SEN, SDATA, RESET, PDN       | -0.3 | 3.9                   |      |
| Temperature                        | Operating free-air, T <sub>A</sub> | -40  | 85                    | °C   |
|                                    | Operating junction, T <sub>J</sub> |      | 125                   |      |
|                                    | Storage, T <sub>stg</sub>          | -65  | 150                   |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±2000 | V    |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(2)</sup>

over operating free-air temperature range (unless otherwise noted)

|                        |   | MIN                             | NOM               | MAX                | UNIT            |
|------------------------|---|---------------------------------|-------------------|--------------------|-----------------|
| <b>SUPPLIES</b>        |   |                                 |                   |                    |                 |
| AVDD                   | Analog supply voltage range                                   | 1.7                             | 1.8               | 1.9                | V               |
| DVDD                   | Digital supply voltage range                                  | 1.7                             | 1.8               | 1.9                | V               |
| <b>ANALOG INPUT</b>    |   |                                 |                   |                    |                 |
| V <sub>ID</sub>        | Differential input voltage                                    | For input frequencies < 450 MHz |                   | 2                  | V <sub>PP</sub> |
|                        |   | For input frequencies < 600 MHz |                   | 1                  |                 |
| V <sub>IC</sub>        | Input common-mode voltage                                     | VCM ± 0.025                     |                   |                    | V               |
| <b>CLOCK INPUT</b>     |   |                                 |                   |                    |                 |
|                        | Input clock frequency   | Sampling clock frequency        | 15 <sup>(3)</sup> | 125 <sup>(1)</sup> | MSPS            |
|                        | Input clock amplitude (differential)                          | Sine wave, ac-coupled           | 0.2               | 1.5                | V <sub>PP</sub> |
|                        |   | LVPECL, ac-coupled              |                   | 1.6                |                 |
|                        |   | LVDS, ac-coupled                |                   | 0.7                |                 |
|                        | Input clock duty cycle  |                                 | 35%               | 50%                | 65%             |
|                        | Input clock common-mode voltage                               |                                 | 0.95              |                    | V               |
| <b>DIGITAL OUTPUTS</b> |   |                                 |                   |                    |                 |
| C <sub>LOAD</sub>      | Maximum external load capacitance from each output pin to GND |                                 | 3.3               |                    | pF              |
| R <sub>LOAD</sub>      | Differential load resistance placed externally                |                                 | 100               |                    | Ω               |

- (1) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.  
 (2) To reset the device for the first time after power-up, only use the RESET pin; see the [Section 8.5.1.1](#) section.  
 (3) See [Table 8-1](#) for details.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ADC322x    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RGZ (VQFN) |      |
|                               |  | 48 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 25.7       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 18.9       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 3.0        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 3          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 0.5        | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics: General

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                           | TEST CONDITIONS                               | MIN  | TYP    | MAX | UNIT            |
|-------------------------------------|---|--|--------|-----|-----------------|
| <b>RESOLUTION</b>                   |   |  |        |     |                 |
| Resolution                          |   | 12   |        |     | Bits            |
| <b>ANALOG INPUT</b>                 |   |  |        |     |                 |
| Differential input full-scale       |   |  | 2.0    |     | V <sub>PP</sub> |
| R <sub>IN</sub>                     | Input resistance                              | Differential at dc   | 6.6    |     | kΩ              |
| C <sub>IN</sub>                     | Input capacitance                             | Differential at dc   | 3.7    |     | pF              |
| V <sub>OC(VCM)</sub>                | VCM common-mode voltage output                | 0.8  | 0.95   | 1.1 | V               |
|                                     | VCM output current capability                 |  | 10     |     | mA              |
|                                     | Input common-mode current                     | Per analog input pin   | 1.5    |     | μA/MSPS         |
|                                     | Analog input bandwidth (3 dB)                 | 50-Ω differential source driving 50-Ω termination across INP and INM | 540    |     | MHz             |
| <b>DC ACCURACY</b>                  |   |  |        |     |                 |
| E <sub>O</sub>                      | Offset error                                  | –25  |        | 25  | mV              |
| α <sub>EO</sub>                     | Temperature coefficient of offset error       |  | ±0.024 |     | mV/°C           |
| E <sub>G(REF)</sub>                 | E_G Overall dc gain error of a channel        | –2%  |        | 2%  |                 |
| α <sub>(EGCHAN)</sub>               | Temperature coefficient of overall gain error |  | ±0.008 |     | Δ%FS/°C         |
| <b>CHANNEL-TO-CHANNEL ISOLATION</b> |   |  |        |     |                 |
| Crosstalk <sup>(1)</sup>            | f <sub>IN</sub> = 10 MHz                      |  | 105    |     | dB              |
|                                     | f <sub>IN</sub> = 100 MHz                     |  | 105    |     |                 |
|                                     | f <sub>IN</sub> = 200 MHz                     |  | 105    |     |                 |
|                                     | f <sub>IN</sub> = 230 MHz                     |  | 105    |     |                 |
|                                     | f <sub>IN</sub> = 300 MHz                     |  | 105    |     |                 |

(1) Crosstalk is measured with a –1-dBFS input signal on one channel and no input on the other channel.

## 6.6 Electrical Characteristics: ADC3221, ADC3222

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                      | ADC3221 |     |     | ADC3222 |     |     | UNIT |
|--------------------------------|---------|-----|-----|---------|-----|-----|------|
|                                | MIN     | TYP | MAX | MIN     | TYP | MAX |      |
| ADC clock frequency            |         |     | 25  |         |     | 50  | MSPS |
| 1.8-V analog supply current    |         | 31  | 71  |         | 39  | 81  | mA   |
| 1.8-V digital supply current   |         | 35  | 65  |         | 43  | 75  | mA   |
| Total power dissipation        |         | 118 | 205 |         | 147 | 245 | mW   |
| Global power-down dissipation  |         | 5   | 17  |         | 5   | 17  | mW   |
| Standby power-down dissipation |         | 78  | 103 |         | 78  | 103 | mW   |

## 6.7 Electrical Characteristics: ADC3223, ADC3224

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                      | ADC3223 |     |     | ADC3224 |     |     | UNIT |
|--------------------------------|---------|-----|-----|---------|-----|-----|------|
|                                | MIN     | TYP | MAX | MIN     | TYP | MAX |      |
| ADC clock frequency            |         |     | 80  |         |     | 125 | MSPS |
| 1.8-V analog supply current    |         | 50  | 91  |         | 65  | 106 | mA   |
| 1.8-V digital supply current   |         | 52  | 85  |         | 64  | 95  | mA   |
| Total power dissipation        |         | 183 | 285 |         | 233 | 325 | mW   |
| Global power-down dissipation  |         | 5   | 17  |         | 5   | 17  | mW   |
| Standby power-down dissipation |         | 72  | 103 |         | 78  | 103 | mW   |

## 6.8 AC Performance: ADC3221

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                         |  | TEST CONDITIONS           | ADC3221 (f <sub>S</sub> = 25 MSPS) |        |     |            |     |     | UNIT    |
|-----------------------------------|--|---------------------------|------------------------------------|--------|-----|------------|-----|-----|---------|
|                                   |  |                           | DITHER ON                          |        |     | DITHER OFF |     |     |         |
|                                   |  |                           | MIN                                | TYP    | MAX | MIN        | TYP | MAX |         |
| <b>DYNAMIC AC CHARACTERISTICS</b> |  |                           |                                    |        |     |            |     |     |         |
| SNR                               | Signal-to-noise ratio<br>(from 1-MHz offset)             | f <sub>IN</sub> = 10 MHz  | 70.9                               |        |     | 71.2       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 68.5                               | 70.8   |     | 71.1       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.6                               |        |     | 70.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.3                               |        |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.7                               |        |     | 69.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 68.8                               |        |     | 69         |     |     |         |
|                                   | Signal-to-noise ratio<br>(full Nyquist band)             | f <sub>IN</sub> = 10 MHz  | 70.2                               |        |     | 70.6       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 70.2                               |        |     | 70.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 69.9                               |        |     | 70.2       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 69.6                               |        |     | 69.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.2                               |        |     | 69.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 68.2                               |        |     | 68.4       |     |     |         |
| NSD <sup>(1)</sup>                | Noise spectral density<br>(averaged across Nyquist zone) | f <sub>IN</sub> = 10 MHz  | –141.9                             |        |     | –142.2     |     |     | dBFS/Hz |
|                                   |  | f <sub>IN</sub> = 20 MHz  | –141.8                             | –139.5 |     | –142.1     |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | –141.6                             |        |     | –141.9     |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | –141.3                             |        |     | –141.6     |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | –140.7                             |        |     | –140.9     |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | –139.8                             |        |     | –140.0     |     |     |         |
| SINAD <sup>(1)</sup>              | Signal-to-noise and distortion ratio                     | f <sub>IN</sub> = 10 MHz  | 70.9                               |        |     | 71.1       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 68.1                               | 70.8   |     | 71         |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.6                               |        |     | 70.7       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.2                               |        |     | 70.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.6                               |        |     | 69.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 68.5                               |        |     | 68.5       |     |     |         |
| ENOB <sup>(1)</sup>               | Effective number of bits                                 | f <sub>IN</sub> = 10 MHz  | 11.5                               |        |     | 11.5       |     |     | Bits    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 11                                 | 11.5   |     | 11.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 11.4                               |        |     | 11.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 11.4                               |        |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 11.3                               |        |     | 11.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 11.1                               |        |     | 11.1       |     |     |         |
| SFDR                              | Spurious-free dynamic range                              | f <sub>IN</sub> = 10 MHz  | 96                                 |        |     | 88         |     |     | dBc     |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 82                                 | 93     |     | 89         |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 93                                 |        |     | 87         |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 85                                 |        |     | 82         |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 86                                 |        |     | 83         |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 81                                 |        |     | 80         |     |     |         |

## 6.8 AC Performance: ADC3221 (continued)

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER  | TEST CONDITIONS   | ADC3221 (f <sub>S</sub> = 25 MSPS) |     |     |            |     |      | UNIT |
|--|---|------------------------------------|-----|-----|------------|-----|------|------|
|  |   | DITHER ON                          |     |     | DITHER OFF |     |      |      |
|  |   | MIN                                | TYP | MAX | MIN        | TYP | MAX  |      |
| HD2<br>Second-order harmonic distortion                                | f <sub>IN</sub> = 10 MHz                                  |                                    | 106 |     |            | 97  | dBc  |      |
|  | f <sub>IN</sub> = 20 MHz                                  | 82                                 | 102 |     |            | 95  |      |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 101 |     |            | 95  |      |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 95  |     |            | 93  |      |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 88  |     |            | 87  |      |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 81  |     |            | 81  |      |      |
| HD3<br>Third-order harmonic distortion                                 | f <sub>IN</sub> = 10 MHz                                  |                                    | 96  |     |            | 88  | dBc  |      |
|  | f <sub>IN</sub> = 20 MHz                                  | 82                                 | 93  |     |            | 92  |      |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 93  |     |            | 87  |      |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 85  |     |            | 82  |      |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 87  |     |            | 83  |      |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 82  |     |            | 80  |      |      |
| Non<br>HD2, HD3<br>Spurious-free dynamic range<br>(excluding HD2, HD3) | f <sub>IN</sub> = 10 MHz                                  |                                    | 99  |     |            | 92  | dBc  |      |
|  | f <sub>IN</sub> = 20 MHz                                  | 87                                 | 101 |     |            | 91  |      |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 99  |     |            | 93  |      |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 98  |     |            | 92  |      |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 99  |     |            | 92  |      |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 97  |     |            | 93  |      |      |
| THD<br>Total harmonic distortion                                       | f <sub>IN</sub> = 10 MHz                                  |                                    | 94  |     |            | 85  | dBc  |      |
|  | f <sub>IN</sub> = 20 MHz                                  | 80                                 | 92  |     |            | 85  |      |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 91  |     |            | 85  |      |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 86  |     |            | 82  |      |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 84  |     |            | 81  |      |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 78  |     |            | 77  |      |      |
| IMD3<br>Two-tone, third-order intermodulation<br>distortion            | f <sub>IN1</sub> = 45 MHz,<br>f <sub>IN2</sub> = 50 MHz   |                                    | –95 |     |            | –94 | dBFS |      |
|  | f <sub>IN1</sub> = 185 MHz,<br>f <sub>IN2</sub> = 190 MHz |                                    | –90 |     |            | –89 |      |      |

(1) Reported from a 1-MHz offset.

## 6.9 AC Performance: ADC3222

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                         |  | TEST CONDITIONS           | ADC3222 (f <sub>S</sub> = 50 MSPS) |        |     |            |     |     | UNIT    |
|-----------------------------------|--|---------------------------|------------------------------------|--------|-----|------------|-----|-----|---------|
|                                   |  |                           | DITHER ON                          |        |     | DITHER OFF |     |     |         |
|                                   |  |                           | MIN                                | TYP    | MAX | MIN        | TYP | MAX |         |
| <b>DYNAMIC AC CHARACTERISTICS</b> |  |                           |                                    |        |     |            |     |     |         |
| SNR                               | Signal-to-noise ratio<br>(from 1-MHz offset)             | f <sub>IN</sub> = 10 MHz  | 70.9                               |        |     | 71.1       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 68.5                               | 70.9   |     | 71.1       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.7                               |        |     | 70.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.5                               |        |     | 70.7       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 70                                 |        |     | 70.1       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.3                               |        |     | 69.6       |     |     |         |
|                                   | Signal-to-noise ratio<br>(full Nyquist band)             | f <sub>IN</sub> = 10 MHz  | 70.3                               |        |     | 70.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 70.1                               |        |     | 70.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.1                               |        |     | 70.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 69.9                               |        |     | 70.2       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.5                               |        |     | 69.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 68.7                               |        |     | 69         |     |     |         |
| NSD <sup>(1)</sup>                | Noise spectral density<br>(averaged across Nyquist zone) | f <sub>IN</sub> = 10 MHz  | –144.9                             |        |     | –145.1     |     |     | dBFS/Hz |
|                                   |  | f <sub>IN</sub> = 20 MHz  | –144.9                             | –142.5 |     | –145.1     |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | –144.7                             |        |     | –144.9     |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | –144.5                             |        |     | –144.7     |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | –144.0                             |        |     | –144.1     |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | –143.3                             |        |     | –143.6     |     |     |         |
| SINAD <sup>(1)</sup>              | Signal-to-noise and distortion ratio                     | f <sub>IN</sub> = 10 MHz  | 70.8                               |        |     | 71         |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 68                                 | 70.8   |     | 71         |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.6                               |        |     | 70.8       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.4                               |        |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.8                               |        |     | 69.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69                                 |        |     | 69.1       |     |     |         |
| ENOB <sup>(1)</sup>               | Effective number of bits                                 | f <sub>IN</sub> = 10 MHz  | 11.5                               |        |     | 11.5       |     |     | Bits    |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 11                                 | 11.5   |     | 11.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 11.4                               |        |     | 11.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 11.4                               |        |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 11.3                               |        |     | 11.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 11.2                               |        |     | 11.2       |     |     |         |
| SFDR                              | Spurious-free dynamic range                              | f <sub>IN</sub> = 10 MHz  | 89                                 |        |     | 95         |     |     | dBc     |
|                                   |  | f <sub>IN</sub> = 20 MHz  | 82                                 | 95     |     | 91         |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 95                                 |        |     | 93         |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 88                                 |        |     | 86         |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 85                                 |        |     | 83         |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 82                                 |        |     | 81         |     |     |         |

## 6.9 AC Performance: ADC3222 (continued)

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER  | TEST CONDITIONS   | ADC3222 (f <sub>S</sub> = 50 MSPS) |     |     |            |     |     | UNIT |
|--|---|------------------------------------|-----|-----|------------|-----|-----|------|
|  |   | DITHER ON                          |     |     | DITHER OFF |     |     |      |
|  |   | MIN                                | TYP | MAX | MIN        | TYP | MAX |      |
| HD2<br>Second-order harmonic distortion                                | f <sub>IN</sub> = 10 MHz                                  |                                    | 103 |     |            | 97  |     | dBc  |
|  | f <sub>IN</sub> = 20 MHz                                  | 82                                 | 100 |     |            | 94  |     |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 97  |     |            | 94  |     |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 94  |     |            | 93  |     |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 89  |     |            | 89  |     |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 83  |     |            | 83  |     |      |
| HD3<br>Third-order harmonic distortion                                 | f <sub>IN</sub> = 10 MHz                                  |                                    | 89  |     |            | 96  |     | dBc  |
|  | f <sub>IN</sub> = 20 MHz                                  | 82                                 | 94  |     |            | 95  |     |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 95  |     |            | 93  |     |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 88  |     |            | 86  |     |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 85  |     |            | 83  |     |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 83  |     |            | 81  |     |      |
| Non<br>HD2, HD3<br>Spurious-free dynamic range<br>(excluding HD2, HD3) | f <sub>IN</sub> = 10 MHz                                  |                                    | 99  |     |            | 95  |     | dBc  |
|  | f <sub>IN</sub> = 20 MHz                                  | 87                                 | 101 |     |            | 93  |     |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 99  |     |            | 94  |     |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 100 |     |            | 94  |     |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 99  |     |            | 93  |     |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 97  |     |            | 93  |     |      |
| THD<br>Total harmonic distortion                                       | f <sub>IN</sub> = 10 MHz                                  |                                    | 89  |     |            | 89  |     | dBc  |
|  | f <sub>IN</sub> = 20 MHz                                  | 80                                 | 93  |     |            | 87  |     |      |
|  | f <sub>IN</sub> = 70 MHz                                  |                                    | 92  |     |            | 88  |     |      |
|  | f <sub>IN</sub> = 100 MHz                                 |                                    | 90  |     |            | 86  |     |      |
|  | f <sub>IN</sub> = 170 MHz                                 |                                    | 83  |     |            | 81  |     |      |
|  | f <sub>IN</sub> = 230 MHz                                 |                                    | 80  |     |            | 78  |     |      |
| IMD3<br>Two-tone, third-order intermodulation<br>distortion            | f <sub>IN1</sub> = 45 MHz,<br>f <sub>IN2</sub> = 50 MHz   |                                    | –95 |     |            | –92 |     | dBFS |
|  | f <sub>IN1</sub> = 185 MHz,<br>f <sub>IN2</sub> = 190 MHz |                                    | –92 |     |            | –92 |     |      |

(1) Reported from a 1-MHz offset.

## 6.10 AC Performance: ADC3223

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                         |  | TEST CONDITIONS           | ADC3223 (f <sub>s</sub> = 80 MSPS) |        |     |            |     |     | UNIT    |
|-----------------------------------|--|---------------------------|------------------------------------|--------|-----|------------|-----|-----|---------|
|                                   |  |                           | DITHER ON                          |        |     | DITHER OFF |     |     |         |
|                                   |  |                           | MIN                                | TYP    | MAX | MIN        | TYP | MAX |         |
| <b>DYNAMIC AC CHARACTERISTICS</b> |  |                           |                                    |        |     |            |     |     |         |
| SNR                               | Signal-to-noise ratio<br>(from 1-MHz offset)             | f <sub>IN</sub> = 10 MHz  | 70.7                               |        |     | 70.9       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 68.5                               | 70.6   |     | 70.8       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.5                               |        |     | 70.7       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 70.1                               |        |     | 70.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.7                               |        |     | 69.9       |     |     |         |
|                                   | Signal-to-noise ratio<br>(full Nyquist band)             | f <sub>IN</sub> = 10 MHz  | 70.3                               |        |     | 70.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.2                               |        |     | 70.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.1                               |        |     | 70.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.7                               |        |     | 69.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.4                               |        |     | 69.6       |     |     |         |
| NSD <sup>(1)</sup>                | Noise spectral density<br>(averaged across Nyquist zone) | f <sub>IN</sub> = 10 MHz  | –146.7                             |        |     | –146.9     |     |     | dBFS/Hz |
|                                   |  | f <sub>IN</sub> = 70 MHz  | –146.6                             | –144.5 |     | –146.8     |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | –146.5                             |        |     | –146.7     |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | –146.1                             |        |     | –146.3     |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | –145.7                             |        |     | –145.9     |     |     |         |
| SINAD <sup>(1)</sup>              | Signal-to-noise and distortion ratio                     | f <sub>IN</sub> = 10 MHz  | 70.7                               |        |     | 70.9       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 68.1                               | 70.6   |     | 70.8       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.5                               |        |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 70                                 |        |     | 70.2       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.5                               |        |     | 69.6       |     |     |         |
| ENOB <sup>(1)</sup>               | Effective number of bits                                 | f <sub>IN</sub> = 10 MHz  | 11.4                               |        |     | 11.5       |     |     | Bits    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 11.02                              | 11.4   |     | 11.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 11.4                               |        |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 11.3                               |        |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 11.3                               |        |     | 11.3       |     |     |         |
| SFDR                              | Spurious-free dynamic range                              | f <sub>IN</sub> = 10 MHz  | 88                                 |        |     | 95         |     |     | dBc     |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 82                                 | 94     |     | 93         |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 93                                 |        |     | 92         |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 88                                 |        |     | 87         |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 85                                 |        |     | 84         |     |     |         |

## 6.10 AC Performance: ADC3223 (continued)

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER       | TEST CONDITIONS                                     | ADC3223 (f <sub>S</sub> = 80 MSPS)                        |      |     |            |     |      | UNIT |
|-----------------|---|---|------|-----|------------|-----|------|------|
|                 |   | DITHER ON   |      |     | DITHER OFF |     |      |      |
|                 |   | MIN   | TYP  | MAX | MIN        | TYP | MAX  |      |
| HD2             | Second-order harmonic distortion                    | f <sub>IN</sub> = 10 MHz                                  |      | 104 |            |     | 99   | dBc  |
|                 |   | f <sub>IN</sub> = 70 MHz                                  | 82   | 95  |            | 94  |      |      |
|                 |   | f <sub>IN</sub> = 100 MHz                                 |      | 95  |            | 93  |      |      |
|                 |   | f <sub>IN</sub> = 170 MHz                                 |      | 88  |            | 87  |      |      |
|                 |   | f <sub>IN</sub> = 230 MHz                                 |      | 85  |            | 85  |      |      |
| HD3             | Third-order harmonic distortion                     | f <sub>IN</sub> = 10 MHz                                  |      | 89  |            | 95  | dBc  |      |
|                 |   | f <sub>IN</sub> = 70 MHz                                  | 82   | 94  |            | 94  |      |      |
|                 |   | f <sub>IN</sub> = 100 MHz                                 |      | 95  |            | 96  |      |      |
|                 |   | f <sub>IN</sub> = 170 MHz                                 |      | 93  |            | 90  |      |      |
|                 |   | f <sub>IN</sub> = 230 MHz                                 |      | 89  |            | 85  |      |      |
| Non<br>HD2, HD3 | Spurious-free dynamic range<br>(excluding HD2, HD3) | f <sub>IN</sub> = 10 MHz                                  |      | 94  |            | 93  | dBc  |      |
|                 |   | f <sub>IN</sub> = 70 MHz                                  | 87   | 100 |            | 95  |      |      |
|                 |   | f <sub>IN</sub> = 100 MHz                                 |      | 99  |            | 96  |      |      |
|                 |   | f <sub>IN</sub> = 170 MHz                                 |      | 99  |            | 95  |      |      |
|                 |   | f <sub>IN</sub> = 230 MHz                                 |      | 98  |            | 95  |      |      |
| THD             | Total harmonic distortion                           | f <sub>IN</sub> = 10 MHz                                  |      | 88  |            | 91  | dBc  |      |
|                 |   | f <sub>IN</sub> = 70 MHz                                  | 79.5 | 91  |            | 89  |      |      |
|                 |   | f <sub>IN</sub> = 100 MHz                                 |      | 91  |            | 88  |      |      |
|                 |   | f <sub>IN</sub> = 170 MHz                                 |      | 86  |            | 84  |      |      |
|                 |   | f <sub>IN</sub> = 230 MHz                                 |      | 83  |            | 81  |      |      |
| IMD3            | Two-tone, third-order intermodulation<br>distortion | f <sub>IN1</sub> = 45 MHz,<br>f <sub>IN2</sub> = 50 MHz   |      | –94 |            | –94 | dBFS |      |
|                 |   | f <sub>IN1</sub> = 185 MHz,<br>f <sub>IN2</sub> = 190 MHz |      | –92 |            | –90 |      |      |

(1) Reported from a 1-MHz offset.

## 6.11 AC Performance: ADC3224

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER                         |  | TEST CONDITIONS           | ADC3224 (f <sub>s</sub> = 125 MSPS) |        |     |            |     |     | UNIT    |
|-----------------------------------|--|---------------------------|-------------------------------------|--------|-----|------------|-----|-----|---------|
|                                   |  |                           | DITHER ON                           |        |     | DITHER OFF |     |     |         |
|                                   |  |                           | MIN                                 | TYP    | MAX | MIN        | TYP | MAX |         |
| <b>DYNAMIC AC CHARACTERISTICS</b> |  |                           |                                     |        |     |            |     |     |         |
| SNR                               | Signal-to-noise ratio<br>(from 1-MHz offset)             | f <sub>IN</sub> = 10 MHz  | 70.5                                |        |     | 70.8       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 68.5                                | 70.4   |     | 70.7       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.3                                |        |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.9                                |        |     | 70.2       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.4                                |        |     | 69.8       |     |     |         |
|                                   | Signal-to-noise ratio<br>(full Nyquist band)             | f <sub>IN</sub> = 10 MHz  | 70.3                                |        |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 70.2                                |        |     | 70.5       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.2                                |        |     | 70.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.7                                |        |     | 70.0       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.2                                |        |     | 69.6       |     |     |         |
| NSD <sup>(1)</sup>                | Noise spectral density<br>(averaged across Nyquist zone) | f <sub>IN</sub> = 10 MHz  | –148.5                              |        |     | –148.8     |     |     | dBFS/Hz |
|                                   |  | f <sub>IN</sub> = 70 MHz  | –148.4                              | –146.5 |     | –148.7     |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | –148.3                              |        |     | –148.6     |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | –147.9                              |        |     | –148.2     |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | –147.4                              |        |     | –147.8     |     |     |         |
| SINAD <sup>(1)</sup>              | Signal-to-noise and distortion ratio                     | f <sub>IN</sub> = 10 MHz  | 70.5                                |        |     | 70.6       |     |     | dBFS    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 68                                  | 70.4   |     | 70.6       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 70.2                                |        |     | 70.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 69.7                                |        |     | 69.9       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 69.2                                |        |     | 69.5       |     |     |         |
| ENOB <sup>(1)</sup>               | Effective number of bits                                 | f <sub>IN</sub> = 10 MHz  | 11.4                                |        |     | 11.4       |     |     | Bits    |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 11                                  | 11.4   |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 11.4                                |        |     | 11.4       |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 11.3                                |        |     | 11.3       |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 11.2                                |        |     | 11.2       |     |     |         |
| SFDR                              | Spurious-free dynamic range                              | f <sub>IN</sub> = 10 MHz  | 93                                  |        |     | 87         |     |     | dBc     |
|                                   |  | f <sub>IN</sub> = 70 MHz  | 82                                  | 95     |     | 89         |     |     |         |
|                                   |  | f <sub>IN</sub> = 100 MHz | 89                                  |        |     | 86         |     |     |         |
|                                   |  | f <sub>IN</sub> = 170 MHz | 86                                  |        |     | 85         |     |     |         |
|                                   |  | f <sub>IN</sub> = 230 MHz | 83                                  |        |     | 83         |     |     |         |

### 6.11 AC Performance: ADC3224 (continued)

At maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input. Typical values are specified at an ambient temperature of 25°C. Minimum and maximum values are specified over an ambient temperature range of –40°C to +85°C (unless otherwise noted).

| PARAMETER    | TEST CONDITIONS                                  | ADC3224 (f <sub>S</sub> = 125 MSPS)                    |     |     |            |     |     | UNIT |
|--------------|--|--|-----|-----|------------|-----|-----|------|
|              |  | DITHER ON  |     |     | DITHER OFF |     |     |      |
|              |  | MIN  | TYP | MAX | MIN        | TYP | MAX |      |
| HD2          | Second-order harmonic distortion                 | f <sub>IN</sub> = 10 MHz                               |     |     | 96         |     |     | dBc  |
|              |  | f <sub>IN</sub> = 70 MHz                               |     |     | 84 96      |     |     |      |
|              |  | f <sub>IN</sub> = 100 MHz                              |     |     | 91         |     |     |      |
|              |  | f <sub>IN</sub> = 170 MHz                              |     |     | 86         |     |     |      |
|              |  | f <sub>IN</sub> = 230 MHz                              |     |     | 83         |     |     |      |
| HD3          | Third-order harmonic distortion                  | f <sub>IN</sub> = 10 MHz                               |     |     | 94         |     |     | dBc  |
|              |  | f <sub>IN</sub> = 70 MHz                               |     |     | 82 95      |     |     |      |
|              |  | f <sub>IN</sub> = 100 MHz                              |     |     | 91         |     |     |      |
|              |  | f <sub>IN</sub> = 170 MHz                              |     |     | 96         |     |     |      |
|              |  | f <sub>IN</sub> = 230 MHz                              |     |     | 88         |     |     |      |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | f <sub>IN</sub> = 10 MHz                               |     |     | 99         |     |     | dBc  |
|              |  | f <sub>IN</sub> = 70 MHz                               |     |     | 87 99      |     |     |      |
|              |  | f <sub>IN</sub> = 100 MHz                              |     |     | 99         |     |     |      |
|              |  | f <sub>IN</sub> = 170 MHz                              |     |     | 99         |     |     |      |
|              |  | f <sub>IN</sub> = 230 MHz                              |     |     | 97         |     |     |      |
| THD          | Total harmonic distortion                        | f <sub>IN</sub> = 10 MHz                               |     |     | 91         |     |     | dBc  |
|              |  | f <sub>IN</sub> = 70 MHz                               |     |     | 80 91      |     |     |      |
|              |  | f <sub>IN</sub> = 100 MHz                              |     |     | 87         |     |     |      |
|              |  | f <sub>IN</sub> = 170 MHz                              |     |     | 85         |     |     |      |
|              |  | f <sub>IN</sub> = 230 MHz                              |     |     | 82         |     |     |      |
| IMD3         | Two-tone, third-order intermodulation distortion | f <sub>IN1</sub> = 45 MHz, f <sub>IN2</sub> = 50 MHz   |     |     | –96        |     |     | dBFS |
|              |  | f <sub>IN1</sub> = 185 MHz, f <sub>IN2</sub> = 190 MHz |     |     | –92        |     |     |      |

(1) Reported from a 1-MHz offset.

## 6.12 Digital Characteristics

the dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1; AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  | MIN                       | TYP  | MAX  | UNIT |
|--|---|--|---------------------------|------|------|------|
| <b>DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN)</b> |   |  |                           |      |      |      |
| V <sub>IH</sub>                                      | High-level input voltage                      | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | 1.3                       |      |      | V    |
| V <sub>IL</sub>                                      | Low-level input voltage                       | All digital inputs support 1.8-V and 3.3-V CMOS logic levels |                           |      | 0.4  | V    |
| I <sub>IH</sub>                                      | High-level input current                      | RESET, SDATA, SCLK, PDN                                      | V <sub>HIGH</sub> = 1.8 V | 10   |      | μA   |
|  |   | SEN <sup>(1)</sup>   | V <sub>HIGH</sub> = 1.8 V | 0    |      |      |
| I <sub>IL</sub>                                      | Low-level input current                       | RESET, SDATA, SCLK, PDN                                      | V <sub>LOW</sub> = 0 V    | 0    |      | μA   |
|  |   | SEN  | V <sub>LOW</sub> = 0 V    | 10   |      |      |
| <b>DIGITAL INPUTS (SYSREFP, SYSREFM)</b>             |   |  |                           |      |      |      |
|  | Differential swing                            |  | 0.2                       | 0.8  | 1    | V    |
|  | Common-mode voltage for SYSREF <sup>(2)</sup> |  |                           | 0.9  |      | V    |
| <b>DIGITAL OUTPUTS, CMOS INTERFACE (SDOUT)</b>       |   |  |                           |      |      |      |
| V <sub>OH</sub>                                      | High-level output voltage                     |  | DVDD – 0.1                | DVDD |      | V    |
| V <sub>OL</sub>                                      | Low-level output voltage                      |  |                           | 0    | 0.1  | V    |
| <b>DIGITAL OUTPUTS, LVDS INTERFACE</b>               |   |  |                           |      |      |      |
| V <sub>ODH</sub>                                     | High-level output differential voltage        | With an external 100-Ω termination                           | 280                       | 350  | 460  | mV   |
| V <sub>ODL</sub>                                     | Low-level output differential voltage         | With an external 100-Ω termination                           | –460                      | –350 | –280 | mV   |
| V <sub>OCM</sub>                                     | Output common-mode voltage                    |  |                           | 1.05 |      | V    |

- (1) SEN has an internal 150-kΩ pull-up resistor to AVDD. SPI pins (SEN, SCLK, SDATA) can be driven by 1.8-V or 3.3-V CMOS buffers.  
(2) SYSREF is internally biased to 0.9 V.

## 6.13 Timing Requirements: General

typical values are at T<sub>A</sub> = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input (unless otherwise noted); minimum and maximum values are across the full temperature range: T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C

|                        |   |  | MIN  | TYP  | MAX  | UNIT               |
|------------------------|---|--|------|------|------|--------------------|
| t <sub>A</sub>         | Aperture delay  |  | 1.24 | 1.44 | 1.64 | ns                 |
|                        | Aperture delay matching between two channels of the same device                     |  |      | ±70  |      |                    |
|                        | Aperture delay variation between two devices at same temperature and supply voltage |  |      | ±150 |      |                    |
| t <sub>J</sub>         | Aperture jitter   |  |      | 130  |      | f <sub>S</sub> rms |
|                        | Wake-up time  | Time to valid data after exiting standby power-down mode   |      | 35   | 65   | μs                 |
|                        |   | Time to valid data after exiting global power-down mode (in this mode, both channels power down) |      | 85   | 140  |                    |
|                        | ADC latency <sup>(1)</sup>  | 2-wire mode (default)  |      | 9    |      | Clock cycles       |
|                        |   | 1-wire mode  |      | 8    |      |                    |
| t <sub>SU_SYSREF</sub> | SYSREF reference time   | Setup time for SYSREF referenced to input clock rising edge                                      | 1000 |      |      | ps                 |
| t <sub>H_SYSREF</sub>  |   | Hold time for SYSREF referenced to input clock rising edge                                       | 100  |      |      |                    |

- (1) Overall latency = ADC latency + t<sub>PDI</sub> (see Figure 7-4)

## 6.14 Timing Requirements: LVDS Output

typical values are at  $T_A = 25^\circ\text{C}$ ,  $AVDD = DVDD = 1.8\text{ V}$ , and  $-1\text{-dBFS}$  differential input, 6x serialization (2-wire mode),  $C_{LOAD} = 3.3\text{ pF}^{(2)}$ , and  $R_{LOAD} = 100\ \Omega^{(3)}$  (unless otherwise noted); minimum and maximum values are across the full temperature range:  $T_{MIN} = -40^\circ\text{C}$  to  $T_{MAX} = 85^\circ\text{C}^{(4)}$  (1)

|                                  |  | MIN         | TYP                           | MAX | UNIT |    |
|----------------------------------|--|-------------|-------------------------------|-----|------|----|
| $t_{SU}$                         | Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM) <sup>(5)</sup>   | 0.43        | 0.5                           |     | ns   |    |
| $t_{HO}$                         | Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid <sup>(5)</sup>   | 0.48        | 0.58                          |     | ns   |    |
| $t_{PDI}$                        | Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over (15 MSPS < sampling frequency < 125 MSPS)                                       | 1-wire mode | 2.7                           | 4.5 | 6.5  | ns |
|                                  |  | 2-wire mode | $0.44 \times t_S + t_{DELAY}$ |     |      |    |
| $t_{DELAY}$                      | Delay time   | 3           | 4.5                           | 5.9 | ns   |    |
|                                  | LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)  | 49%         |                               |     |      |    |
| $t_{FALL}$ ,<br>$t_{RISE}$       | Data fall time, data rise time: rise time measured from $-100\text{ mV}$ to $100\text{ mV}$ , $15\text{ MSPS} \leq \text{Sampling frequency} \leq 125\text{ MSPS}$                 | 0.11        |                               |     | ns   |    |
| $t_{CLKRISE}$ ,<br>$t_{CLKFALL}$ | Output clock rise time, output clock fall time: rise time measured from $-100\text{ mV}$ to $100\text{ mV}$ , $10\text{ MSPS} \leq \text{Sampling frequency} \leq 125\text{ MSPS}$ | 0.11        |                               |     | ns   |    |

- (1) Timing parameters are specified by design and characterization and are not tested in production.
- (2)  $C_{LOAD}$  is the effective external single-ended load capacitance between each output pin and ground.
- (3)  $R_{LOAD}$  is the differential load resistance between the LVDS output pair.
- (4) Measurements are done with a transmission line of a  $100\text{-}\Omega$  characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (5) Data valid refers to a logic high of  $100\text{ mV}$  and a logic low of  $-100\text{ mV}$ .

**Table 6-1. LVDS Timing at Lower Sampling Frequencies: 6X Serialization (2-Wire Mode)**

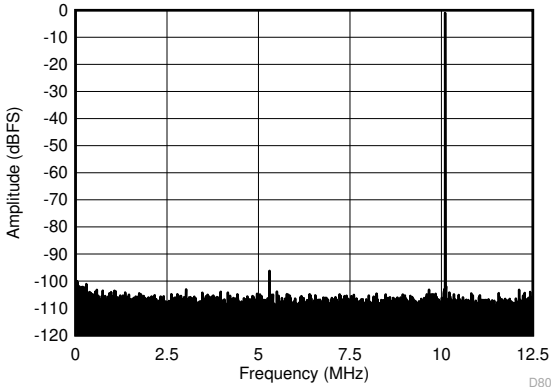
| SAMPLING FREQUENCY<br>(MSPS) | SETUP TIME<br>( $t_{SU}$ , ns) |      |     | HOLD TIME<br>( $t_{HO}$ , ns) |      |     |
|------------------------------|--------------------------------|------|-----|-------------------------------|------|-----|
|                              | MIN                            | TYP  | MAX | MIN                           | TYP  | MAX |
| 25                           | 2.61                           | 3.06 |     | 2.75                          | 3.12 |     |
| 40                           | 1.69                           | 1.9  |     | 1.8                           | 1.98 |     |
| 60                           | 1.11                           | 1.23 |     | 1.18                          | 1.31 |     |
| 80                           | 0.81                           | 0.89 |     | 0.88                          | 0.97 |     |
| 100                          | 0.6                            | 0.68 |     | 0.68                          | 0.77 |     |

**Table 6-2. LVDS Timings at Lower Sampling Frequencies: 12X Serialization (1-Wire Mode)**

| SAMPLING FREQUENCY<br>(MSPS) | SETUP TIME<br>( $t_{SU}$ , ns) |      |     | HOLD TIME<br>( $t_{HO}$ , ns) |      |     |
|------------------------------|--------------------------------|------|-----|-------------------------------|------|-----|
|                              | MIN                            | TYP  | MAX | MIN                           | TYP  | MAX |
| 25                           | 1.3                            | 1.48 |     | 1.32                          | 1.57 |     |
| 40                           | 0.76                           | 0.88 |     | 0.79                          | 0.97 |     |
| 50                           | 0.57                           | 0.68 |     | 0.61                          | 0.77 |     |
| 60                           | 0.42                           | 0.55 |     | 0.45                          | 0.62 |     |
| 70                           | 0.35                           | 0.44 |     | 0.4                           | 0.51 |     |
| 80                           | 0.26                           | 0.35 |     | 0.35                          | 0.43 |     |

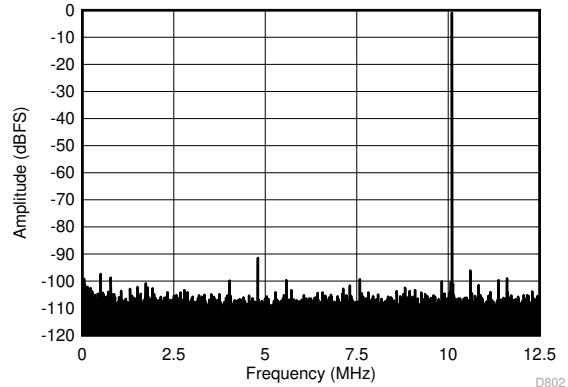
### 6.15 Typical Characteristics: ADC3221

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



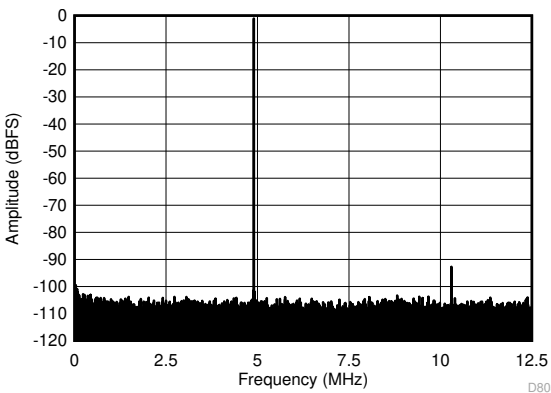
SFDR = 95.2 dBc, SNR = 71.2 dBFS, SINAD = 71.2 dBFS,  
THD = 94.1 dBc, HD2 = 106.0 dBc, HD3 = 95.2 dBc

**Figure 6-1. FFT for 10-MHz Input Signal (Dither On)**



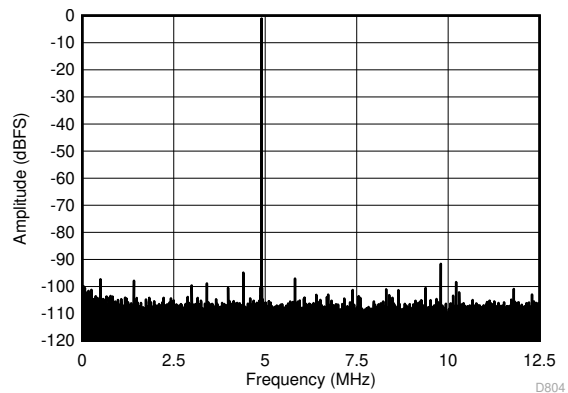
SFDR = 90.4 dBc, SNR = 71.6 dBFS, SINAD = 71.5 dBFS,  
THD = 88.6 dBc, HD2 = 90.4 dBc, HD3 = 105.5 dBc

**Figure 6-2. FFT for 10-MHz Input Signal (Dither Off)**



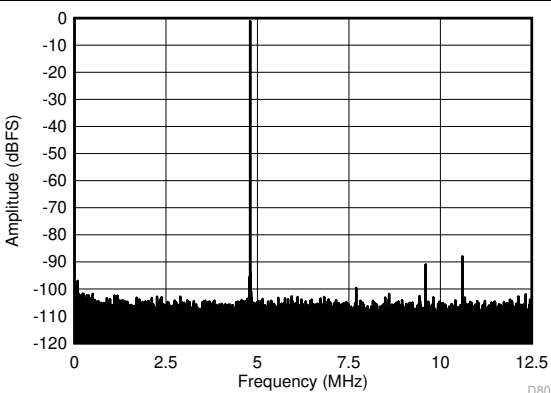
SFDR = 91.6 dBc, SNR = 71.1 dBFS, SINAD = 71.1 dBFS,  
THD = 91 dBc, HD2 = 105.3 dBc, HD3 = 91.6 dBc

**Figure 6-3. FFT for 70-MHz Input Signal (Dither On)**



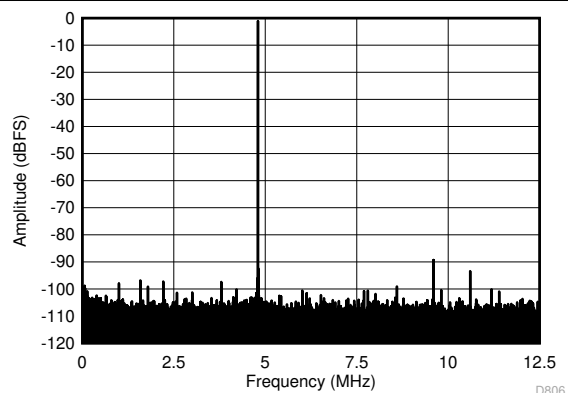
SFDR = 90.6 dBc, SNR = 71.4 dBFS, SINAD = 71.3 dBFS,  
THD = 88.4 dBc, HD2 = 90.6 dBc, HD3 = 101.1 dBc

**Figure 6-4. FFT for 70-MHz Input Signal (Dither Off)**



SFDR = 86.8 dBc, SNR = 70.2 dBFS, SINAD = 70.1 dBFS,  
THD = 84.8 dBc, HD2 = 89.9 dBc, HD3 = 86.8 dBc

**Figure 6-5. FFT for 170-MHz Input Signal (Dither On)**

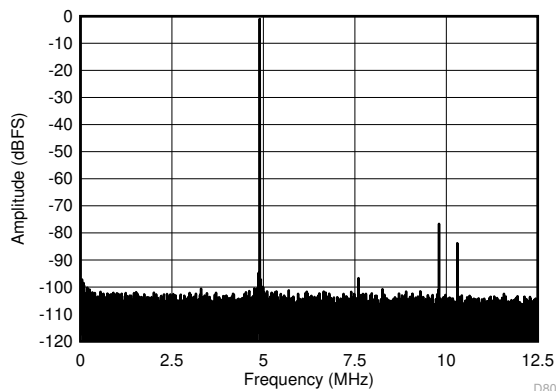


SFDR = 88.2 dBc, SNR = 70.5 dBFS, SINAD = 70.4 dBFS,  
THD = 85.7 dBc, HD2 = 88.2 dBc, HD3 = 92.3 dBc

**Figure 6-6. FFT for 170-MHz Input Signal (Dither Off)**

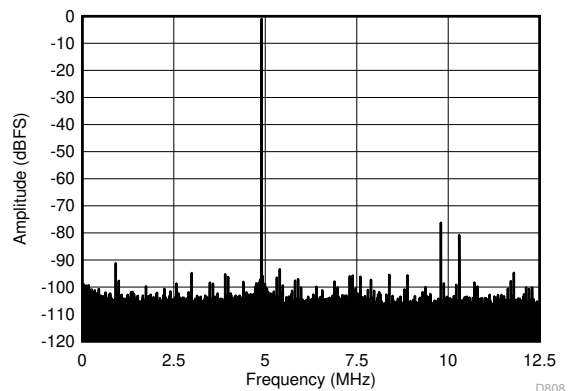
## 6.15 Typical Characteristics: ADC3221 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



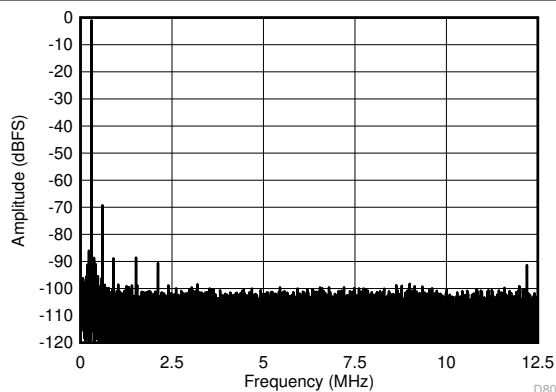
SFDR = 75.7 dBc, SNR = 68.6 dBFS, SINAD = 67.8 dBFS,  
THD = 74.9 dBc, HD2 = 75.7 dBc, HD3 = 82.8 dBc

Figure 6-7. FFT for 270-MHz Input Signal (Dither On)



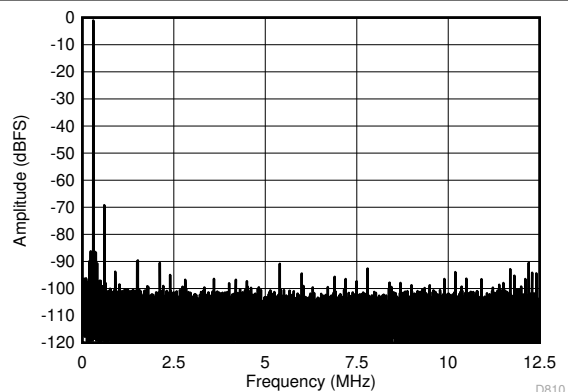
SFDR = 75.3 dBc, SNR = 68.7 dBFS, SINAD = 67.7 dBFS,  
THD = 73.8 dBc, HD2 = 75.3 dBc, HD3 = 79.8 dBc

Figure 6-8. FFT for 270-MHz Input Signal (Dither Off)



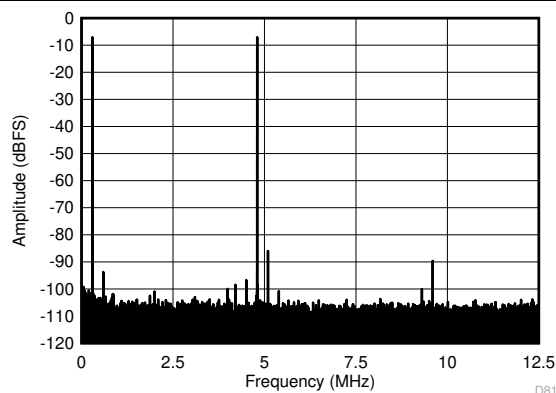
SFDR = 68.2 dBc, SNR = 66.6 dBFS, SINAD = 66.6 dBFS,  
THD = 92.7 dBc, HD2 = 68.2 dBc, HD3 = 87.8 dBc

Figure 6-9. FFT for 450-MHz Input Signal (Dither On)



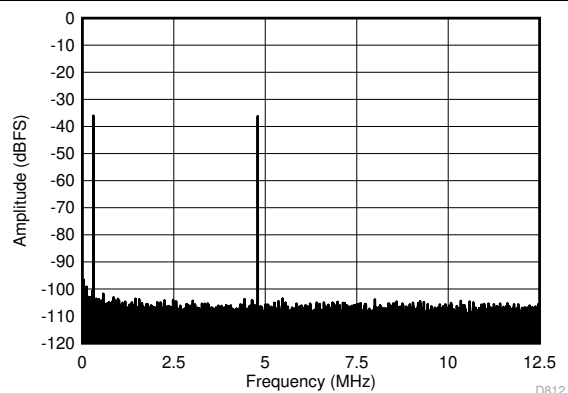
SFDR = 68.2 dBc, SNR = 66.5 dBFS, SINAD = 66.5 dBFS,  
THD = 87.1 dBc, HD2 = 68.2 dBc, HD3 = 92.7 dBc

Figure 6-10. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 84 dBFS, each tone at  $-7\text{ dBFS}$

Figure 6-11. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)

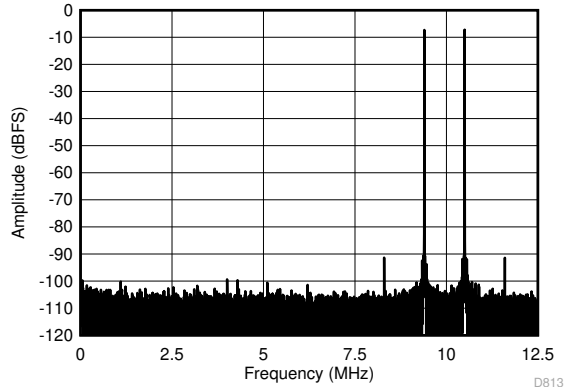


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 105 dBFS, each tone at  $-36\text{ dBFS}$

Figure 6-12. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)

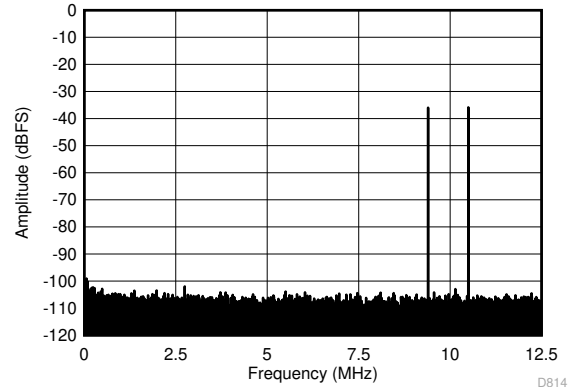
### 6.15 Typical Characteristics: ADC3221 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



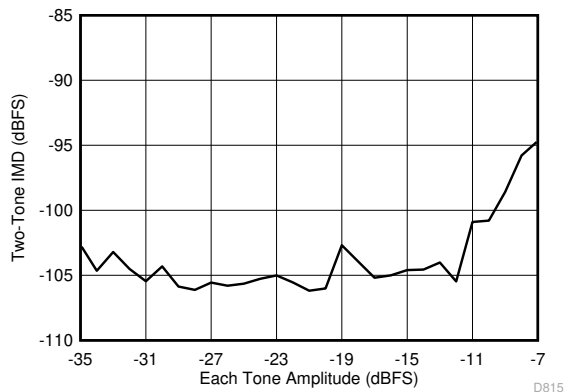
$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 91\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 6-13. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 185 MHz and 190 MHz)**

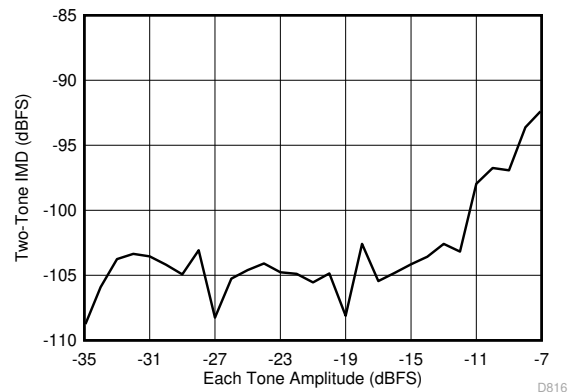


$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 105\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

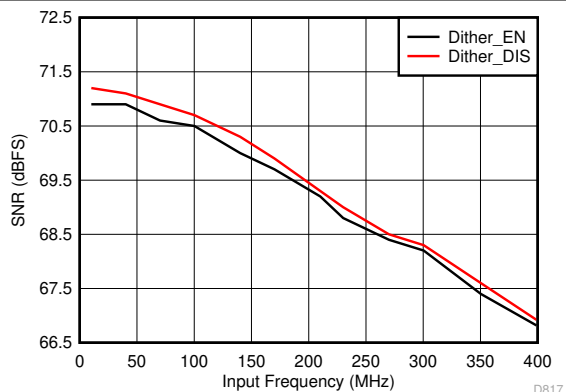
**Figure 6-14. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 185 MHz and 190 MHz)**



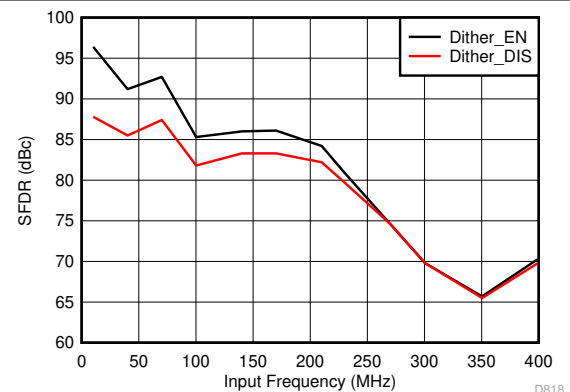
**Figure 6-15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 6-16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



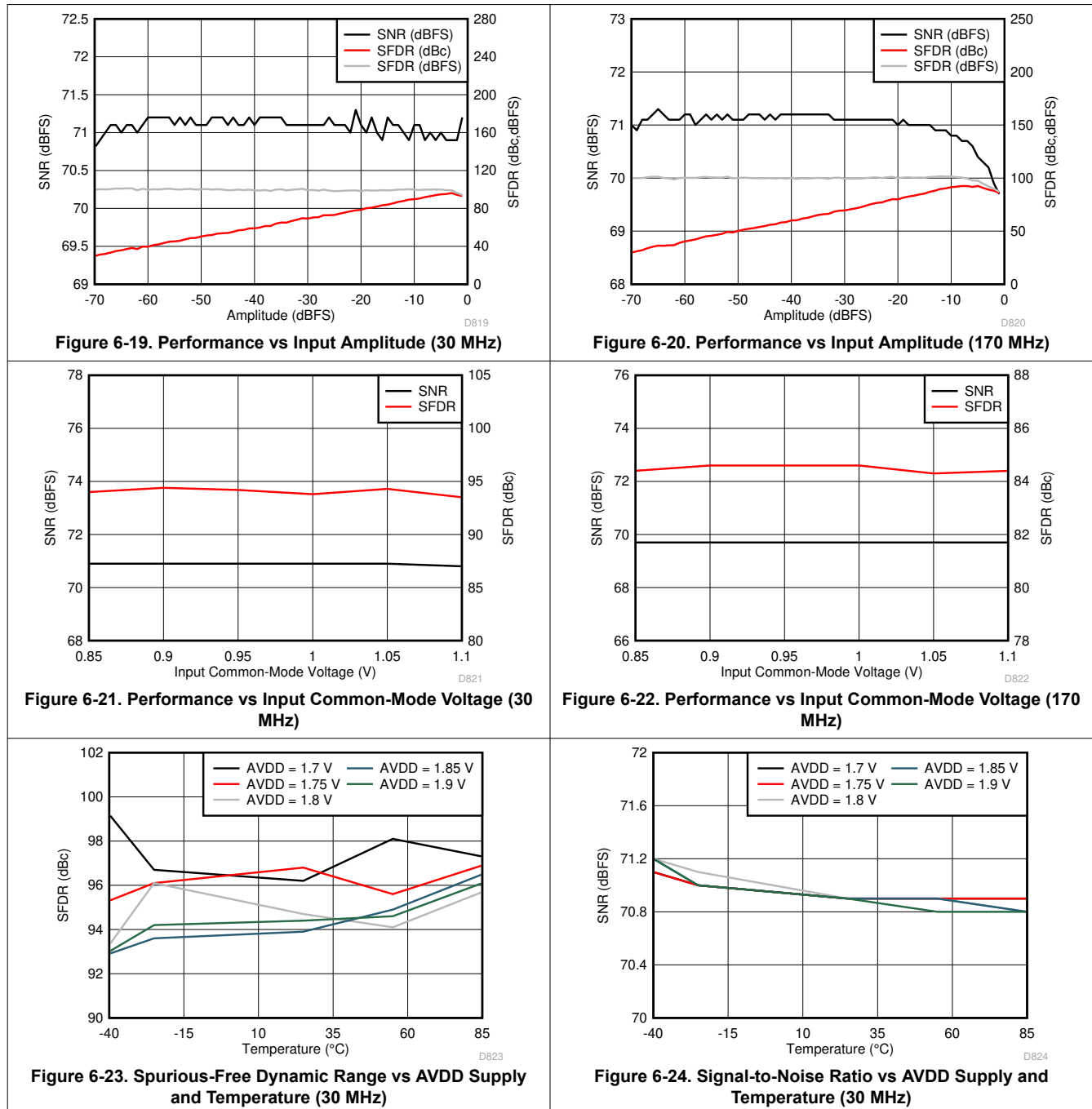
**Figure 6-17. Signal-to-Noise Ratio vs Input Frequency**



**Figure 6-18. Spurious-Free Dynamic Range vs Input Frequency**

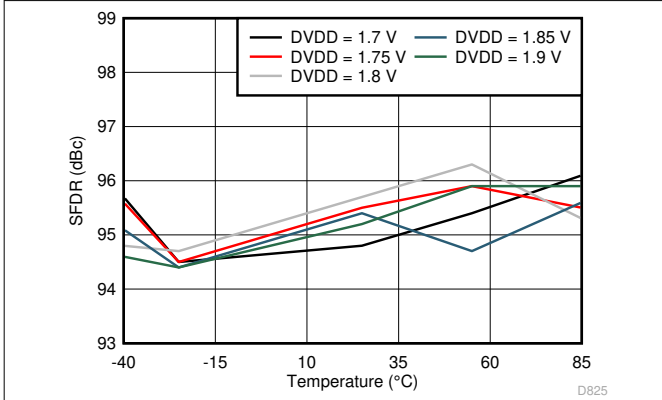
## 6.15 Typical Characteristics: ADC3221 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- $V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).

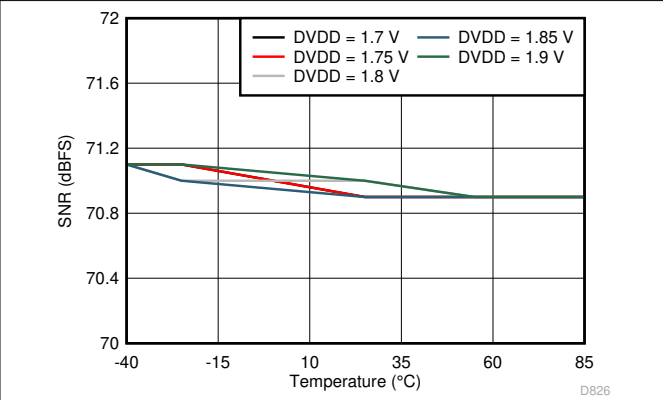


### 6.15 Typical Characteristics: ADC3221 (continued)

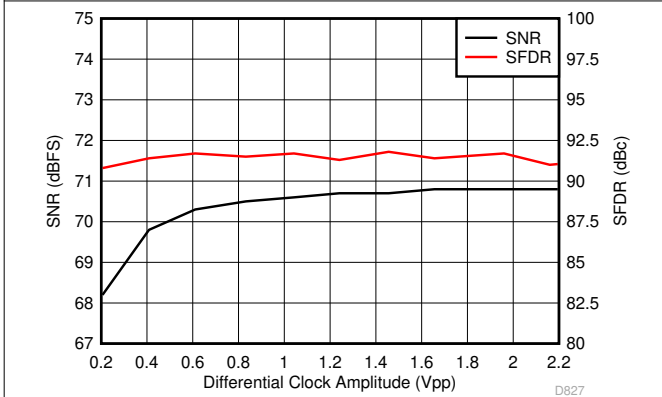
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 25 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



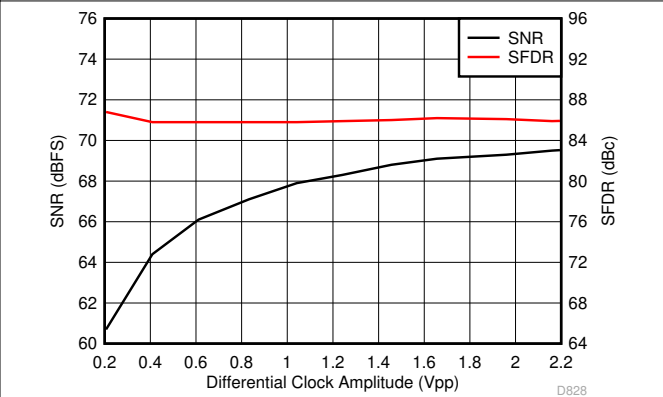
**Figure 6-25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)**



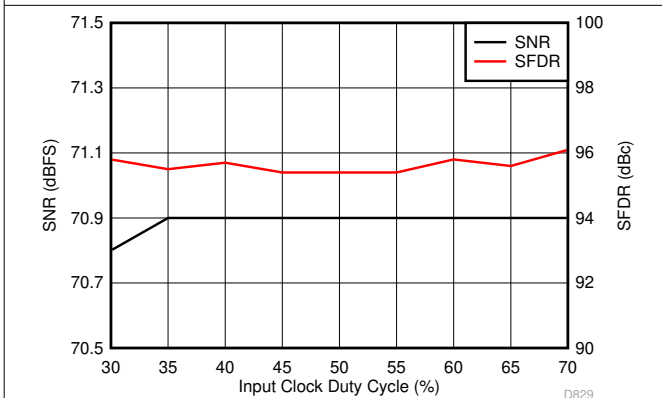
**Figure 6-26. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)**



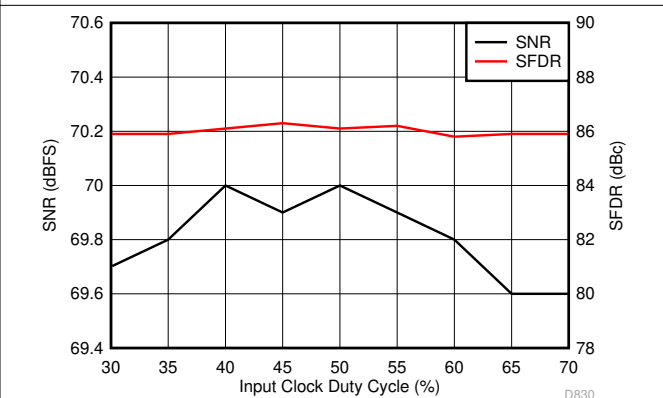
**Figure 6-27. Performance vs Differential Clock Amplitude (40 MHz)**



**Figure 6-28. Performance vs Differential Clock Amplitude (150 MHz)**



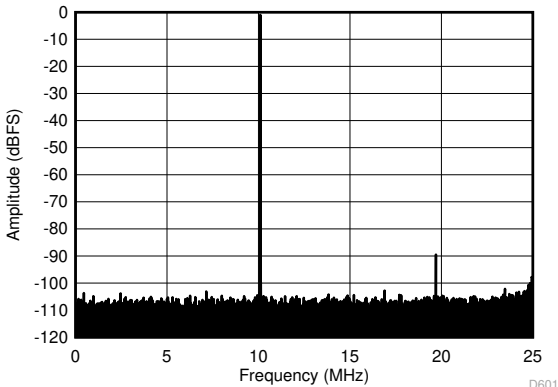
**Figure 6-29. Performance vs Clock Duty Cycle (30 MHz)**



**Figure 6-30. Performance vs Clock Duty Cycle (150 MHz)**

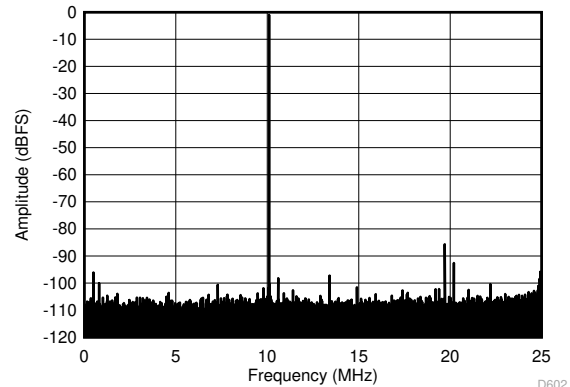
## 6.16 Typical Characteristics: ADC3222

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



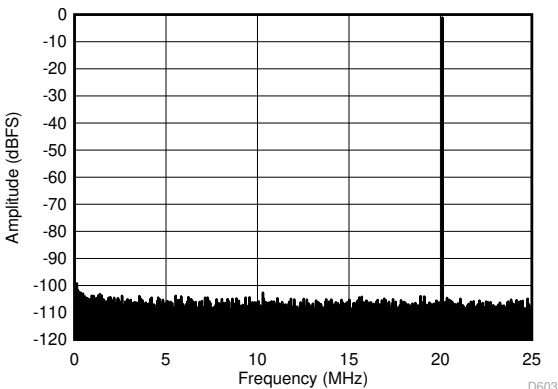
SFDR = 88.5 dBc, SFDR = 99.8 dBc (non 23), SNR = 71.1 dBFS, SINAD = 71 dBFS, THD = 88.1 dBc, HD2 = 109.9 dBc, HD3 = 88.5 dBc

Figure 6-31. FFT for 10-MHz Input Signal (Dither On)



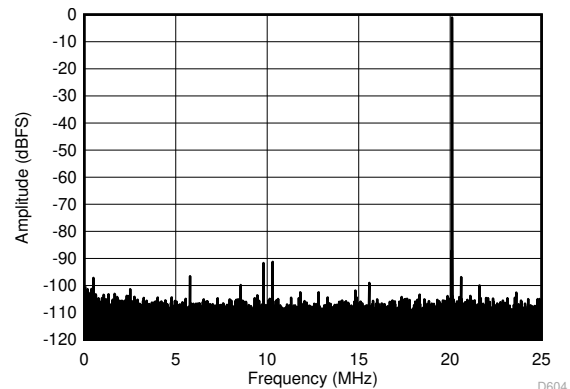
SFDR = 84.6 dBc, SFDR = 96.1 dBc (non 23), SNR = 71.4 dBFS, SINAD = 71.1 dBFS, THD = 83.2 dBc, HD2 = 91.6 dBc, HD3 = 84.6 dBc

Figure 6-32. FFT for 10-MHz Input Signal (Dither Off)



SFDR = 101.6 dBc, SFDR = 100.3 dBc (non 23), SNR = 70.9 dBFS, SINAD = 70.9 dBFS, THD = 98.1 dBc, HD2 = 106.6 dBc, HD3 = 101.6 dBc

Figure 6-33. FFT for 70-MHz Input Signal (Dither On)

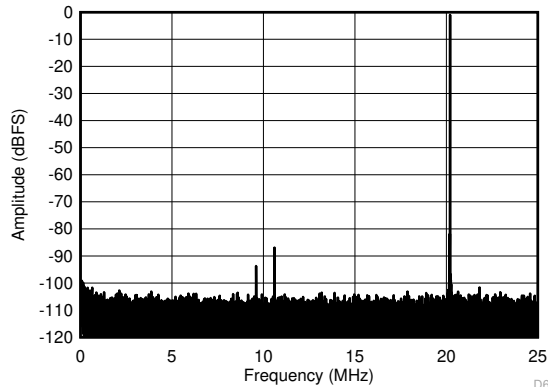


SFDR = 90.2 dBc, SFDR = 94.7 dBc (non 23), SNR = 71.2 dBFS, SINAD = 71.1 dBFS, THD = 86.7 dBc, HD2 = 90.6 dBc, HD3 = 90.2 dBc

Figure 6-34. FFT for 70-MHz Input Signal (Dither Off)

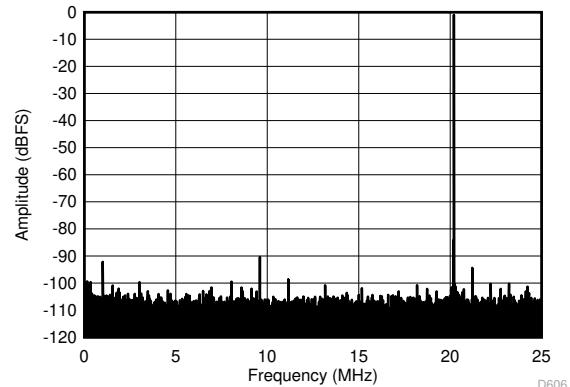
## 6.16 Typical Characteristics: ADC3222 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



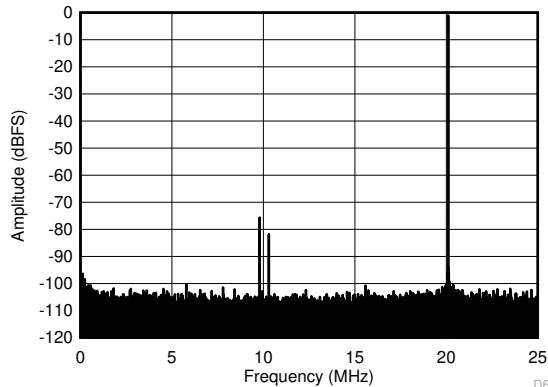
SFDR = 85.9 dBc, SFDR = 99.1 dBc (non 23), SNR = 70.4 dBFS, SINAD = 70.2 dBFS, THD = 84.8 dBc, HD2 = 92.7 dBc, HD3 = 85.9 dBc

**Figure 6-35. FFT for 170-MHz Input Signal (Dither On)**



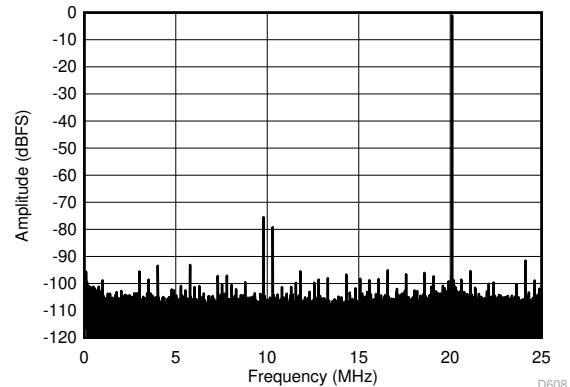
SFDR = 89.3 dBc, SFDR = 93 dBc (non 23), SNR = 70.7 dBFS, SINAD = 70.6 dBFS, THD = 85.8 dBc, HD2 = 89.3 dBc, HD3 = 111.9 dBc

**Figure 6-36. FFT for 170-MHz Input Signal (Dither Off)**



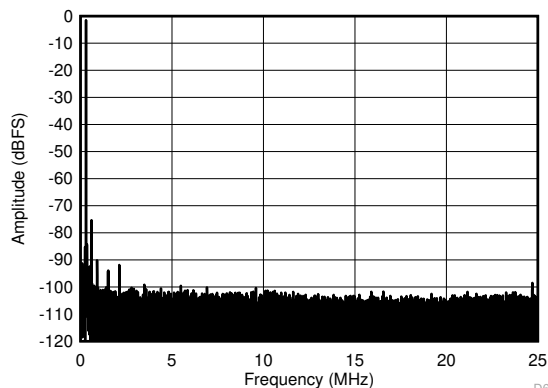
SFDR = 74.7 dBc, SFDR = 95.2 dBc (non 23), SNR = 69.2 dBFS, SINAD = 68.1 dBFS, THD = 73.7 dBc, HD2 = 74.7 dBc, HD3 = 80.9 dBc

**Figure 6-37. FFT for 270-MHz Input Signal (Dither On)**



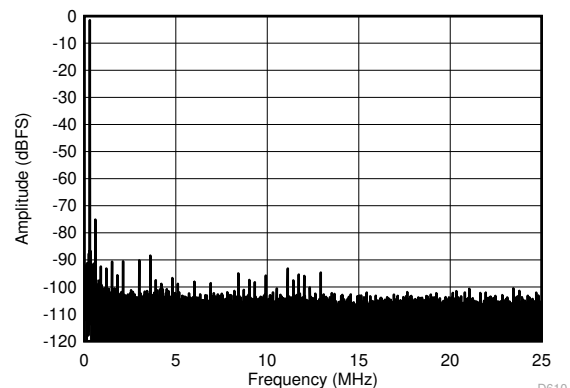
SFDR = 74.5 dBc, SFDR = 91.1 dBc (non 23), SNR = 69.4 dBFS, SINAD = 68.1 dBFS, THD = 72.9 dBc, HD2 = 74.5 dBc, HD3 = 78.2 dBc

**Figure 6-38. FFT for 270-MHz Input Signal (Dither Off)**



SFDR = 68.2 dBc, SNR = 67.4 dBFS, SINAD = 67.3 dBFS, THD = 86.4 dBc, HD2 = 68.2 dBc, HD3 = 87.3 dBc

**Figure 6-39. FFT for 450-MHz Input Signal (Dither On)**

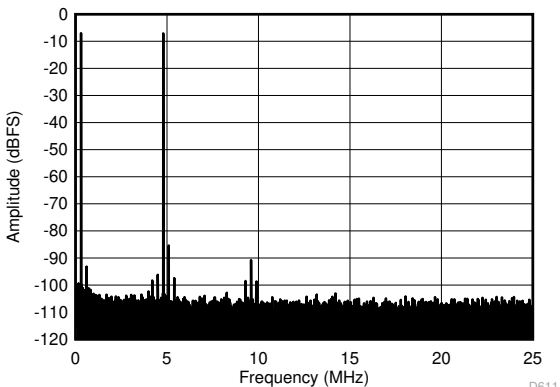


SFDR = 68.1 dBc, SNR = 67.7 dBFS, SINAD = 67.6 dBFS, THD = 86.6 dBc, HD2 = 68.1 dBc, HD3 = 87.3 dBc

**Figure 6-40. FFT for 450-MHz Input Signal (Dither Off)**

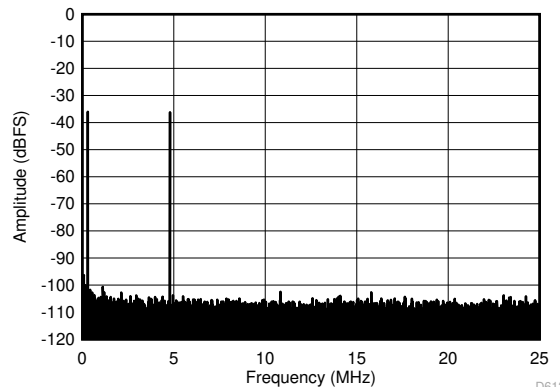
## 6.16 Typical Characteristics: ADC3222 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



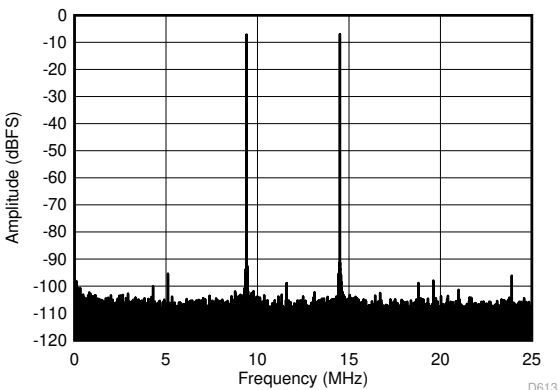
$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ ,  $\text{IMD3} = 85.4\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 6-41. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)**



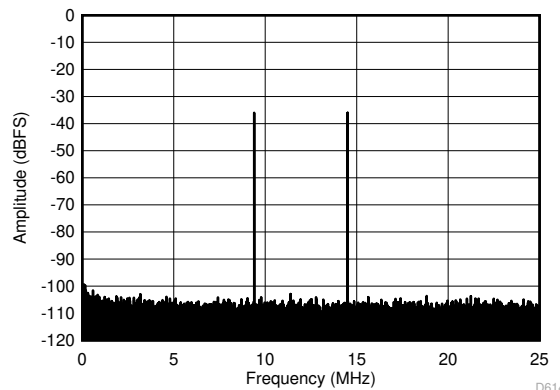
$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ ,  $\text{IMD3} = 103\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

**Figure 6-42. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)**



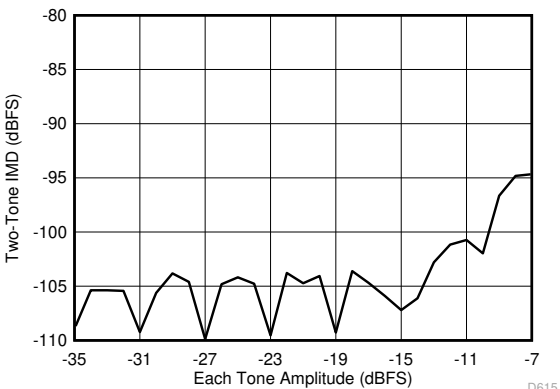
$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 95\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 6-43. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 185 MHz and 190 MHz)**

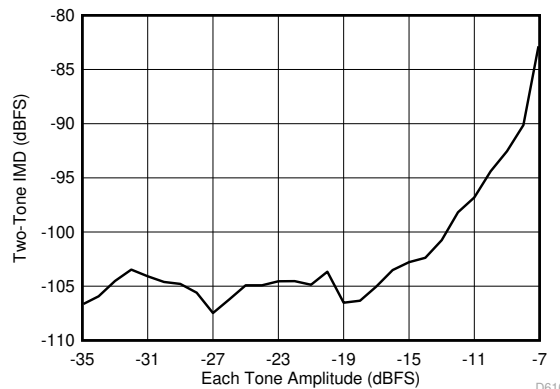


$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 105\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

**Figure 6-44. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 185 MHz and 190 MHz)**



**Figure 6-45. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 6-46. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**

## 6.16 Typical Characteristics: ADC3222 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).

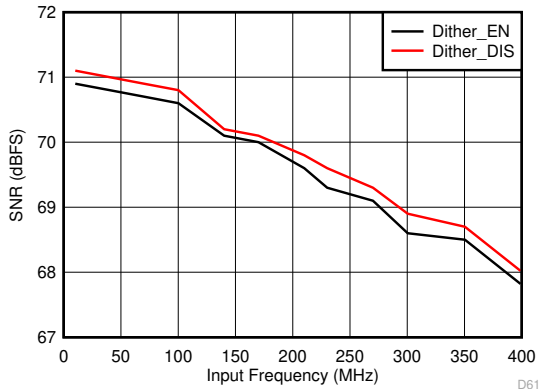


Figure 6-47. Signal-to-Noise Ratio vs Input Frequency

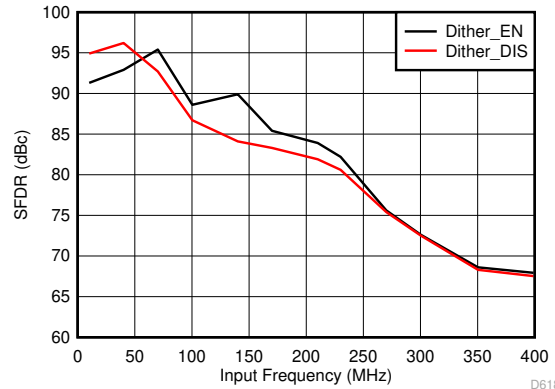


Figure 6-48. Spurious-Free Dynamic Range vs Input Frequency

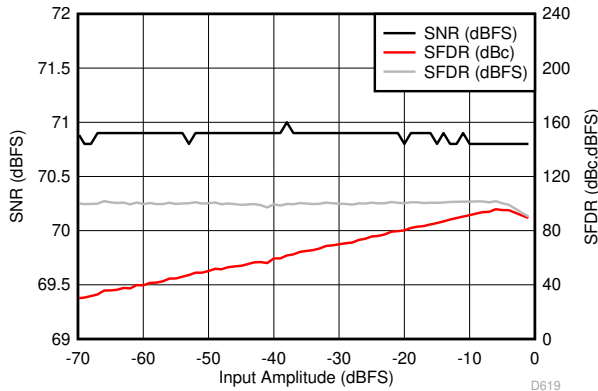


Figure 6-49. Performance vs Input Amplitude (30 MHz)

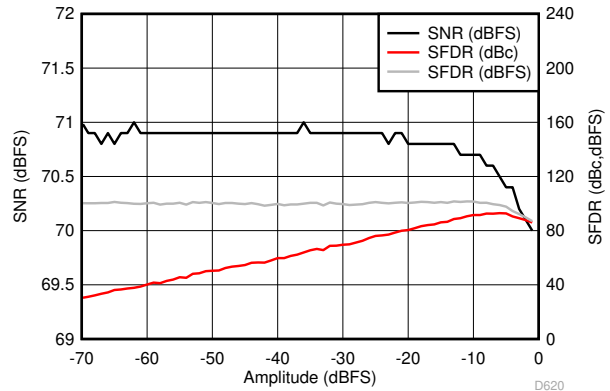


Figure 6-50. Performance vs Input Amplitude (170 MHz)

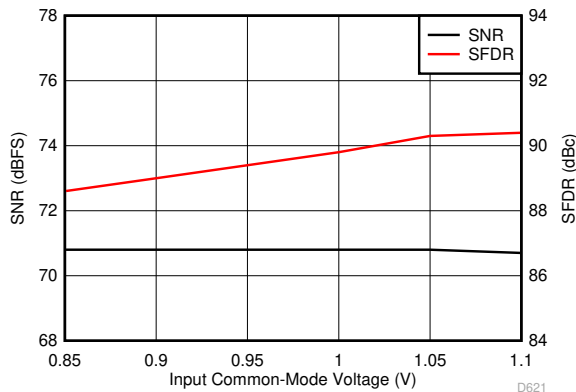


Figure 6-51. Performance vs Input Common-Mode Voltage (30 MHz)

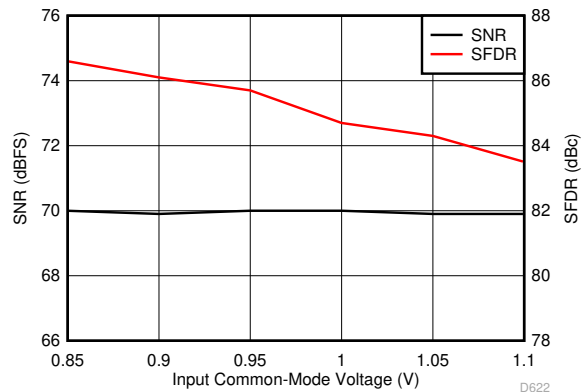
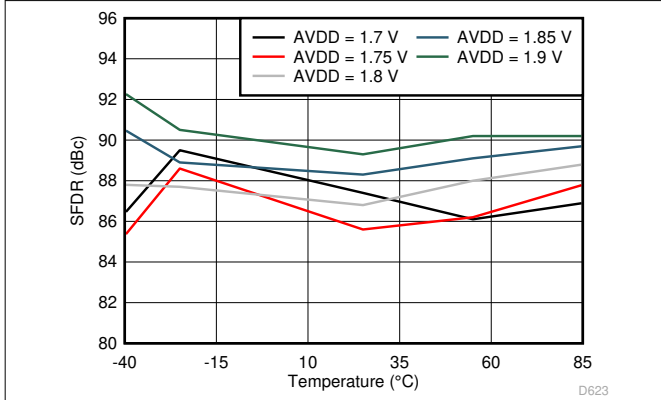


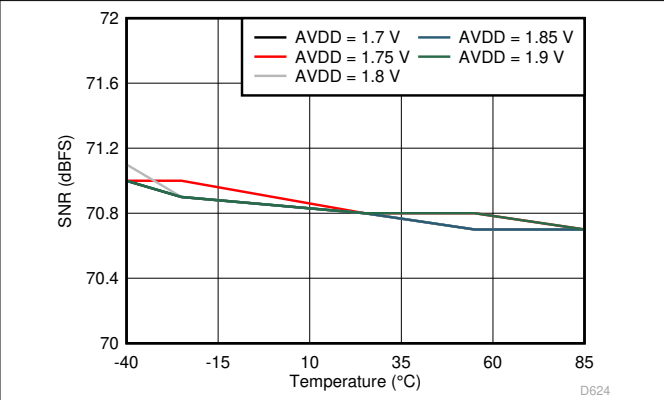
Figure 6-52. Performance vs Input Common-Mode Voltage (170 MHz)

## 6.16 Typical Characteristics: ADC3222 (continued)

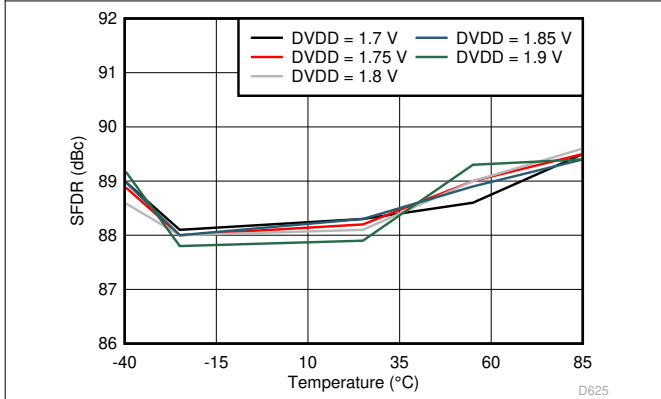
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2-V<sub>PP</sub> full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



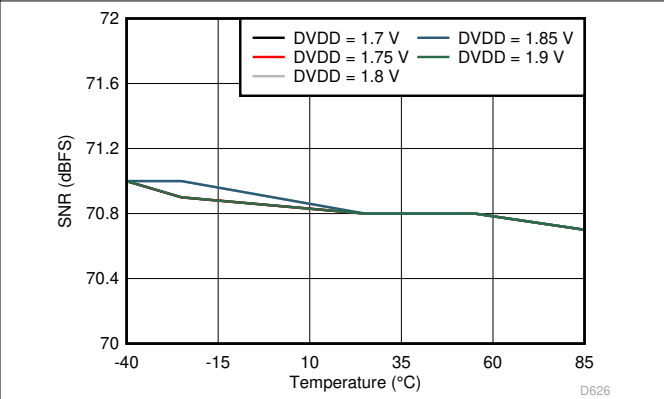
**Figure 6-53. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)**



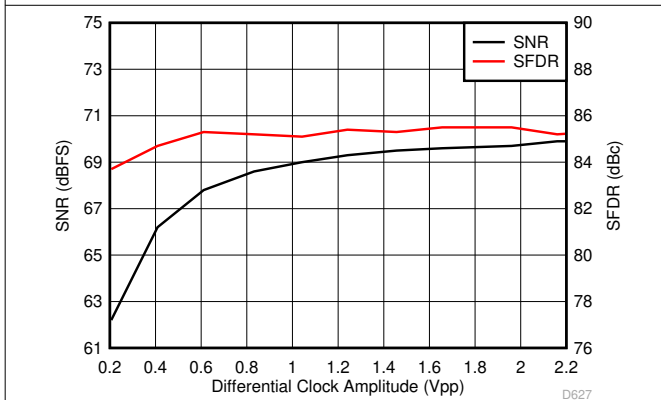
**Figure 6-54. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)**



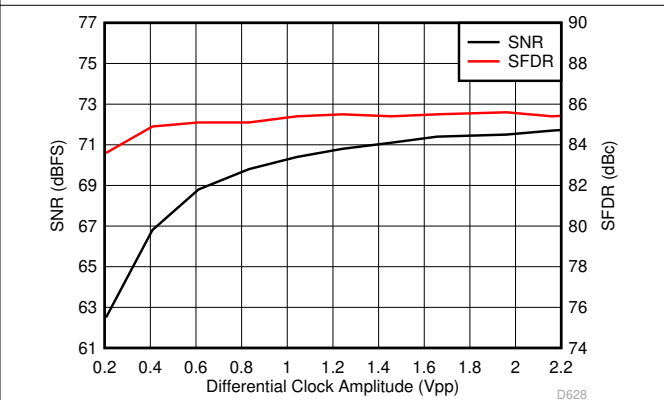
**Figure 6-55. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)**



**Figure 6-56. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)**



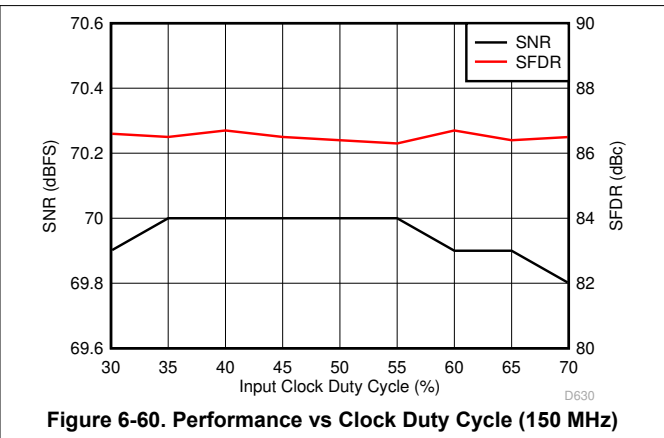
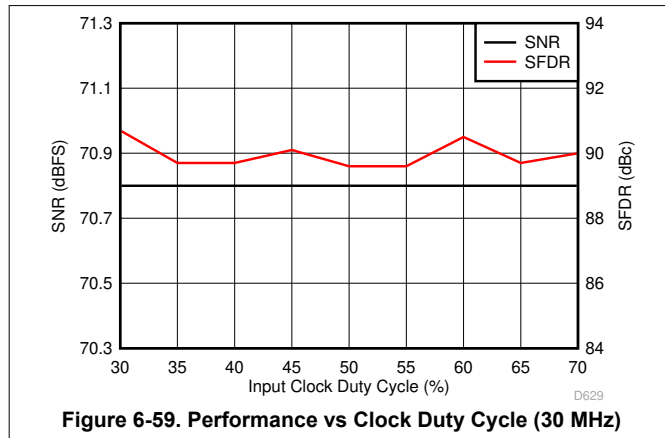
**Figure 6-57. Performance vs Differential Clock Amplitude (40 MHz)**



**Figure 6-58. Performance vs Differential Clock Amplitude (150 MHz)**

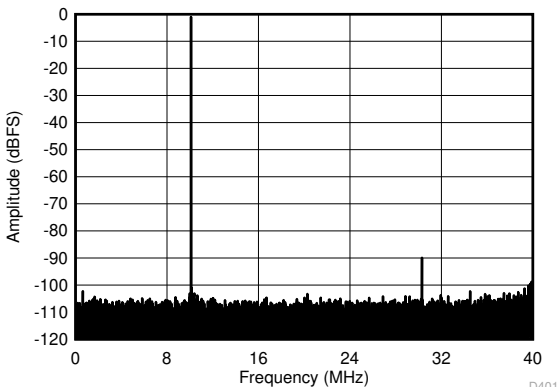
### 6.16 Typical Characteristics: ADC3222 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input,  $2-V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



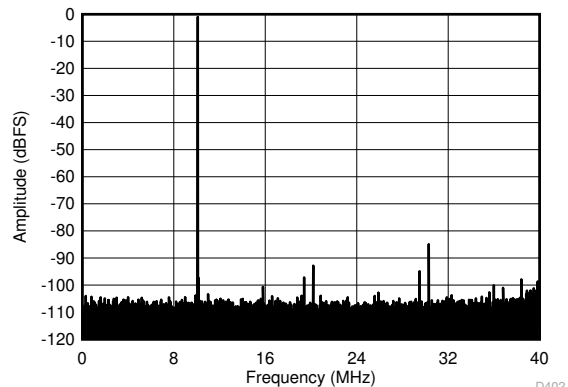
## 6.17 Typical Characteristics: ADC3223

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



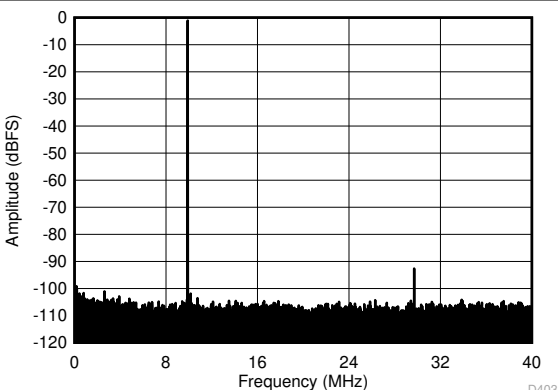
SFDR = 88.9 dBc, SNR = 70.9 dBFS, SINAD = 70.8 dBFS,  
THD = 88.6 dBc, HD2 = 108.1 dBc, HD3 = 88.9 dBc

Figure 6-61. FFT for 10-MHz Input Signal (Dither On)



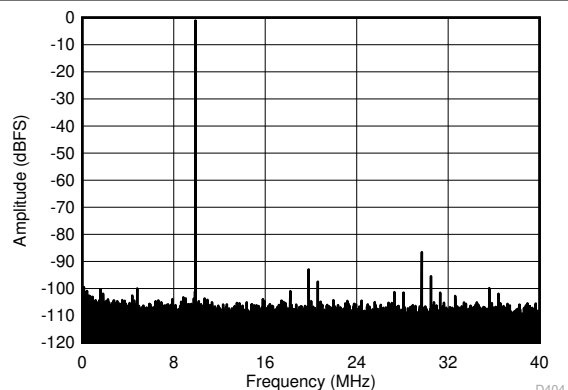
SFDR = 83.9 dBc, SNR = 71.1 dBFS, SINAD = 70.9 dBFS,  
THD = 82.6 dBc, HD2 = 91.8 dBc, HD3 = 83.9 dBc

Figure 6-62. FFT for 10-MHz Input Signal (Dither Off)



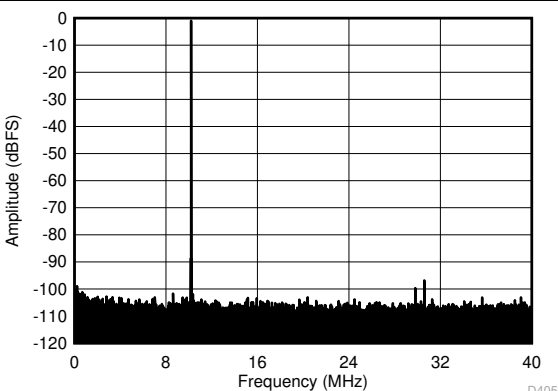
SFDR = 91.6 dBc, SNR = 70.8 dBFS, SINAD = 70.8 dBFS,  
THD = 91 dBc, HD2 = 112.2 dBc, HD3 = 91.6 dBc

Figure 6-63. FFT for 70-MHz Input Signal (Dither On)



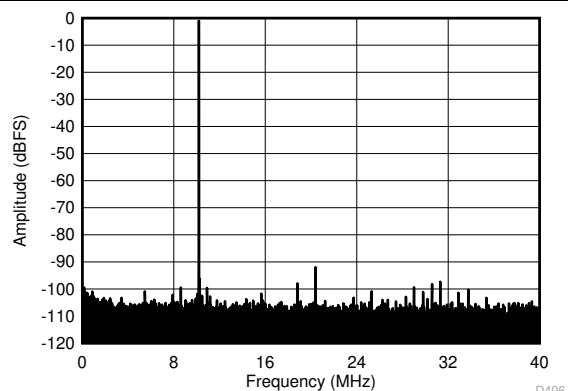
SFDR = 85.5 dBc, SNR = 71.1 dBFS, SINAD = 70.9 dBFS,  
THD = 83.8 dBc, HD2 = 91.9 dBc, HD3 = 85.5 dBc

Figure 6-64. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 95.8 dBc, SNR = 70.4 dBFS, SINAD = 70.3 dBFS,  
THD = 92.9 dBc, HD2 = 102.1 dBc, HD3 = 95.8 dBc

Figure 6-65. FFT for 170-MHz Input Signal (Dither On)

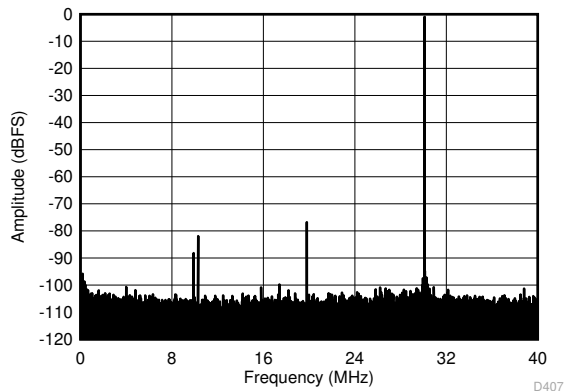


SFDR = 91.0 dBc, SNR = 70.7 dBFS, SINAD = 70.6 dBFS,  
THD = 88 dBc, HD2 = 91.0 dBc, HD3 = 97.2 dBc

Figure 6-66. FFT for 170-MHz Input Signal (Dither Off)

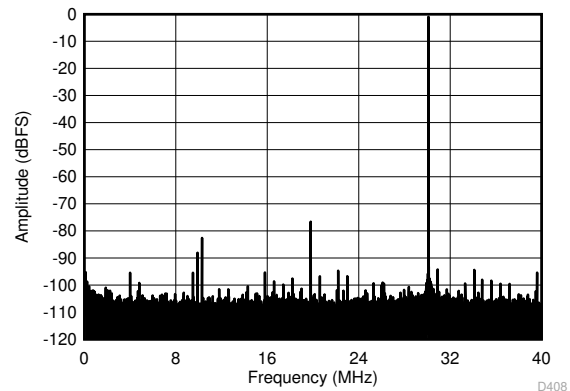
### 6.17 Typical Characteristics: ADC3223 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



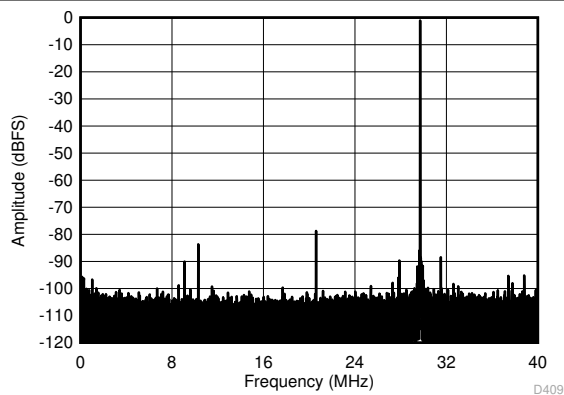
SFDR = 75.8 dBc, SNR = 69.4 dBFS, SINAD = 68.5 dBFS,  
THD = 74.6 dBc, HD2 = 75.8 dBc, HD3 = 80.9 dBc

**Figure 6-67. FFT for 270-MHz Input Signal (Dither On)**



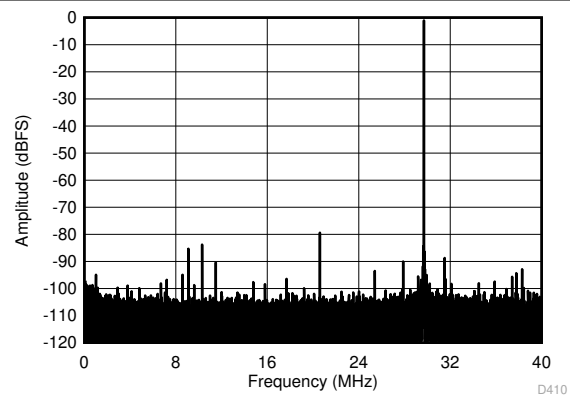
SFDR = 75.6 dBc, SNR = 69.7 dBFS, SINAD = 68.6 dBFS,  
THD = 74.5 dBc, HD2 = 75.6 dBc, HD3 = 81.6 dBc

**Figure 6-68. FFT for 270-MHz Input Signal (Dither Off)**



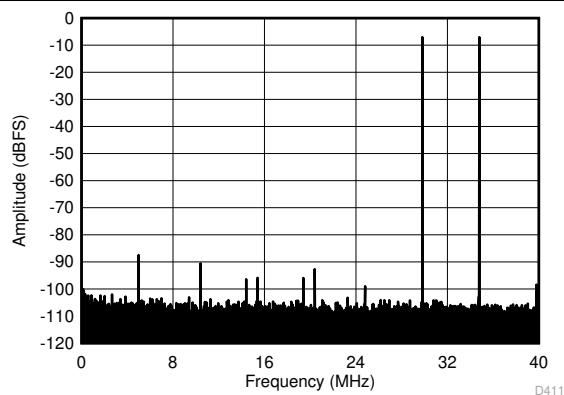
SFDR = 77.7 dBc, SNR = 67.7 dBFS, SINAD = 67.3 dBFS,  
THD = 77.2 dBc, HD2 = 77.7 dBc, HD3 = 89.0 dBc

**Figure 6-69. FFT for 450-MHz Input Signal (Dither On)**



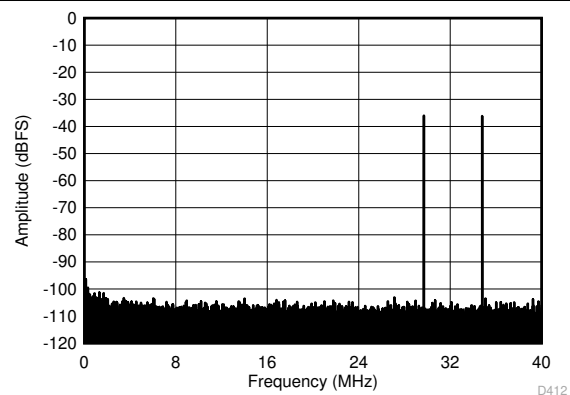
SFDR = 78.4 dBc, SNR = 67.9 dBFS, SINAD = 67.5 dBFS,  
THD = 77 dBc, HD2 = 78.4 dBc, HD3 = 84.3 dBc

**Figure 6-70. FFT for 450-MHz Input Signal (Dither Off)**



$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 87.5 dBFS, each tone at  $-7\text{ dBFS}$

**Figure 6-71. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)**

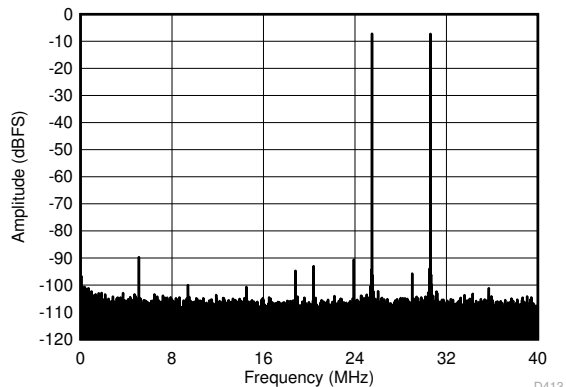


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 105 dBFS, each tone at  $-36\text{ dBFS}$

**Figure 6-72. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)**

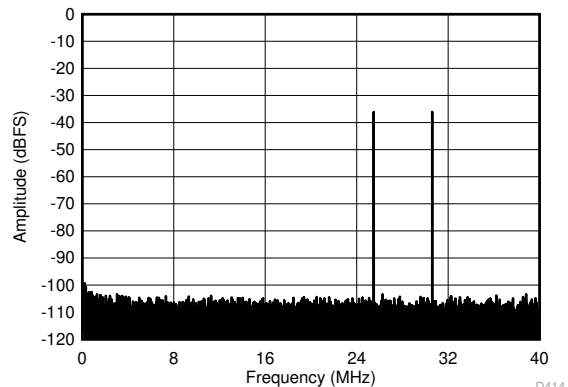
### 6.17 Typical Characteristics: ADC3223 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



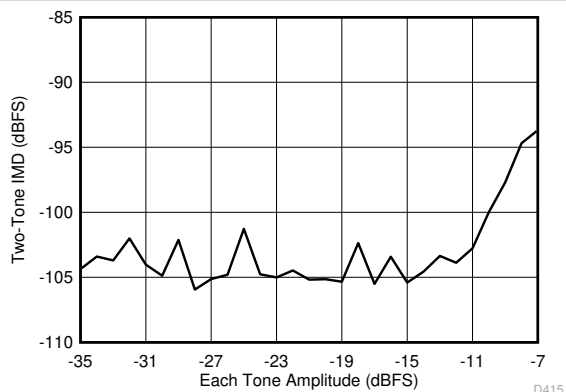
$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 89\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 6-73. FFT FOR Two-Tone Input Signal ( $-7\text{ dBFS}$  at 185 MHz and 190 MHz)**

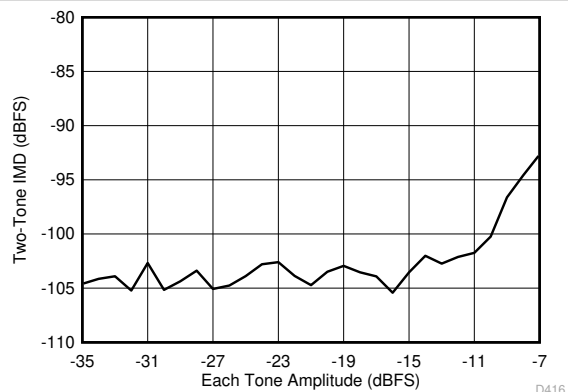


$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 105\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

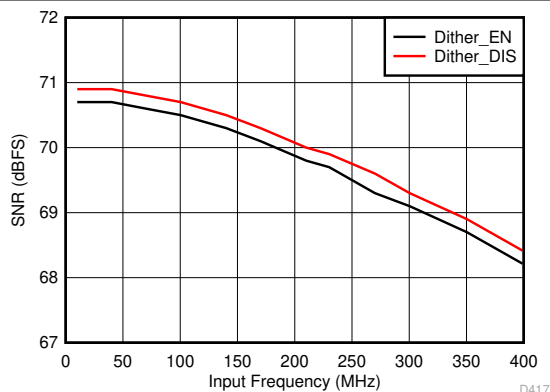
**Figure 6-74. FFT FOR Two-Tone Input Signal ( $-36\text{ dBFS}$  at 185 MHz and 190 MHz)**



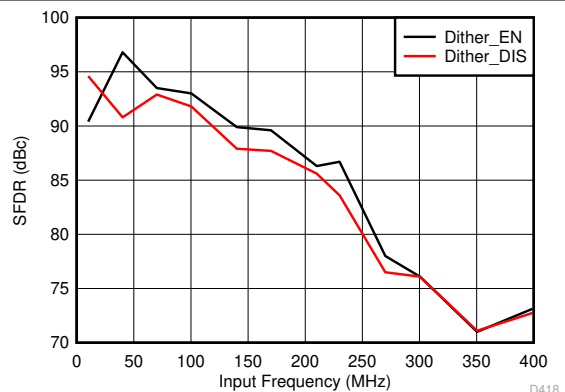
**Figure 6-75. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 6-76. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



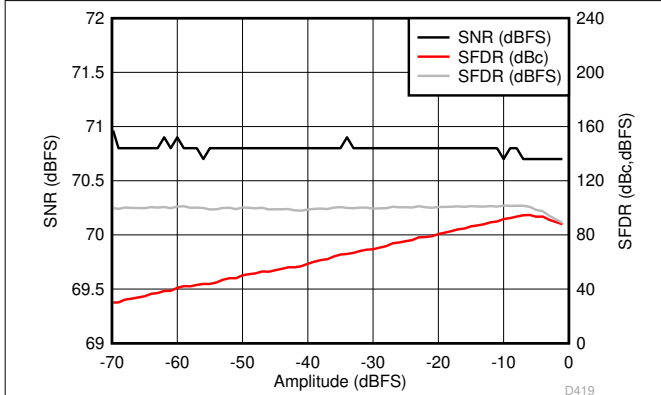
**Figure 6-77. Signal-to-Noise Ratio vs Input Frequency**



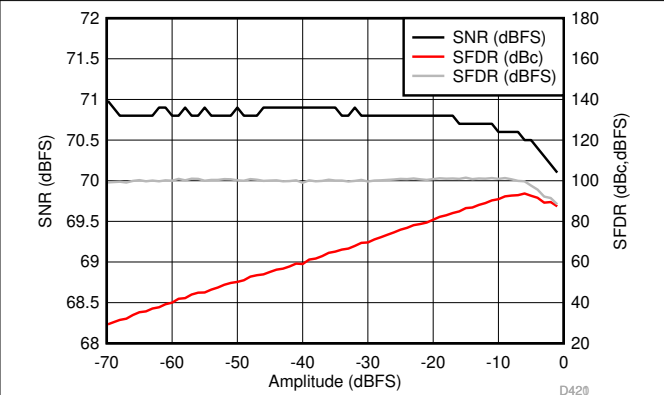
**Figure 6-78. Spurious-Free Dynamic Range vs Input Frequency**

### 6.17 Typical Characteristics: ADC3223 (continued)

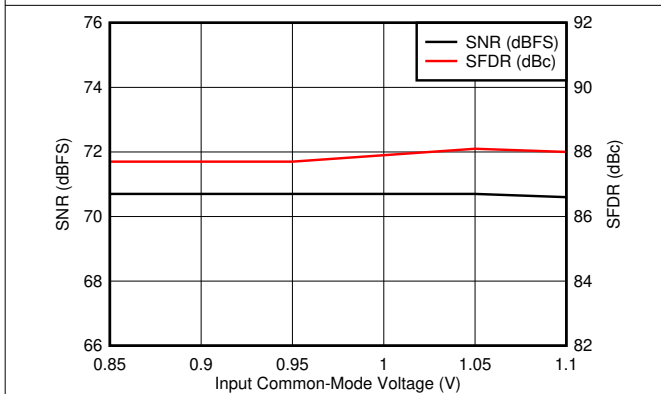
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- $V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



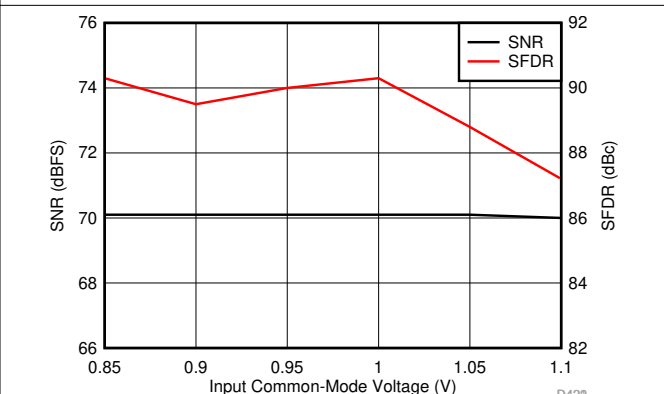
**Figure 6-79. Performance vs Input Amplitude (30 MHz)**



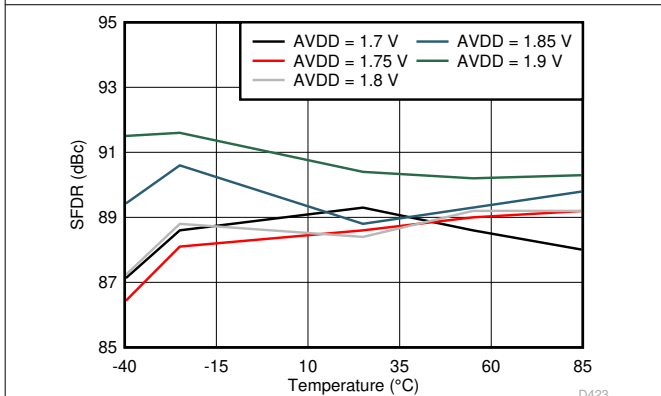
**Figure 6-80. Performance vs Input Amplitude (170 MHz)**



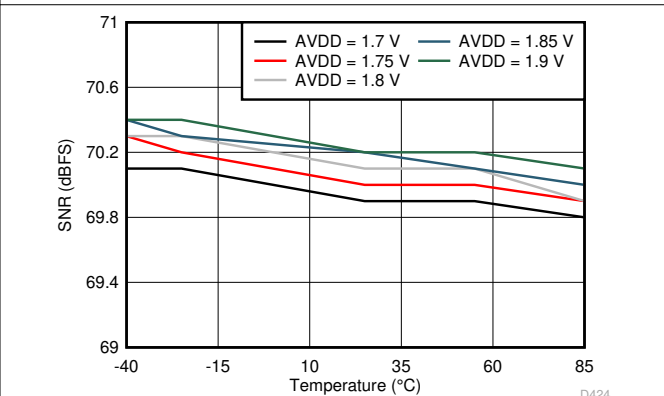
**Figure 6-81. Performance vs Input Common-Mode Voltage (30 MHz)**



**Figure 6-82. Performance vs Input Common-Mode Voltage (170 MHz)**



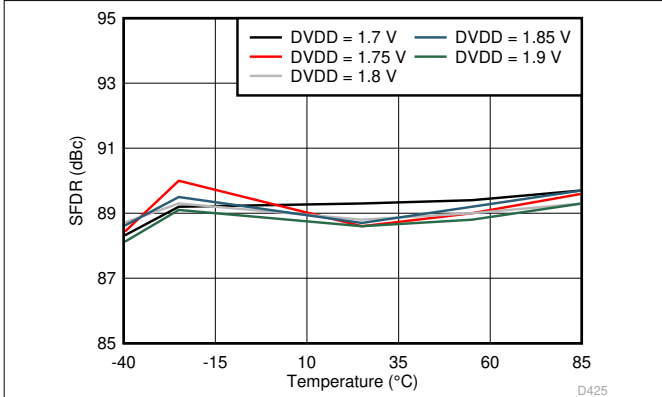
**Figure 6-83. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)**



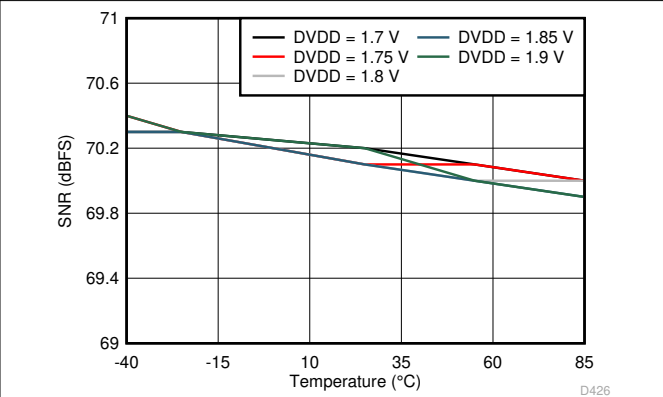
**Figure 6-84. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)**

### 6.17 Typical Characteristics: ADC3223 (continued)

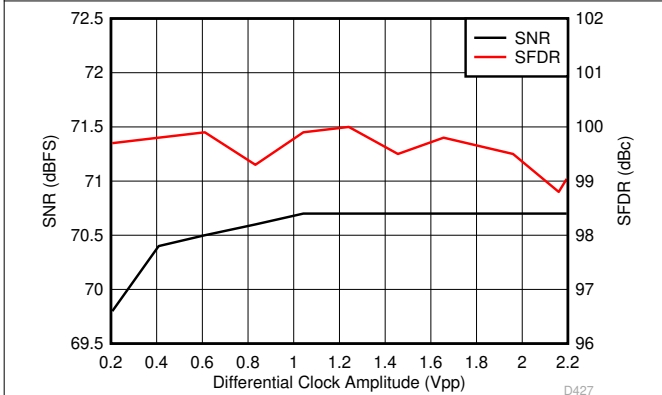
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 80 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



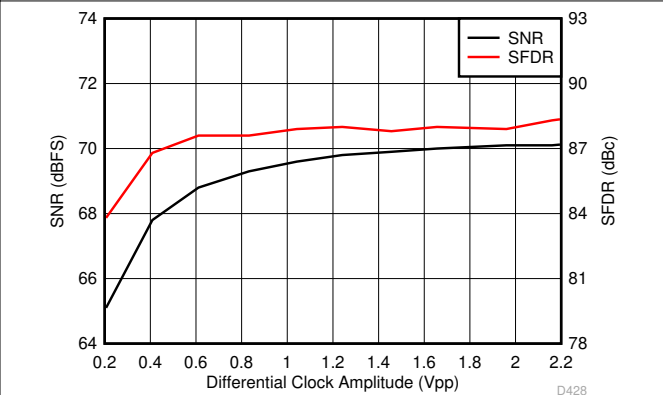
**Figure 6-85. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)**



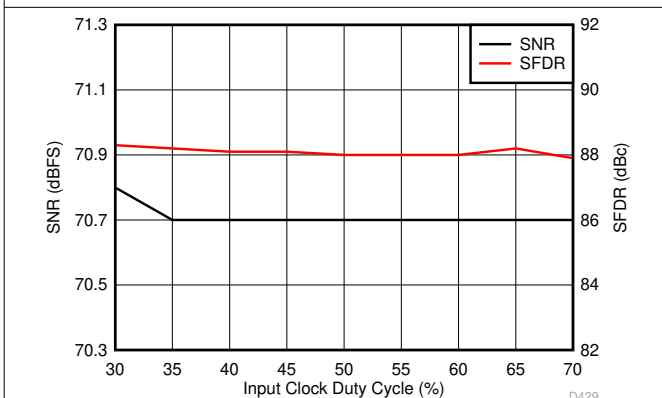
**Figure 6-86. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)**



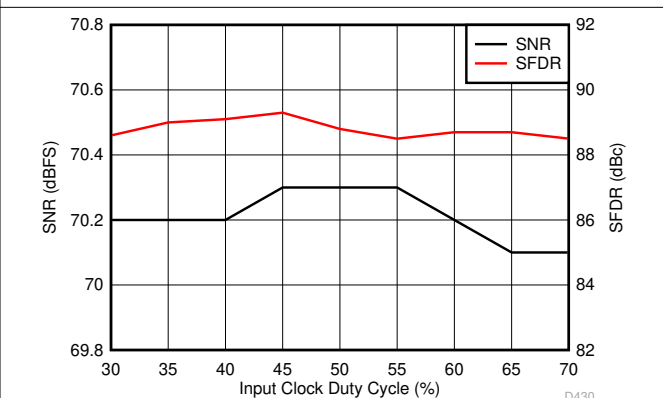
**Figure 6-87. Performance vs Differential Clock Amplitude (40 MHz)**



**Figure 6-88. Performance vs Differential Clock Amplitude (150 MHz)**



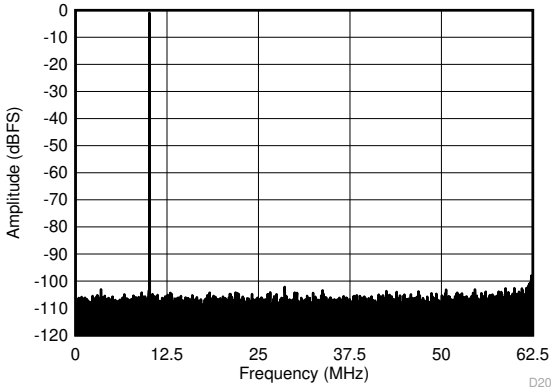
**Figure 6-89. Performance vs Clock Duty Cycle (30 MHz)**



**Figure 6-90. Performance vs Clock Duty Cycle (150 MHz)**

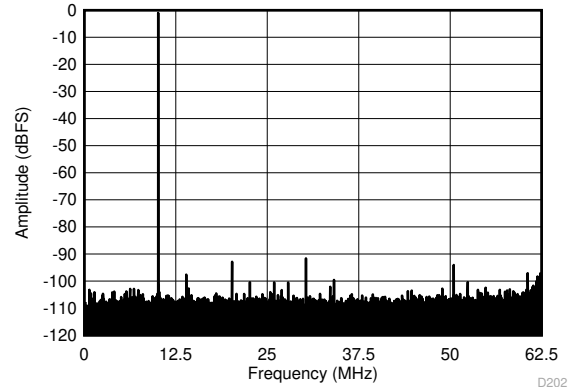
## 6.18 Typical Characteristics: ADC3224

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



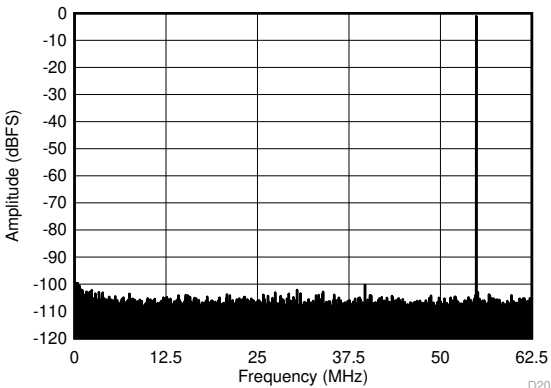
SFDR = 101.1 dBc, SNR = 70.6 dBFS, SINAD = 70.6 dBFS,  
THD = 97.6 dBc, HD2 = 107.0 dBc, HD3 = 106.0 dBc

**Figure 6-91. FFT for 10 MHz Input Signal (Chopper On, Dither On)**



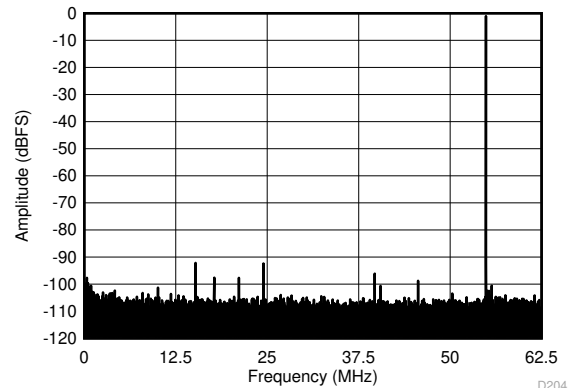
SFDR = 90.6 dBc, SNR = 70.9 dBFS, SINAD = 70.8 dBFS,  
THD = 86 dBc, HD2 = 91.8 dBc, HD3 = 90.6 dBc

**Figure 6-92. FFT for 10-MHz Input Signal (Chopper On, Dither Off)**



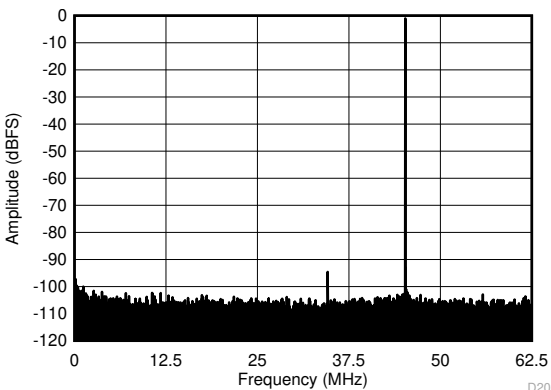
SFDR = 99.2 dBc, SNR = 70.5 dBFS, SINAD = 70.5 dBFS,  
THD = 94.8 dBc, HD2 = 102.9 dBc, HD3 = 99.2 dBc

**Figure 6-93. FFT for 70-MHz Input Signal (Dither On)**



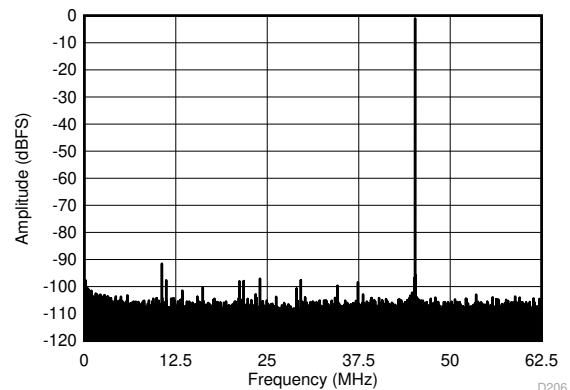
SFDR = 91.1 dBc, SNR = 70.8 dBFS, SINAD = 70.8 dBFS,  
THD = 86.8 dBc, HD2 = 91.1 dBc, HD3 = 95.1 dBc

**Figure 6-94. FFT for 70-MHz Input Signal (Dither Off)**



SFDR = 93.6 dBc, SNR = 70.0 dBFS, SINAD = 70.0 dBFS,  
THD = 91.4 dBc, HD2 = 93.6 dBc, HD3 = 101.3 dBc

**Figure 6-95. FFT for 170-MHz Input Signal (Dither On)**

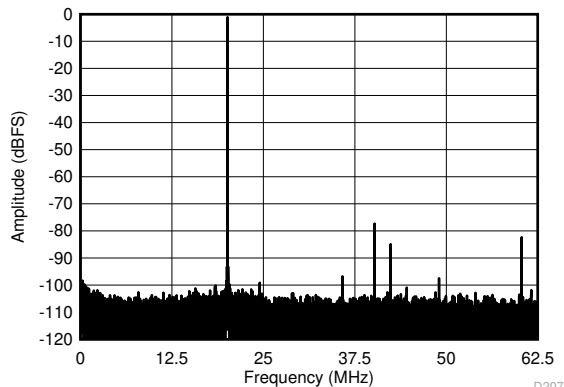


SFDR = 90.6 dBc, SNR = 70.5 dBFS, SINAD = 70.4 dBFS,  
THD = 87.8 dBc, HD2 = 98.6 dBc, HD3 = 90.6 dBc

**Figure 6-96. FFT for 170 MHz Input Signal (Dither Off)**

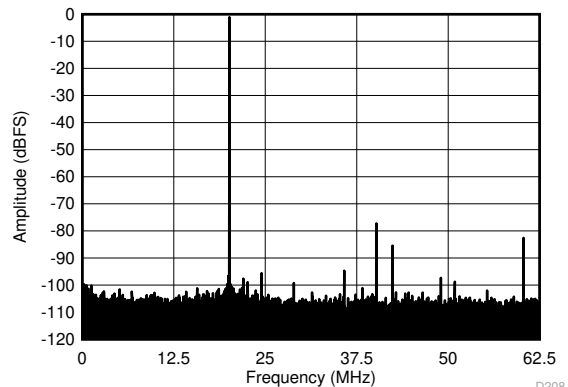
## 6.18 Typical Characteristics: ADC3224 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



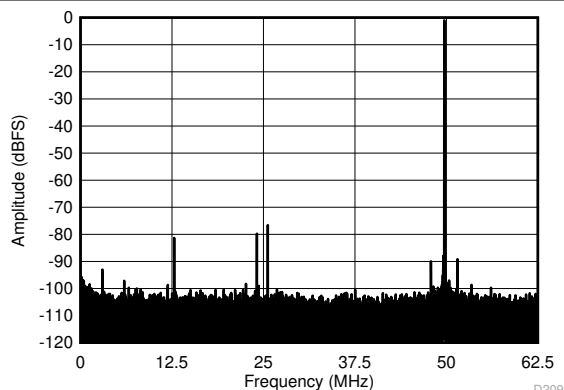
SFDR = 76.2 dBc, SNR = 69.4 dBFS, SINAD = 68.6 dBFS,  
 THD = 74.9 dBc, HD2 = 76.2 dBc, HD3 = 81.2 dBc

Figure 6-97. FFT for 270-MHz Input Signal (Dither On)



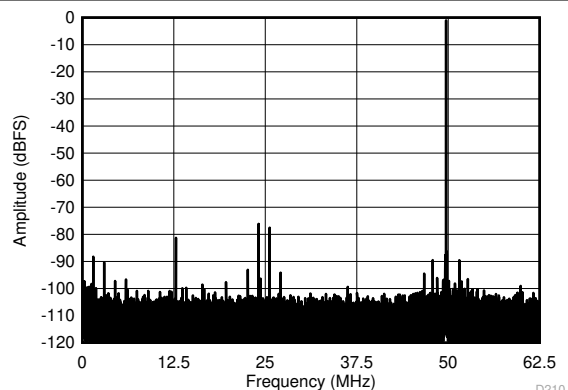
SFDR = 76.1 dBc, SNR = 69.7 dBFS, SINAD = 68.8 dBFS,  
 THD = 74.9 dBc, HD2 = 76.1 dBc, HD3 = 81.5 dBc

Figure 6-98. FFT for 270-MHz Input Signal (Dither Off)



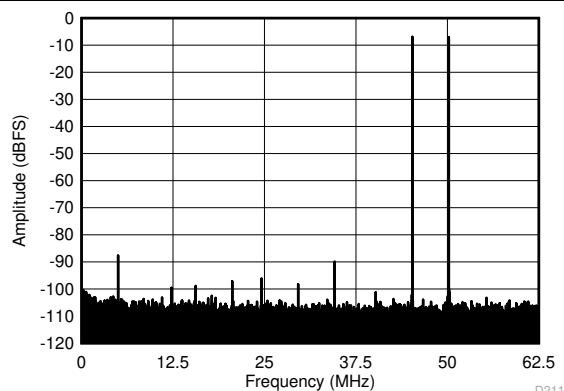
SFDR = 75.5 dBc, SNR = 67.4 dBFS, SINAD = 66.7 dBFS,  
 THD = 73.8 dBc, HD2 = 75.5 dBc, HD3 = 78.7 dBc

Figure 6-99. FFT for 450-MHz Input Signal (Dither On)



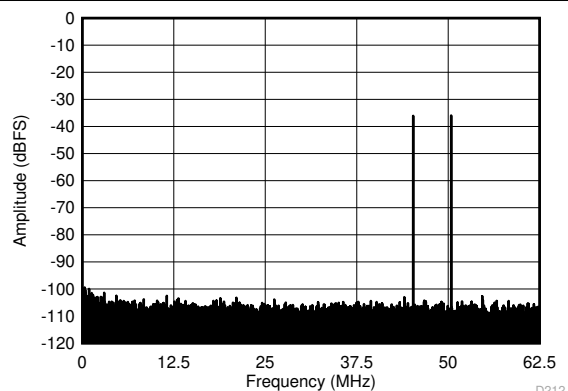
SFDR = 75.2 dBc, SNR = 68 dBFS, SINAD = 67.0 dBFS, THD  
 = 72.5 dBc, HD2 = 76.5 dBc, HD3 = 75.2 dBc

Figure 6-100. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 88 dBFS, each tone at  
 $-7\text{ dBFS}$

Figure 6-101. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 46 MHz and 50 MHz)

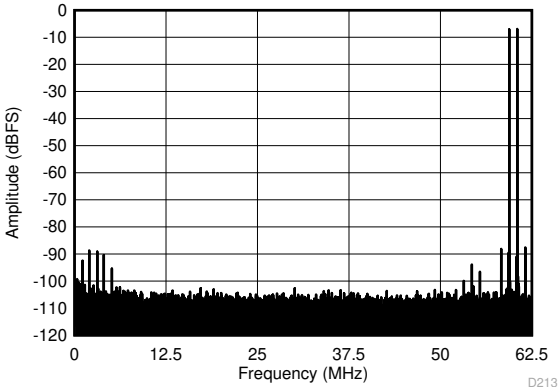


$f_{IN1} = 46\text{ MHz}$ ,  $f_{IN2} = 50\text{ MHz}$ , IMD3 = 105 dBFS, each tone at  
 $-36\text{ dBFS}$

Figure 6-102. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 46 MHz and 50 MHz)

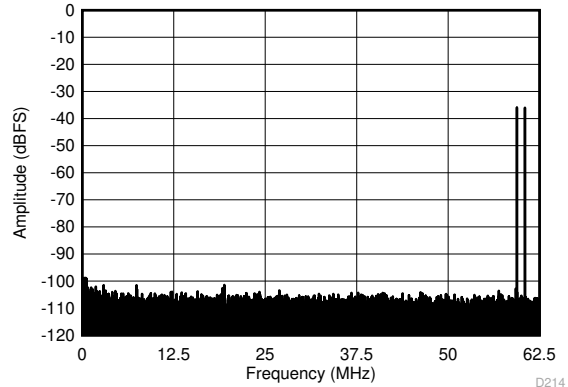
### 6.18 Typical Characteristics: ADC3224 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{ dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



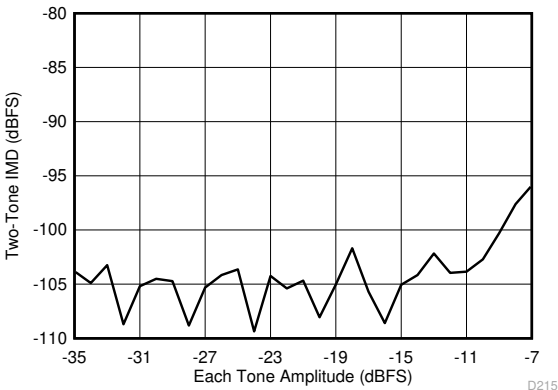
$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 87.5\text{ dBFS}$ , each tone at  $-7\text{ dBFS}$

**Figure 6-103. FFT for Two-Tone Input Signal ( $-7\text{ dBFS}$  at 185 MHz and 190 MHz)**

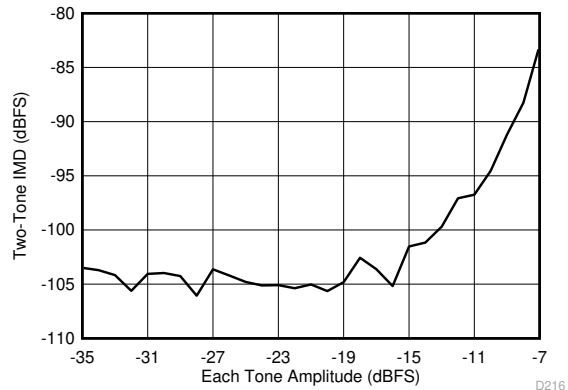


$f_{IN1} = 185\text{ MHz}$ ,  $f_{IN2} = 190\text{ MHz}$ ,  $\text{IMD3} = 96.5\text{ dBFS}$ , each tone at  $-36\text{ dBFS}$

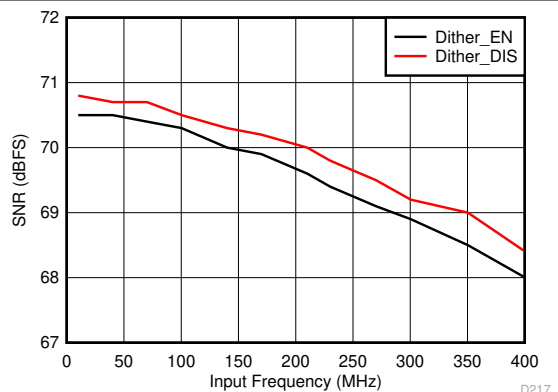
**Figure 6-104. FFT for Two-Tone Input Signal ( $-36\text{ dBFS}$  at 185 MHz and 190 MHz)**



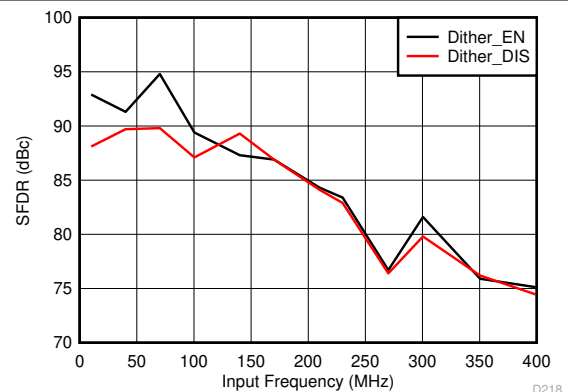
**Figure 6-105. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)**



**Figure 6-106. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)**



**Figure 6-107. Signal-to-Noise Ratio vs Input Frequency**



**Figure 6-108. Spurious-Free Dynamic Range vs Input Frequency**

## 6.18 Typical Characteristics: ADC3224 (continued)

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AV_{DD} = 1.8\text{ V}$ ,  $DV_{DD} = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).

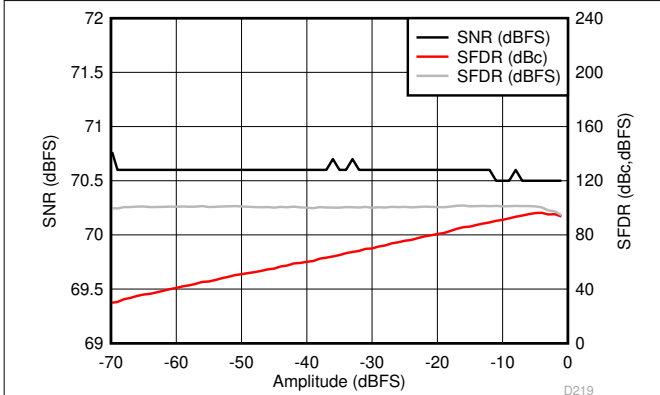


Figure 6-109. Performance vs Input Amplitude (30 MHz)

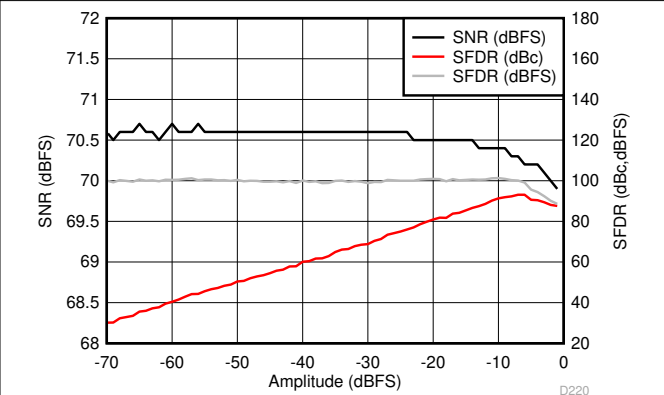


Figure 6-110. Performance vs Input Amplitude (170 MHz)

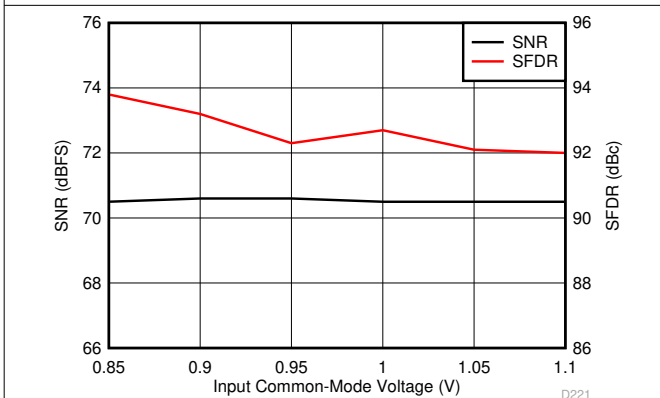


Figure 6-111. Performance vs Input Common-Mode Voltage (30 MHz)

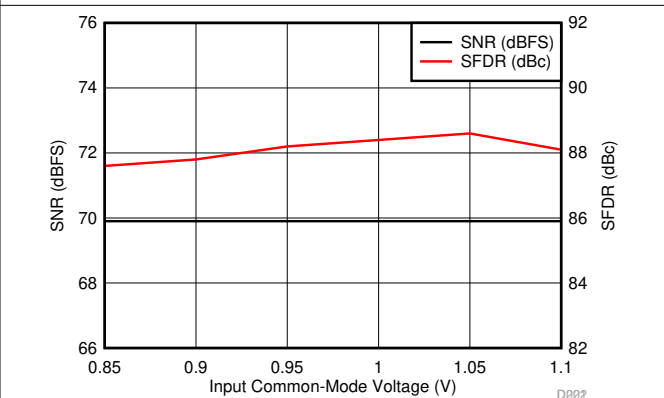


Figure 6-112. Performance vs Input Common-Mode Voltage (170 MHz)

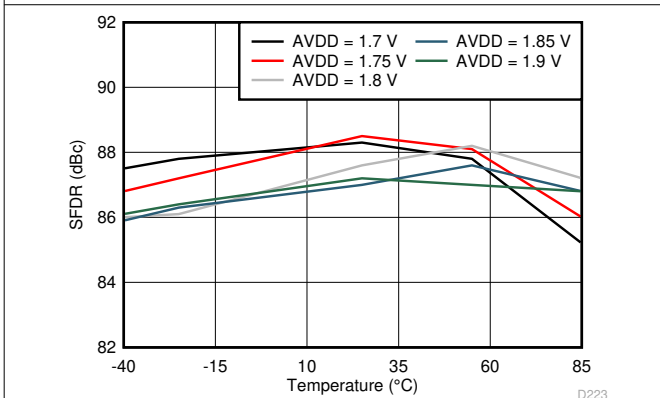


Figure 6-113. Spurious-Free Dynamic Range vs  $AV_{DD}$  Supply and Temperature (170 MHz)

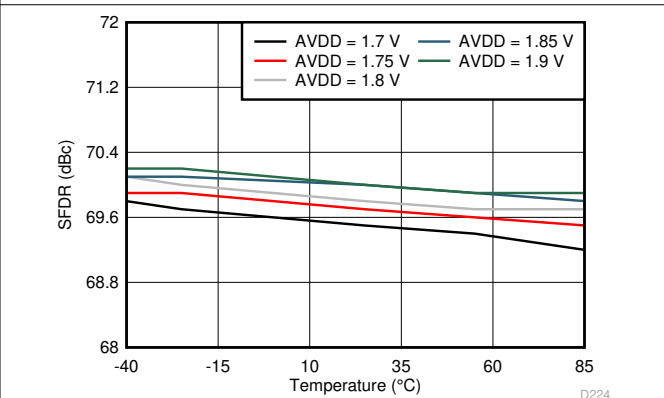
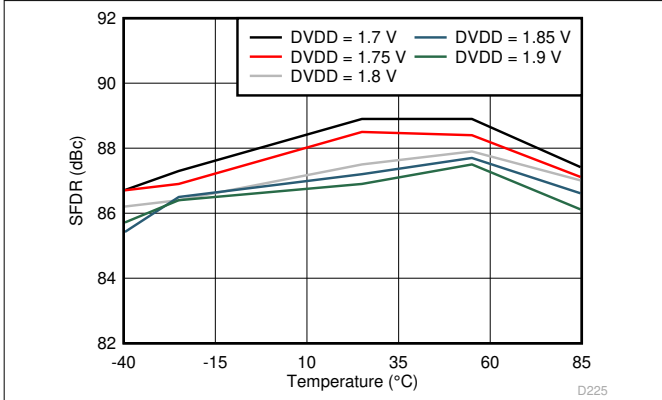


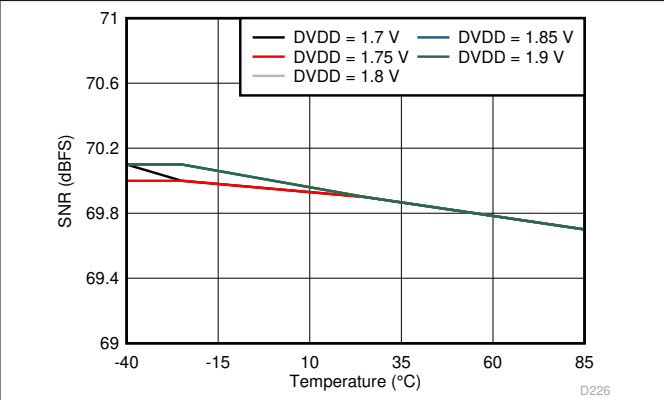
Figure 6-114. Signal-to-Noise Ratio vs  $AV_{DD}$  Supply and Temperature (170 MHz)

### 6.18 Typical Characteristics: ADC3224 (continued)

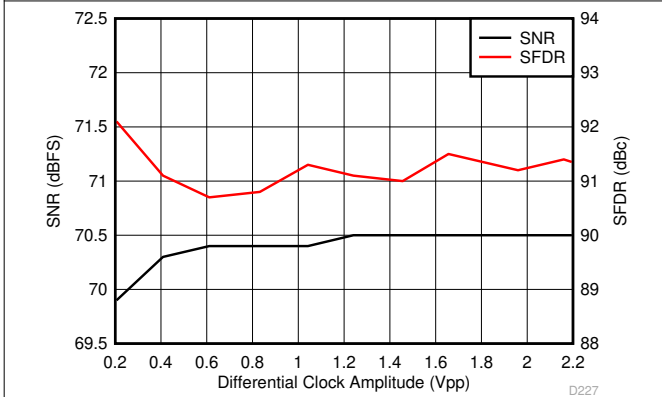
Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



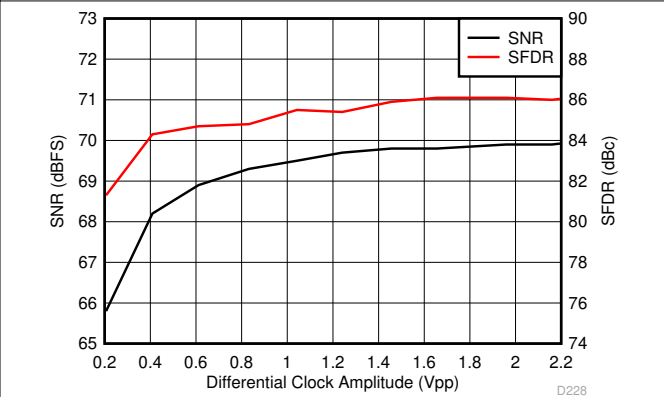
**Figure 6-115. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)**



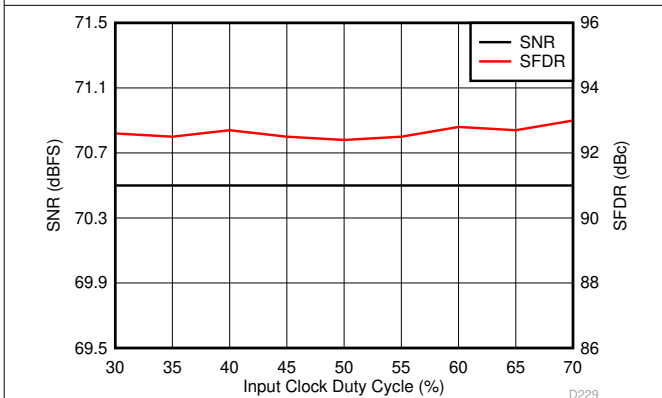
**Figure 6-116. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)**



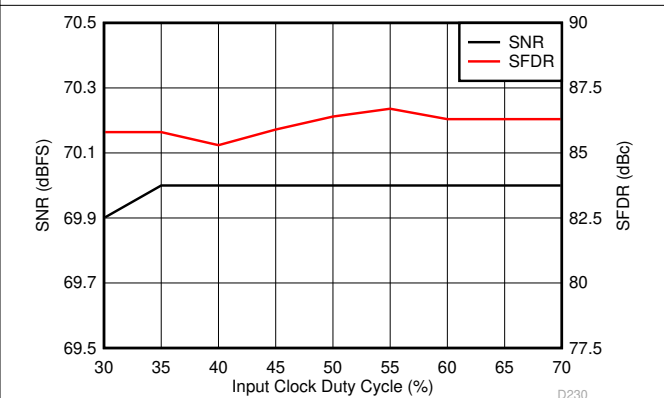
**Figure 6-117. Performance vs Differential Clock Amplitude (40 MHz)**



**Figure 6-118. Performance vs Differential Clock Amplitude (150 MHz)**



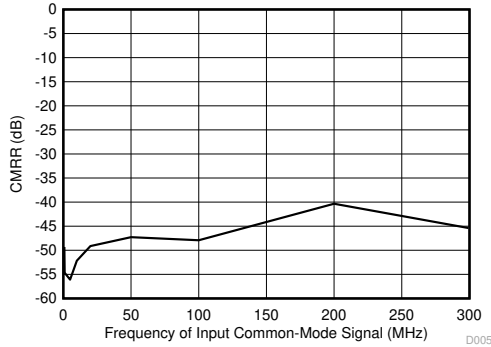
**Figure 6-119. Performance vs Clock Duty Cycle (30 MHz)**



**Figure 6-120. Performance vs Clock Duty Cycle (150 MHz)**

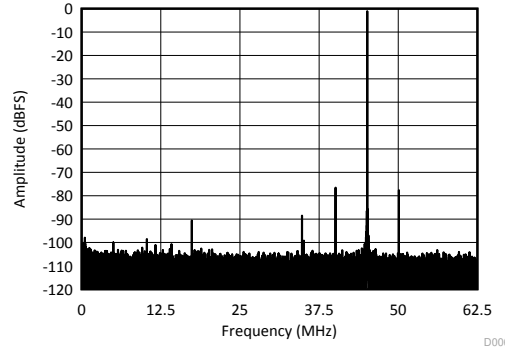
## 6.19 Typical Characteristics: Common

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when chopper is enabled (unless otherwise noted).



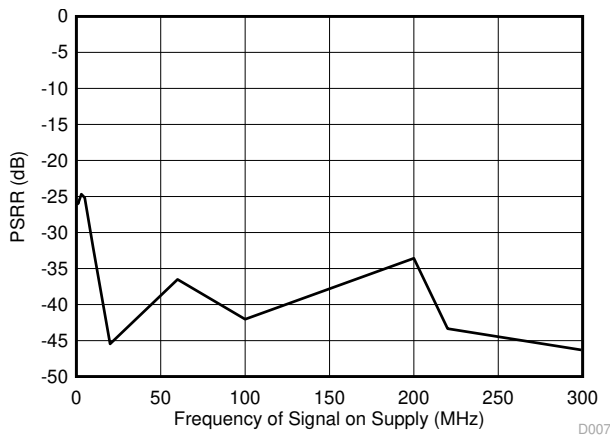
$f_{IN} = 30\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , common-mode signal amplitude =  $50\text{ mV}_{PP}$

**Figure 6-121. Common-Mode Rejection Ratio vs Common-Mode Signal Frequency**



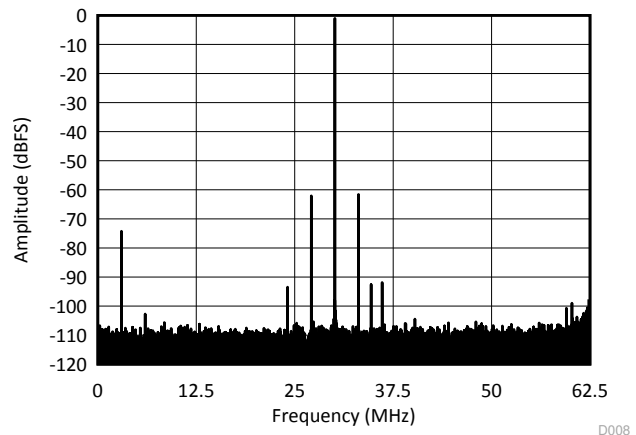
$f_{IN} = 170.1\text{ MHz}$ ,  $f_{CMRR} = 5\text{ MHz}$ ,  $A_{CMRR} = 50\text{ mV}_{PP}$ ,  $SINAD = 69.66\text{ dBFS}$ ,  $SFDR = 75.66\text{ dBc}$

**Figure 6-122. Common-Mode Rejection Ratio Spectrum**



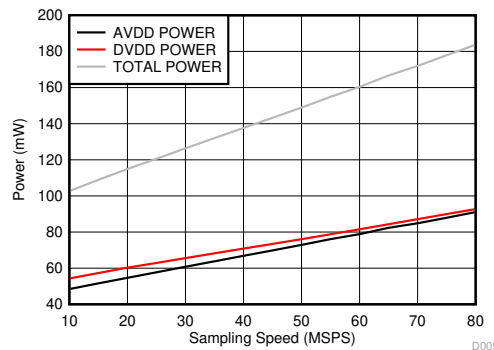
$f_{IN} = 30\text{ MHz}$ ,  $A_{IN} = -1\text{ dBFS}$ , test signal amplitude =  $50\text{ mV}_{PP}$

**Figure 6-123. Power-Supply Rejection Ratio vs Power-Supply Signal Frequency**



$f_{IN} = 30.1\text{ MHz}$ ,  $f_{PSRR} = 3\text{ MHz}$ ,  $A_{PSRR} = 50\text{ mV}_{PP}$ ,  $SINAD = 58.51\text{ dBFS}$ ,  $SFDR = 60.53\text{ dBc}$

**Figure 6-124. Power-Supply Rejection Ratio Spectrum**



**Figure 6-125. Power vs Sampling Speed (One-Wire Mode)**

## 6.20 Typical Characteristics: Contour

Typical values are at  $T_A = 25^\circ\text{C}$ , ADC sampling rate = 125 MSPS, 50% clock duty cycle,  $AVDD = 1.8\text{ V}$ ,  $DVDD = 1.8\text{ V}$ ,  $-1\text{-dBFS}$  differential input,  $2\text{-}V_{PP}$  full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from  $f_S / 2$  when is chopper enabled (unless otherwise noted).

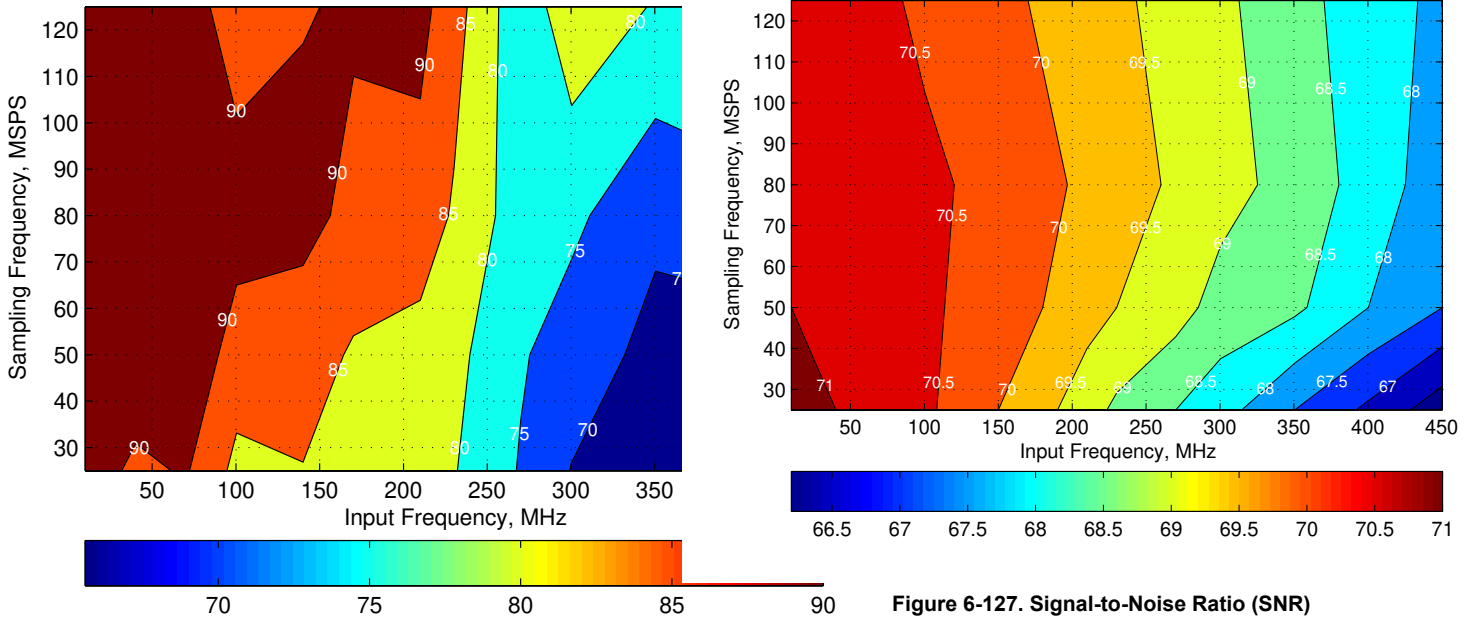
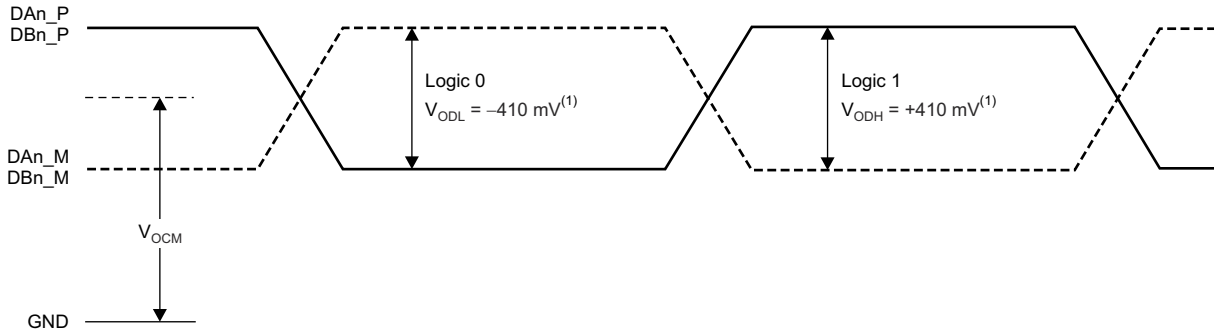


Figure 6-126. Spurious-Free Dynamic Range (SFDR)

Figure 6-127. Signal-to-Noise Ratio (SNR)

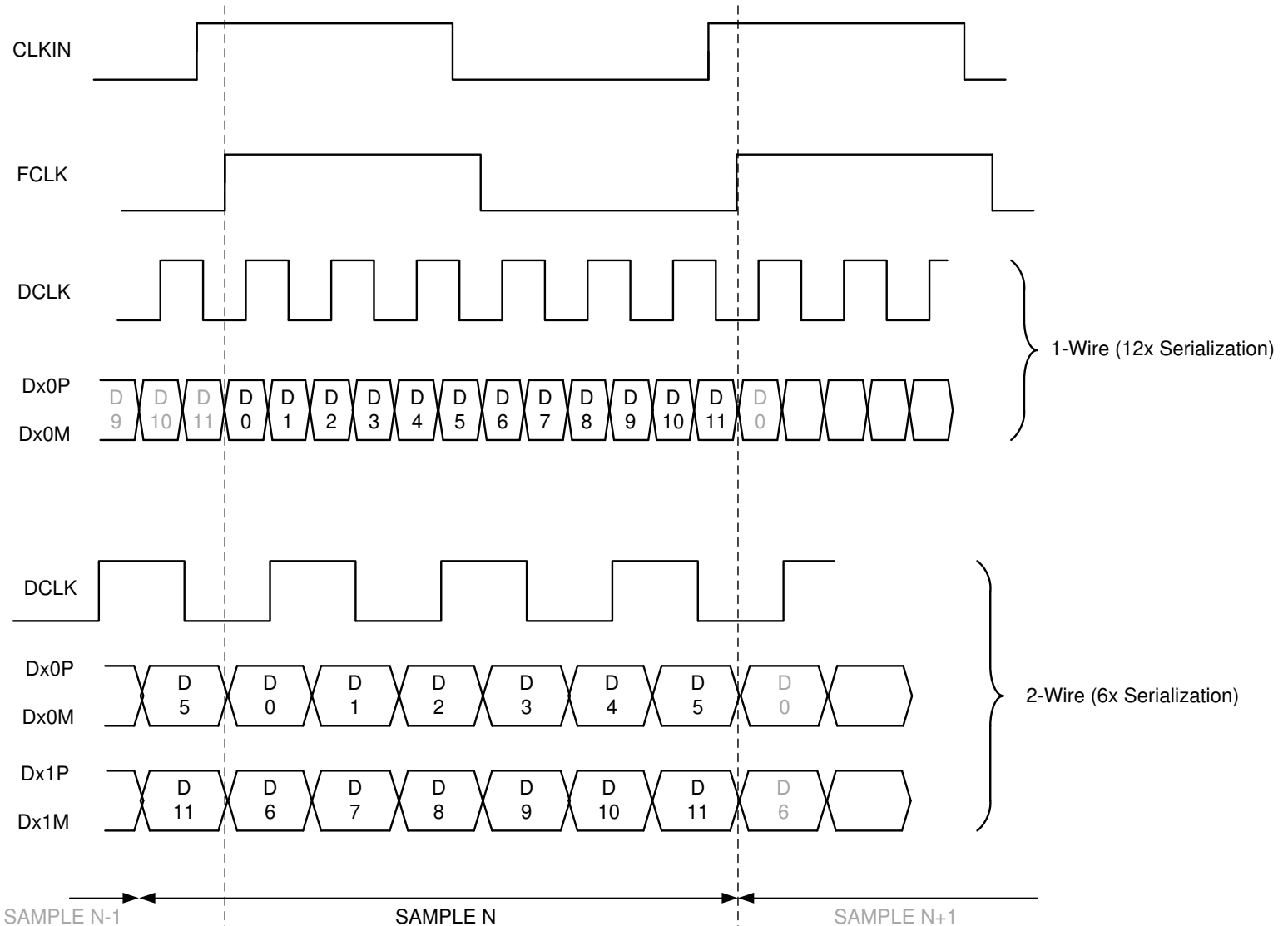
## 7 Parameter Measurement Information

### 7.1 Timing Diagrams

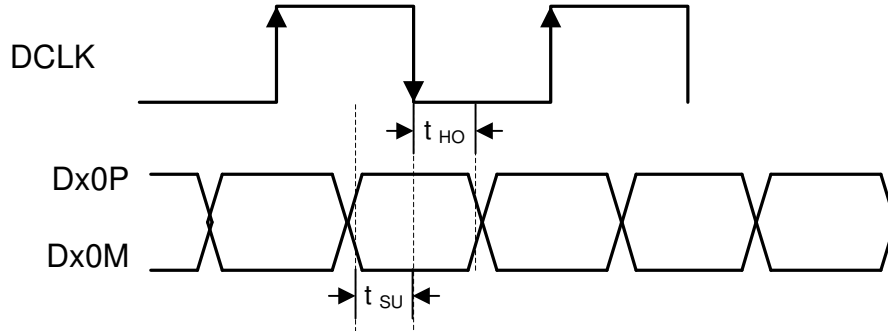


A. With an external 100-Ω termination.

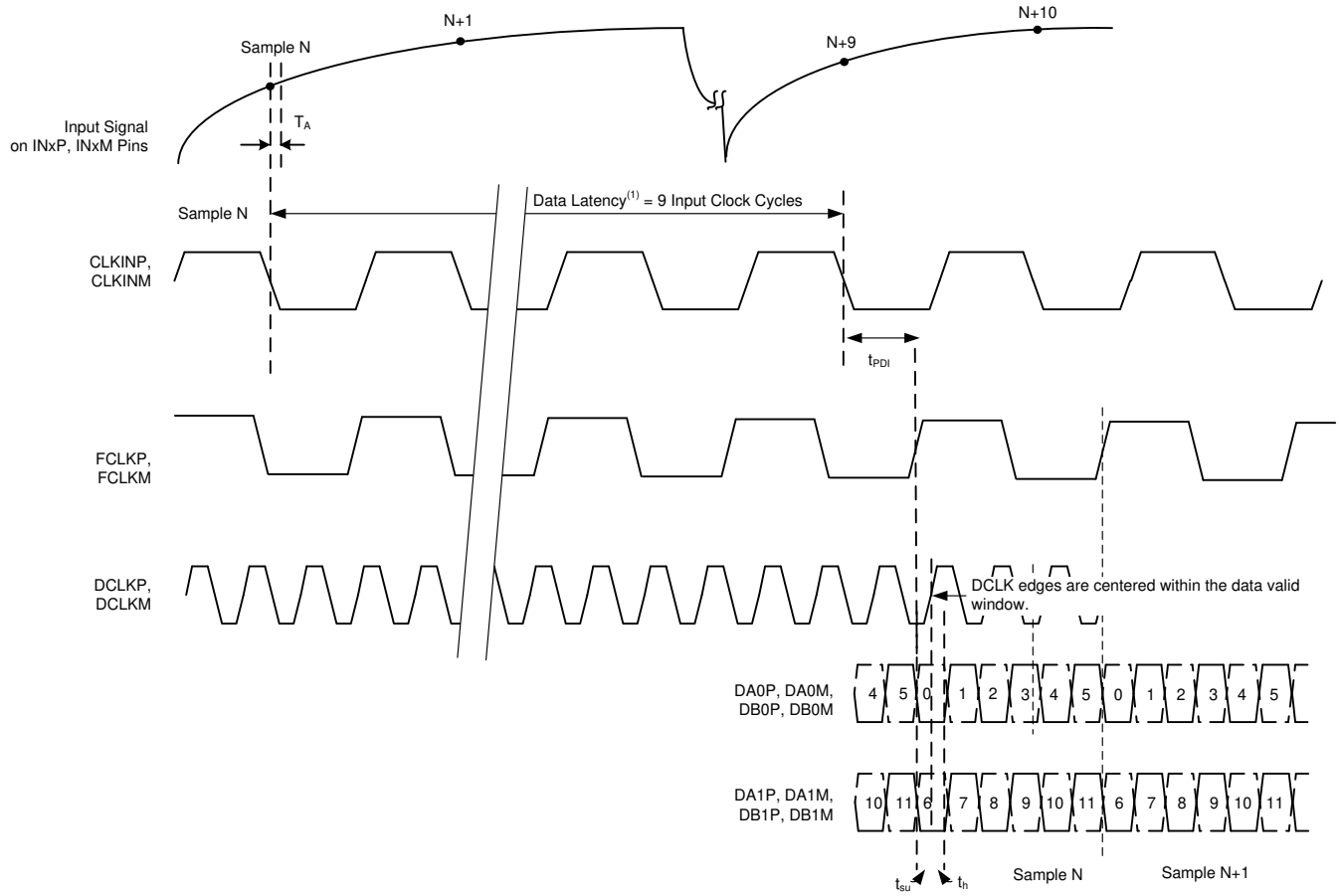
**Figure 7-1. Serial LVDS Output Voltage Levels**



**Figure 7-2. Output Timing Diagram**



**Figure 7-3. Setup and Hold Time**



A. Overall latency = data latency +  $t_{PD}$ .

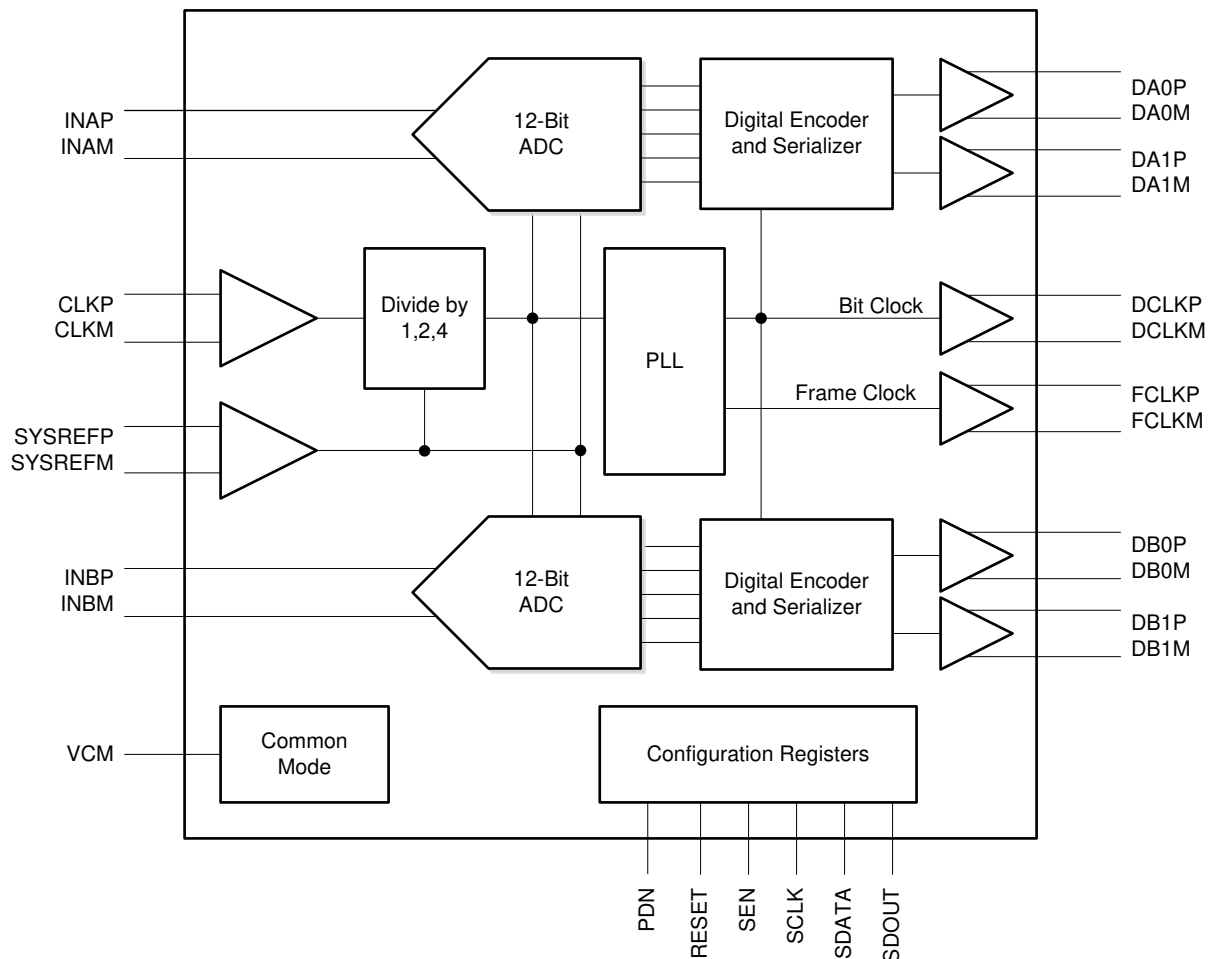
**Figure 7-4. Latency Diagram**

## 8 Detailed Description

### 8.1 Overview

The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization by resetting the clock divider. The ADC322x family supports serial LVDS interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

### 8.2 Functional Block Diagram



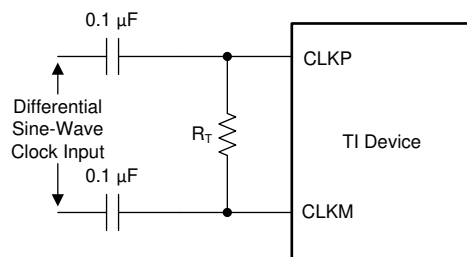
## 8.3 Feature Description

### 8.3.1 Analog Inputs

The ADC322x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between  $(V_{CM} + 0.5\text{ V})$  and  $(V_{CM} - 0.5\text{ V})$ , resulting in a  $2\text{-}V_{PP}$  (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50- $\Omega$  source driving a 50- $\Omega$  termination between INP and INM).

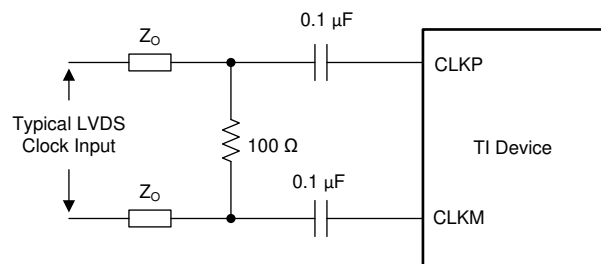
### 8.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-k $\Omega$  resistors. The self-bias clock inputs of the ADC322x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in [Figure 8-1](#), [Figure 8-2](#), and [Figure 8-3](#). See [Figure 8-4](#) for details regarding the internal clock buffer.

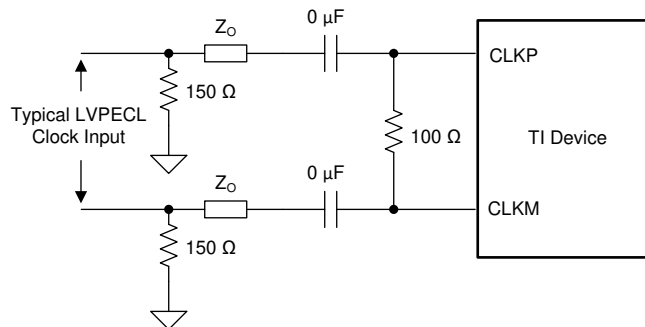


$R_T$  = termination resistor, if necessary.

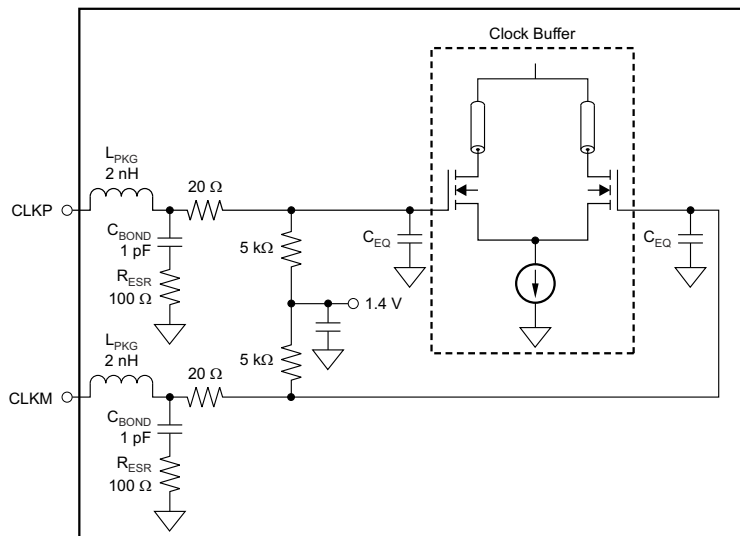
**Figure 8-1. Differential Sine-Wave Clock Driving Circuit**



**Figure 8-2. LVDS Clock Driving Circuit**



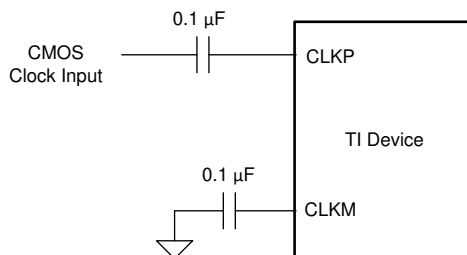
**Figure 8-3. LVPECL Clock Driving Circuit**



$C_{EQ}$  is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

**Figure 8-4. Internal Clock Buffer**

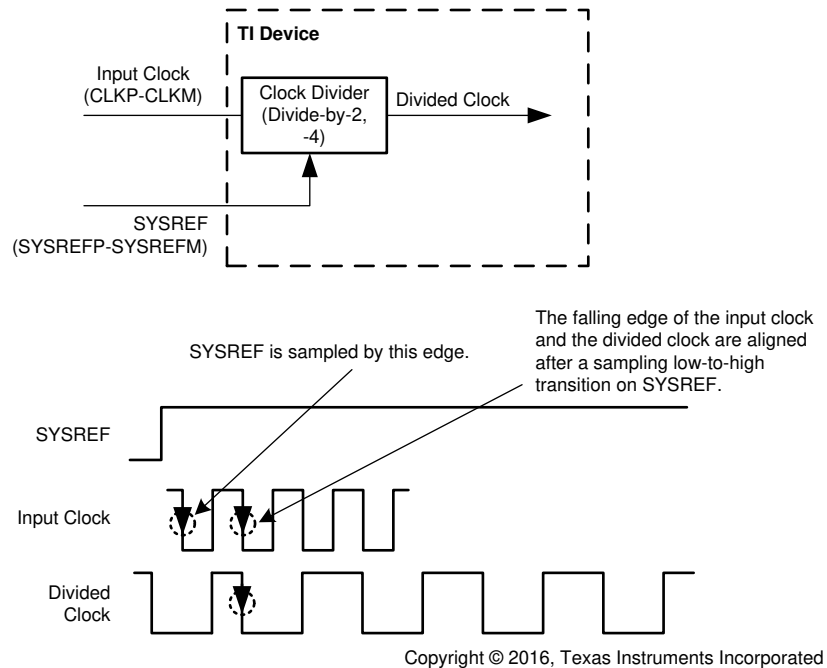
A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1- $\mu$ F capacitor, as shown in [Figure 8-5](#). However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.



**Figure 8-5. Single-Ended Clock Driving Circuit**

### 8.3.2.1 Using the SYSREF Input

The ADC344x has a SYSREF input pin that can be used when the clock-divider feature is used. A logic low-to-high transition on the SYSREF pin aligns the falling edge of the divided clock with the next falling edge of the input clock, essentially resetting the phase of the divided clock, as shown in Figure 8-6. When multiple ADC344x devices are onboard and the clock divider option is used, the phase of the divided clock among the devices may not be the same. The phase of the divided clock in each device can be synchronized to the common sampling clock by using the SYSREF pins. SYSREF can be applied as mono-shot or periodic waveform. When applied as periodic waveform, its period must be integer multiple of period of the divided clock. When not used, the SYSREFP and SYSREFM pins can be connected to AVDD and GND, respectively. Alternatively, the SYSREF buffer inside the device can be powered down using the PDN SYSREF register bit.



**Figure 8-6. Using SYSREF for Synchronization**

### 8.3.2.2 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 74 dB for a 12-bit ADC) and thermal noise limit SNR at low input frequencies, and clock jitter sets SNR for higher input frequencies.

$$\text{SNR}_{\text{ADC}}[\text{dBc}] = -20 \cdot \log \sqrt{\left( 10^{\frac{\text{SNR}_{\text{Quantization\_Noise}}}{20}} \right)^2 + \left( 10^{\frac{\text{SNR}_{\text{Thermal\_Noise}}}{20}} \right)^2 + \left( 10^{\frac{\text{SNR}_{\text{Jitter}}}{20}} \right)^2} \quad (1)$$

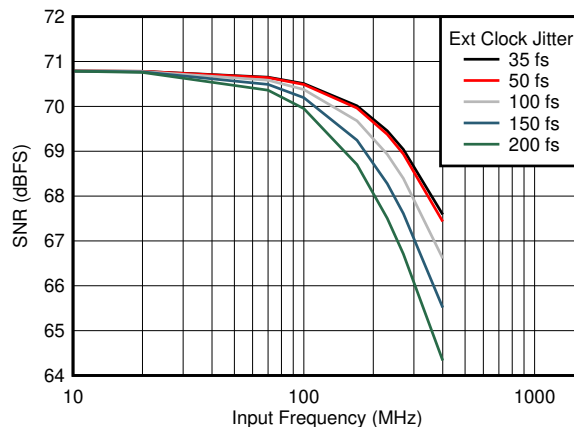
The SNR limitation resulting from sample clock jitter can be calculated with Equation 2.

$$\text{SNR}_{\text{Jitter}}[\text{dBc}] = -20 \cdot \log(2\pi \cdot f_{\text{in}} \cdot t_{\text{Jitter}}) \quad (2)$$

The total clock jitter ( $T_{\text{Jitter}}$ ) has two components: the internal aperture jitter (130 fs for the device), which is set by the noise of the clock input buffer, and the external clock.  $T_{\text{Jitter}}$  can be calculated with Equation 3.

$$t_{\text{Jitter}} = \sqrt{\left( t_{\text{Jitter,Ext.Clock\_Input}} \right)^2 + \left( t_{\text{Aperture\_ADC}} \right)^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input and a faster clock slew rate improves ADC aperture jitter. The devices have a typical thermal noise of 73.5 dBFS and an internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies. Figure 8-7 shows SNR (from 1 MHz offset leaving the 1/f flicker noise) for different jitter of clock driver.



**Figure 8-7. SNR vs Frequency for Different Clock Jitter**

### 8.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in Table 8-1. The output interface options are:

- One-wire, 1X frame clock, 12X serialization with the DDR bit clock and
- Two-wire, 1X frame clock, 6X serialization with the DDR bit clock.

**Table 8-1. Interface Rates**

| INTERFACE OPTIONS | SERIALIZATION | MAXIMUM RECOMMENDED SAMPLING FREQUENCY (MSPS) |     | BIT CLOCK FREQUENCY (MHz) | FRAME CLOCK FREQUENCY (MHz) | SERIAL DATA RATE PER WIRE (Mbps) |
|-------------------|---------------|---|-----|---------------------------|-----------------------------|----------------------------------|
|                   |               | MIN   | MAX |                           |                             |                                  |
| One-wire          | 12X           | 15 <sup>(1)</sup>                             |     | 90                        | 15                          | 180                              |
|                   |               |   | 65  | 390                       | 65                          | 780                              |
| Two-wire          | 6X            | 20 <sup>(1)</sup>                             |     | 60                        | 20                          | 120                              |
|                   |               |   | 125 | 375                       | 125                         | 750                              |

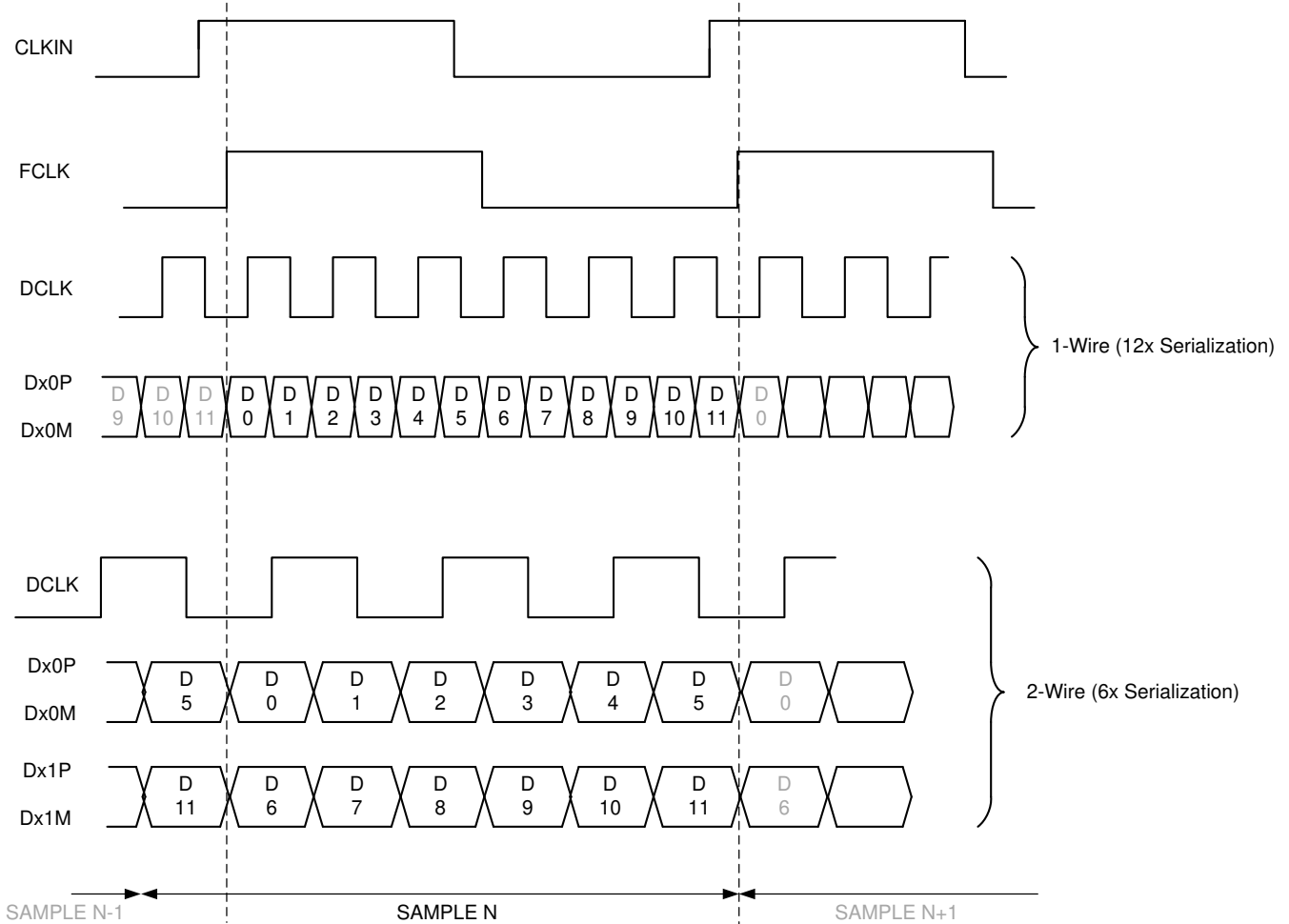
(1) Use the LOW SPEED ENABLE register bits for low speed operation; see Table 8-20.

#### 8.3.3.1 One-Wire Interface: 12X Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. The data rate is a 12X sample frequency (12X serialization).

### 8.3.3.2 Two-Wire Interface: 6X Serialization

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is a 6X sample frequency because six data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the six MSBs on Dx1P, Dx1M and the six LSBs on Dx0P, Dx0M, as shown in Figure 8-8.



**Figure 8-8. Output Timing Diagram**

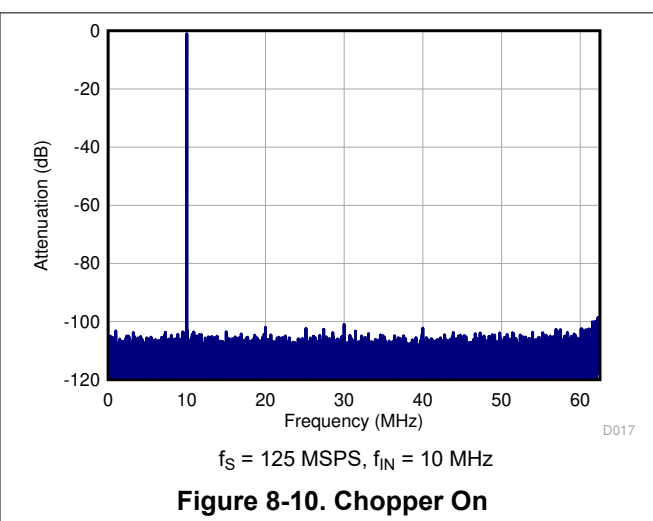
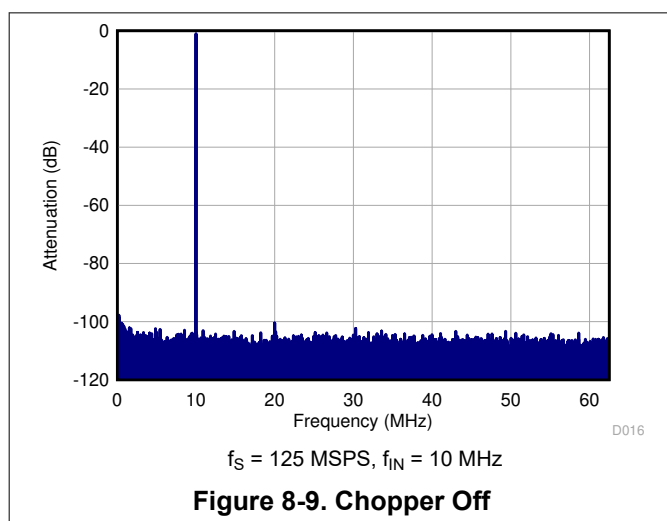
## 8.4 Device Functional Modes

### 8.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed for operation with a 125-MHz clock; the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

### 8.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the  $1/f$  noise from dc to  $f_S / 2$ . [Figure 8-9](#) shows the noise spectrum with the chopper off and [Figure 8-10](#) shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at  $f_S / 2$  that must be filtered out digitally.



### 8.4.3 Power-Down Control

The power-down functions of the ADC322x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see [register 15h](#)). The PDN pin can also be configured via the SPI to a global power-down or standby functionality, as shown in [Table 8-2](#).

**Table 8-2. Power-Down Modes**

| FUNCTION          | POWER CONSUMPTION (mW) | WAKE-UP TIME ( $\mu$ s) |
|-------------------|------------------------|-------------------------|
| Global power-down | 5                      | 85                      |
| Standby           | 81                     | 35                      |

### 8.4.3.1 Improving Wake-Up Time From Global Power-Down

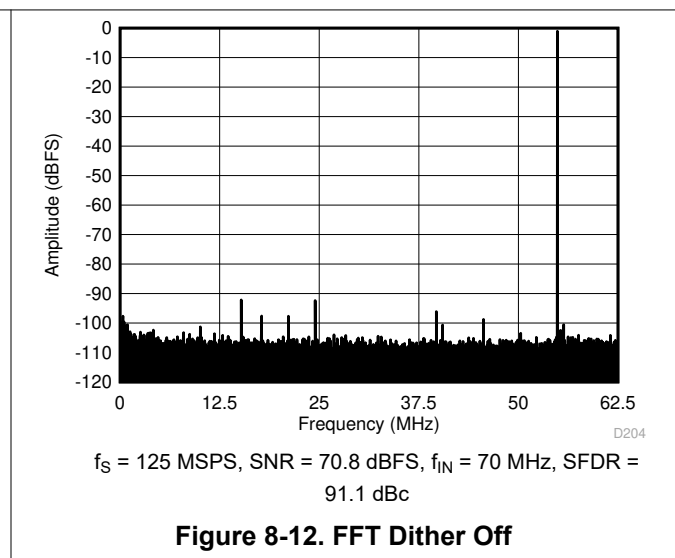
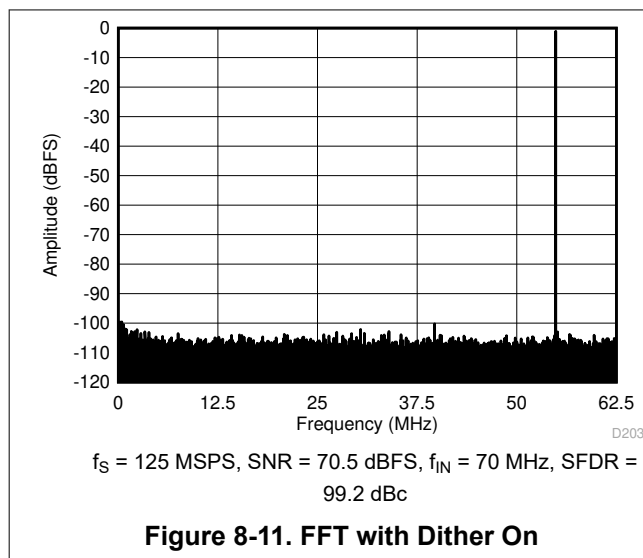
The device has an internal low-pass filter in the sampling clock path. This low-pass filter helps improve the aperture jitter of the device. However, in applications where input frequencies are < 200 MHz, noise from the aperture jitter does not dominate the overall SNR of the device. In such applications, the wake-up time from a global power-down can be reduced by bypassing the low-pass filter using the DIS CLK FILT register bit (write 80h to register address 70Ah). As shown in Table 8-3, setting the DIS CLK FILT bit improves the wake-up time from a global power-down from 85  $\mu$ s to 55  $\mu$ s.

**Table 8-3. Wake-Up Time From Global Power-Down**

| DIS CLK FILT REGISTER BIT | GLOBAL PDN REGISTER BIT | WAKE-UP TIME |     |         |
|---------------------------|-------------------------|--------------|-----|---------|
|                           |                         | TYP          | MAX | UNIT    |
| 0                         | 0→1→0                   | 85           | 140 | $\mu$ s |
| 1                         | 0→1→0                   | 55           | 81  | $\mu$ s |

### 8.4.4 Internal Dither Algorithm

The ADC322x use an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 8-11 and Figure 8-12 show the effect of using dither algorithms.



## 8.5 Programming

The ADC322x can be configured using a serial programming interface, as described in this section.

### 8.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

### 8.5.1.1 Register Initialization

After power-up, the internal registers **must be** initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 8-13. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

#### 8.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Figure 8-13 and Table 8-4 show the timing requirements for the serial register write operation.

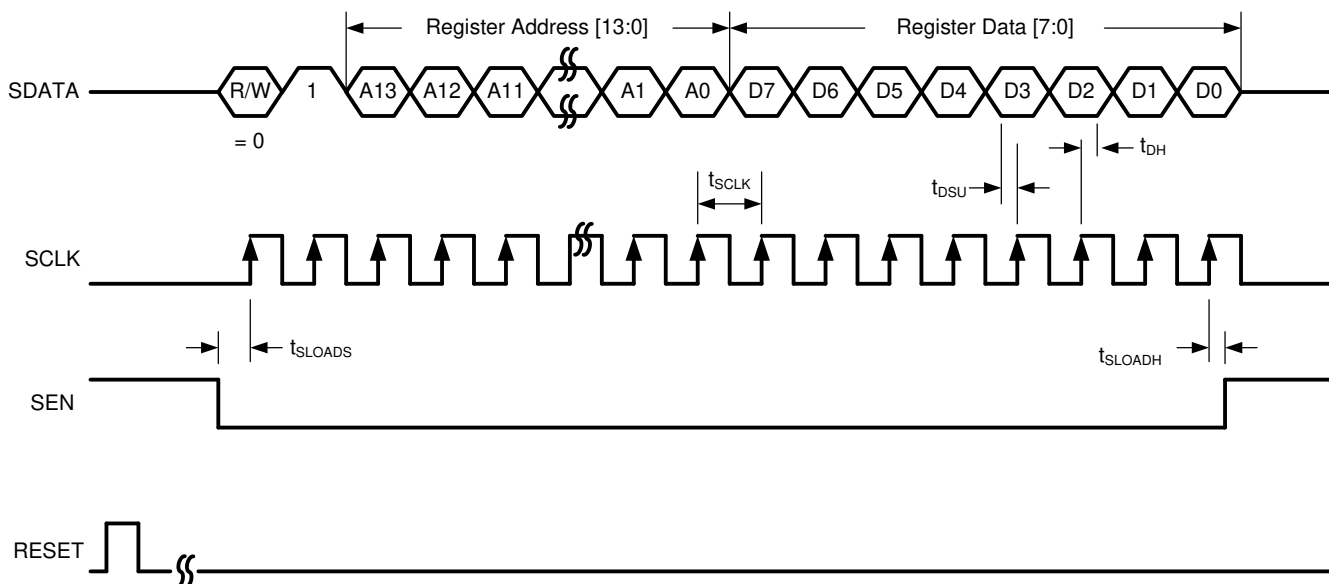


Figure 8-13. Serial Register Write Timing Diagram

Table 8-4. Serial Interface Timing<sup>(1)</sup>

|              |   | MIN  | TYP | MAX | UNIT |
|--------------|---|------|-----|-----|------|
| $f_{SCLK}$   | SCLK frequency (equal to $1 / t_{SCLK}$ ) | > dc |     | 20  | MHz  |
| $t_{SLOADS}$ | SEN to SCLK setup time                    | 25   |     |     | ns   |
| $t_{SLOADH}$ | SCLK to SEN hold time                     | 25   |     |     | ns   |
| $t_{DSU}$    | SDIO setup time                           | 25   |     |     | ns   |
| $t_{DH}$     | SDIO hold time                            | 25   |     |     | ns   |

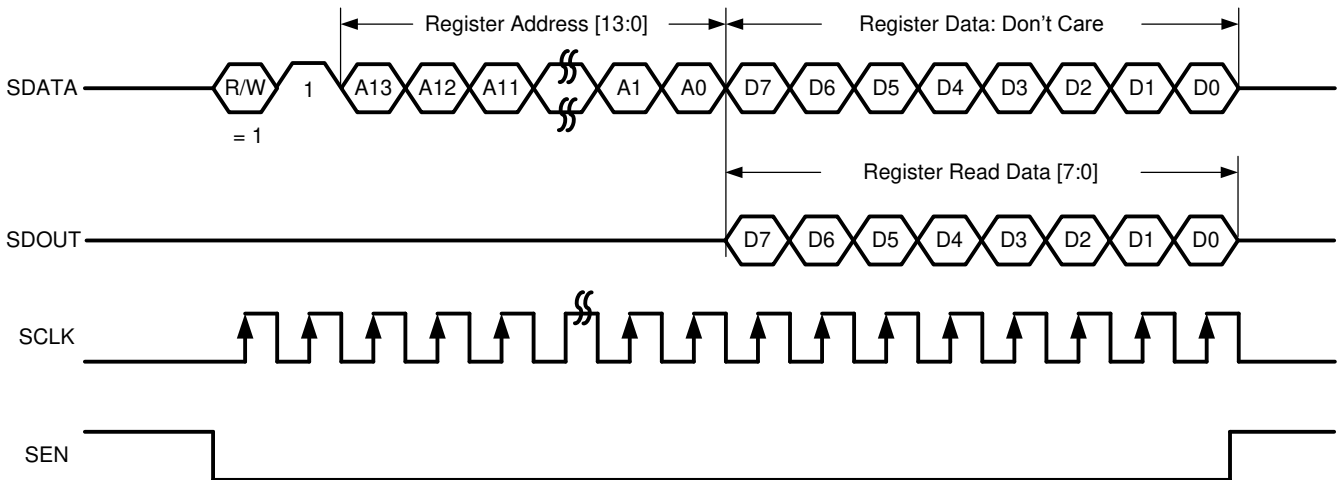
(1) Typical values are at 25°C, full temperature range is from  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , and  $AVDD = DVDD = 1.8\text{ V}$ , unless otherwise noted.

### 8.5.1.1.2 Serial Register Readout

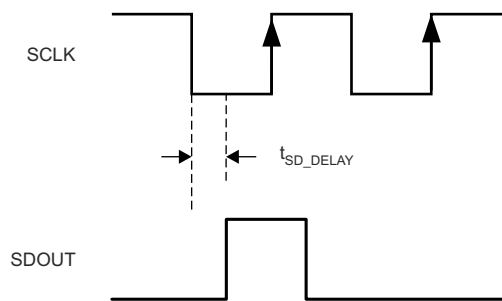
The device includes a mode where the contents of the internal registers can be read back using the SDOOUT pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A[13:0]) whose content must be read.
5. The device outputs the contents (D[7:0]) of the selected register on the SDOOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOOUT pin is in a high-impedance mode. If serial readout is not used, the SDOOUT pin must float. [Figure 8-14](#) shows a timing diagram of the serial register read operation. Data appear on the SDOOUT pin at the SCLK falling edge with an approximate delay ( $t_{SD\_DELAY}$ ) of 20 ns, as shown in [Figure 8-15](#).



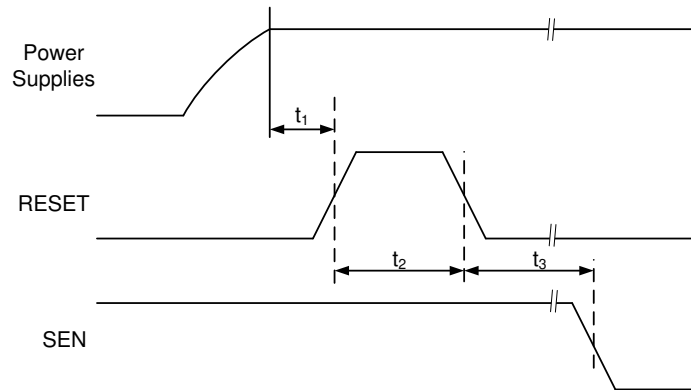
**Figure 8-14. Serial Register Read Timing Diagram**



**Figure 8-15. SDOOUT Timing Diagram**

### 8.5.2 Register Initialization through SPI

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 8-16 and Table 8-5.



**Figure 8-16. Initialization of Serial Registers after Power-Up**

**Table 8-5. Power-Up Timing**

|       |   | MIN | TYP | MAX | UNIT |
|-------|---|-----|-----|-----|------|
| $t_1$ | Power-on delay from power up to active high RESET pulse | 1   |     |     | ms   |
| $t_2$ | Reset pulse duration: active high RESET pulse duration  | 10  |     |     | ns   |
| $t_3$ | Register write delay from RESET disable to SEN active   | 100 |     |     | ns   |

If required, the serial interface registers may be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) to high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

## 8.6 Register Maps

**Table 8-6. Register Map Summary**

| REGISTER ADDRESS | REGISTER DATA        |         |              |   |                  |            |                    |                |
|------------------|----------------------|---------|--------------|---|------------------|------------|--------------------|----------------|
|                  | 7                    | 6       | 5            | 4 | 3                | 2          | 1                  | 0              |
| Register 01h     | 0                    | 0       | DIS DITH CHA |   | DIS DITH CHB     |            | 0                  | 0              |
| Register 03h     | 0                    | 0       | 0            | 0 | 0                | 0          | 0                  | ODD EVEN       |
| Register 04h     | 0                    | 0       | 0            | 0 | 0                | 0          | 0                  | FLIP WIRE      |
| Register 05h     | 0                    | 0       | 0            | 0 | 0                | 0          | 0                  | 1W-2W          |
| Register 06h     | 0                    | 0       | 0            | 0 | 0                | 0          | TEST PATTERN EN    | RESET          |
| Register 07h     | 0                    | 0       | 0            | 0 | 0                | 0          | 0                  | OVR ON LSB     |
| Register 09h     | 0                    | 0       | 0            | 0 | 0                | 0          | ALIGN TEST PATTERN | DATA FORMAT    |
| Register 0Ah     | 0                    | 0       | 0            | 0 | CHA TEST PATTERN |            |                    |                |
| Register 0Bh     | CHB TEST PATTERN     |         |              | 0 | 0                | 0          | 0                  | 0              |
| Register 0Eh     | CUSTOM PATTERN[11:4] |         |              |   |                  |            |                    |                |
| Register 0Fh     | CUSTOM PATTERN[3:0]  |         |              |   | 0                | 0          | 0                  | 0              |
| Register 13h     | 0                    | 0       | 0            | 0 | 0                | 0          | LOW SPEED ENABLE   |                |
| Register 15h     | 0                    | CHA PDN | CHB PDN      | 0 | STANDBY          | GLOBAL PDN | 0                  | CONFIG PDN PIN |
| Register 25h     | LVDS SWING           |         |              |   |                  |            |                    |                |
| Register 27h     | CLK DIV              |         | 0            | 0 | 0                | 0          | 0                  | 0              |
| Register 41Dh    | 0                    | 0       | 0            | 0 | 0                | 0          | HIGH IF MODE0      | 0              |
| Register 422h    | 0                    | 0       | 0            | 0 | 0                | 0          | DIS CHOP CHA       | 0              |
| Register 434h    | 0                    | 0       | DIS DITH CHA | 0 | DIS DITH CHA     | 0          | 0                  | 0              |
| Register 439h    | 0                    | 0       | 0            | 0 | SP1 CHA          | 0          | 0                  | 0              |
| Register 51Dh    | 0                    | 0       | 0            | 0 | 0                | 0          | HIGH IF MODE1      | 0              |
| Register 522h    | 0                    | 0       | 0            | 0 | 0                | 0          | DIS CHOP CHB       | 0              |
| Register 534h    | 0                    | 0       | DIS DITH CHB | 0 | DIS DITH CHB     | 0          | 0                  | 0              |
| Register 539h    | 0                    | 0       | 0            | 0 | SP1 CHB          | 0          | 0                  | 0              |
| Register 608h    | HIGH IF MODE[3:2]    |         | 0            | 0 | 0                | 0          | 0                  | 0              |
| Register 70Ah    | DIS CLK FILT         | 0       | 0            | 0 | 0                | 0          | 0                  | PDN SYSREF     |

## 8.6.1 Summary of Special Mode Registers

Table 8-7 lists the location, value, and functions of special mode registers in the device.

**Table 8-7. Special Modes Summary**

| MODE            | REGISTER SETTINGS   | DESCRIPTION                                     |
|-----------------|---|---|
| Special modes   | Registers 439h (bit 3) and 539h (bit 3)                               | Always set these bits high for best performance |
| Disable dither  | Registers 1h (bits 5-2), 434h (bits 5 and 3), and 534h (bits 5 and 3) | Disable dither to improve SNR                   |
| Disable chopper | Registers 422h (bit 1) and 522h (bit 1)                               | Disable chopper to shift 1/f noise floor at dc  |
| High IF modes   | Registers 41Dh (bit 1), 51Dh (bit 1), and 608h (bits 7-6)             | Improves HD3 for IF > 100 MHz                   |

## 8.6.2 Serial Register Description

### 8.6.2.1 Register 01h

**Figure 8-17. Register 01h**

| 7    | 6    | 5            | 4 | 3            | 2 | 1    | 0    |
|------|------|--------------|---|--------------|---|------|------|
| 0    | 0    | DIS DITH CHA |   | DIS DITH CHB |   | 0    | 0    |
| W-0h | W-0h | R/W-0h       |   | R/W-0h       |   | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-8. Register 01h Description**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7-6 | 0            | W    | 0h    | Must write 0  |
| 5-4 | DIS DITH CHA | R/W  | 0h    | These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz. |
| 3-2 | DIS DITH CHB | R/W  | 0h    | These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz. |
| 1-0 | 0            | W    | 0h    | Must write 0  |

### 8.6.2.2 Register 03h

**Figure 8-18. Register 03h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0        |
|------|------|------|------|------|------|------|----------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | ODD EVEN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h   |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-9. Register 03h Description**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7-1 | 0        | W    | 0h    | Must write 0   |
| 0   | ODD EVEN | R/W  | 0h    | This bit selects the bit sequence on the output wires (in 2-wire mode only). 0 = Bits 0, 1, and 2 appear on wire 0; bits 7, 8, and 9 appear on wire 1 1 = Bits 0, 2, and 4 appear on wire 0; bits 1, 3, and 5 appear on wire 1 |

### 8.6.2.3 Register 04h

**Figure 8-19. Register 04h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0         |
|------|------|------|------|------|------|------|-----------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | FLIP WIRE |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h    |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-10. Register 04h Description**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7-1 | 0         | W    | 0h    | Must write 0   |
| 0   | FLIP WIRE | R/W  | 0h    | This bit flips the data on the output wires. Valid only in two wire configuration.<br>0 = Default<br>1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa. |

### 8.6.2.4 Register 05h

**Figure 8-20. Register 05h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0      |
|------|------|------|------|------|------|------|--------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1W-2W  |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-11. Register 05h Description**

| Bit | Field | Type | Reset | Description   |
|-----|-------|------|-------|---|
| 7-1 | 0     | W    | 0h    | Must write 0  |
| 0   | 1W-2W | R/W  | 0h    | This bit transmits output data on either one or two wires.<br>0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M)<br>1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended $f_s$ is less than 62.5 MSPS. |

### 8.6.2.5 Register 06h

**Figure 8-21. Register 06h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1               | 0     |
|------|------|------|------|------|------|-----------------|-------|
| 0    | 0    | 0    | 0    | 0    | 0    | TEST PATTERN EN | RESET |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h          | W-0h  |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-12. Register 06h Description**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7-2 | 0               | W    | 0h    | Must write 0   |
| 1   | TEST PATTERN EN | R/W  | 0h    | This bit enables test pattern selection for the digital outputs.<br>0 = Normal output<br>1 = Test pattern output enabled |
| 0   | RESET           | W    | 0h    | This bit applies a software reset.<br>This bit resets all internal registers to the default values and self-clears to 0. |

### 8.6.2.6 Register 07h

**Figure 8-22. Register 07h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0          |
|------|------|------|------|------|------|------|------------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | OVR ON LSB |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h     |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-13. Register 07h Description**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 7-1 | 0          | W    | 0h    | Must write 0  |
| 0   | OVR ON LSB | R/W  | 0h    | This bit provides the overrange (OVR) information on the LSB bits.<br>0 = Output data bit 0 functions as the LSB of the 12-bit data<br>1 = Output data bit 0 carries the OVR information. |

### 8.6.2.7 Register 09h

**Figure 8-23. Register 09h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1                  | 0           |
|------|------|------|------|------|------|--------------------|-------------|
| 0    | 0    | 0    | 0    | 0    | 0    | ALIGN TEST PATTERN | DATA FORMAT |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h             | R/W-0h      |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-14. Register 09h Description**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7-2 | 0                  | W    | 0h    | Must write 0  |
| 1   | ALIGN TEST PATTERN | R/W  | 0h    | This bit aligns the test patterns across the outputs of both channels.<br>0 = Test patterns of both channels are free running<br>1 = Test patterns of both channels are aligned |
| 0   | DATA FORMAT        | R/W  | 0h    | This bit programs the digital output data format.<br>0 = Twos complement<br>1 = Offset binary   |

### 8.6.2.8 Register 0Ah

**Figure 8-24. Register 0Ah**

|      |      |      |      |                  |   |   |   |
|------|------|------|------|------------------|---|---|---|
| 7    | 6    | 5    | 4    | 3                | 2 | 1 | 0 |
| 0    | 0    | 0    | 0    | CHA TEST PATTERN |   |   |   |
| W-0h | W-0h | W-0h | W-0h | R/W-0h           |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-15. Register 0Ah Description**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7-4 | 0                | W    | 0h    | Must write 0   |
| 3-0 | CHA TEST PATTERN | R/W  | 0h    | These bits control the test pattern for channel A after the TEST PATTERN EN bit is set.<br>0000 = Normal operation<br>0001 = All 0's<br>0010 = All 1's<br>0011 = Toggle pattern: data alternate between 101010101010 and 010101010101<br>0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095<br>0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits<br>0110 = Deskew pattern: data are AAAh<br>1000 = PRBS pattern: data are a sequence of pseudo random numbers<br>1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599<br>Others = Do not use |

### 8.6.2.9 Register 0Bh

**Figure 8-25. Register 0Bh**

|                  |   |   |   |      |      |      |      |
|------------------|---|---|---|------|------|------|------|
| 7                | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
| CHB TEST PATTERN |   |   |   | 0    | 0    | 0    | 0    |
| R/W-0h           |   |   |   | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-16. Register 0Bh Description**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7-4 | CHB TEST PATTERN | R/W  | 0h    | These bits control the test pattern for channel B after the TEST PATTERN EN bit is set.<br>0000 = Normal operation<br>0001 = All 0's<br>0010 = All 1's<br>0011 = Toggle pattern: data alternate between 101010101010 and 010101010101<br>0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095<br>0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits<br>0110 = Deskew pattern: data are AAAh<br>1000 = PRBS pattern: data are a sequence of pseudo random numbers<br>1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599<br>Others = Do not use |
| 3-0 | 0                | W    | 0h    | Must write 0   |

### 8.6.2.10 Register 0Eh

**Figure 8-26. Register 0Eh**

|                      |   |   |   |   |   |   |   |
|----------------------|---|---|---|---|---|---|---|
| 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM PATTERN[11:4] |   |   |   |   |   |   |   |
| R/W-0h               |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 8-17. Register 0Eh Description**

| Bit | Field                | Type | Reset | Description  |
|-----|----------------------|------|-------|--|
| 7-0 | CUSTOM PATTERN[11:4] | R/W  | 0h    | These bits set the 12-bit custom pattern (bits 11-4) for all channels. |

### 8.6.2.11 Register 0Fh

**Figure 8-27. Register 0Fh**

|                     |   |   |   |      |      |      |      |
|---------------------|---|---|---|------|------|------|------|
| 7                   | 6 | 5 | 4 | 3    | 2    | 1    | 0    |
| CUSTOM PATTERN[3:0] |   |   |   | 0    | 0    | 0    | 0    |
| R/W-0h              |   |   |   | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-18. Register 0Fh Description**

| Bit | Field               | Type | Reset | Description   |
|-----|---------------------|------|-------|---|
| 7-4 | CUSTOM PATTERN[3:0] | R/W  | 0h    | These bits set the 12-bit custom pattern (bits 3-0) for all channels. |
| 3-0 | 0                   | W    | 0h    | Must write 0  |

### 8.6.2.12 Register 13h

**Figure 8-28. Register 13h**

|      |        |        |      |        |        |                  |        |
|------|--------|--------|------|--------|--------|------------------|--------|
| 7    | 6      | 5      | 4    | 3      | 2      | 1                | 0      |
| 0    | 0      | 0      | 0    | 0      | 0      | LOW SPEED ENABLE |        |
| W-0h | R/W-0h | R/W-0h | W-0h | R/W-0h | R/W-0h | W-0h             | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-19. Register 13h Description**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7-2 | 0                | W    | 0h    | Must write 0   |
| 1-0 | LOW SPEED ENABLE | R/W  | 0h    | Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per <a href="#">Table 8-20</a> . |

**Table 8-20. LOW SPEED ENABLE Register Bit Settings Across  $f_s$**

| $f_s$ (MSPS) |     | REGISTER BIT LOW SPEED ENABLE |               |
|--------------|-----|-------------------------------|---------------|
| MIN          | MAX | 1-WIRE MODE                   | 2-WIRE MODE   |
| 25           | 125 | 00                            | 00            |
| 20           | 25  | 10                            | 11            |
| 15           | 20  | 10                            | Not supported |

### 8.6.2.13 Register 15h

**Figure 8-29. Register 15h**

| 7    | 6       | 5       | 4    | 3       | 2          | 1    | 0              |
|------|---------|---------|------|---------|------------|------|----------------|
| 0    | CHA PDN | CHB PDN | 0    | STANDBY | GLOBAL PDN | 0    | CONFIG PDN PIN |
| W-0h | R/W-0h  | R/W-0h  | W-0h | R/W-0h  | R/W-0h     | W-0h | R/W-0h         |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-21. Register 15h Description**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 7   | 0              | W    | 0h    | Must write 0  |
| 6   | CHA PDN        | R/W  | 0h    | 0 = Normal operation<br>1 = Power-down channel A  |
| 5   | CHB PDN        | R/W  | 0h    | 0 = Normal operation<br>1 = Power-down channel B  |
| 4   | 0              | W    | 0h    | Must write 0  |
| 3   | STANDBY        | R/W  | 0h    | The ADCs of both channels enter standby.<br>0 = Normal operation<br>1 = Standby   |
| 2   | GLOBAL PDN     | R/W  | 0h    | 0 = Normal operation<br>1 = Global power-down   |
| 1   | 0              | W    | 0h    | Must write 0  |
| 0   | CONFIG PDN PIN | R/W  | 0h    | This bit configures the PDN pin as either a global power-down or standby pin.<br>0 = Logic high voltage on the PDN pin sends the device into global power-down<br>1 = Logic high voltage on the PDN pin sends the device into standby |

### 8.6.2.14 Register 25h

**Figure 8-30. Register 25h**

| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| LVDS SWING |   |   |   |   |   |   |   |
| R/W-0h     |   |   |   |   |   |   |   |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 8-22. Register 25h Description**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7-0 | LVDS SWING | R/W  | 0h    | These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock). For details see <a href="#">Table 8-23</a> . |

**Table 8-23. LVDS Output Swing**

| BITS 7-4 | BITS 3-0 | LVDS OUTPUT SWING         |
|----------|----------|---------------------------|
| 0h       | 0h       | Default ( $\pm 425$ mV)   |
| Dh       | 9h       | Swing reduces by 50 mV    |
| Eh       | Ah       | Swing reduces by 100 mV   |
| Fh       | Dh       | Swing reduces by 300 mV   |
| Ch       | Eh       | Swing increases by 100 mV |
| Others   | Others   | Do not use                |

### 8.6.2.15 Register 27h

**Figure 8-31. Register 27h**

| 7       | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|
| CLK DIV | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W-0h  | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-24. Register 27h Description**

| Bit | Field   | Type | Reset | Description   |
|-----|---------|------|-------|---|
| 7-6 | CLK DIV | R/W  | 0h    | These bits set the internal clock divider for the input sampling clock.<br>00 = Divide-by-1<br>01 = Divide-by-1<br>10 = Divide-by-2<br>11 = Divide-by-4 |
| 5-0 | 0       | W    | 0h    | Must write 0  |

### 8.6.2.16 Register 41Dh

**Figure 8-32. Register 41Dh**

| 7    | 6    | 5    | 4    | 3    | 2    | 1             | 0    |
|------|------|------|------|------|------|---------------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | HIGH IF MODE0 | 0    |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h        | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-25. Register 41Dh Description**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7-2 | 0             | W    | 0h    | Must write 0  |
| 1   | HIGH IF MODE0 | R/W  | 0h    | This bit improves HD3 for IF > 100 MHz.<br>0 = Normal operation<br>For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 0   | 0             | W    | 0h    | Must write 0  |

### 8.6.2.17 Register 422h

**Figure 8-33. Register 422h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1            | 0    |
|------|------|------|------|------|------|--------------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | DIS CHOP CHA | 0    |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h       | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-26. Register 422h Description**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-2 | 0            | W    | 0h    | Must write 0   |
| 1   | DIS CHOP CHA | R/W  | 0h    | Disable chopper.<br>Set this bit to shift a 1/f noise floor at dc.<br>0 = 1/f noise floor is centered at $f_S / 2$ (default)<br>1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc |
| 0   | 0            | W    | 0h    | Must write 0   |

### 8.6.2.18 Register 434h

**Figure 8-34. Register 434h**

| 7    | 6    | 5            | 4    | 3            | 2    | 1    | 0    |
|------|------|--------------|------|--------------|------|------|------|
| 0    | 0    | DIS DITH CHA | 0    | DIS DITH CHA | 0    | 0    | 0    |
| W-0h | W-0h | R/W-0h       | W-0h | R/W-0h       | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-27. Register 434h Description**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7-6 | 0            | W    | 0h    | Must write 0  |
| 5   | DIS DITH CHA | R/W  | 0h    | Set this bit with bits 5 and 4 of register 01h.<br>00 = Default<br>11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 4   | 0            | W    | 0h    | Must write 0  |
| 3   | DIS DITH CHA | R/W  | 0h    | Set this bit with bits 5 and 4 of register 01h.<br>00 = Default<br>11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 2-0 | 0            | W    | 0h    | Must write 0  |

### 8.6.2.19 Register 439h

**Figure 8-35. Register 439h**

| 7    | 6    | 5    | 4    | 3       | 2    | 1    | 0    |
|------|------|------|------|---------|------|------|------|
| 0    | 0    | 0    | 0    | SP1 CHA | 0    | 0    | 0    |
| W-0h | W-0h | W-0h | W-0h | R/W-0h  | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-28. Register 439h Description**

| Bit | Field   | Type | Reset | Description  |
|-----|---------|------|-------|--|
| 7-4 | 0       | W    | 0h    | Must write 0   |
| 3   | SP1 CHA | R/W  | 0h    | Special mode for best performance on channel A.<br>Always write 1 after reset. |
| 2-0 | 0       | W    | 0h    | Must write 0   |

### 8.6.2.20 Register 51Dh

**Figure 8-36. Register 51Dh**

| 7    | 6    | 5    | 4    | 3    | 2    | 1             | 0    |
|------|------|------|------|------|------|---------------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | HIGH IF MODE1 | 0    |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h        | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-29. Register 51Dh Description**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7-2 | 0             | W    | 0h    | Must write 0  |
| 1   | HIGH IF MODE1 | R/W  | 0h    | This bit improves HD3 for IF > 100 MHz.<br>0 = Normal operation<br>For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 0   | 0             | W    | 0h    | Must write 0  |

### 8.6.2.21 Register 522h

**Figure 8-37. Register 522h**

| 7    | 6    | 5    | 4    | 3    | 2    | 1            | 0    |
|------|------|------|------|------|------|--------------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | DIS CHOP CHB | 0    |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h       | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-30. Register 522h Description**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-2 | 0            | W    | 0h    | Must write 0   |
| 1   | DIS CHOP CHB | R/W  | 0h    | Disable chopper.<br>Set this bit to shift a 1/f noise floor at dc.<br>0 = 1/f noise floor is centered at $f_s / 2$ (default)<br>1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc |
| 0   | 0            | W    | 0h    | Must write 0   |

### 8.6.2.22 Register 534h

**Figure 8-38. Register 534h**

| 7    | 6    | 5            | 4    | 3            | 2    | 1    | 0    |
|------|------|--------------|------|--------------|------|------|------|
| 0    | 0    | DIS DITH CHA | 0    | DIS DITH CHA | 0    | 0    | 0    |
| W-0h | W-0h | R/W-0h       | W-0h | R/W-0h       | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-31. Register 534h Description**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7-6 | 0            | W    | 0h    | Must write 0  |
| 5   | DIS DITH CHA | R/W  | 0h    | Set this bit with bits 3 and 2 of register 01h.<br>00 = Default<br>11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 4   | 0            | W    | 0h    | Must write 0  |
| 3   | DIS DITH CHA | R/W  | 0h    | Set this bit with bits 3 and 2 of register 01h.<br>00 = Default<br>11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 2-0 | 0            | W    | 0h    | Must write 0  |

### 8.6.2.23 Register 539h

**Figure 8-39. Register 539h**

| 7    | 6    | 5    | 4    | 3       | 2    | 1    | 0    |
|------|------|------|------|---------|------|------|------|
| 0    | 0    | 0    | 0    | SP1 CHB | 0    | 0    | 0    |
| W-0h | W-0h | W-0h | W-0h | R/W-0h  | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-32. Register 539h Description**

| Bit | Field   | Type | Reset | Description  |
|-----|---------|------|-------|--|
| 7-4 | 0       | W    | 0h    | Must write 0   |
| 3   | SP1 CHB | R/W  | 0h    | Special mode for best performance on channel B.<br>Always write 1 after reset. |

**Table 8-32. Register 539h Description (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
| 0   | 0     | W    | 0h    | Must write 0 |

### 8.6.2.24 Register 608h

**Figure 8-40. Register 608h**

| 7                 | 6 | 5    | 4    | 3    | 2    | 1    | 0    |
|-------------------|---|------|------|------|------|------|------|
| HIGH IF MODE[3:2] |   | 0    | 0    | 0    | 0    | 0    | 0    |
| R/W-0h            |   | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-33. Register 608h Description**

| Bit | Field             | Type | Reset | Description   |
|-----|-------------------|------|-------|---|
| 7-6 | HIGH IF MODE[3:2] | R/W  | 0h    | This bit improves HD3 for IF > 100 MHz.<br>0 = Normal operation<br>For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 5-0 | 0                 | W    | 0h    | Must write 0  |

### 8.6.2.25 Register 70Ah

**Figure 8-41. Register 70Ah**

| 7            | 6    | 5    | 4    | 3    | 2    | 1    | 0          |
|--------------|------|------|------|------|------|------|------------|
| DIS CLK FILT | 0    | 0    | 0    | 0    | 0    | 0    | PDN SYSREF |
| R/W-0h       | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h     |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

**Table 8-34. Register 70Ah Description**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7   | DIS CLK FILT | R/W  | 0h    | Set this bit to improve wake-up time from global power-down mode; see the <a href="#">Section 8.4.3.1</a> section for details.  |
| 6-1 | 0            | W    | 0h    | Must write 0  |
| 0   | PDN SYSREF   | R/W  | 0h    | If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit.<br>0 = Normal operation<br>1 = Powers down the SYSREF buffer |

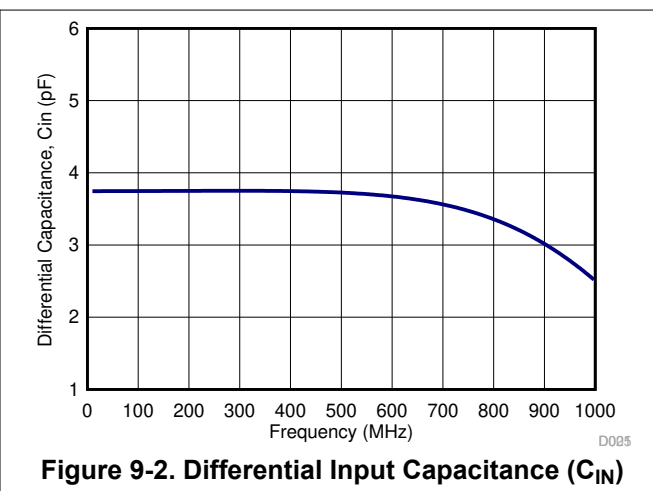
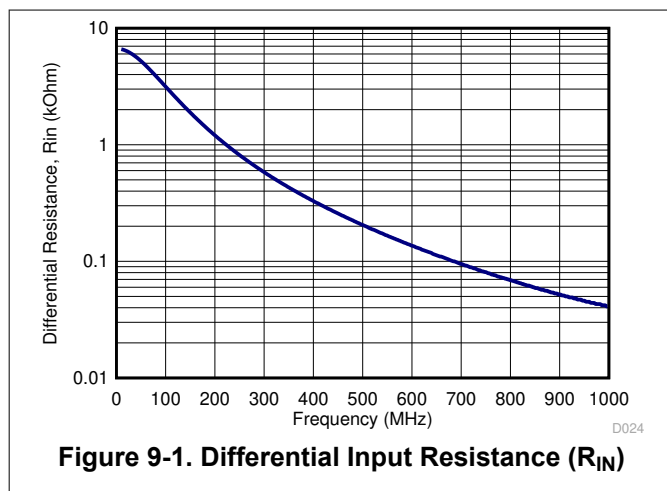
## 9 Applications and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at the ADC inputs. When designing the dc-driving circuits, the ADC input impedance must be considered. [Figure 9-1](#) and [Figure 9-2](#) show the impedance ( $Z_{in} = R_{in} \parallel C_{in}$ ) across the ADC input pins.



## 9.2 Typical Applications

### 9.2.1 Driving Circuit Design: Low Input Frequencies

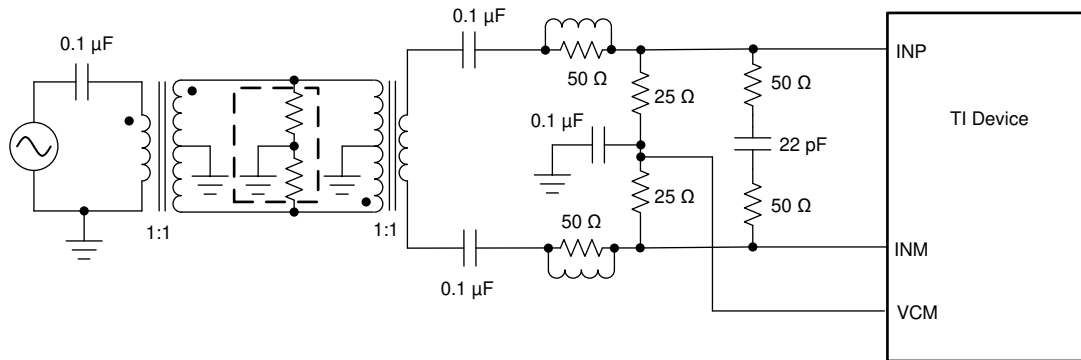


Figure 9-3. Driving Circuit for Low Input Frequencies

#### 9.2.1.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the affect of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

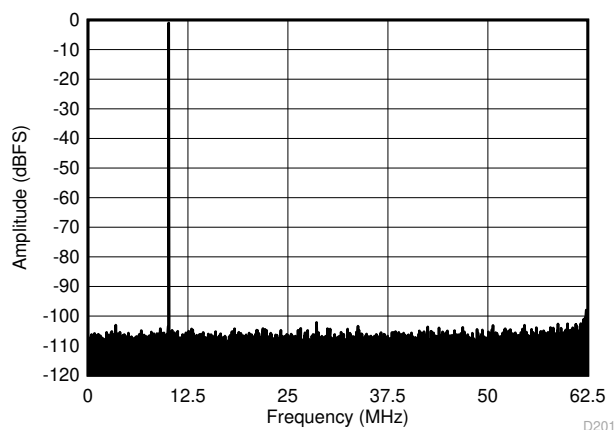
#### 9.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is shown in [Figure 9-3](#). This circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH); this combination helps absorb the sampling glitches.

To improve phase and amplitude balance of first transformer, the termination resistors can be split between two transformers. For example, 25-Ω to 25-Ω termination across the secondary winding of the second transformer can be changed to 50-Ω to 50-Ω termination and another 50-Ω to 50-Ω resistor can be placed inside the dashed box between the transformers in [Figure 9-3](#).

#### 9.2.1.3 Application Curve

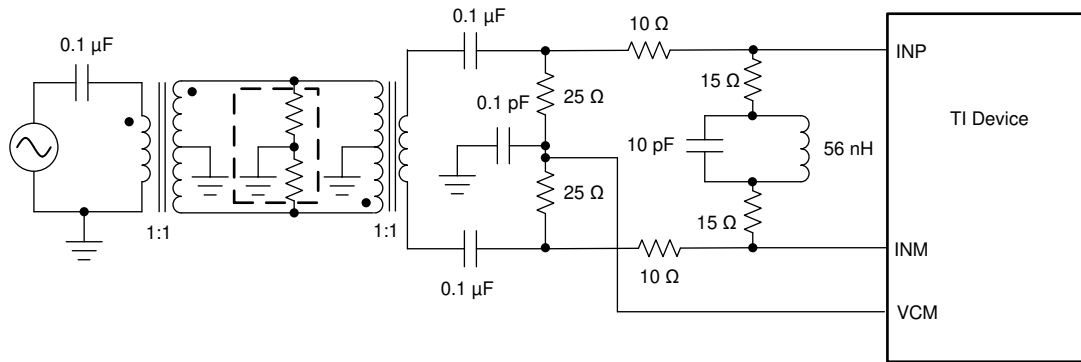
[Figure 9-4](#) shows the performance obtained by using the circuit shown in [Figure 9-3](#).



$f_S = 125$  MSPS, SNR = 70.6 dBFS,  $f_{IN} = 10$  MHz, SFDR = 101.1 dBc

Figure 9-4. Performance FFT at 10 MHz (Low Input Frequency)

## 9.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz



**Figure 9-5. Driving Circuit for Mid-Range Input Frequencies ( $100 \text{ MHz} < f_{\text{IN}} < 230 \text{ MHz}$ )**

### 9.2.2.1 Design Requirements

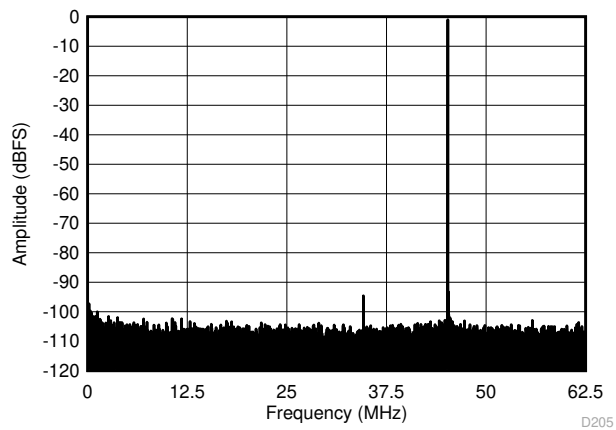
See the [Section 9.2.1.1](#) section for further details.

### 9.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in [Figure 9-5](#).

### 9.2.2.3 Application Curve

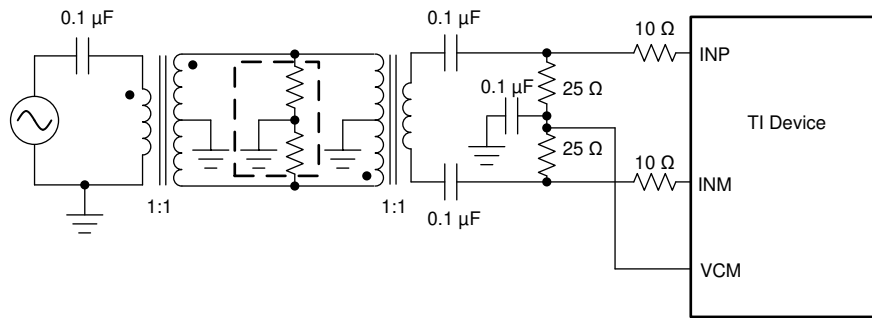
[Figure 9-6](#) shows the performance obtained by using the circuit shown in [Figure 9-5](#).



$f_s = 125 \text{ MSPS}$ ,  $\text{SNR} = 70 \text{ dBFS}$ ,  $f_{\text{IN}} = 170 \text{ MHz}$ ,  $\text{SFDR} = 93.6 \text{ dBc}$

**Figure 9-6. Performance FFT at 170 MHz (Mid Input Frequency)**

### 9.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz



**Figure 9-7. Driving Circuit for High Input Frequencies ( $f_{IN} > 230$  MHz)**

#### 9.2.3.1 Design Requirements

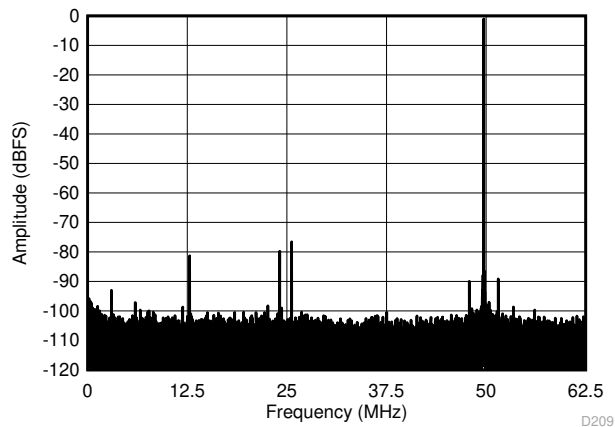
See the [Section 9.2.1.1](#) section for further details.

#### 9.2.3.2 Detailed Design Procedure

For high input frequencies ( $> 230$  MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of  $10\ \Omega$  can be used as shown in [Figure 9-7](#).

#### 9.2.3.3 Application Curve

[Figure 9-8](#) shows the performance obtained by using the circuit shown in [Figure 9-7](#).



$f_S = 125$  MSPS, SNR = 67.4 dBFS,  $f_{IN} = 450$  MHz, SFDR = 75.5 dBc

**Figure 9-8. Performance FFT at 450 MHz (High Input Frequency)**

### 9.3 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

## 9.4 Layout

### 9.4.1 Layout Guidelines

The ADC322x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in [Figure 9-9](#). Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to make sure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of [Figure 9-9](#) as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of [Figure 9-9](#) as much as possible.
3. Keep digital outputs away from analog inputs. When these digital outputs exit the pin out, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver (such as an FPGA or an ASIC) must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), a 0.1- $\mu$ F decoupling capacitor must be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- $\mu$ F, 1- $\mu$ F, and 0.1- $\mu$ F capacitors can be kept close to the supply source.

### 9.4.2 Layout Example

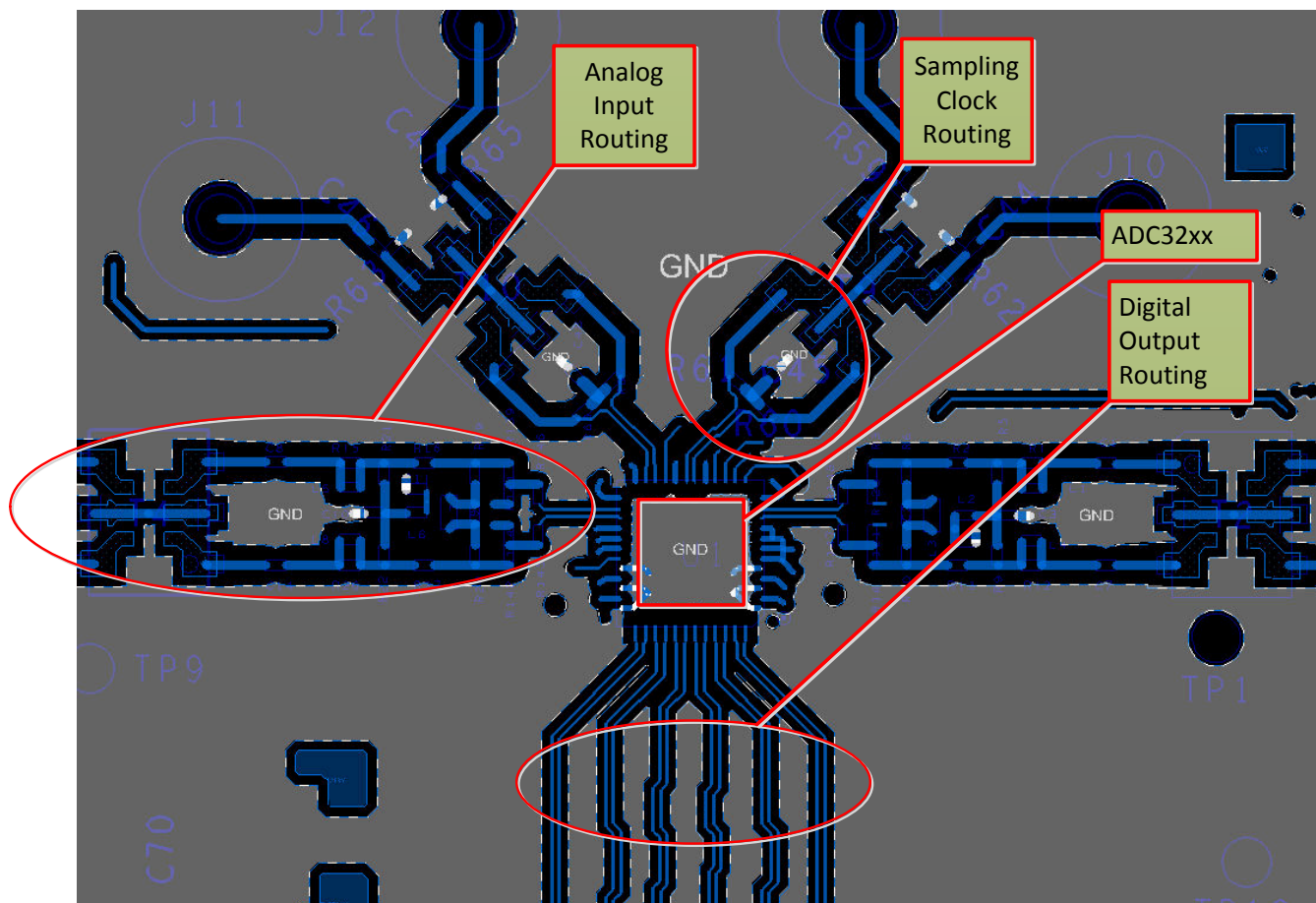


Figure 9-9. Typical Layout of the ADC322x Board

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

PowerPAD™ is a trademark of Texas Instruments, Inc.

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADC3221IRGZR     | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3221                  | <a href="#">Samples</a> |
| ADC3221IRGZT     | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3221                  | <a href="#">Samples</a> |
| ADC3222IRGZR     | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3222                  | <a href="#">Samples</a> |
| ADC3222IRGZT     | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3222                  | <a href="#">Samples</a> |
| ADC3223IRGZR     | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3223                  | <a href="#">Samples</a> |
| ADC3223IRGZT     | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3223                  | <a href="#">Samples</a> |
| ADC3224IRGZR     | ACTIVE        | VQFN         | RGZ             | 48   | 2500        | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3224                  | <a href="#">Samples</a> |
| ADC3224IRGZT     | ACTIVE        | VQFN         | RGZ             | 48   | 250         | RoHS & Green    | NIPDAUAG                             | Level-3-260C-168 HR  | -40 to 85    | AZ3224                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

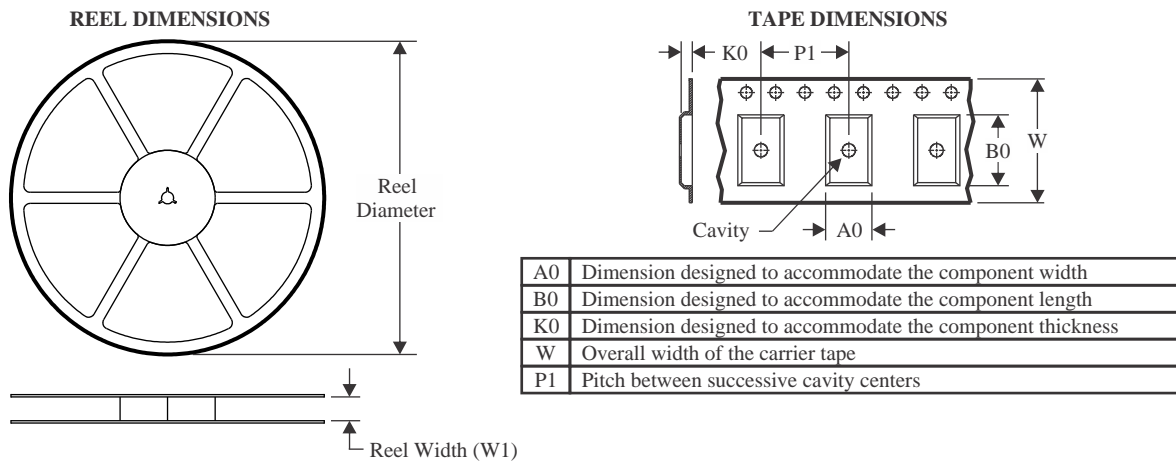
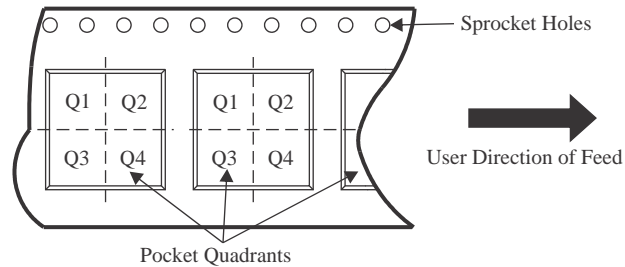
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

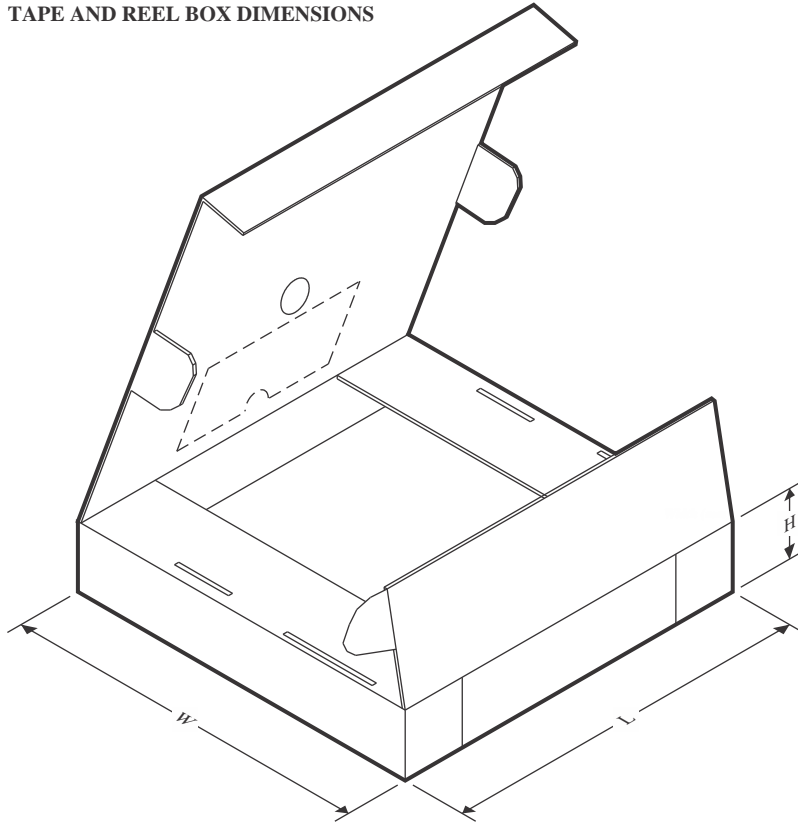
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADC3221IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADC3222IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADC3223IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADC3224IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADC3221IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |
| ADC3222IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |
| ADC3223IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |
| ADC3224IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |

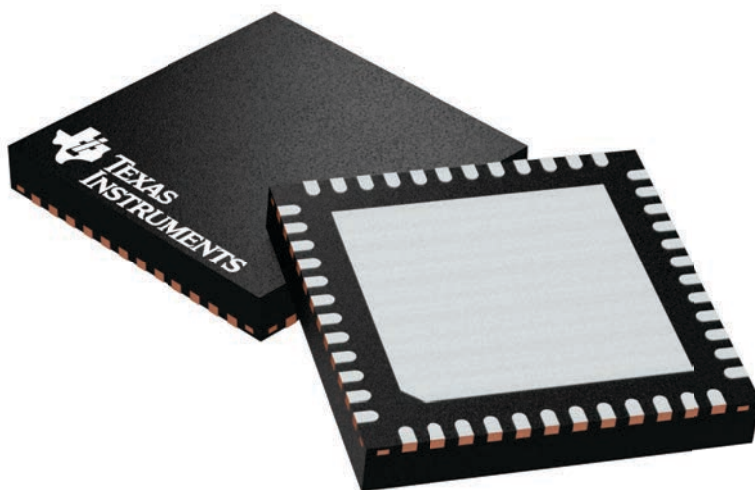
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

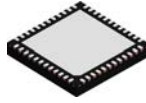
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A

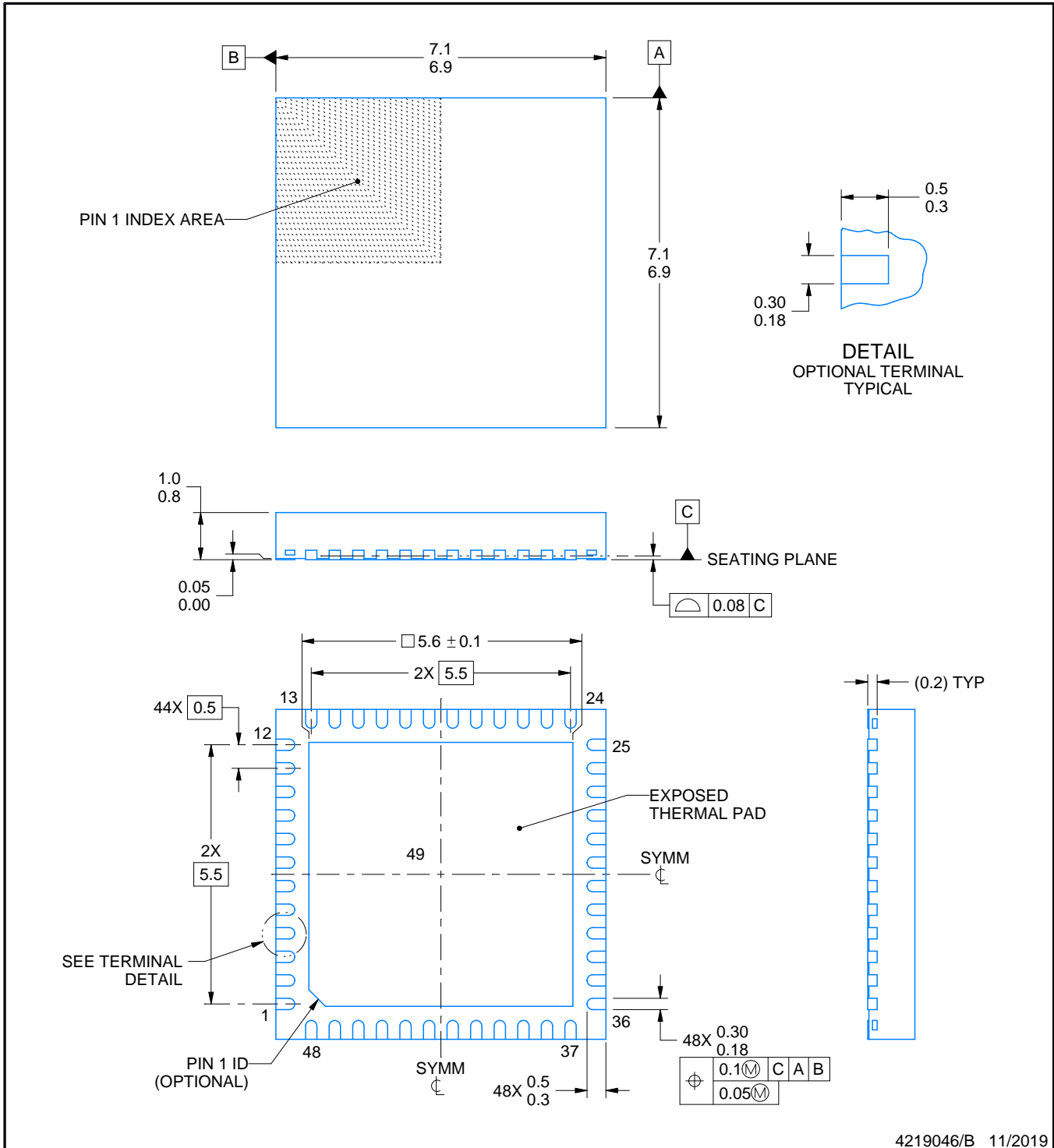
# RGZ0048D



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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**NOTES:**

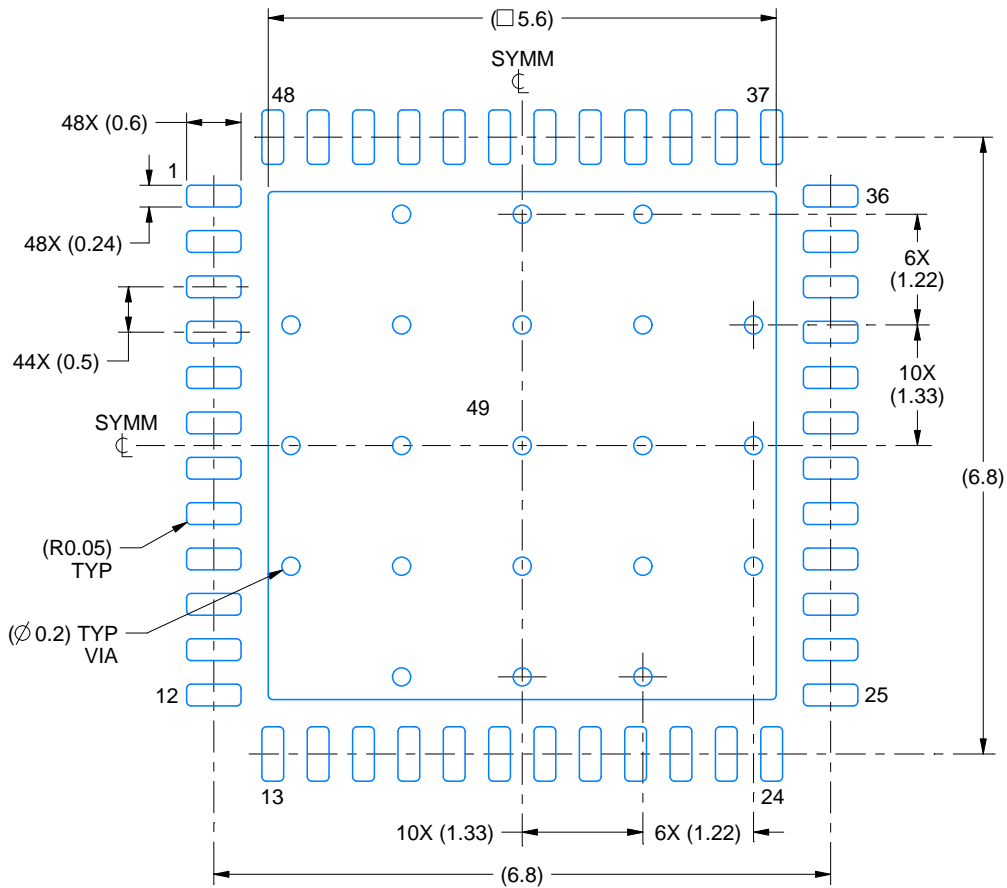
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

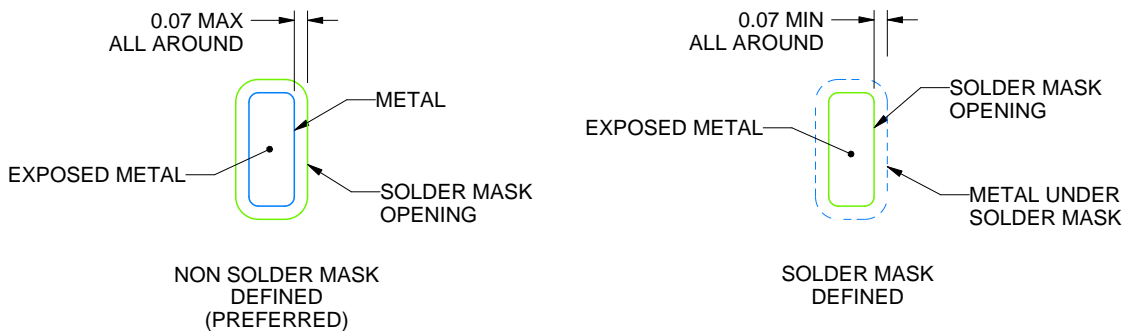
**RGZ0048D**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:12X



**SOLDER MASK DETAILS**

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NOTES: (continued)

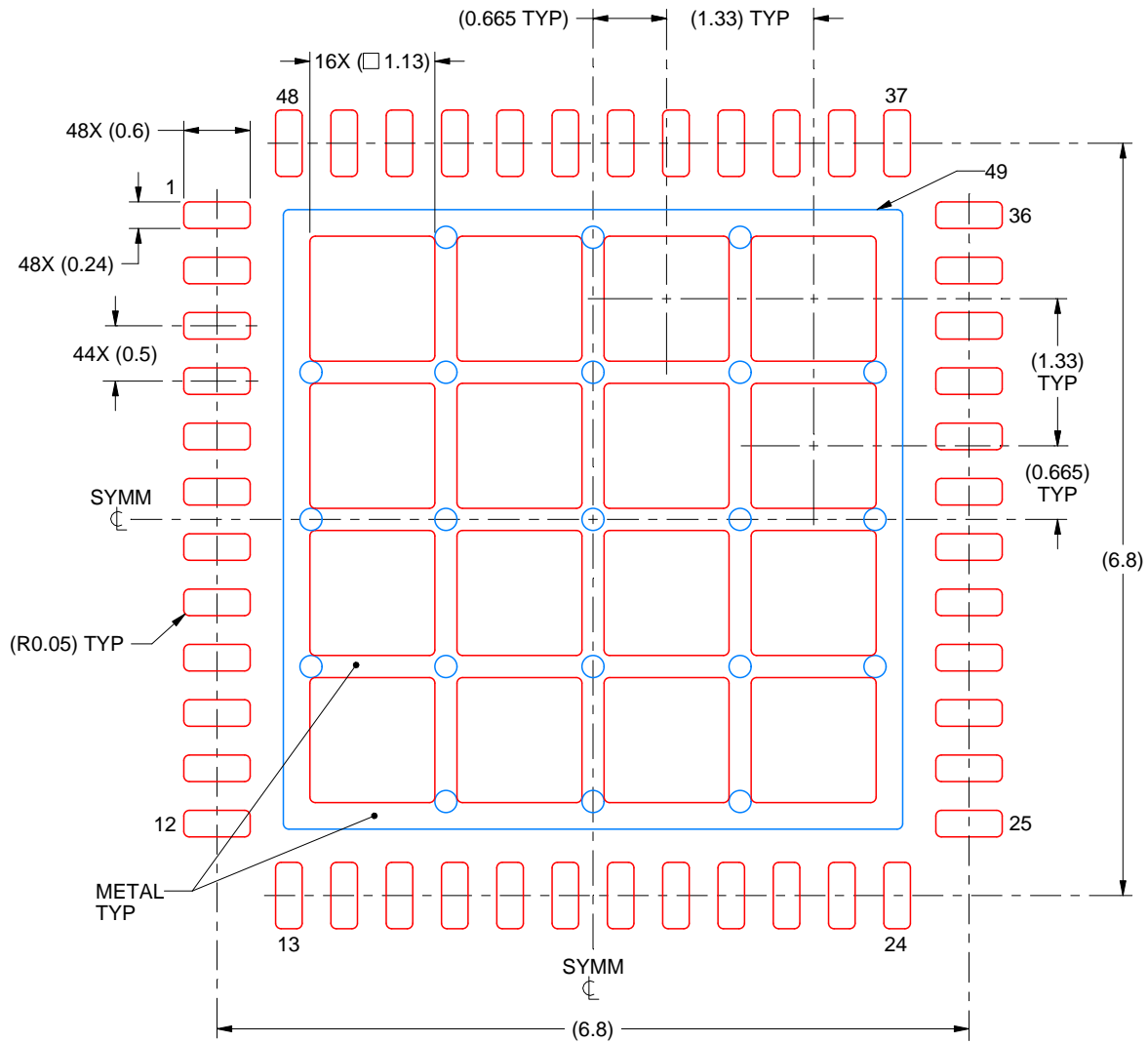
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49  
 66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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