THE DATASHEET OF

DAC7734EC

16-Bit, Quad Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 200mW
- UNIPOLAR OR BIPOLAR OPERATION
- SINGLE SUPPLY OUTPUT RANGE: +10V
- DUAL SUPPLY OUTPUT RANGE: ±10V
- SETTLING TIME: 10μs to 0.003%
- 16-BIT MONOTONICITY: –40°C to +85°C
- PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE
- DOUBLE-BUFFERED DATA INPUTS
- ±1 LSB DNL: –40°C to +85°C

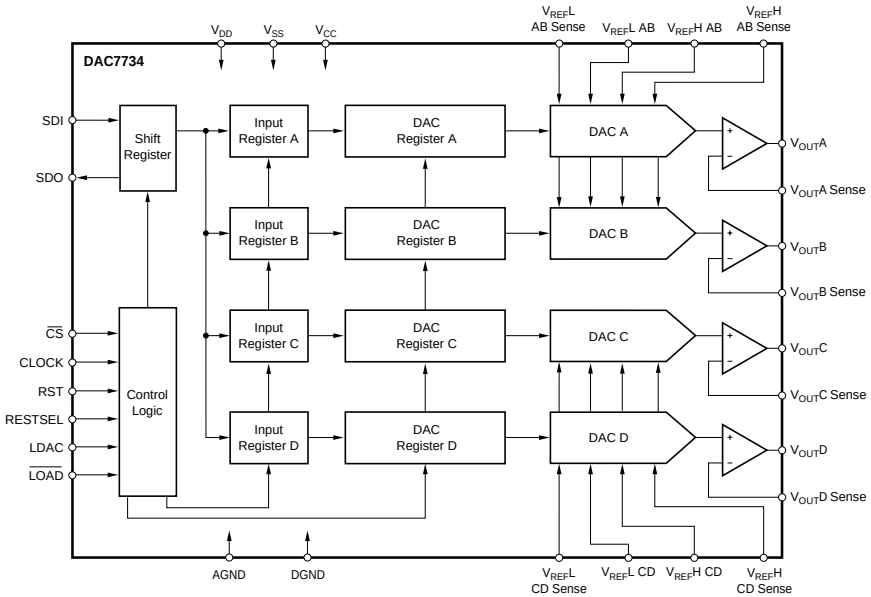
APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

DESCRIPTION

The DAC7734 is a 16-bit, quad voltage output, digital-to-analog converter (DAC) with ensured 16-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000h or to a zero-scale of 0000h. The DAC7734 can operate from a single +15V supply or from +15V and –15V, and +5V supplies.

Low power and small size per DAC make the DAC7734 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7734 is available in a 48-lead SSOP package and offers ensured specifications over the –40°C to +85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7734E			DAC7734EB			DAC7734EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error (INL)	T = 25°C			±3			*			±2	LSB
T_{MIN} to T_{MAX}				±4			*			±3	LSB
Linearity Match			±4			*			±2		LSB
Differential Linearity Error (DNL)	T = 25°C			±3			±2			±1	LSB
T_{MIN} to T_{MAX}				±3			±2			±1	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bits
Bipolar Zero Error	T = 25°C		±0.01	±0.025			*			*	% of FSR
Bipolar Zero Error, T_{MIN} to T_{MAX}				±0.05			*			*	% of FSR
Full-Scale Error	T = 25°C			±0.025			*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}				±0.05			*			*	% of FSR
Bipolar Zero Matching	Channel-to-Channel Matching			±0.024			*			*	% of FSR
Full-Scale Matching	Channel-to-Channel Matching			±0.024			*			*	% of FSR
Power Supply Rejection Ratio (PSRR)	At Full Scale			25			*			*	ppm/V
ANALOG OUTPUT											
Voltage Output		$V_{REF}L$		$V_{REF}H$	*		*	*		*	V
Output Current		±5			*			*			mA
Maximum Load Capacitance			500			*			*		pF
Short-Circuit Current			±20			*			*		mA
Short-Circuit Duration	To V_{SS}, V_{CC} or GND		Indefinite			*			*		
REFERENCE INPUT											
Ref High Input Voltage Range		$V_{REF}L$ + 1.25		+10	*		*	*		*	V
Ref Low Input Voltage Range		–10		$V_{REF}H$ – 1.25	*		*	*		*	V
Ref High Input Current		–0.3		2.6		*			*		mA
Ref Low Input Current		–3.2		–0.3		*			*		mA
DYNAMIC PERFORMANCE											
Settling Time	To ±0.003%, 20V Output Step		9	11		*	*		*	*	µs
Channel-to-Channel Crosstalk	See Figure 5		0.5			*			*		LSB
Digital Feedthrough			2			*			*		nV-s
Output Noise Voltage	f = 10kHz		60			*			*		nV/√Hz
DIGITAL INPUT											
V_{IH}		0.7 • V_{DD}		V_{DD}	*			*			V
V_{IL}		0		0.3 • V_{DD}			*				V
I_{IH}				±10			*				µA
I_{IL}				±10			*				µA
DIGITAL OUTPUT											
V_{OH}	I_{OH} = –0.8mA	3.6	4.5		*	*		*	*		V
V_{OL}	I_{OL} = 1.6mA		0.3	0.4		*	*		*	*	V
POWER SUPPLY											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+14.25	+15.0	+15.75	*	*	*	*	*	*	V
V_{SS}		–14.25	–15.0	–15.75	*	*	*	*	*	*	V
I_{DD}			50			*			*		µA
I_{CC}			6			*			*		mA
I_{SS}			–5			*			*		mA
Power			170	200		*			*		mW
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		*	°C

* Specifications same as grade to the left.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = GND, $V_{REF}H$ = +10V, and $V_{REF}L$ = +50mV, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7734E			DAC7734EB			DAC7734EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error(1) (INL)	T = 25°C			±3			*			±2	LSB
T_{MIN} to T_{MAX}				±4			*			±3	LSB
Linearity Match			±4			*			±2		LSB
Differential Linearity Error (DNL)	T = 25°C			±3			±2			±1	LSB
T_{MIN} to T_{MAX}				±3			±2			±1	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bits
Unipolar Zero	T = 25°C		±0.01	±0.025			*			*	% of FSR
Unipolar Zero Error, T_{MIN} to T_{MAX}				±0.05			*			*	% of FSR
Full-Scale Error	T = 25°C			±0.025			*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}				±0.05			*			*	% of FSR
Unipolar Zero Matching	Channel-to-Channel Matching			±0.024			*			*	% of FSR
Full-Scale Matching	Channel-to-Channel Matching			±0.024			*			*	% of FSR
Power Supply Rejection Ratio (PSRR)	At Full Scale			25			*			*	ppm/V
ANALOG OUTPUT											
Voltage Output	$V_{REF}L$ = 0V, V_{SS} = 0V R = 10kΩ	0		$V_{REF}H$	*		*	*		*	V
Output Current		±5			*			*			mA
Maximum Load Capacitance			500			*			*		pF
Short-Circuit Current			±20			*			*		mA
Short-Circuit Duration	To V_{CC} or GND		Indefinite			*			*		
REFERENCE INPUT											
Ref High Input Voltage Range		$V_{REF}L$ + 1.25		+10	*		*	*		*	V
Ref Low Input Voltage Range		0		$V_{REF}H$ – 1.25	*		*	*		*	V
Ref High Input Current		–0.3		1.0		*			*		mA
Ref Low Input Current		–1.5		–0.3		*			*		mA
DYNAMIC PERFORMANCE											
Settling Time	To ±0.003%, 10V Output Step		8	10		*	*		*	*	µs
Channel-to-Channel Crosstalk	See Figure 6		0.5			*			*		LSB
Digital Feedthrough			2			*			*		nV-s
Output Noise Voltage	f = 10kHz		60			*			*		nV/√Hz
DIGITAL INPUT											
V_{IH}		0.7 • V_{DD}		V_{DD}	*			*			V
V_{IL}		0		0.3 • V_{DD}			*				V
I_{IH}				±10			*				µA
I_{IL}				±10			*				µA
DIGITAL OUTPUT											
V_{OH}	I_{OH} = –0.8mA	3.6	4.5		*	*		*	*		V
V_{OL}	I_{OL} = 1.6mA		0.3	0.4		*	*		*	*	V
POWER SUPPLY											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+14.25	+15.0	+15.75	*	*	*	*	*	*	V
V_{SS}			0			*			*		V
I_{DD}			50			*			*		µA
I_{CC}			3.5			*			*		mA
Power			50	70		*			*		mW
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		*	°C

* Specifications same as grade to the left.

NOTE: (1) If V_{SS} = 0V, the specification applies at code 0021_H and above, due to possible negative zero scale error.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} to V_{SS}	–0.3V to +32V
V_{CC} to AGND	–0.3V to +16V
V_{SS} to AGND	+0.3V to –16V
AGND to DGND	–0.3V to +0.3V
$V_{REF}H$ to AGND	–9V to +11V
$V_{REF}L$ to AGND	–11V to +9V
V_{DD} to GND	–0.3V to +6V
$V_{REF}H$ to $V_{REF}L$	–1V to 22V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

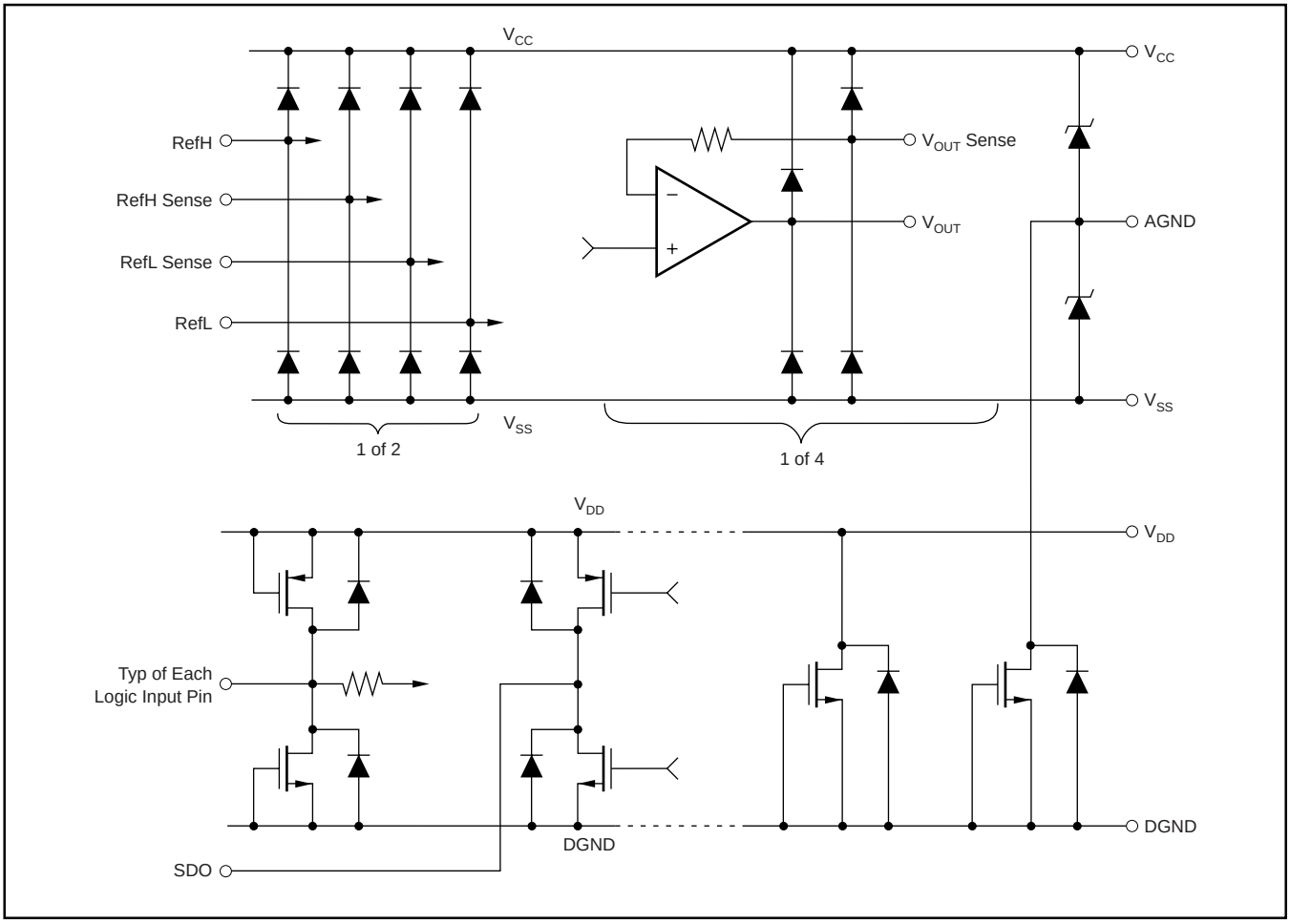
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

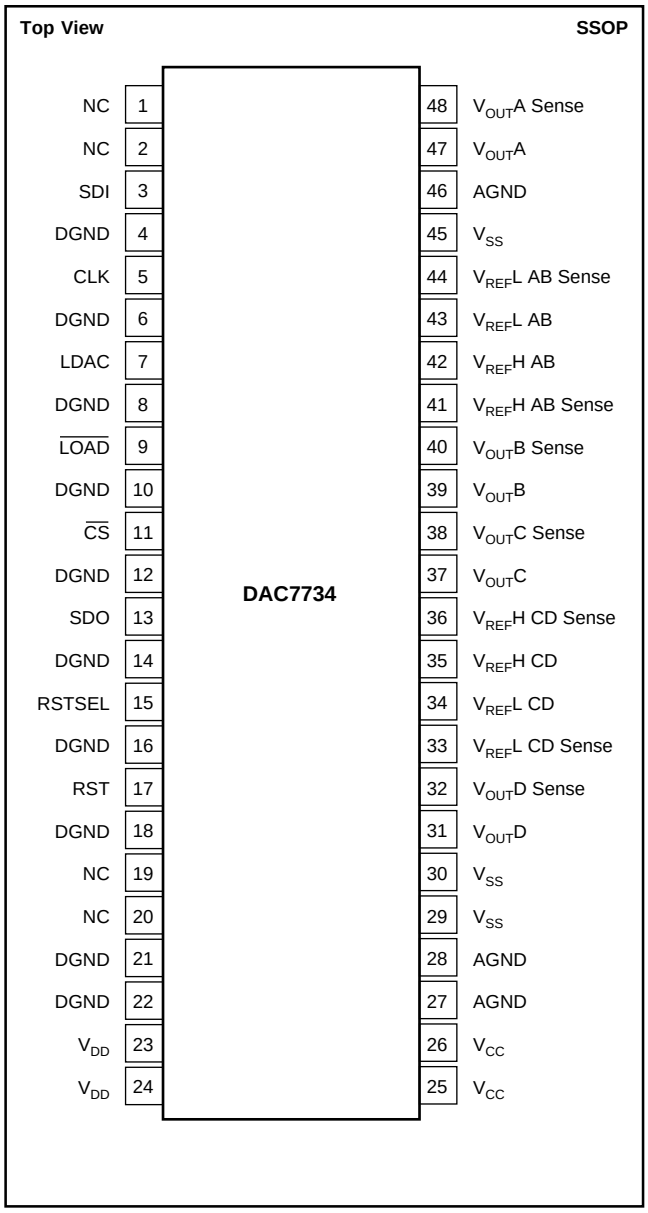
PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7734E	±4	±3	SSOP-48	333	–40°C to +85°C	DAC7734E	Rails, 30
"	"	"	"	"	"	DAC7734E/1K	Tape and Reel, 1000
DAC7734EB	±4	±2	SSOP-48	333	–40°C to +85°C	DAC7734EB	Rails, 30
"	"	"	"	"	"	DAC7734EB/1K	Tape and Reel, 1000
DAC7734EC	±3	±1	SSOP-48	333	–40°C to +85°C	DAC7734EC	Rails, 30
"	"	"	"	"	"	DAC7734EC/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ESD PROTECTION CIRCUITS



PIN CONFIGURATION



PIN DESCRIPTIONS

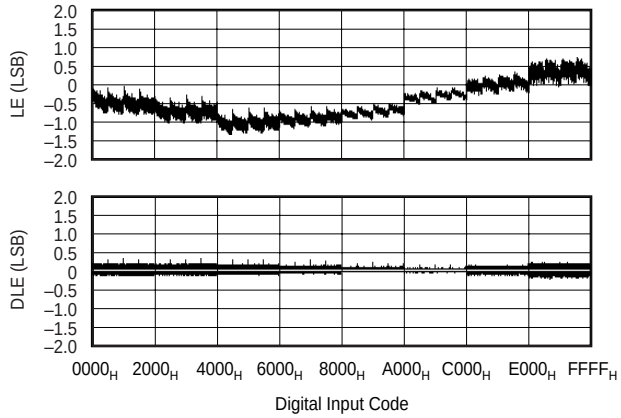
PIN	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	SDI	Serial Data Input
4	DGND	Digital Ground
5	CLK	Data Clock Input
6	DGND	Digital Ground
7	LDAC	DAC Register Load Control, Rising Edge Triggered
8	DGND	Digital Ground
9	$\overline{\text{LOAD}}$	DAC Input Register Load Control, Active Low
10	DGND	Digital Ground
11	$\overline{\text{CS}}$	Chip Select, Active Low
12	DGND	Digital Ground
13	SDO	Serial Data Output
14	DGND	Digital Ground
15	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST common will set the DAC registers to mid-scale (8000H). If LOW, a RST command will set the DAC registers to zero (0000H).
16	DGND	Digital Ground
17	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
18	DGND	Digital Ground
19	NC	No Connection
20	NC	No Connection
21	DGND	Digital Ground
22	DGND	Digital Ground
23	V_{DD}	Digital +5V Power Supply
24	V_{DD}	Digital +5V Power Supply
25	V_{CC}	Analog +15V Power Supply
26	V_{CC}	Analog +15V Power Supply
27	AGND	Analog Ground
28	AGND	Analog Ground
29	V_{SS}	Analog –15V Power Supply or 0V Single Supply
30	V_{SS}	Analog –15V Power Supply or 0V Single Supply
31	$V_{OUT}D$	DAC D Output Voltage
32	$V_{OUT}D$ Sense	DAC D's Output Amplifier Inverting Input. Used to close feedback loop at load.
33	$V_{REF}L$ CD Sense	DAC C and D Reference Low Sense Input
34	$V_{REF}L$ CD	DAC C and D Reference Low Input
35	$V_{REF}H$ CD	DAC C and D Reference High Input
36	$V_{REF}H$ CD Sense	DAC C and D Reference High Sense Input
37	$V_{OUT}C$	DAC C Output Voltage
38	$V_{OUT}C$ Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
39	$V_{OUT}B$	DAC B Output Voltage
40	$V_{OUT}B$ Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
41	$V_{REF}H$ AB Sense	DAC A and B Reference High Sense Input
42	$V_{REF}H$ AB	DAC A and B Reference High Input
43	$V_{OUT}L$ AB	DAC A and B Reference Low Input
44	$V_{REF}L$ AB Sense	DAC A and B Reference Low Sense Input
45	V_{SS}	Analog –15V Power Supply or 0V Single Supply
46	AGND	Analog Ground
47	$V_{OUT}A$	DAC A Output Voltage
48	$V_{OUT}A$ Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.

TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

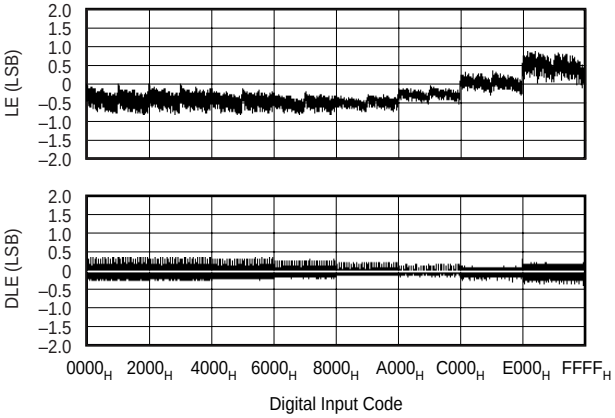
At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = 0, $V_{REF}H$ = +10V, and $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

+25°C

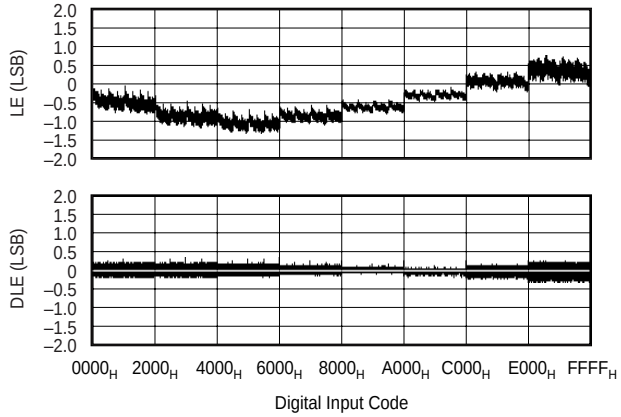
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



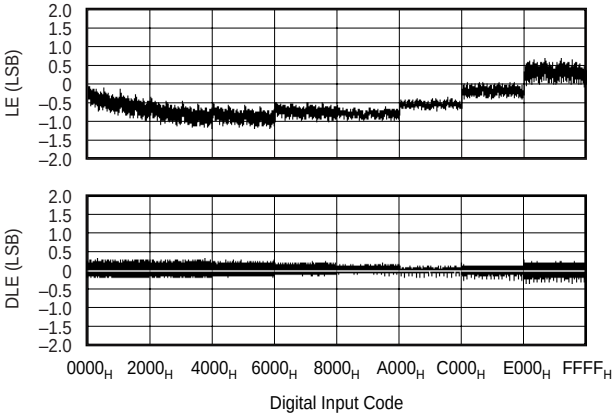
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

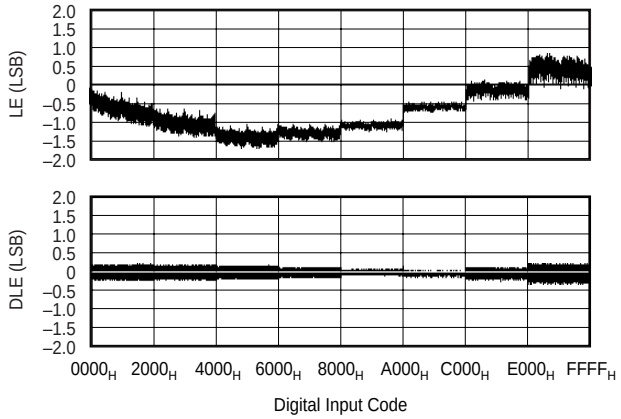


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

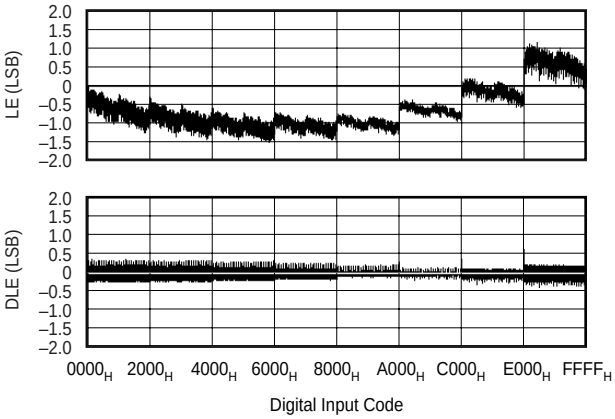


+85°C

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

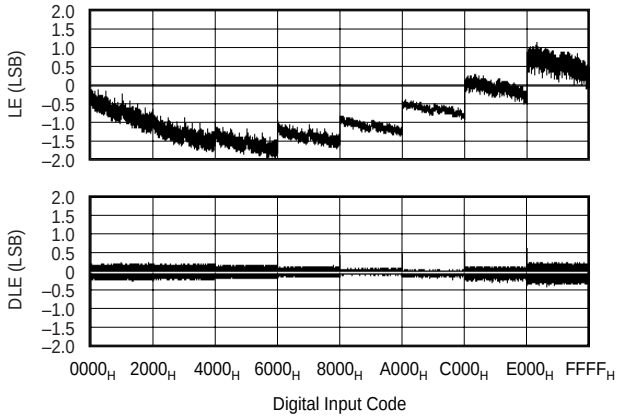


TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

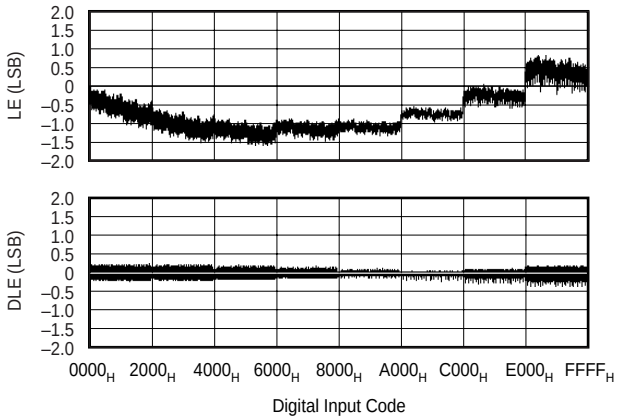
At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = 0, $V_{REF}H$ = +10V, and $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

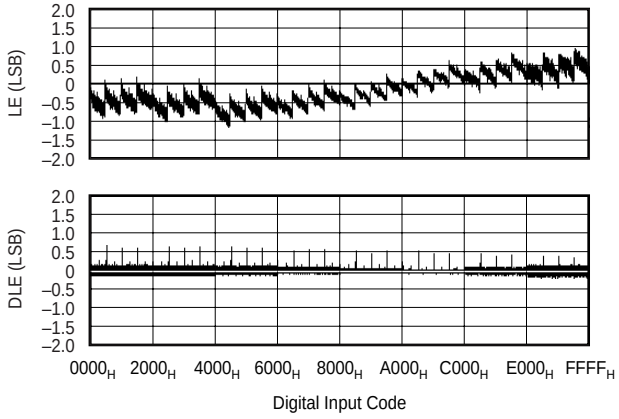


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

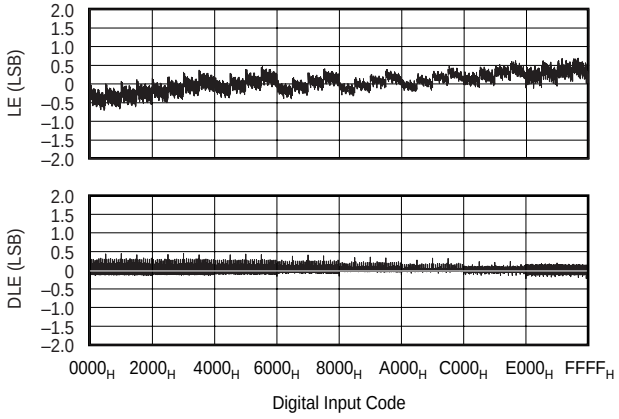


–40°C

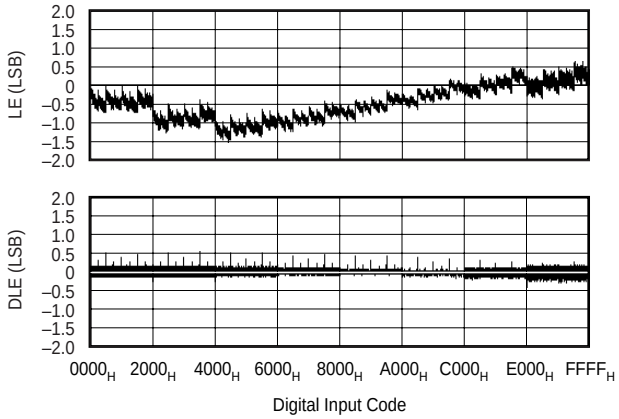
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



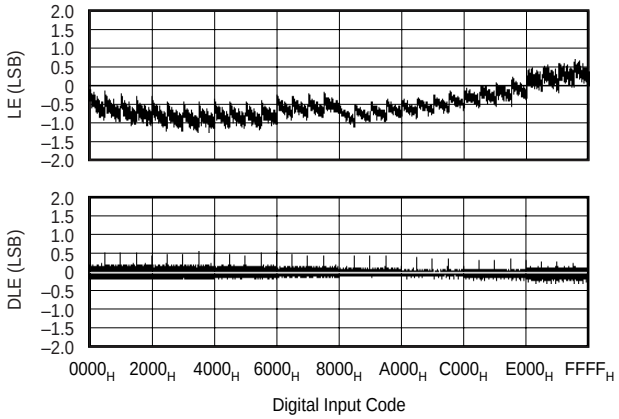
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)



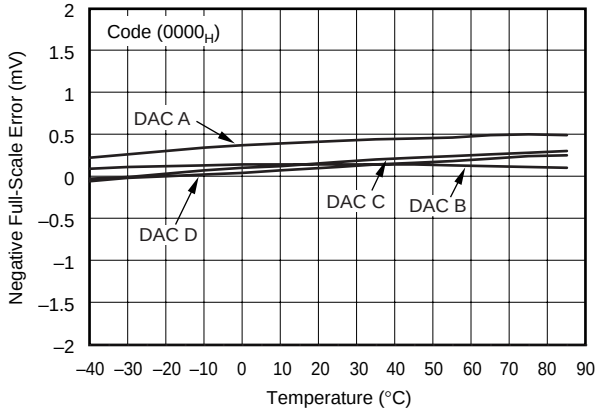
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)



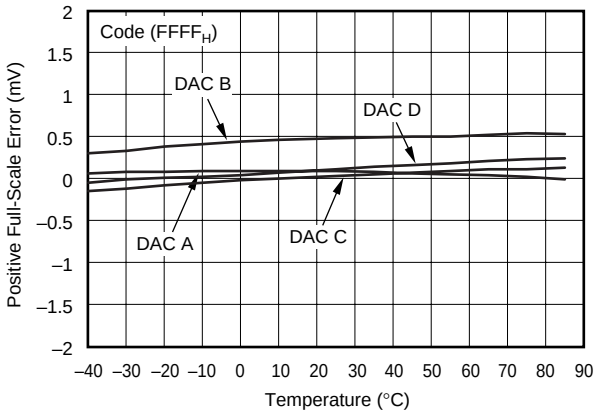
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = 0, $V_{REF}H$ = +10V, and $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

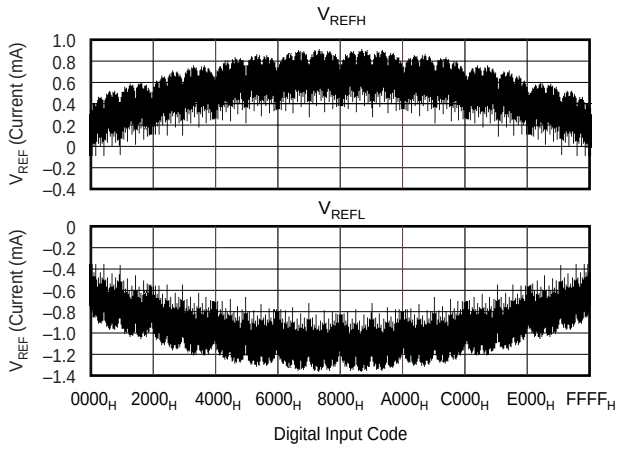
ZERO-SCALE ERROR vs TEMPERATURE



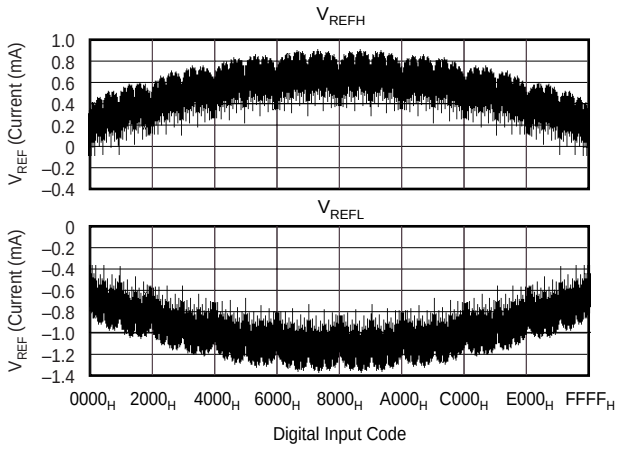
POSITIVE FULL-SCALE ERROR vs TEMPERATURE



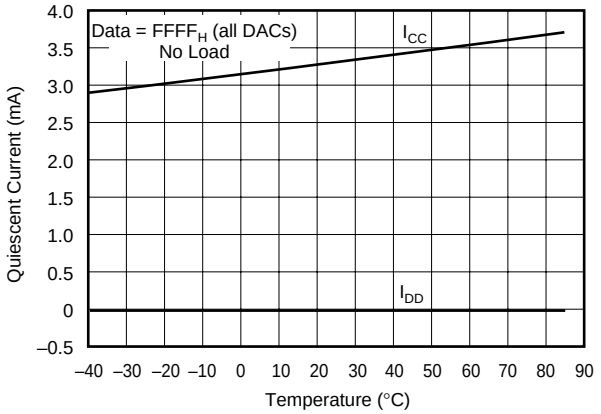
REFERENCE CURRENT vs CODE
All DACs Sent to Indicated Code
(DAC A and B)



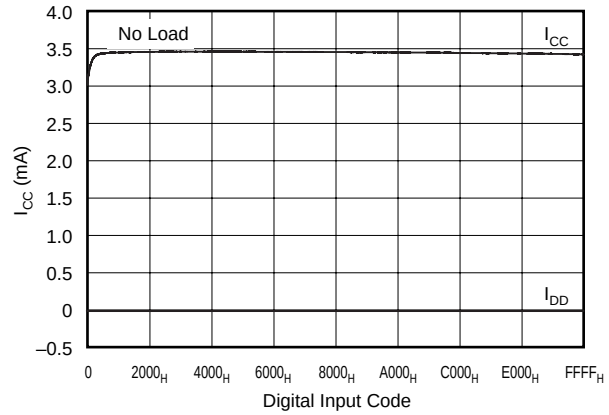
REFERENCE CURRENT vs CODE
All DACs Sent to Indicated Code
(DAC C and D)



POWER SUPPLY CURRENT vs TEMPERATURE



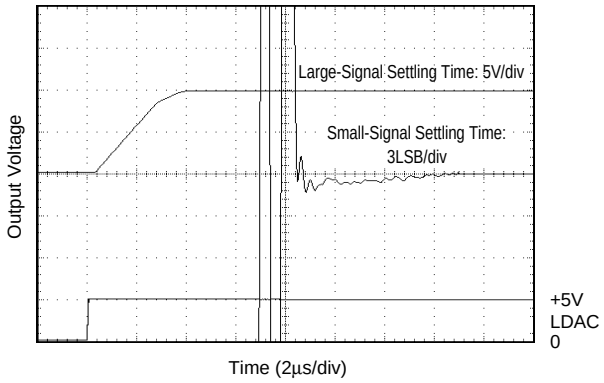
POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE



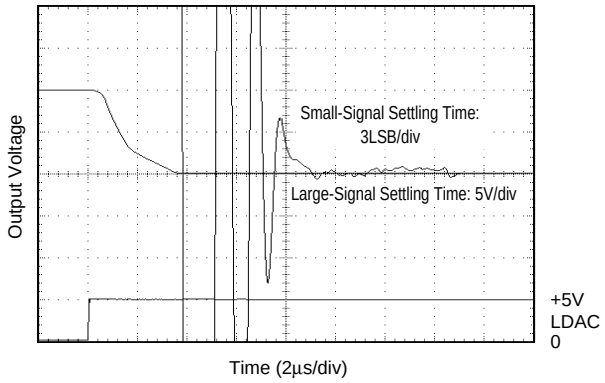
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = 0, $V_{REF}H$ = +10V, and $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

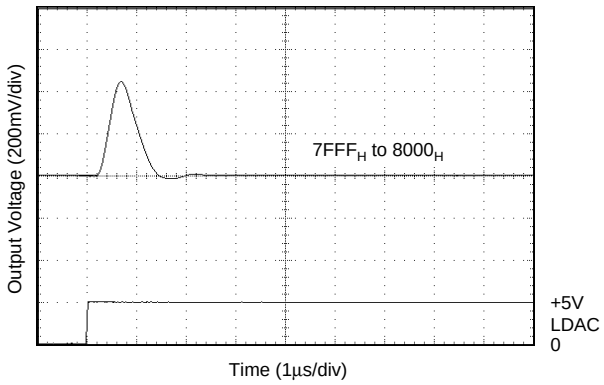
OUTPUT VOLTAGE vs SETTLING TIME
(0V to +10V)



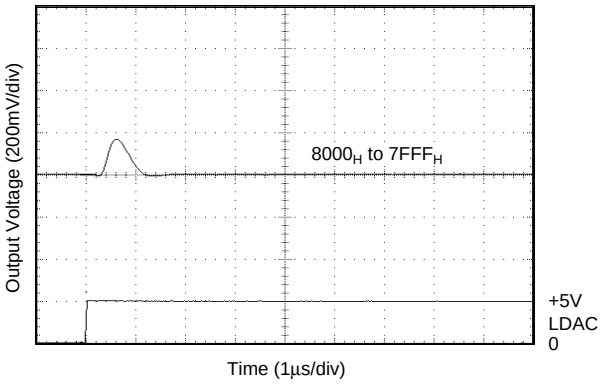
OUTPUT VOLTAGE vs SETTLING TIME
(+10V to 0V)



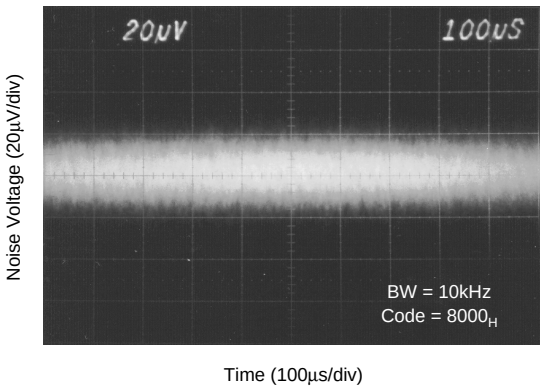
OUTPUT VOLTAGE
MIDSCALE GLITCH PERFORMANCE



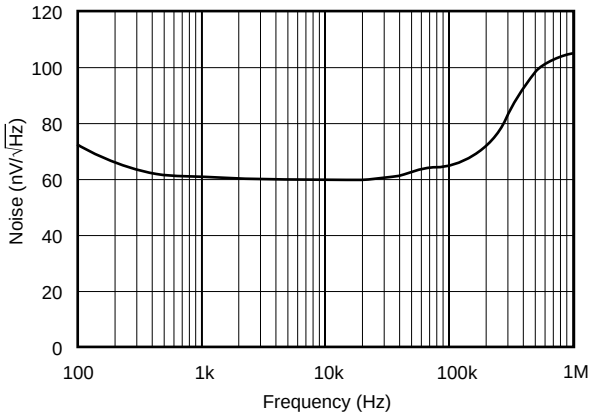
OUTPUT VOLTAGE
MIDSCALE GLITCH PERFORMANCE



BROADBAND NOISE



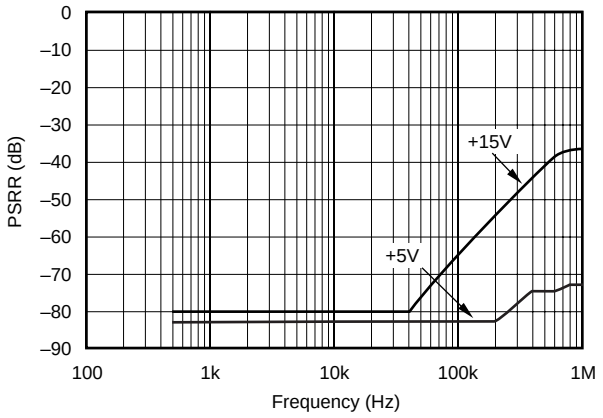
OUTPUT NOISE VOLTAGE vs FREQUENCY



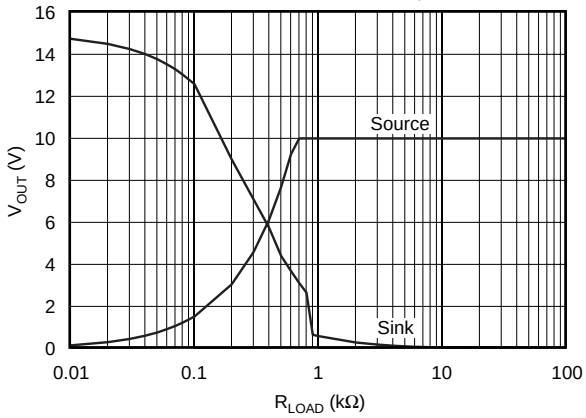
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = 0, $V_{REF}H$ = +10V, and $V_{REF}L$ = 0V, representative unit, unless otherwise specified.

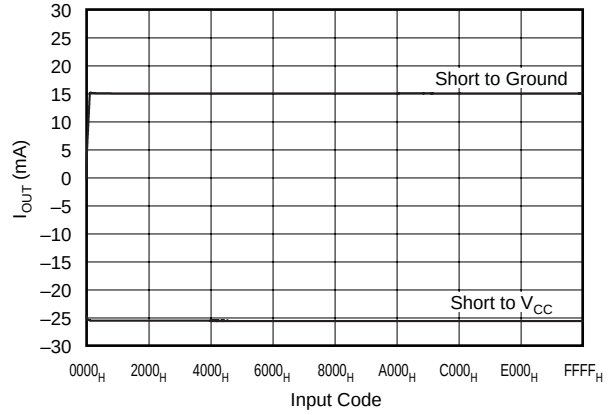
POWER SUPPLY REJECTION RATIO vs FREQUENCY



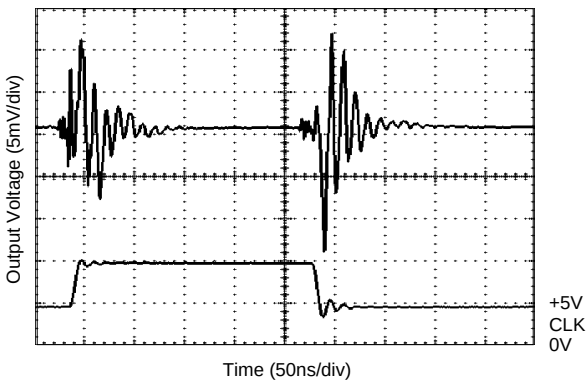
OUTPUT VOLTAGE vs R_{LOAD}



SINGLE-SUPPLY CURRENT LIMIT vs INPUT CODE



CLOCK FEEDTHROUGH

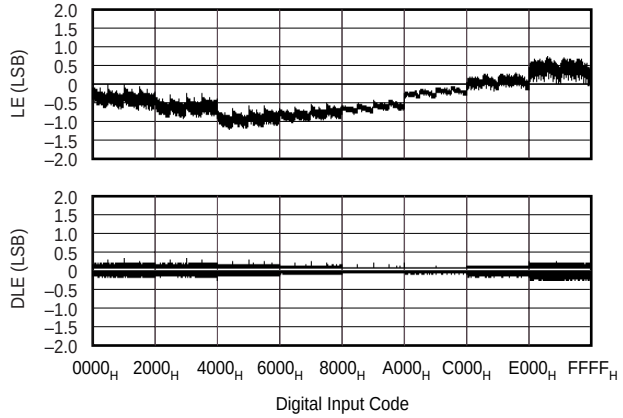


TYPICAL PERFORMANCE CURVES: V_{SS} = –15V

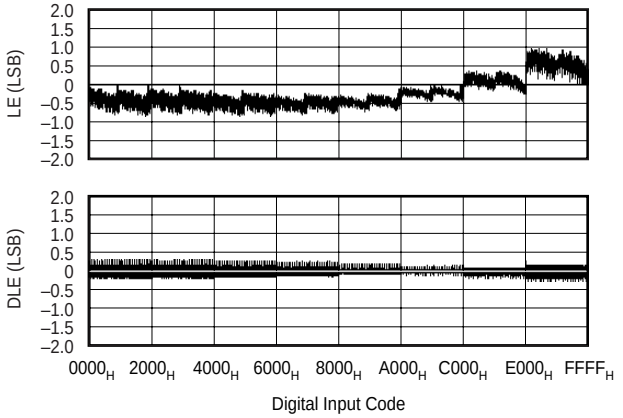
At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, representative unit, unless otherwise specified.

+25°C

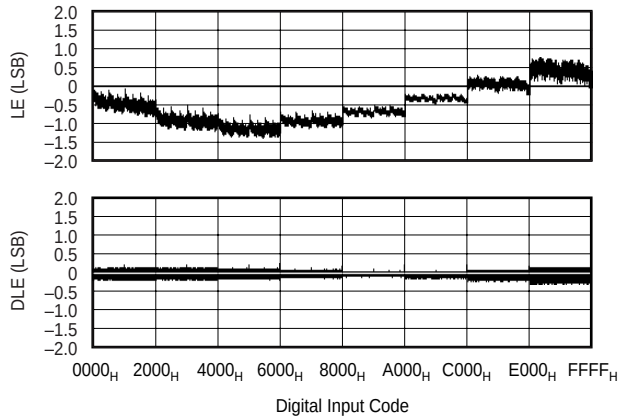
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



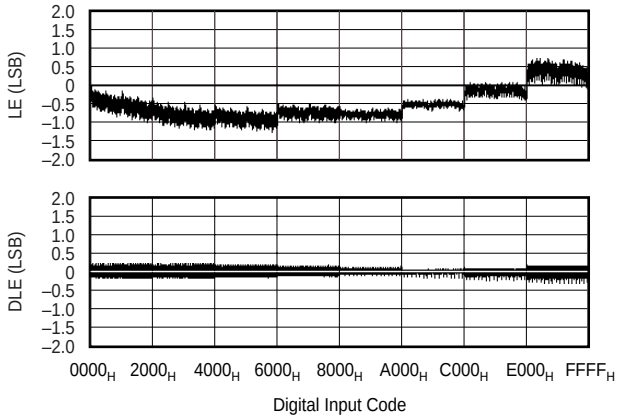
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

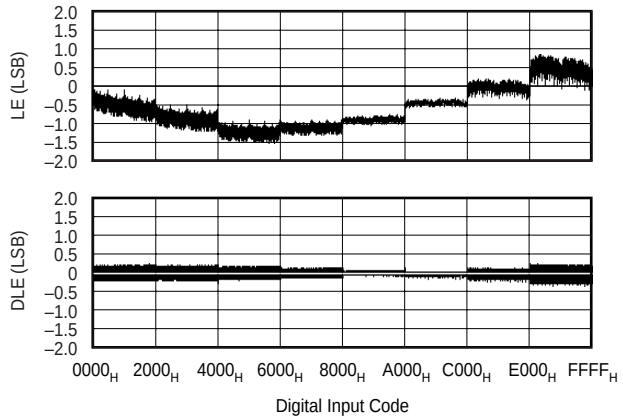


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

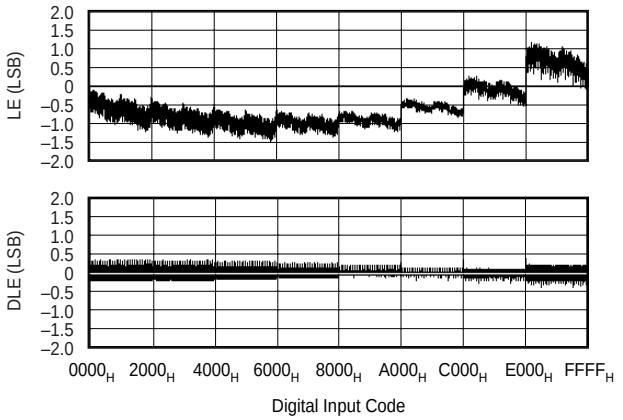


+85°C

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

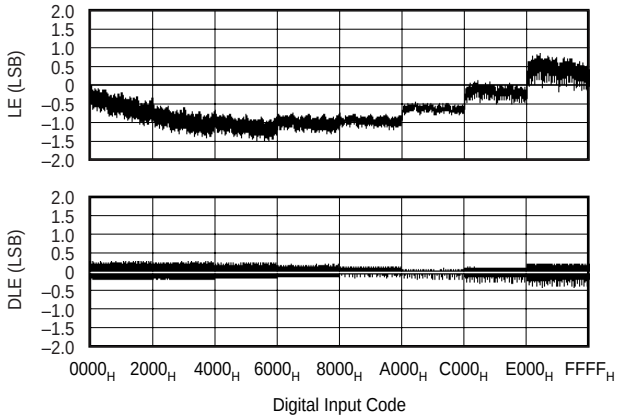


TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

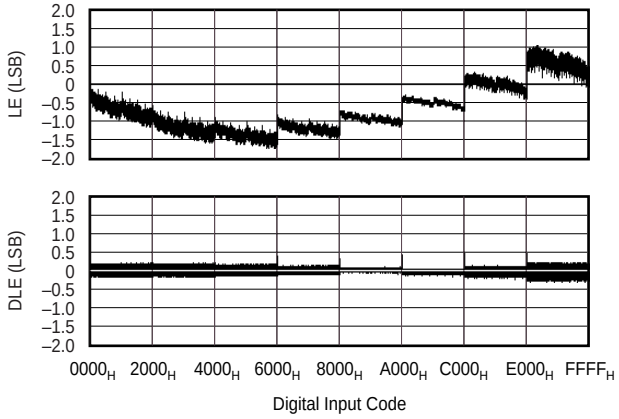
At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

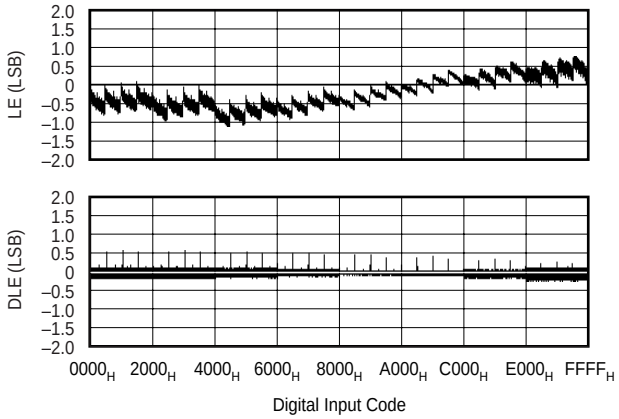


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

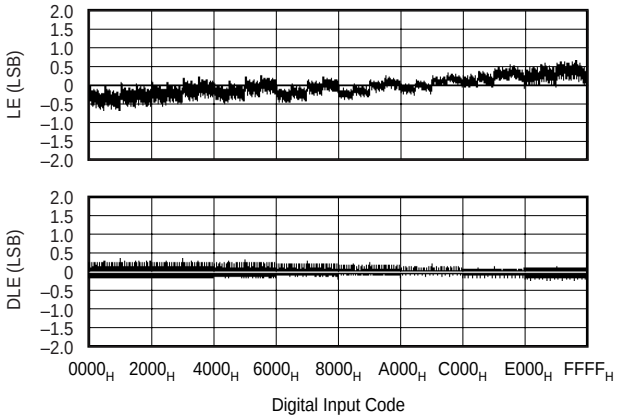


–40°C

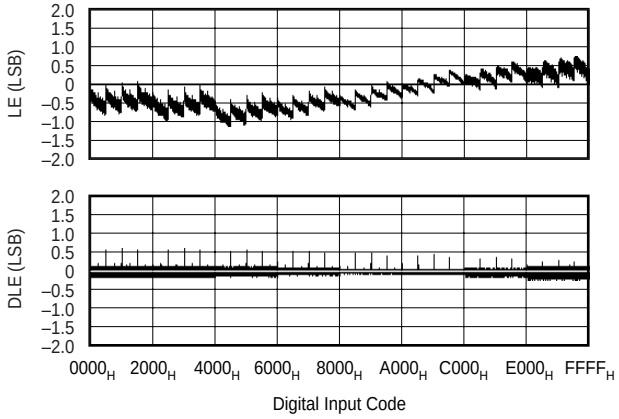
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



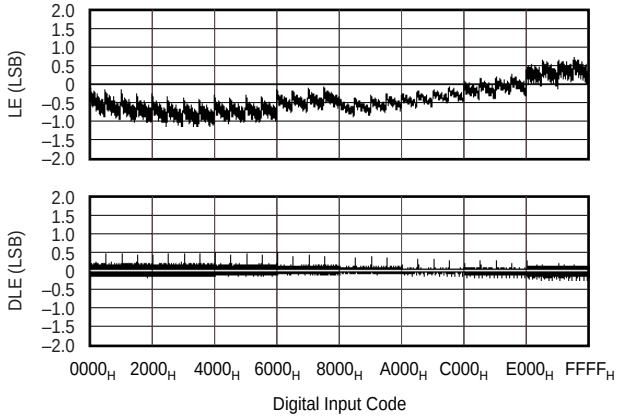
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)



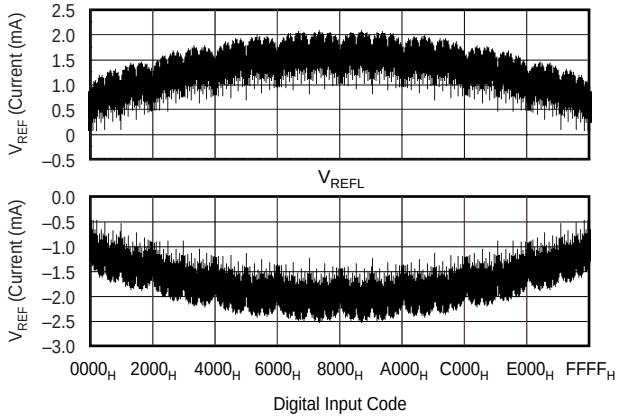
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)



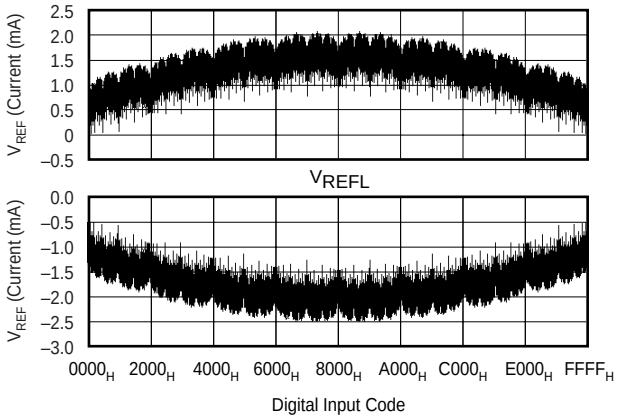
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, representative unit, unless otherwise specified.

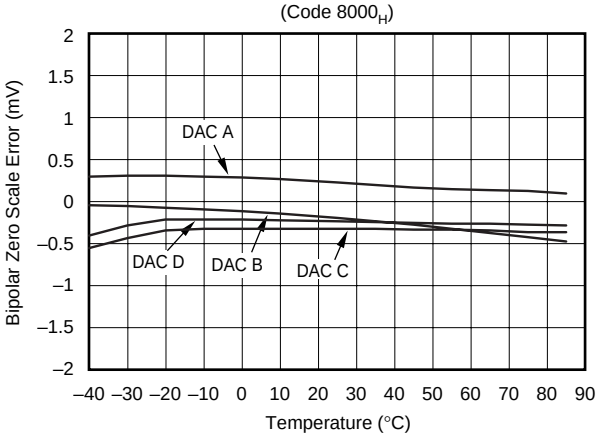
REFERENCE CURRENT vs CODE
All DACs Sent to Indicated Code
(DAC A and B)



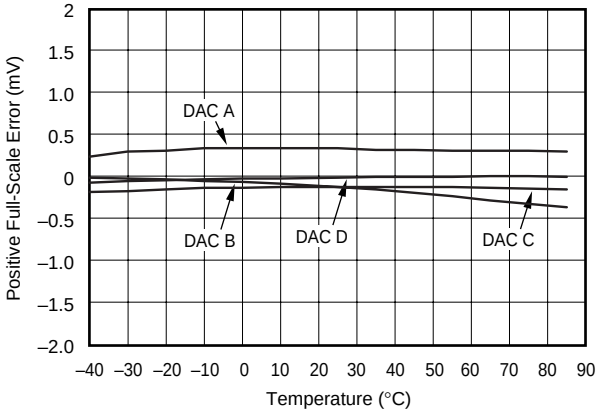
REFERENCE CURRENT vs CODE
All DACs Sent to Indicated Code
(DAC C and D)



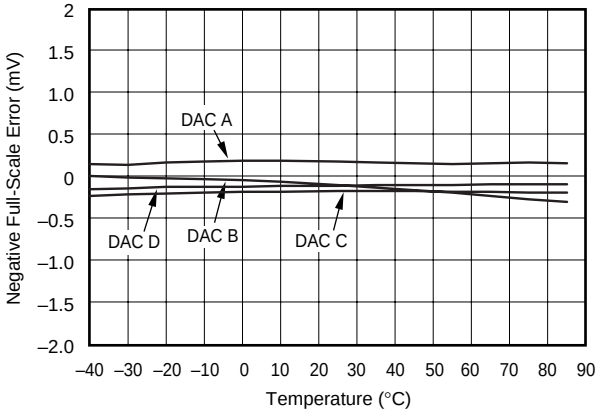
BIPOLAR ZERO SCALE ERROR vs TEMPERATURE
(Code 8000_H)



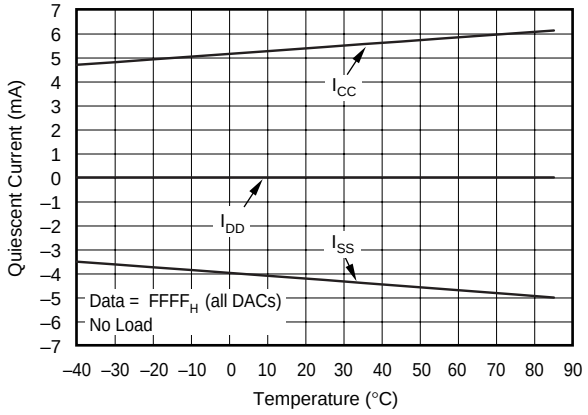
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code $FFFF_H$)



NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 0000_H)



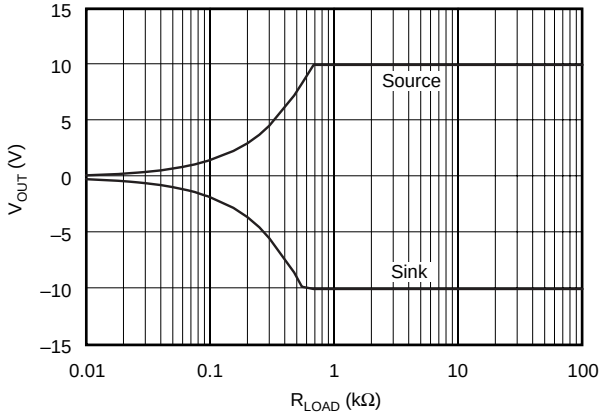
POWER SUPPLY CURRENT vs TEMPERTURE



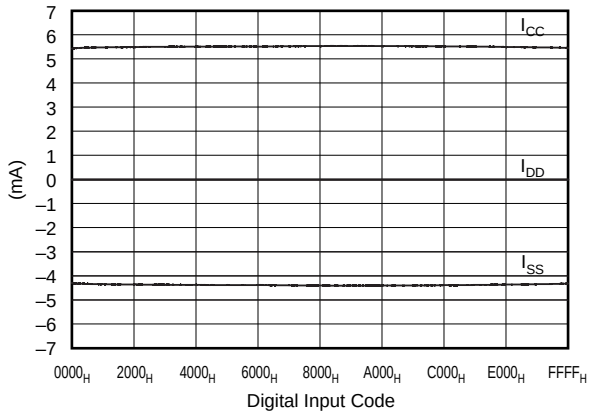
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, representative unit, unless otherwise specified.

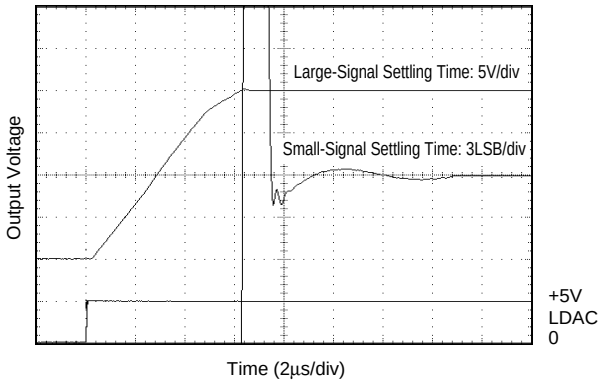
OUTPUT VOLTAGE vs R_{LOAD}



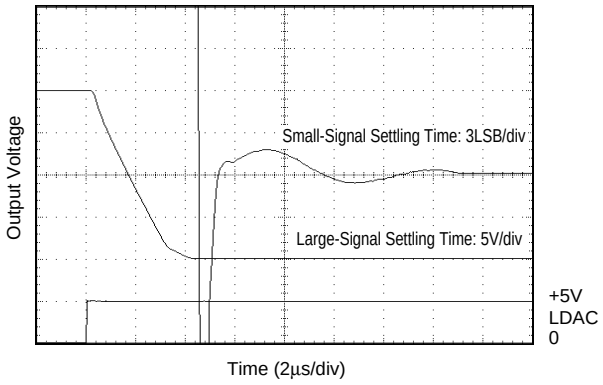
SUPPLY CURRENT vs CODE



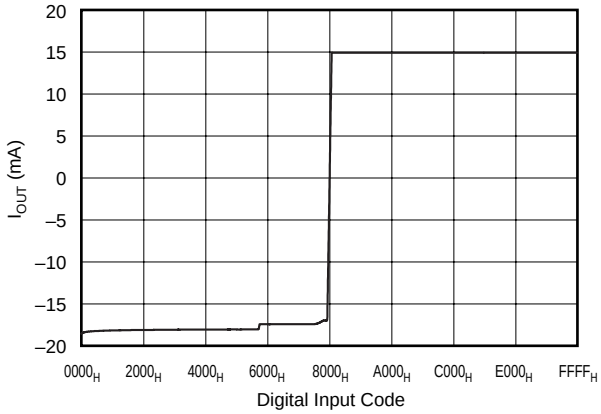
OUTPUT VOLTAGE vs SETTLING TIME
(–10V to +10V)



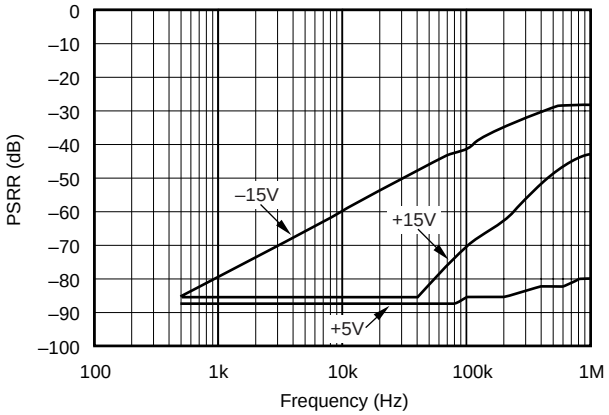
OUTPUT VOLTAGE vs SETTLING TIME
(+10V to –10V)



DUAL-SUPPLY CURRENT LIMIT vs INPUT CODE
(Short-to-Ground)



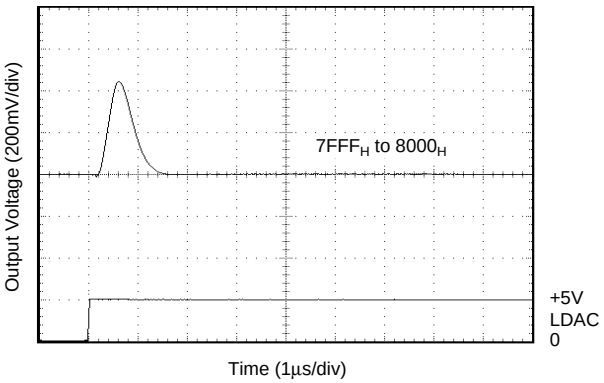
POWER SUPPLY REJECTION RATIO vs FREQUENCY



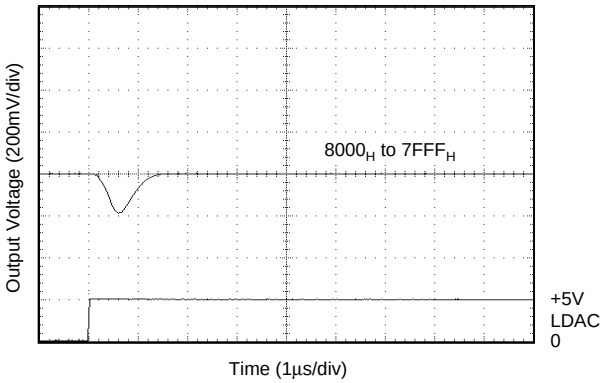
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{DD} = +5V, V_{CC} = +15V, V_{SS} = –15V, $V_{REF}H$ = +10V, and $V_{REF}L$ = –10V, representative unit, unless otherwise specified.

OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



THEORY OF OPERATION

The DAC7734 is a quad voltage output, 16-bit Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references $V_{REF}L$ and $V_{REF}H$.

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits, and the 16-bit DAC code (MSB first). The converters can be powered from either a single +15V supply or a dual ±15V supply and a +5V logic supply. The device offers a reset function that immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7734.

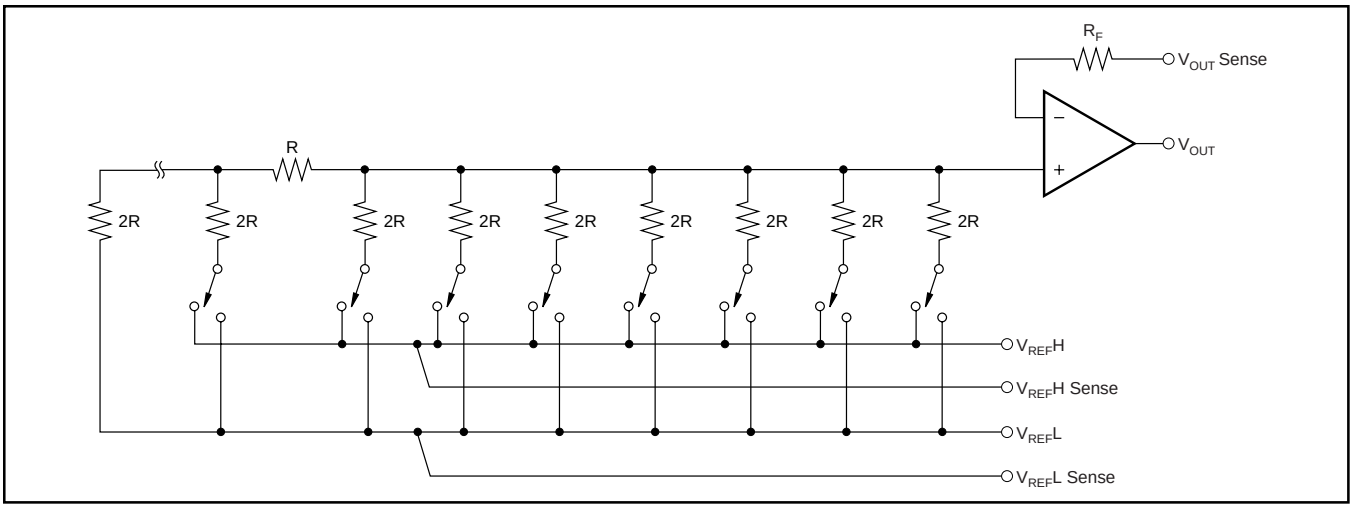


FIGURE 1. DAC7734 Architecture.

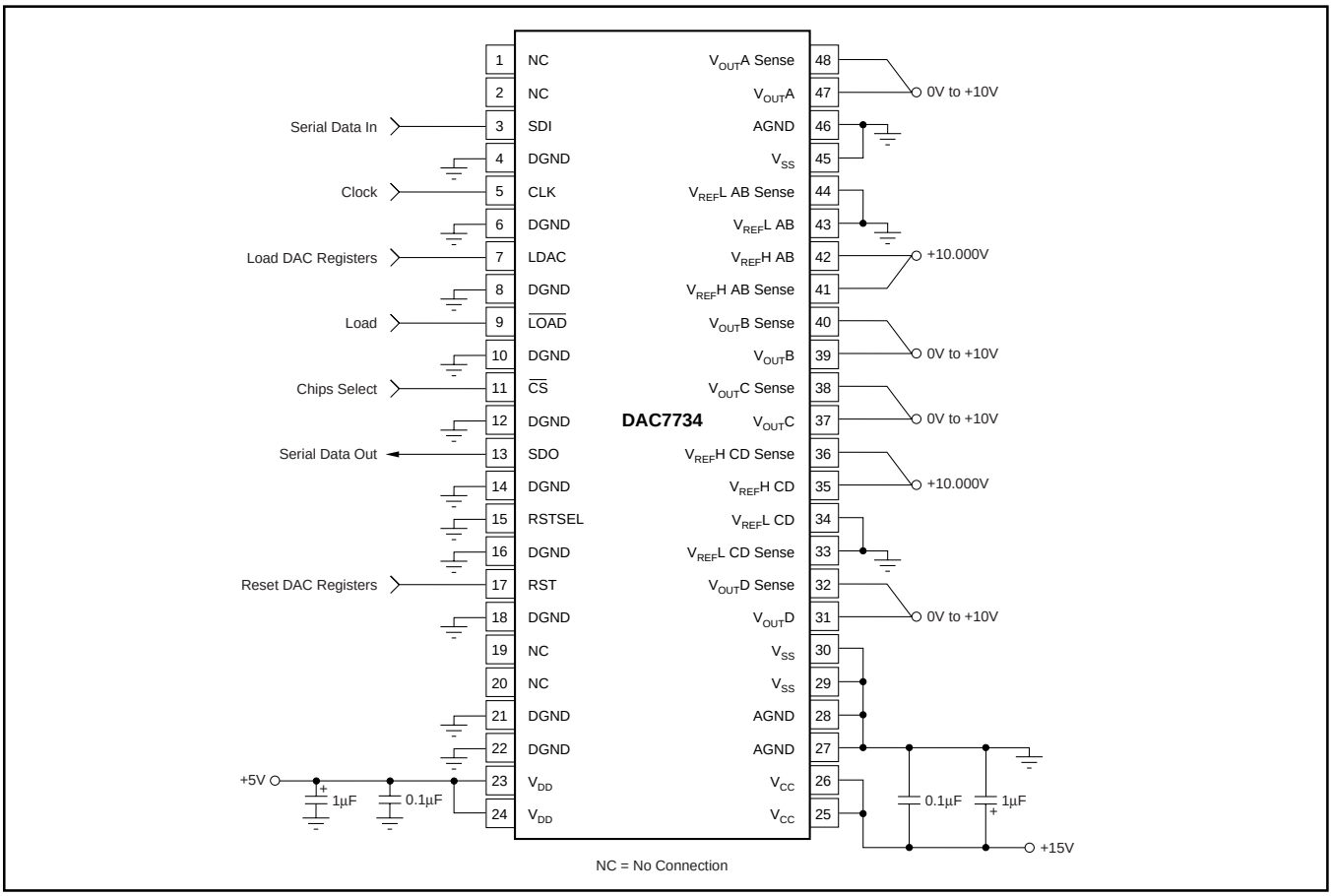


FIGURE 2. Basic Single-Supply Operation of the DAC7734.

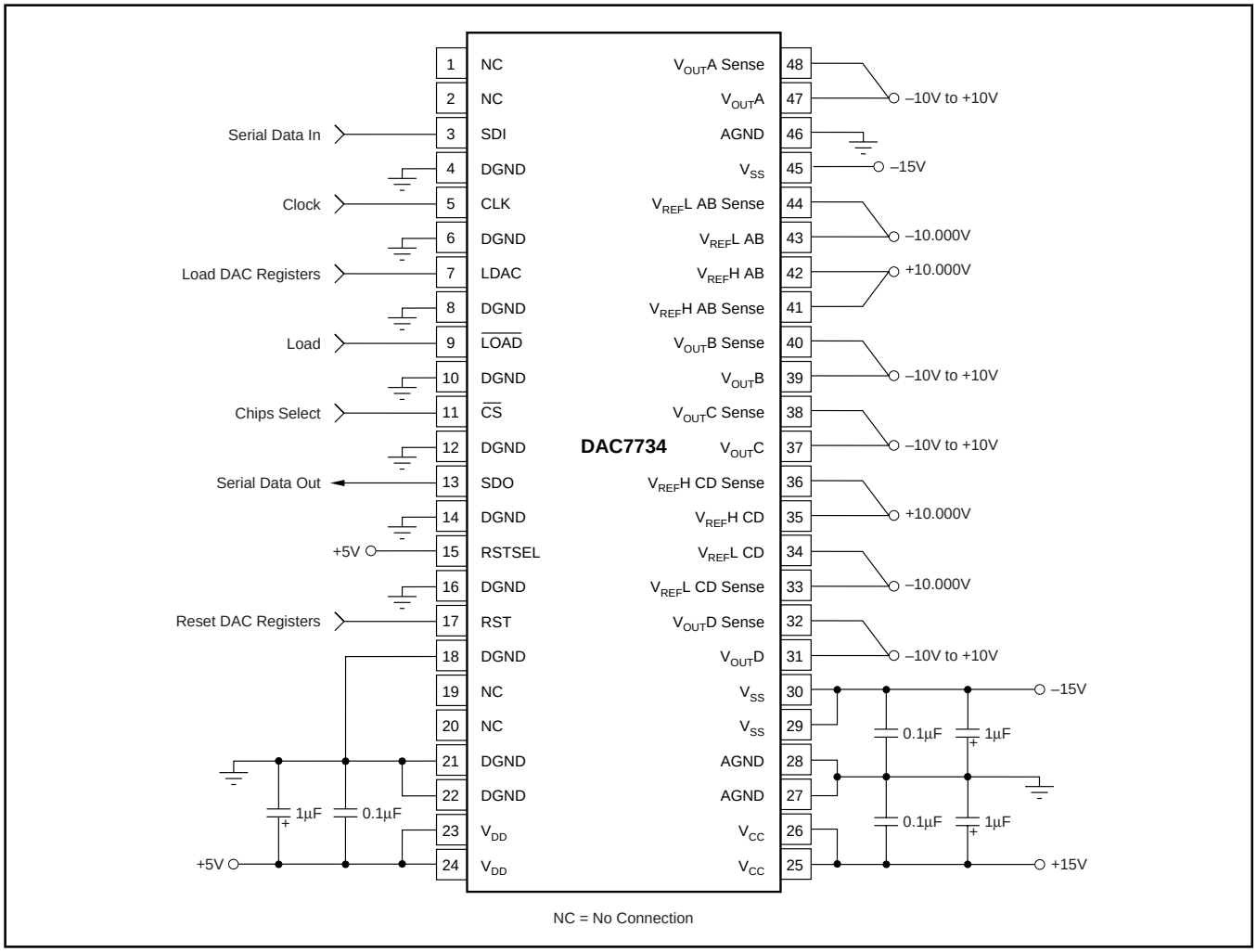


FIGURE 3. Basic Dual-Supply Operation of the DAC7734.

ANALOG OUTPUTS

When V_{SS} = –15V (dual-supply operation), the output amplifier can swing to within 4V of the supply rails, ensured over the –40°C to +85°C temperature range. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –5mV, the first specified output starts at code 0021_H.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of 152µV. With a load current of 1mA, series wiring and connector resistance of only 150mΩ (R_{W2}) will cause a voltage drop of 150µV, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 20 milli-inch wide printed circuit conductor 6 inches long will result in a voltage drop of 150µV.

The DAC7734 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

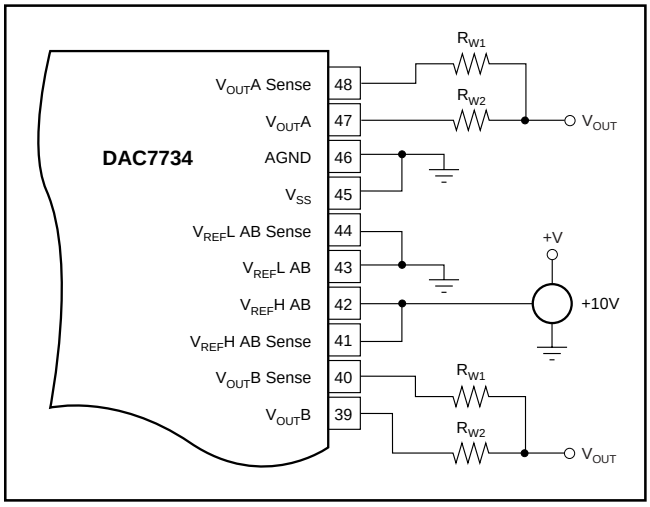


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7734). R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between V_{SS} + 4V and V_{CC} – 4V, provided that $V_{REF}H$ is at least 1.25V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –14.25V to –15.75V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not ensured.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltages, and can vary from a few microamps to approximately 2.0mA. The reference input appears as a varying load to the reference. The DAC7734 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 9 show different reference configurations, and the effect on the linearity and differential linearity.

The analog supplies must come up first. If V_{CC} and V_{SS} do not come up together, then V_{SS} should come up first. If the power supplies for the reference come up first, then the V_{CC} and V_{SS} supplies will be powered from the reference via the ESD protection diode; see the ESD protection circuits on page 4.

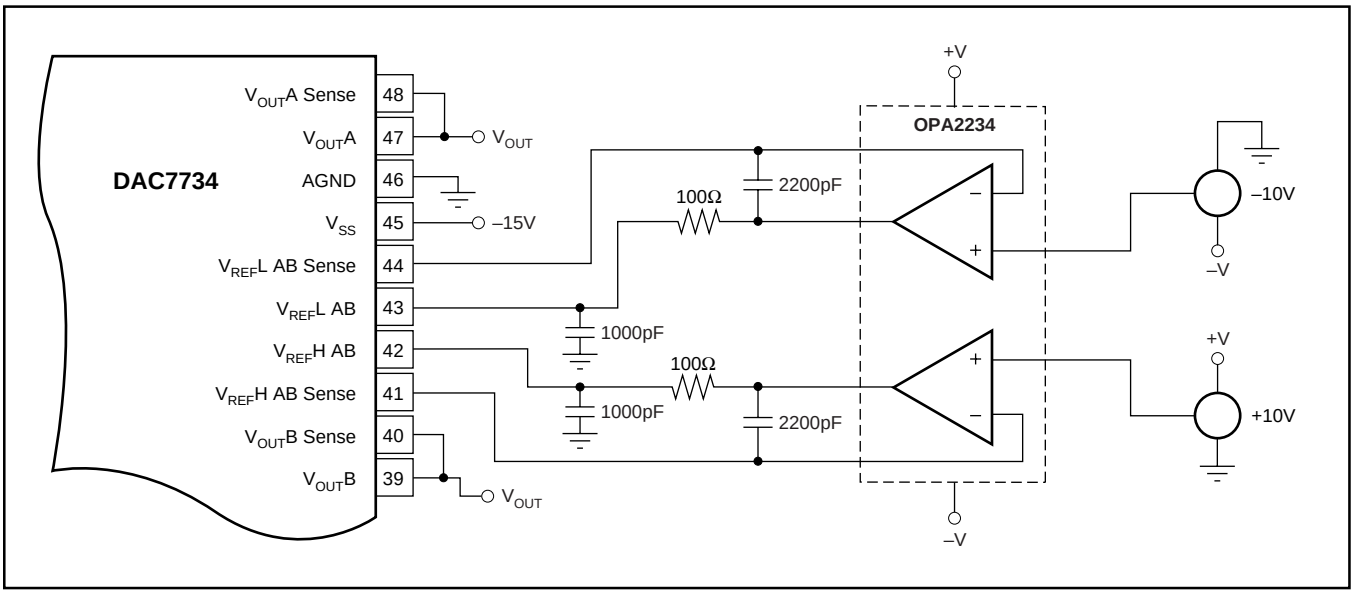


FIGURE 5. Dual-Supply Configuration-Buffered References, used for Dual-Supply Performance (1/2 DAC7734).

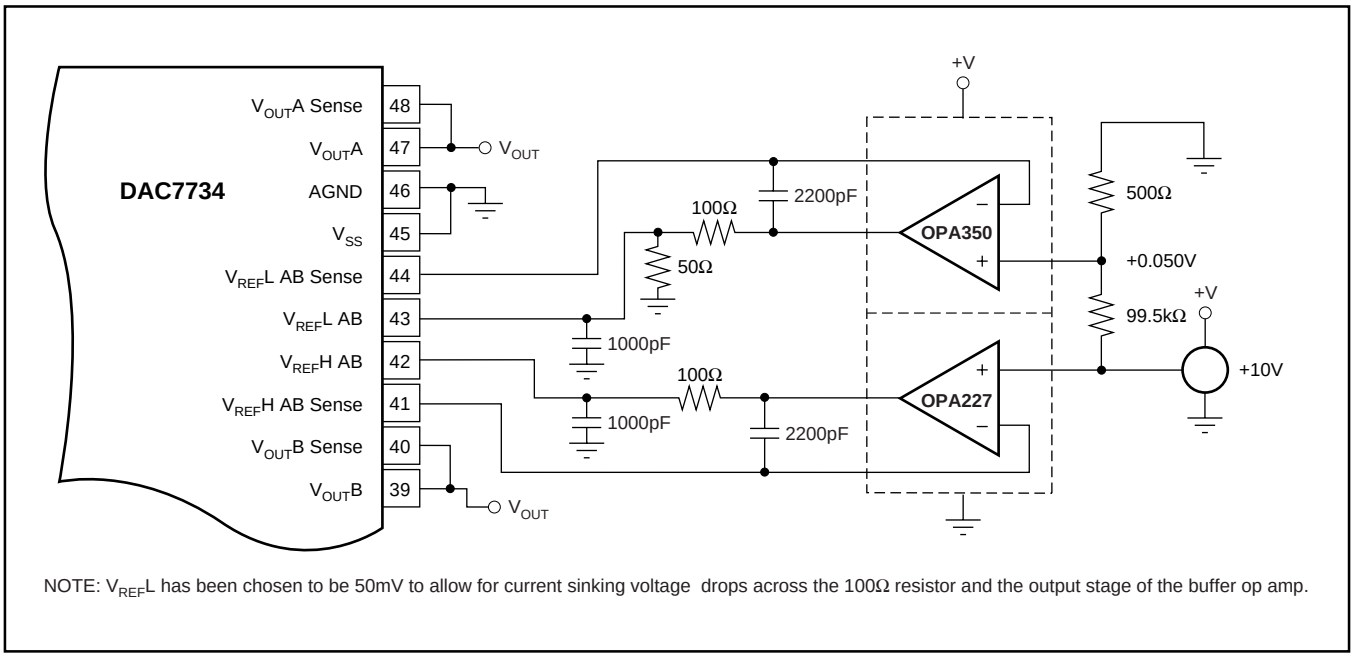


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV used for Single-Supply Performance Curves (1/2 DAC7734).

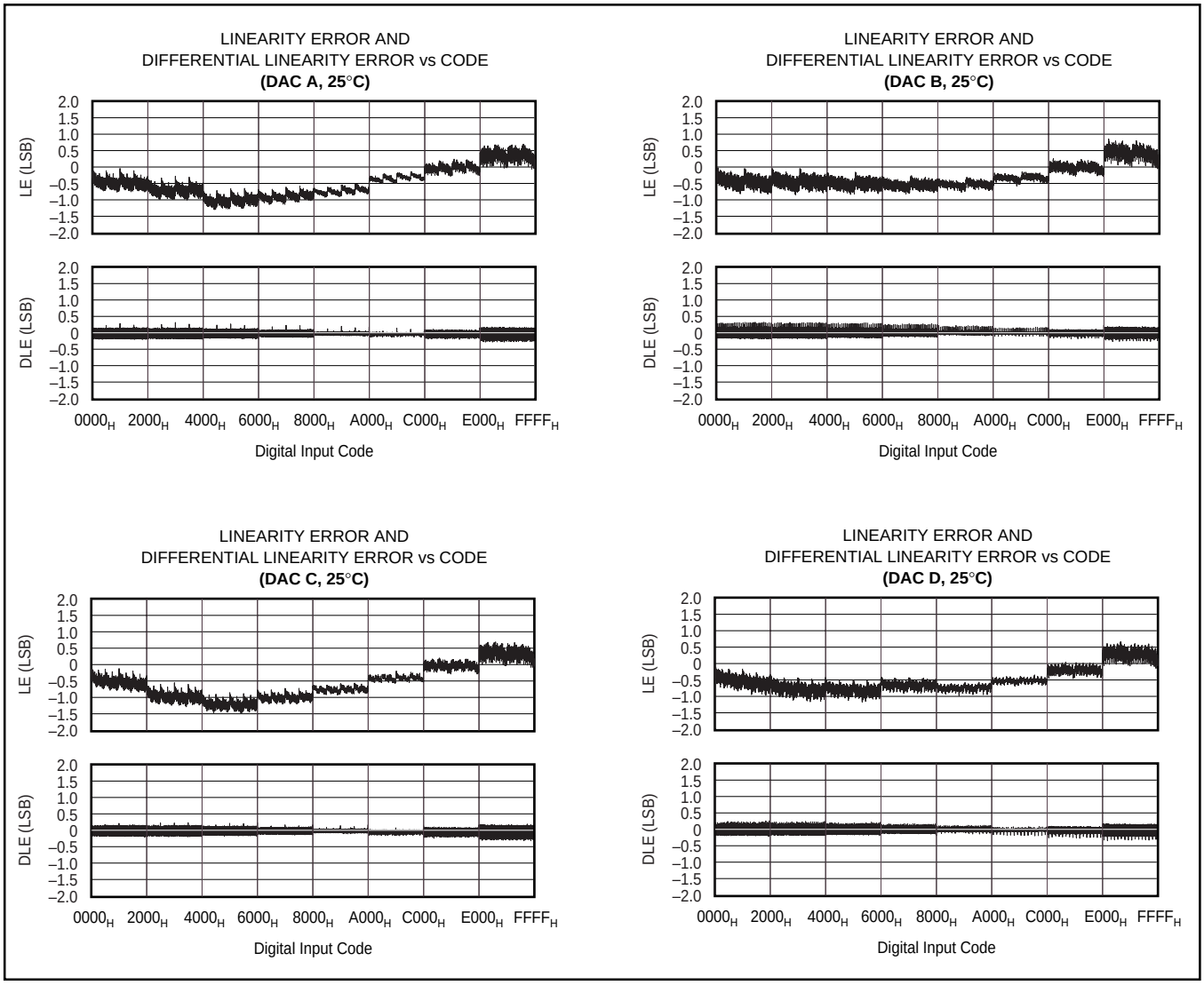


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 8.

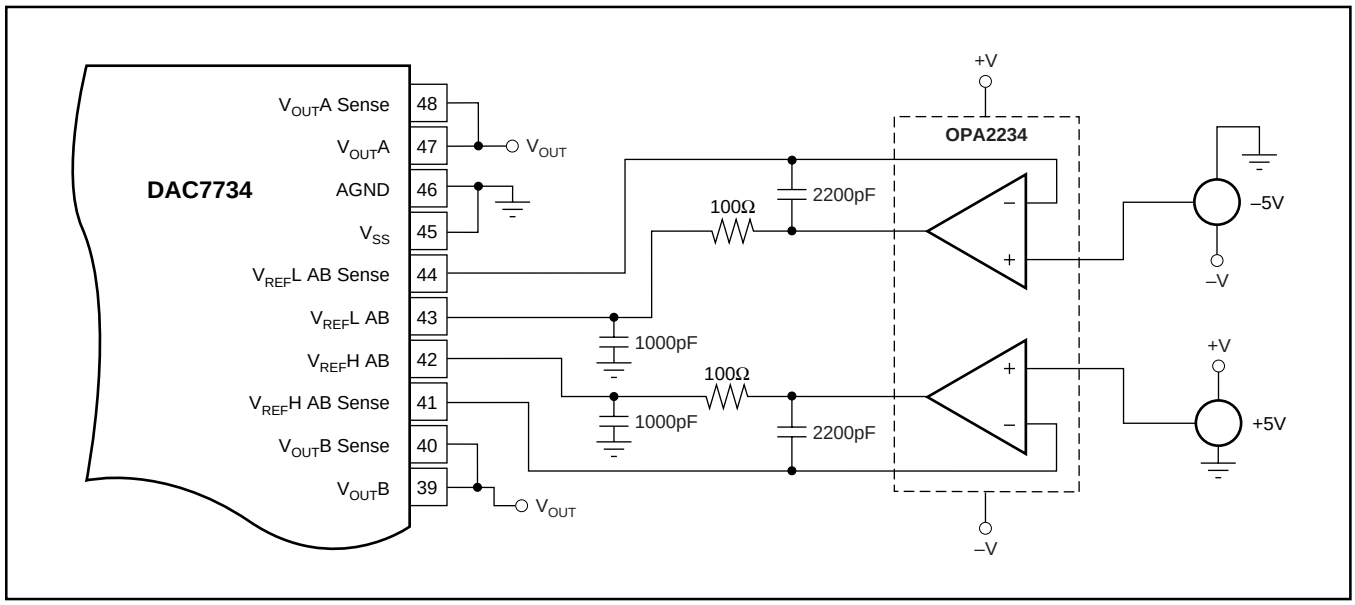
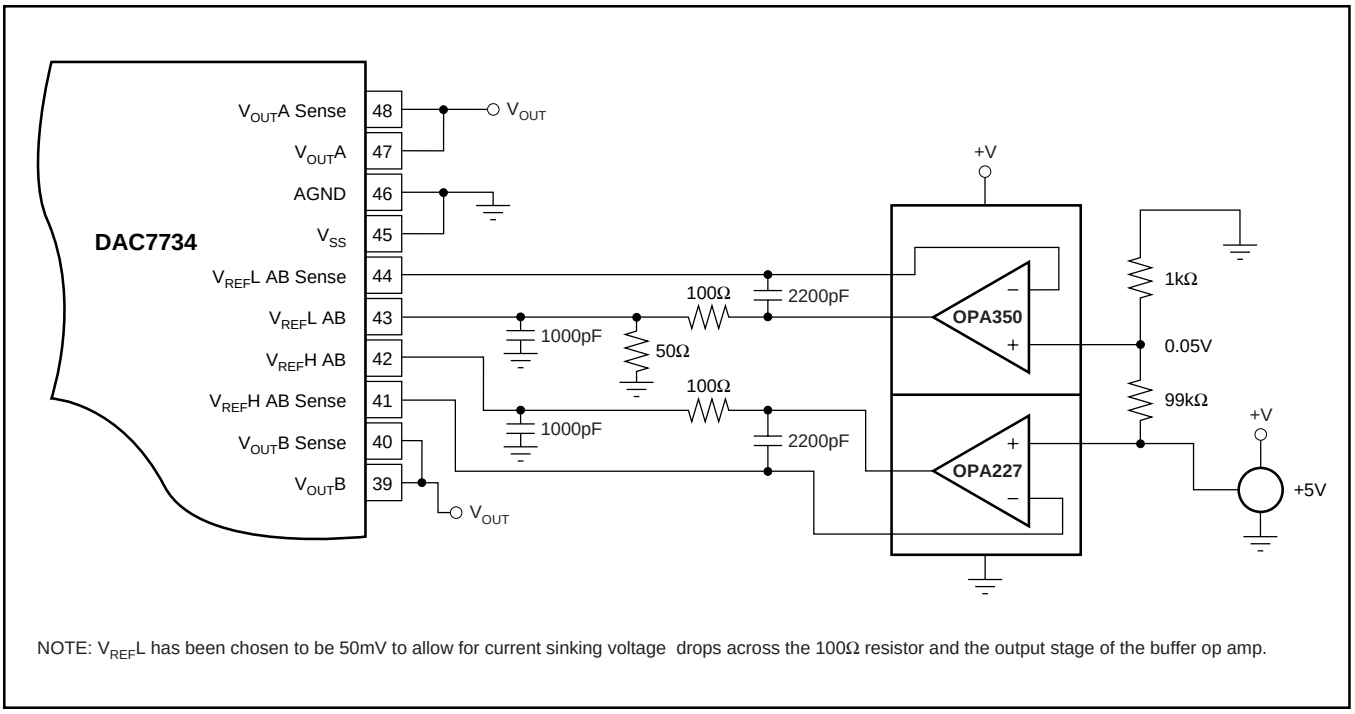


FIGURE 8. Dual-Supply Buffered Reference with $V_{REF}L$ = –5V and $V_{REF}H$ = +5V (1/2 DAC7734).



NOTE: V_{REF}L has been chosen to be 50mV to allow for current sinking voltage drops across the 100Ω resistor and the output stage of the buffer op amp.

FIGURE 9. Single-Supply Buffered Reference with a Reference Low of 50mV and Reference High of +5V.

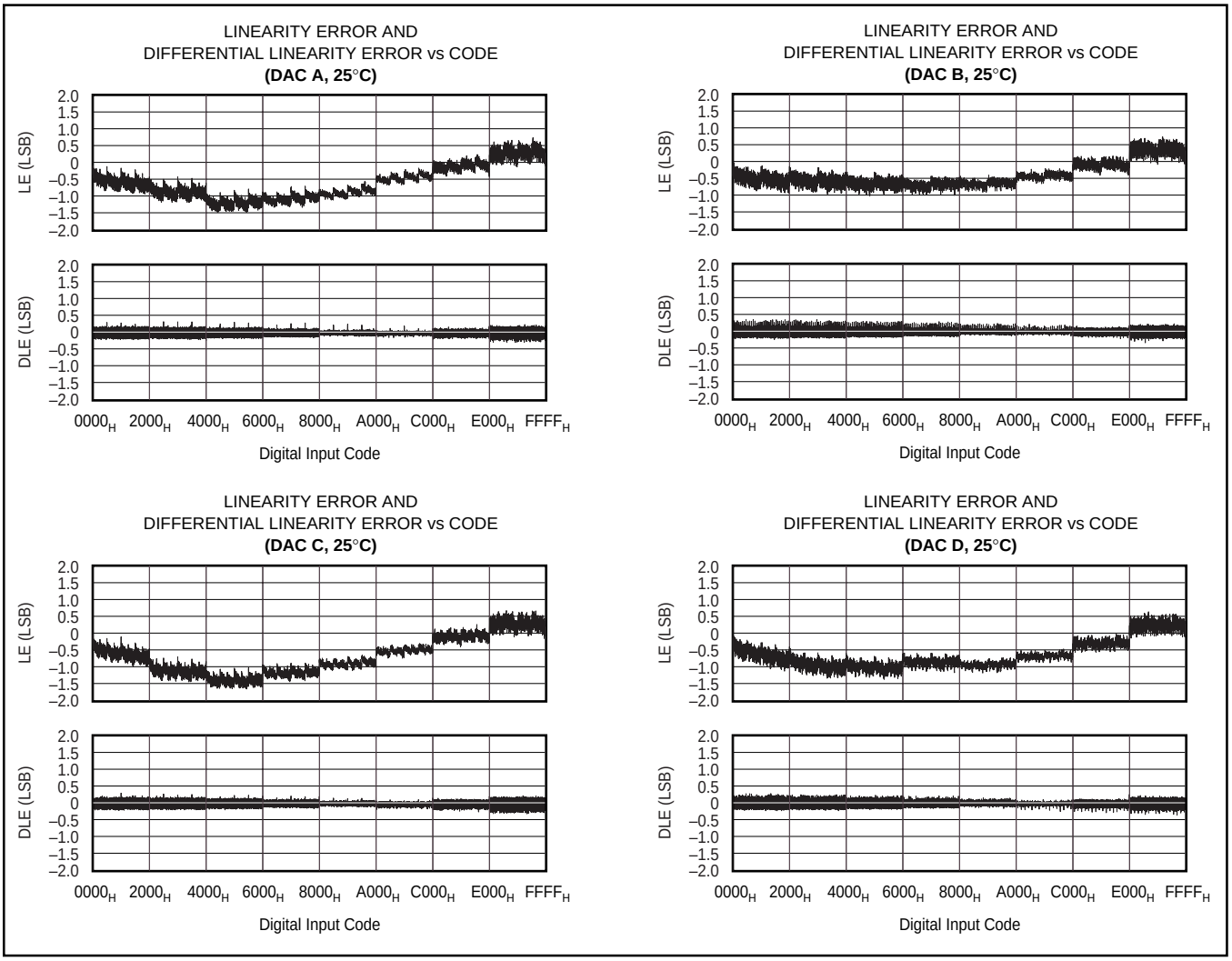


FIGURE 10. Integral Linearity and Differential Linearity Error Curves for Figure 9.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7734. The interface consists of a Signal Data Clock (CLK) input, Serial Data (SDI), DAC Input Register Load Control Signal ($\overline{LOAD}$), and DAC Register Load Control Signal (LDAC). In addition, a Chip Select ($\overline{CS}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous Reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Table I). The first two bits shifted into the shift register, B23 and B22, are the DAC register address. These bits select the input register that will be updated when $\overline{LOAD}$ goes LOW. The third bit, B21, is a "Quick Load" bit such that if HIGH, the code in the shift register is loaded into ALL DAC input registers when the $\overline{LOAD}$ signal goes LOW, independent of the state of the address bits, B23 and B22. If the "Quick Load" bit is LOW, the contents of the shift register is loaded only to the DAC register that is addressed. Bits B20 through B16 are not used and can assume any logical value. The last sixteen bits, B15 through B0, make up the DAC code to be loaded into the selected input register.

The internal DAC register is edge-triggered and not level-triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level triggered via the $\overline{LOAD}$ signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that $\overline{CS}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{CS}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{CS}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both $\overline{CS}$ and CLK are used, $\overline{CS}$ should rise only when CLK is HIGH. If not, then either $\overline{CS}$ or CLK can be used to operate the shift register. See Table II for more information.

$\overline{CS}$(1)	CLK(1)	$\overline{LOAD}$	RST	SERIAL SHIFT REGISTER
H(2)	X(3)	H	H	No Change
L(4)	L	H	H	No Change
L	↑(5)	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H(6)	X	L(7)	H	No Change
H(6)	X	H	↑(8)	No Change

NOTES: (1) $\overline{CS}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{LOAD}$ is LOW, the selected DAC register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A1	A0	$\overline{CS}$	RST	RSTSEL	LDAC	$\overline{LOAD}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write Input	A
L	H	L	H	X	X	L	Write	Hold	Write Input	B
H	L	L	H	X	X	L	Write	Hold	Write Input	C
H	H	L	H	X	X	L	Write	Hold	Write Input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero	All
X	X	X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7734 Logic Truth Table.

SERIAL-DATA OUTPUT

The Serial-Data Output (SDO) is the internal shift register output. For DAC7734, the SDO is a driven output and does not require an external pull-up. Any number of DAC7734s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 11.

DIGITAL TIMING

Figure 12 and Table III provide detailed timing for the digital interface of the DAC7734.

DIGITAL INPUT CODING

The DAC7734 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REF}L + \frac{\left(V_{REF}H - V_{REF}L\right) \bullet N}{65,536} \qquad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7734 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7734 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \bullet \left(\frac{N}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \qquad (2)$$

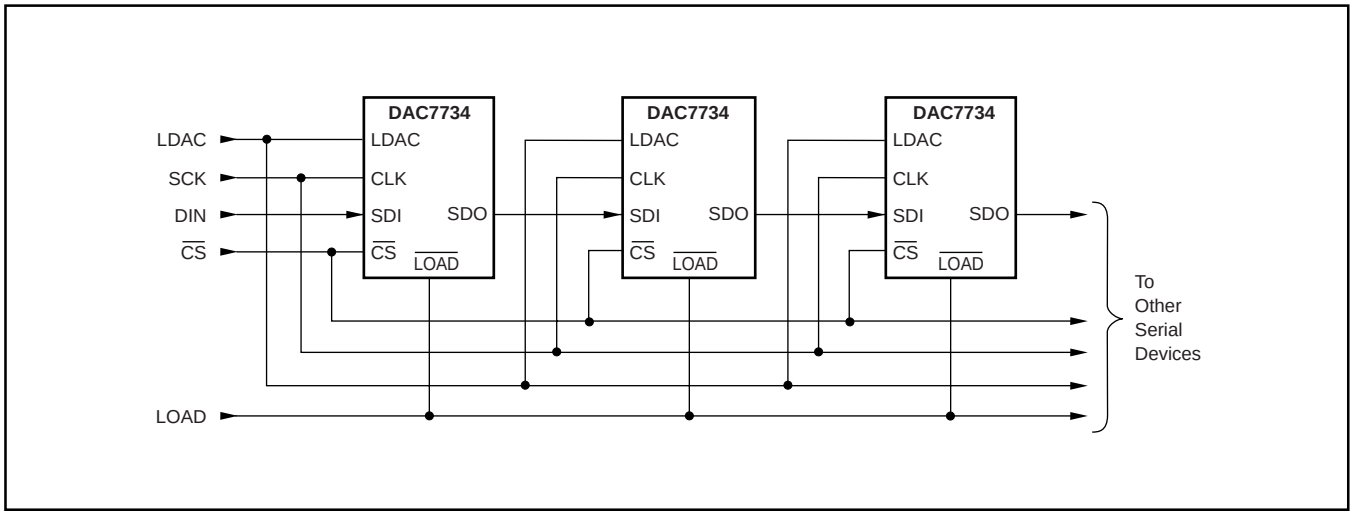


FIGURE 11. Daisy-Chaining DAC7734.

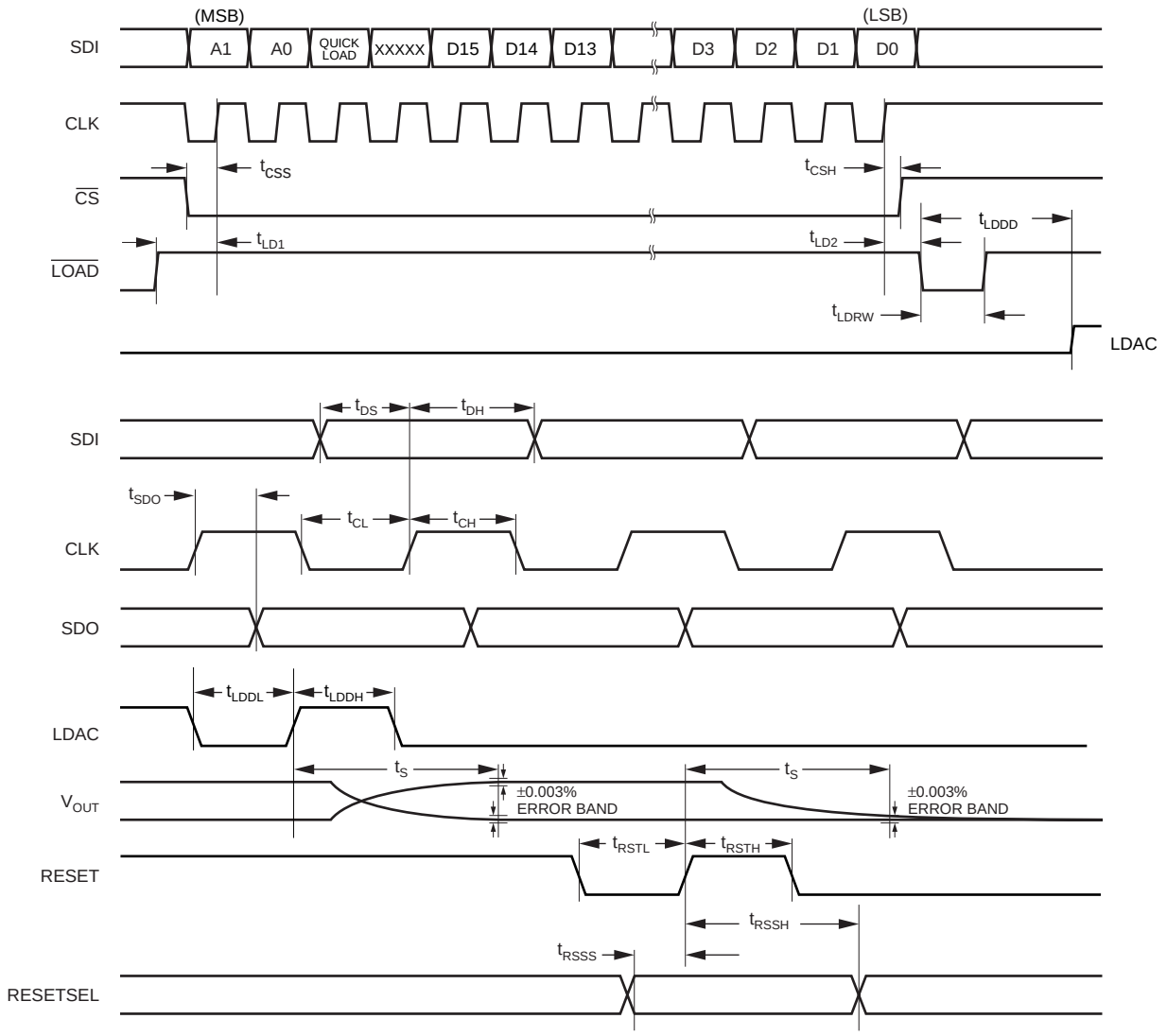


FIGURE 12. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	10		ns
t_{DH}	Data Held Valid after CLK Rises	20		ns
t_{CH}	CLK HIGH	25		ns
t_{CL}	CLK LOW	25		ns
t_{CSS}	$\overline{CS}$ LOW to CLK Rising	15		ns
t_{CSH}	CLK HIGH to $\overline{CS}$ Rising	0		ns
t_{LD1}	$\overline{LOAD}$ HIGH to CLK Rising	10		ns
t_{LD2}	CLK Rising to $\overline{LOAD}$ LOW	30		ns
t_{LDRW}	$\overline{LOAD}$ LOW Time	30		ns
t_{LDDL}	LDAC LOW Time	40		ns
t_{LDDH}	LDAC HIGH Time	40		ns
t_{SDO}	SDO Propagation Delay	10	45	ns
t_{RSSS}	RESETSEL Valid to RESET HIGH	0		ns
t_{RSSH}	RESET HIGH to RESETSEL Not Valid	100		ns
t_{RSTL}	RESET LOW Time	10		ns
t_{RSTH}	RESET HIGH Time	10		ns
t_{LDDD}	$\overline{LOAD}$ LOW to LDAC Rising Time	40		ns
t_S	Settling Time		11 (dual) /10(single)	µs

TABLE III. Timing Specifications (T_A = –40°C to +85°C).

Figure 13 shows a DAC7734 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{5V - 1V}{250\Omega}\right) \bullet \left(\frac{N}{65,536}\right)\right) + \left(\frac{1V}{250\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale, the output current is the offset current of 4mA (1V/250Ω).

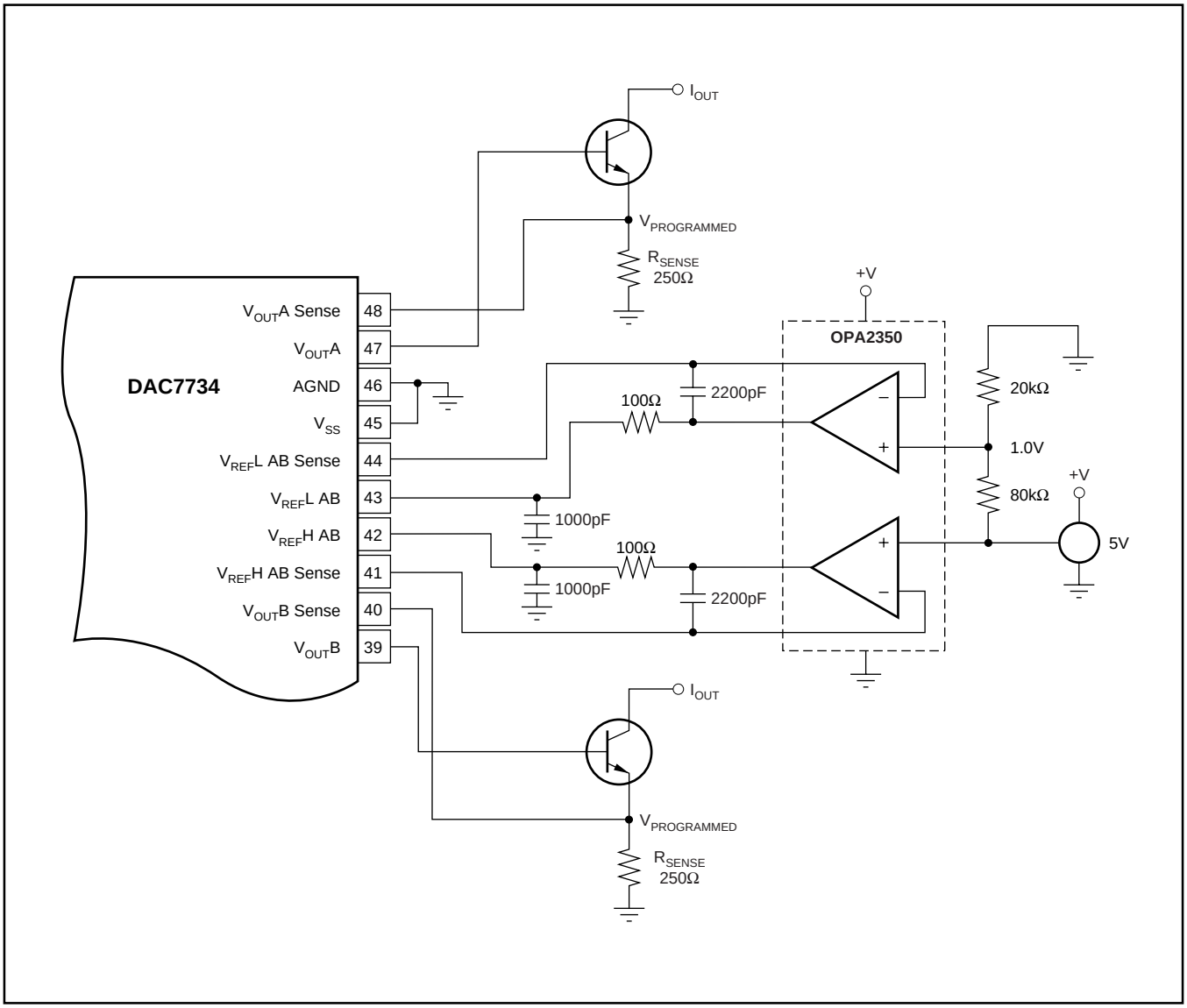


FIGURE 13. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7734).

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/08	A	1	—	Updated front page format to current standard; some page layout changed.
		23	Table III	Changed symbol from "t_{LDDWL}" to "t_{LDDL}" (typo).

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7734E	ACTIVE	SSOP	DL	48	25	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7734E	Samples
DAC7734E/1K	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E	Samples
DAC7734EB	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E B	Samples
DAC7734EC	ACTIVE	SSOP	DL	48	25	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7734E C	Samples
DAC7734EC/1K	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7734E C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

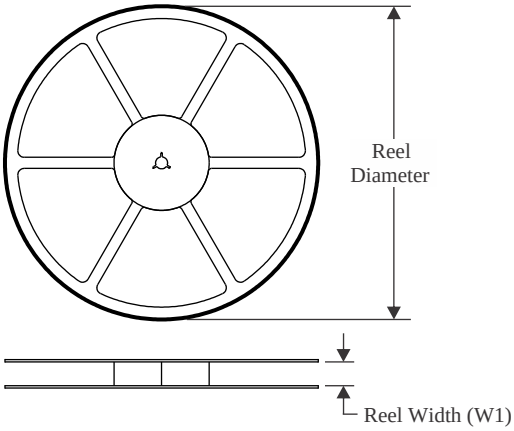
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

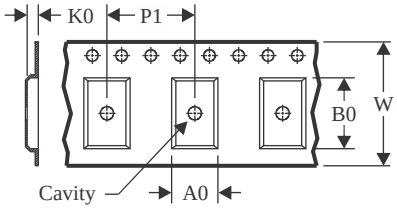
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

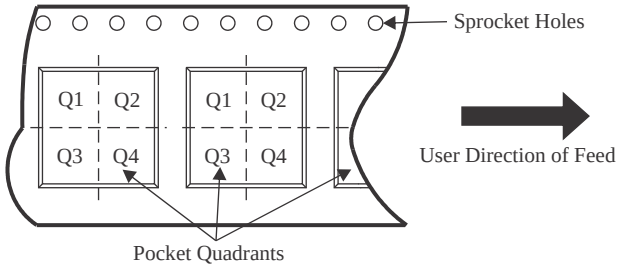


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

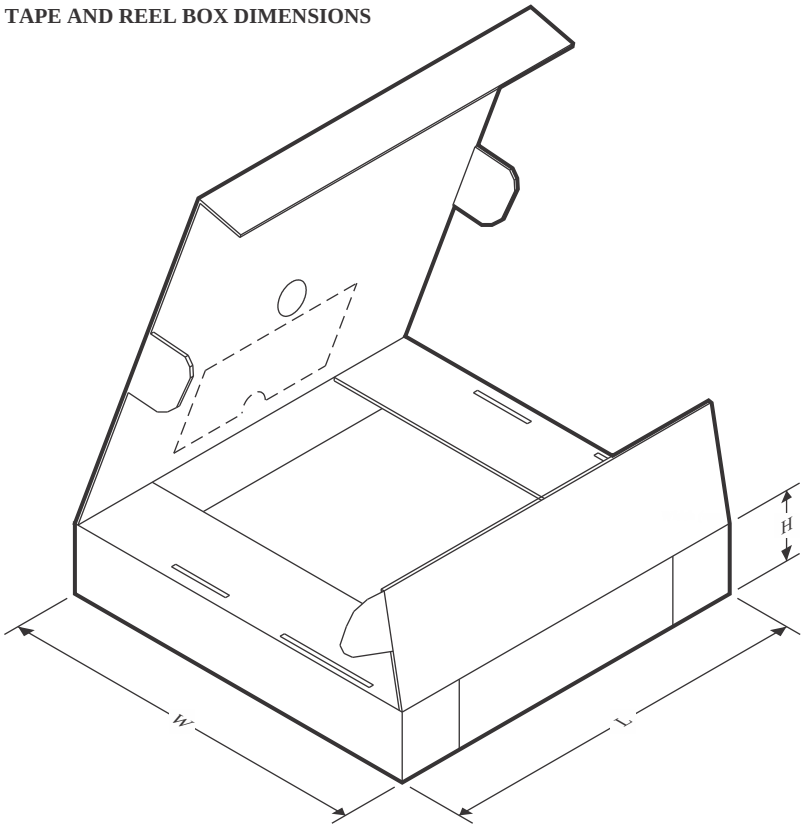
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7734E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
DAC7734EC/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

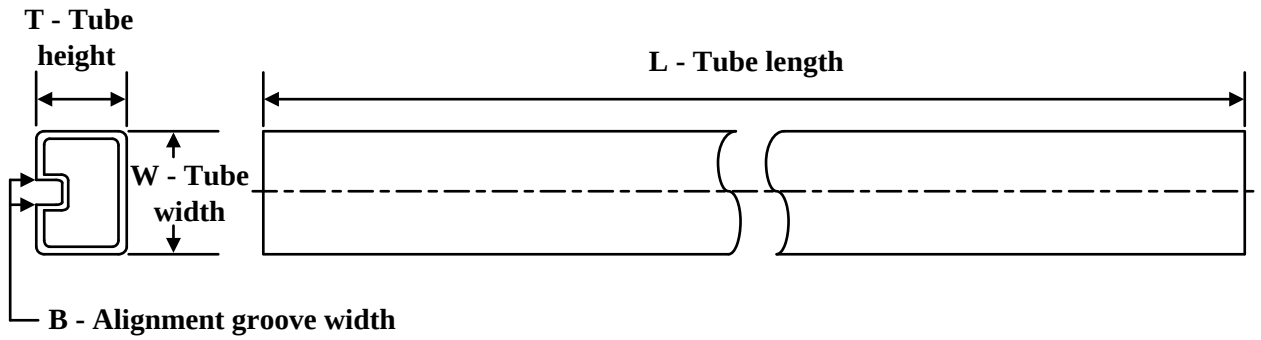
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7734E/1K	SSOP	DL	48	1000	367.0	367.0	55.0
DAC7734EC/1K	SSOP	DL	48	1000	367.0	367.0	55.0

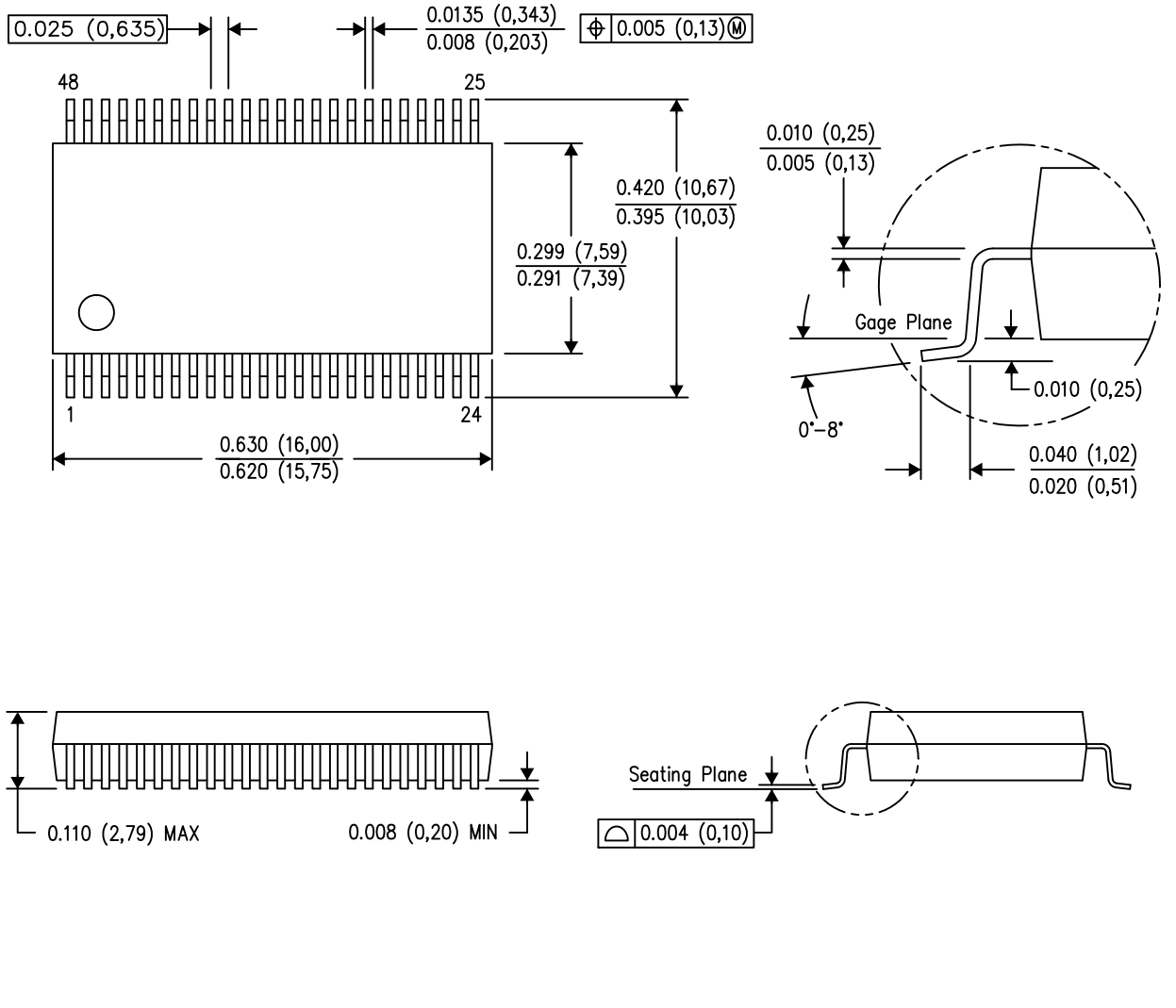
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7734E	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7734EB	DL	SSOP	48	25	473.7	14.24	5110	7.87
DAC7734EC	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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