THE DATASHEET OF

LTC3419IMS-1#PBF

Dual Monolithic 600mA Synchronous Step-Down Regulator

FEATURES

- **High Efficiency Dual Step-Down Outputs: Up to 96%**
- **600mA Current per Channel at V_{IN} = 3V**
- **Only 35µA Quiescent Current During Operation (Both Channels)**
- **2.25MHz Constant-Frequency Operation**
- **2.5V to 5.5V Input Voltage Range**
- **Low Dropout Operation: 100% Duty Cycle**
- **No Schottky Diodes Required**
- **Internally Compensated for All Ceramic Capacitors**
- **Independent Internal Soft-Start for Each Channel**
- Available in Fixed Output Versions
- Current Mode Operation for Excellent Line and Load Transient Response
- 0.6V Reference Allows Low Output Voltages
- User-Selectable Burst Mode® Operation
- Short-Circuit Protected
- Ultralow Shutdown Current: I_Q < 1µA
- Available in Small MSOP or 3mm × 3mm DFN-8 Packages

APPLICATIONS

- Cellular Telephones
- Digital Still Cameras
- Wireless and DSL Modems
- Portable Media Players
- PDAs/Palmtop PCs

DESCRIPTION

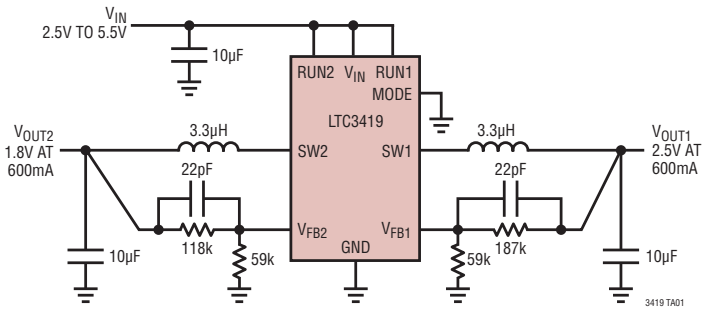
The LTC®3419 is a dual, 2.25MHz, constant-frequency, synchronous step-down DC/DC converter in a tiny 3mm × 3mm DFN package. 100% duty cycle provides low dropout operation, extending battery life in portable systems. Low output voltages are supported with the 0.6V feedback reference voltage. Each regulator can supply 600mA output current.

The input voltage range is 2.5V to 5.5V, making it ideal for Li-Ion and USB powered applications. Supply current during operation is only 35µA and drops to <1µA in shutdown. A user-selectable mode input allows the user to trade off between high efficiency Burst Mode operation and pulse-skipping mode.

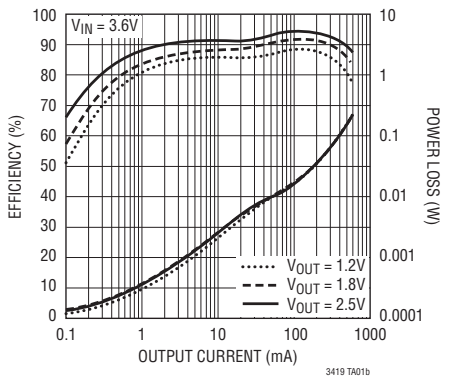
An internally set 2.25MHz switching frequency allows the use of tiny surface mount inductors and capacitors. Internal soft-start reduces inrush current during start-up. Both outputs are internally compensated to work with ceramic output capacitors. The LTC3419 is available in a low profile (0.75mm) 3mm × 3mm DFN package. The LTC3419 is also available in a fixed output voltage configuration selected via internal resistor dividers (see Table 2).

TYPICAL APPLICATION

Dual Monolithic Buck Regulator in 8-Lead 3 × 3 DFN



Efficiency and Power Loss vs Output Current

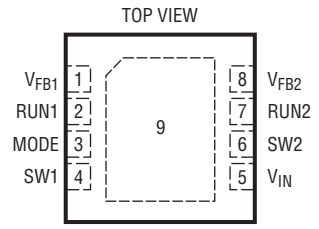


ABSOLUTE MAXIMUM RATINGS

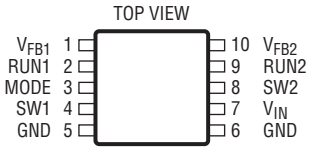
(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3 to 6V
V_{FB1}, V_{FB2} ..... –0.3V to V_{IN} + 0.3V
RUN1, RUN2, MODE ..... –0.3V to V_{IN} + 0.3V
SW1, SW2 ..... –0.3V to V_{IN} + 0.3V
P-Channel SW Source Current (DC) (Note 2) 800mA
N-Channel SW Source Current (DC) (Note 2) 800mA
Peak SW Source and Sink Current (Note 2) 1.3A
Operating Junction Temperature Range
(Note 3) ..... –40 to 125°C
Junction Temperature (Note 6) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSOP Package ..... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3419EDD#PBF	LTC3419EDD#TRPBF	LCQJ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3419EDD-1#PBF	LTC3419EDD-1#TRPBF	LCWW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3419IDD#PBF	LTC3419IDD#TRPBF	LCQJ	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3419IDD-1#PBF	LTC3419IDD-1#TRPBF	LCWW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3419EMS#PBF	LTC3419EMS#TRPBF	LTCQK	10-Lead Plastic MSOP	–40°C to 125°C
LTC3419EMS-1#PBF	LTC3419EMS-1#TRPBF	LTCWX	10-Lead Plastic MSOP	–40°C to 125°C
LTC3419IMS#PBF	LTC3419IMS#TRPBF	LTCQK	10-Lead Plastic MSOP	–40°C to 125°C
LTC3419IMS-1#PBF	LTC3419IMS-1#TRPBF	LTCWX	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Operating Voltage		●	2.5		5.5	V
V_{UV}	V_{IN} Undervoltage Lockout	V_{IN} Low to High	●		2.1	2.5	V
I_{FB}	Feedback Pin Input Current	LTC3419 LTC3419-1	● ●		 3	±30 5	nA µA
V_{FBREG1}	Regulated Feedback Voltage (Channel 1)	LTC3419E, 0°C < T_J < 85°C LTC3419E, –40°C < T_J < 85°C LTC3419E-1, –40°C < T_J < 85°C LTC3419I, –40°C < T_J < 125°C LTC3419I-1, –40°C < T_J < 125°C	 ● ● ● ●	0.590 0.588 1.544 0.582 1.533	0.600 0.600 1.575 0.6 1.575	0.610 0.612 1.606 0.618 1.617	V V V V V
V_{FBREG2}	Regulated Feedback Voltage (Channel 2)	LTC3419E, 0°C < T_J < 85°C LTC3419E, –40°C < T_J < 85°C LTC3419E-1, –40°C < T_J < 85°C LTC3419I, –40°C < T_J < 125°C LTC3419I-1, –40°C < T_J < 125°C	 ● ● ● ●	0.590 0.588 1.764 0.582 1.753	0.600 0.600 1.8 0.6 1.8	0.610 0.612 1.836 0.618 1.847	V V V V V
$\Delta V_{LINE\ REG}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 7)			0.3	0.5	%/V
$\Delta V_{LOAD\ REG}$	Output Voltage Load Regulation	I_{LOAD} = 0mA to 600mA (Note 7)			0.5		%
I_S	Input DC Supply Current Active Mode (Note 4) Sleep Mode Shutdown	 $V_{FB1} = V_{FB2} = 0.95 \times V_{FBREG}$ $V_{FB1} = V_{FB2} = 1.05 \times V_{FBREG}$, V_{IN} = 5.5V RUN1 = RUN2 = 0V, V_{IN} = 5.5V			 500 35 0.1	 700 60 1	 µA µA µA
f_{OSC}	Oscillator Frequency	$V_{FB} = V_{FBREG}$	●	1.8	2.25	2.7	MHz
I_{LIM}	Peak Switch Current Limit Channel 1 (600mA) Channel 2 (600mA)	V_{IN} = 3V, $V_{FB} < V_{FBREG}$, Duty Cycle < 35%		 900 900	 1200 1200	 	 mA mA
$R_{DS(ON)}$	Channel 1 (Note 5) Top Switch On-Resistance Bottom Switch On-Resistance Channel 2 (Note 5) Top Switch On-Resistance Bottom Switch On-Resistance	 V_{IN} = 3.6V, I_{SW} = 100mA V_{IN} = 3.6V, I_{SW} = 100mA V_{IN} = 3.6V, I_{SW} = 100mA V_{IN} = 3.6V, I_{SW} = 100mA			 0.4 0.4 0.4 0.4	 0.6 0.6 0.6 0.6	 Ω Ω Ω Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5V, V_{RUN} = 0V			0.01	1	µA
$t_{SOFTSTART}$	Soft-Start Time	V_{FB} from 10% to 90% Full Scale		0.1	0.95	1.3	ms
V_{RUN}	RUN Threshold High		●	0.4	1	1.2	V
I_{RUN}	RUN Leakage Current		●		0.01	1	µA
V_{MODE}	MODE Threshold High		●	0.4	1	1.2	V
I_{MODE}	MODE Leakage Current		●		0.01	1	µA
V_{BURST}	Output Ripple in Burst Mode Operation	V_{OUT} = 1.5V, C_{OUT} = 10µF			20		mV_{P-P}

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by long term current density limitations.

Note 3: The LTC3419E and LTC3419E-1 are guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3419I and LTC3419I-1 are guaranteed to meet specified performance over the full –40°C to 125°C operating junction temperature range.

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: The DFN switch on-resistance is guaranteed by correlation to wafer level measurements.

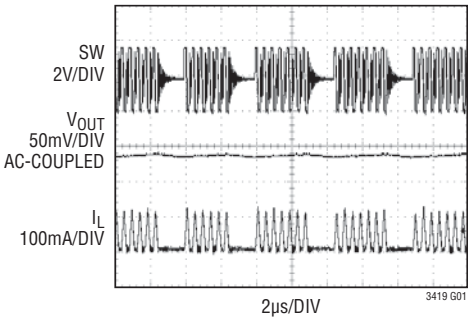
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: The converter is tested in a proprietary test mode that connects the output of the error amplifier to the SW pin, which is connected to an external servo loop.

TYPICAL PERFORMANCE CHARACTERISTICS

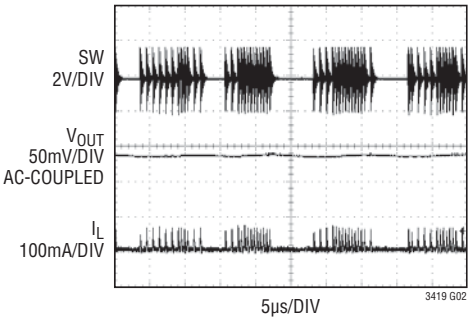
T_A = 25°C, V_{IN} = 3.6V, unless otherwise noted.

Burst Mode Operation



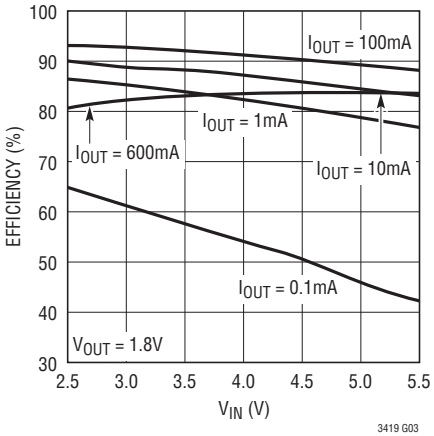
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 25mA

Pulse Skip Mode Operation

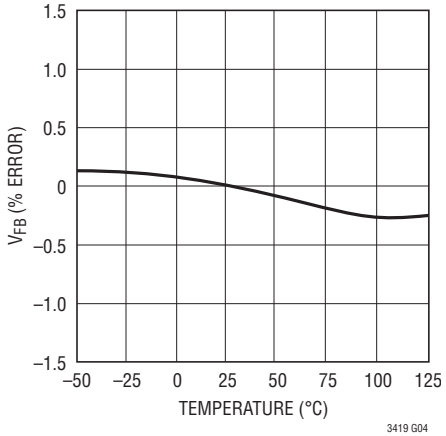


V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 5mA

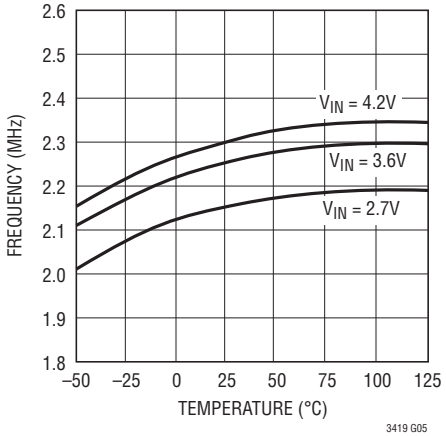
Efficiency vs Input Voltage



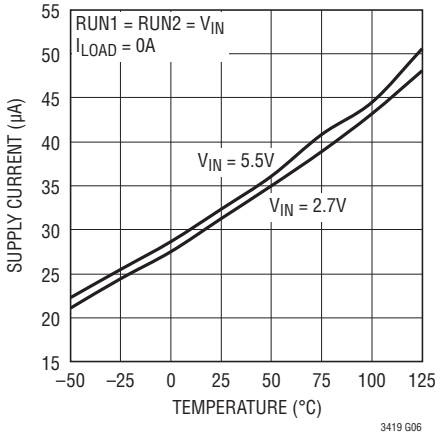
Reference Voltage vs Temperature



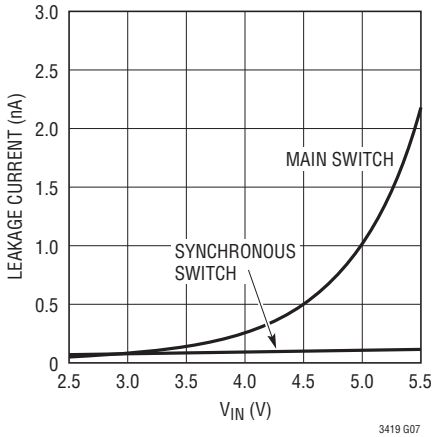
Oscillator Frequency vs Temperature



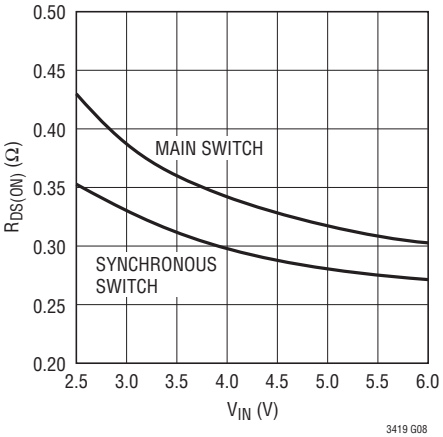
Supply Current vs Temperature



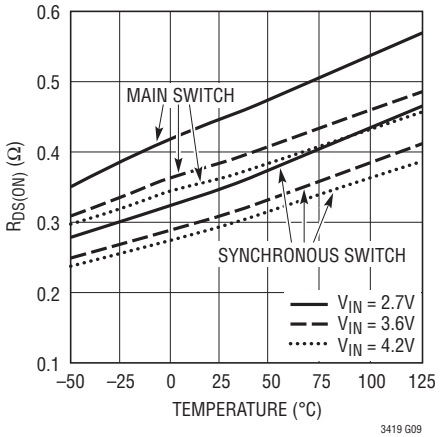
Switch Leakage vs Input Voltage



Switch On-Resistance vs Input Voltage



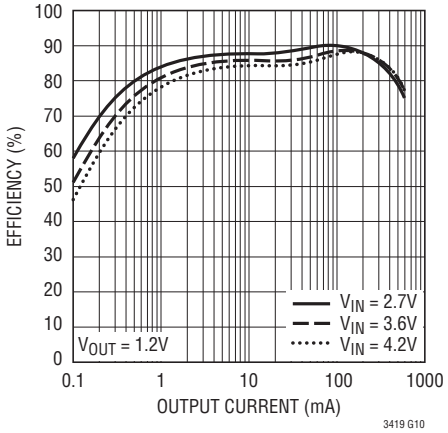
Switch On-Resistance vs Temperature



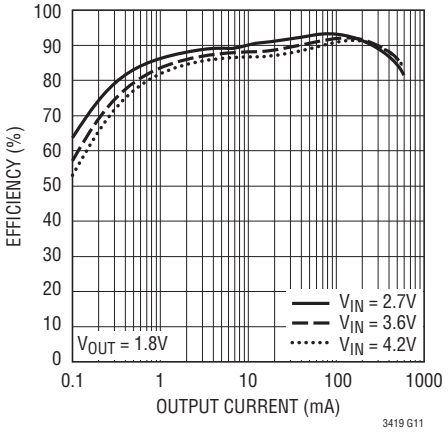
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.6V, unless otherwise noted.

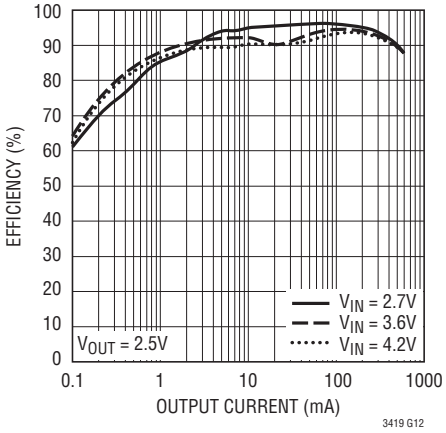
Efficiency vs Load Current



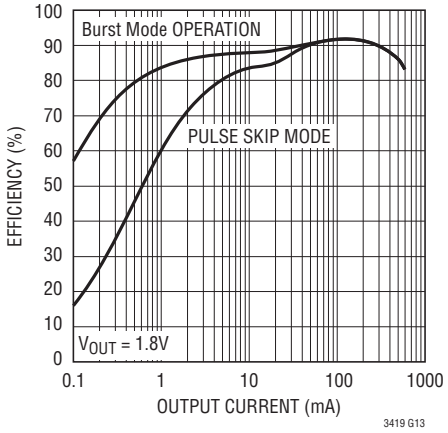
Efficiency vs Load Current



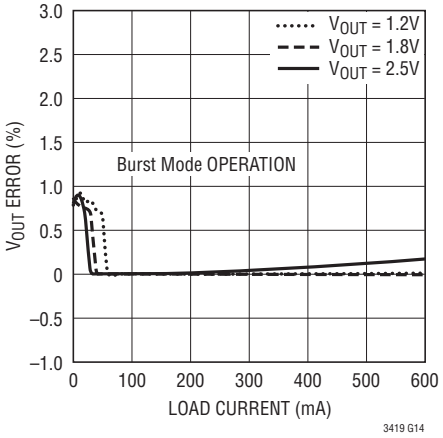
Efficiency vs Load Current



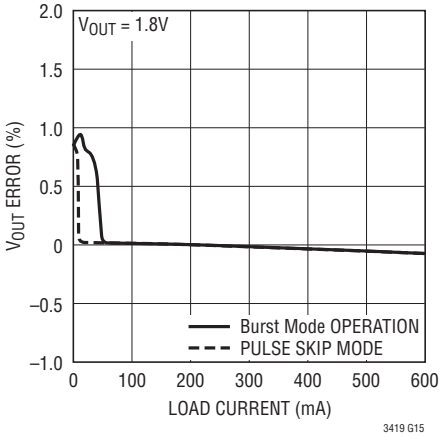
Efficiency vs Load Current



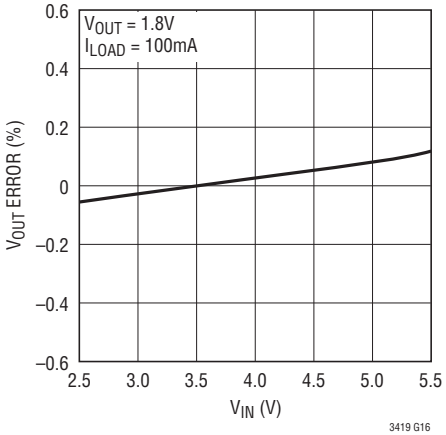
Load Regulation



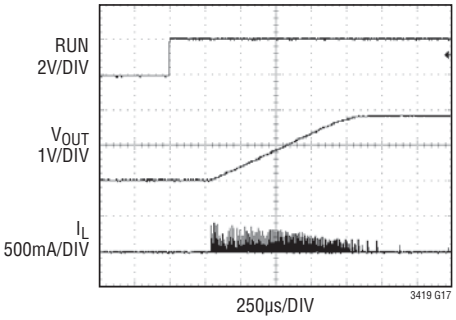
Load Regulation



Line Regulation

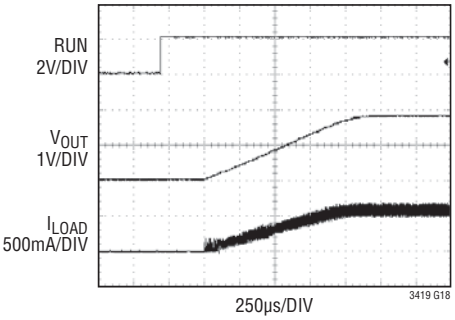


Start-Up from Shutdown



V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A

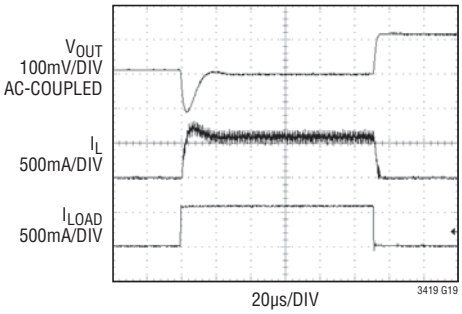
Start-Up from Shutdown



V_{IN} = 3.6V
V_{OUT} = 1.8V
R_{LOAD} = 3Ω

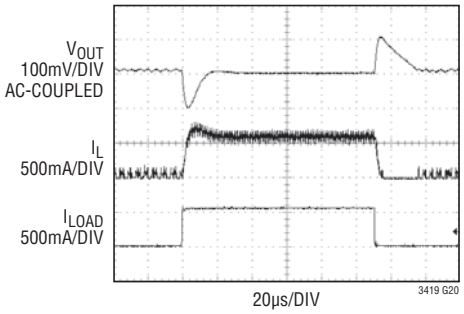
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{IN} = 3.6V, unless otherwise noted.

Load Step



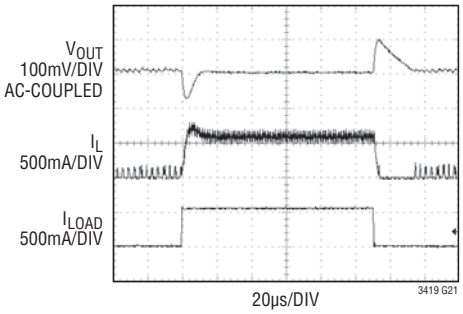
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A TO 600mA

Load Step



V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 40mA TO 600mA

Load Step



V_{IN} = 3.6V
V_{OUT} = 1.2V
I_{LOAD} = 40mA TO 600mA

PIN FUNCTIONS (DD/MS)

V_{FB1} (Pin 1/Pin 1): Regulator 1 Output Feedback. Receives the feedback voltage from the external resistive divider across the regulator 1 output. Nominal voltage for this pin is 0.6V.

RUN1 (Pin 2/Pin 2): Regulator 1 Enable. Forcing this pin to V_{IN} enables regulator 1, while forcing it to GND causes regulator 1 to shut down.

MODE (Pin 3/Pin 3): Mode Select Input. To select pulse-skipping mode, tie to V_{IN}. Grounding this pin selects Burst Mode operation. Do not leave this pin floating.

SW1 (Pin 4/Pin 4): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

V_{IN} (Pin 5/Pin 7): Main Power Supply. Must be closely de-coupled to GND.

SW2 (Pin 6/Pin 8): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

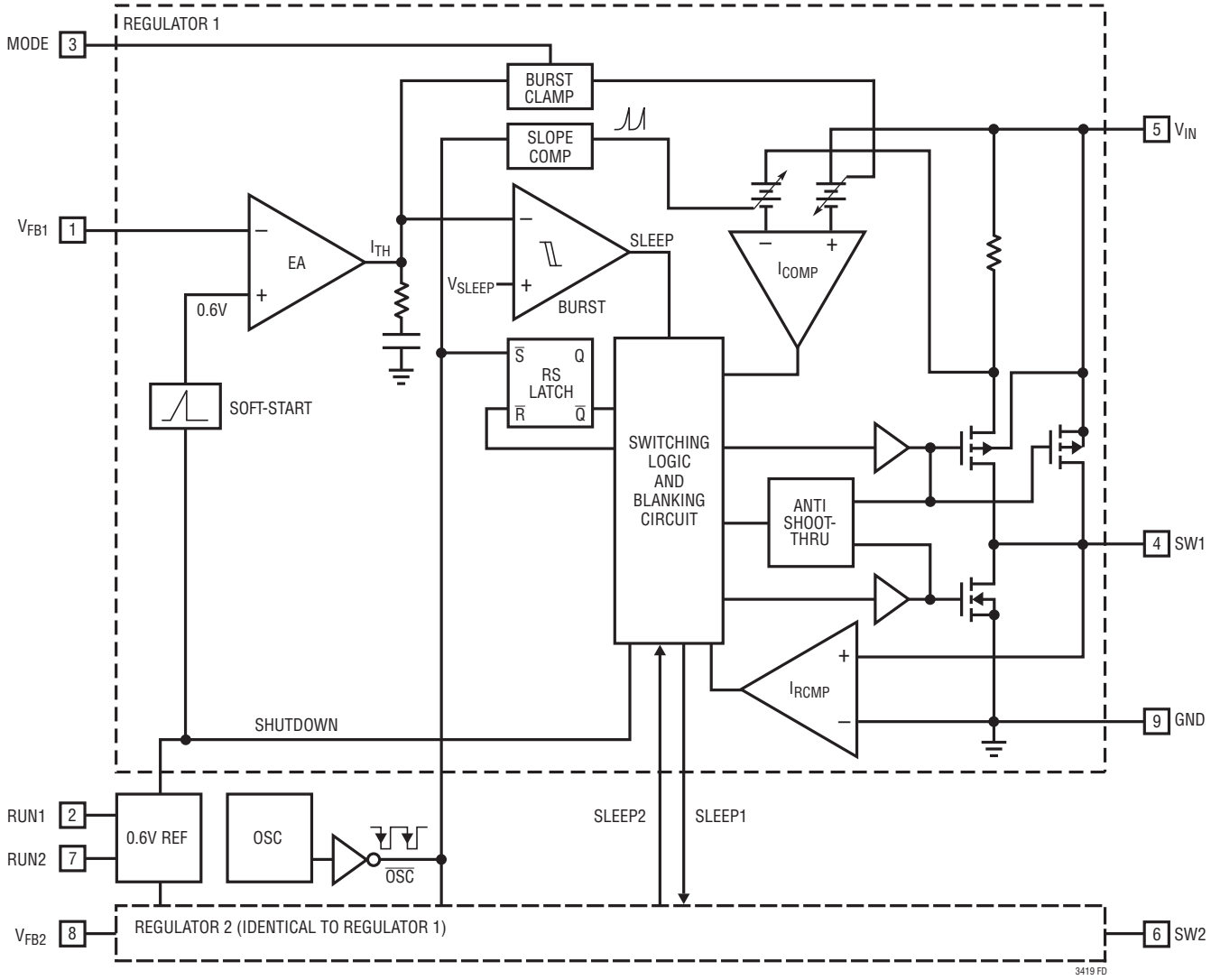
RUN2 (Pin 7/Pin 9): Regulator 2 Enable. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down.

V_{FB2} (Pin 8/Pin 10): Regulator 2 Output Feedback. Receives the feedback voltage from the external resistive divider across the regulator 2 output. Nominal voltage for this pin is 0.6V.

Exposed Pad (Pin 9/NA): Ground. The Exposed Pad must be soldered to PCB for optimal thermal performance.

GND (NA/Pins 5, 6): Ground. Connect to the (–) terminal of C_{OUT}, and the (–) terminal of C_{IN}. Pin 5 of the MS package must be soldered to the PC board for optimal thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

The LTC3419 uses a constant-frequency, current mode architecture. The operating frequency is set at 2.25MHz. Both channels share the same clock and run in-phase.

The output voltage is set by an external resistor divider returned to the V_{FB} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and regulates the peak inductor current accordingly.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the peak inductor current (controlled by I_{TH}) is reached. The RS latch turns off the synchronous switch and energy stored in the inductor is discharged through the bottom switch (N-channel MOSFET) into the load until the next clock cycle begins, or until the inductor current begins to reverse (sensed by the I_{RCMP} comparator).

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier regulates the V_{FB} pin to the internal 0.6V reference by adjusting the peak inductor current accordingly.

Light Load Operation

There are two modes to control the LTC3419 at light load currents: Burst Mode operation and pulse-skipping mode. Both automatically transition from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by grounding the MODE pin. When the load is relatively light, the peak inductor current (as set by I_{TH}) remains fixed at approximately 60mA and the PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized.

The duration of each burst event can range from a few cycles at light load to almost continuous cycling with short sleep intervals at moderate loads. During the sleep intervals, the load current is being supplied solely from the output capacitor. As the output voltage droops, the error amplifier output rises above the sleep threshold, signaling the burst comparator to trip and turn the top MOSFET on. This cycle repeats at a rate that is dependent on load demand.

For applications where low ripple voltage and constant-frequency operation is a higher priority than light load efficiency, pulse-skipping mode can be used by connecting the MODE pin to V_{IN}. In this mode, the peak inductor current is not fixed, which allows the LTC3419 to switch at a constant-frequency down to very low currents, where it will begin skipping pulses.

Dropout Operation

When the input supply voltage decreases toward the output voltage the duty cycle increases to 100%, which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the worst-case power dissipation when the LTC3419 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Soft-Start

In order to minimize the inrush current on the input bypass capacitor, the LTC3419 slowly ramps up the output voltage during start-up. Whenever the RUN1 or RUN2 pin is pulled high, the corresponding output will ramp from zero to full-scale over a time period of approximately 750µs. This prevents the LTC3419 from having to quickly charge the output capacitor and thus supplying an excessive amount of instantaneous current.

Short-Circuit Protection

When either regulator output is shorted to ground, the corresponding internal N-channel switch is forced on for a longer time period for each cycle in order to allow the inductor to discharge, thus preventing inductor current runaway. This technique has the effect of decreasing switching frequency. Once the short is removed, normal operation resumes and the regulator output will return to its nominal voltage.

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A general LTC3419 application circuit is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is 40% of the maximum output load current. So, for a 600mA regulator, ΔI_L = 240mA (40% of 600mA).

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the internal burst clamp. Lower inductor values result in higher ripple current which causes the transition to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. Furthermore, lower inductance values will cause the bursts to occur with increased frequency.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price versus size requirements, and any radiated field/EMI requirements, than on what the LTC3419 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3419 applications.

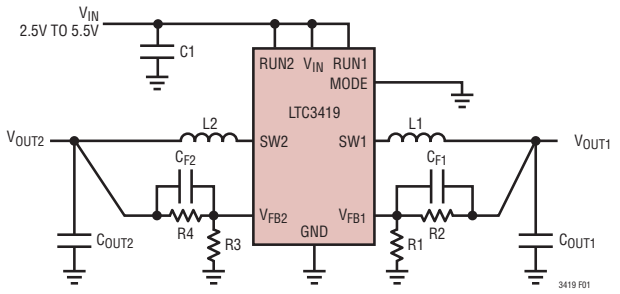

Figure 1. LTC3419 General Schematic

Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX DC CURRENT	DCR	HEIGHT
Taiyo Yuden	CB2016T2R2M CB2012T2R2M CB2016T3R3M	2.2µH 2.2µH 3.3µH	510mA 530mA 410mA	0.13Ω 0.33Ω 0.27Ω	1.6mm 1.25mm 1.6mm
Panasonic	ELT5KT4R7M	4.7µH	950mA	0.2Ω	1.2mm
Sumida	CDRH2D18/LD	4.7µH	630mA	0.086Ω	2mm
Murata	LQH32CN4R7M23	4.7µH	450mA	0.2Ω	2mm
Taiyo Yuden	NR30102R2M NR30104R7M	2.2µH 4.7µH	1100mA 750mA	0.1Ω 0.19Ω	1mm 1mm
FDK	FDKMIPF2520D FDKMIPF2520D FDKMIPF2520D	4.7µH 3.3µH 2.2µH	1100mA 1200mA 1300mA	0.11Ω 0.1Ω 0.08Ω	1mm 1mm 1mm
TDK	VLF3010AT4R7-MR70 VLF3010AT3R3-MR87 VLF3010AT2R2-M1R0	4.7µH 3.3µH 2.2µH	700mA 870mA 1000mA	0.28Ω 0.17Ω 0.12Ω	1mm 1mm 1mm

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$. This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant

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deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling when not using an all-ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_0 C_{OUT}} \right)$$

where f_0 = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

If tantalum capacitors are used, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3419 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part. For more information, see Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Setting the Output Voltage

The LTC3419 regulates the V_{FB1} and V_{FB2} pins to 0.6V during regulation. Thus, the output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \left(1 + \frac{R2}{R1} \right) \quad (2)$$

Keeping the current small (<10µA) in these resistors maximizes efficiency, but making it too small may allow stray capacitance to cause noise problems or reduce the phase margin of the error amp loop.

To improve the frequency response of the main control loop, a feedback capacitor (C_F) may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Fixed output versions of the LTC3419 (e.g. LTC3419-1) include an internal resistive divider, eliminating the need for external resistors. The resistor divider is chosen such that the V_{FB} input current is approximately 3µA. For these versions the V_{FB} pin should be connected directly to V_{OUT}. Table 2 lists the fixed output voltages available for the LTC3419.

Table 2. Fixed Output Voltage Versions

PART NUMBER	V_{OUT1}	V_{OUT2}
LTC3419	Adjustable	Adjustable
LTC3419-1	1.575V	1.8V

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Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine the phase margin. In addition, feedback capacitors (C_{F1} and C_{F2}) can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four sources usually account for the losses in LTC3419 circuits: 1) V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other system losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.
2. The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
3. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP}) \bullet (DC) + (R_{DS(ON)BOT}) \bullet (1 - DC)$$

Hot Swap is a trademark of Linear Technology Corporation.

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The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2 \bullet (R_{SW} + R_L)$$

4. Other "hidden" losses, such as copper trace and internal battery resistances, can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses, including diode conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3419 does not dissipate much heat due to its high efficiency. In the unlikely event that the junction temperature somehow reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance. The goal of the following thermal analysis is to determine whether the power dissipated causes enough temperature rise to exceed the maximum junction temperature (125°C) of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

Where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As a worst-case example, consider the case when the LTC3419 is in dropout on both channels at an input voltage of 2.7V with a load current of 600mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ of the main switch is 0.6Ω. Therefore, power dissipated by each channel is:

$$P_D = I_{OUT}^2 \bullet R_{DS(ON)} = 216mV$$

Given that the thermal resistance of a properly soldered DFN package is approximately 40°C/W, the junction temperature of an LTC3419 device operating in a 70°C ambient temperature is approximately:

$$T_J = (2 \bullet 0.216W \bullet 40°C/W) + 70°C = 87.3°C$$

which is well below the absolute maximum junction temperature of 125°C.

PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3419. These items are also illustrated graphically in the layout diagrams of Figures 2 and 3. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 5) and GND (Pin 9) as closely as possible? This capacitor provides the AC current of the internal power MOSFETs and their drivers.
2. Are the respective C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT1} and a ground sense line terminated near GND (Pin 9). The feedback signals V_{FB1} and V_{FB2} should be routed away from noisy components and traces, such as the SW lines (Pins 4 and 6), and their trace length should be minimized.
4. Keep sensitive components away from the SW pins, if possible. The input capacitor C_{IN} and the resistors R1, R2, R3 and R4 should be routed away from the SW traces and the inductors.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at a single point. These ground traces should not share the high current path of C_{IN} or C_{OUT}.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.

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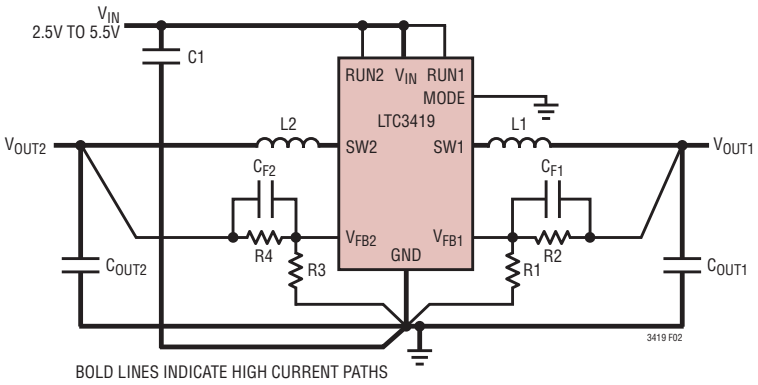

Figure 2. LTC3419 Layout Diagram (See Board Layout Checklist)

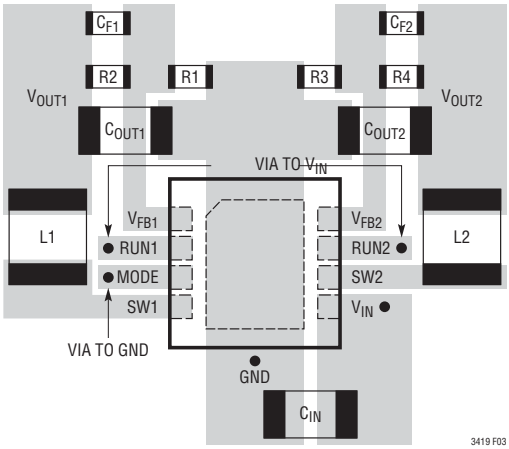

Figure 3. LTC3419 Suggested Layout

Design Example

As a design example, consider using the LTC3419 in a portable application with a Li-Ion battery. The battery provides a V_{IN} ranging from 2.8V to 4.2V. The load on each channel requires a maximum of 600mA in active mode and 2mA in standby mode. The output voltages are V_{OUT1} = 2.5V and V_{OUT2} = 1.8V.

Start with channel 1. First, calculate the inductor value for about 40% ripple current (240mA in this example) at maximum V_{IN}. Using a derivation of Equation 1:

$$L1 = \frac{2.5V}{2.25MHz \bullet (240mA)} \bullet \left(1 - \frac{2.5V}{4.2V}\right) = 1.87\mu H$$

For the inductor, use the closest standard value of 2.2µH.

A 10µF ceramic capacitor should be more than sufficient for this output capacitor. As for the input capacitor, a typical value of C_{IN} = 10µF should suffice, as the source impedance of a Li-Ion battery is very low.

The feedback resistors program the output voltage. To maintain high efficiency at light loads, the current in these resistors should be kept small. Choosing 10µA with the 0.6V feedback voltage makes R1~60k. A close standard 1% resistor is 59k. Using Equation 2.

$$R2 = \left(\frac{V_{OUT}}{0.6} - 1\right) \bullet R1 = 187k$$

An optional 22pF feedback capacitor (C_{F1}) may be used to improve transient response.

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Using the same analysis for channel 2 (V_{OUT2} = 1.8V), the results are:

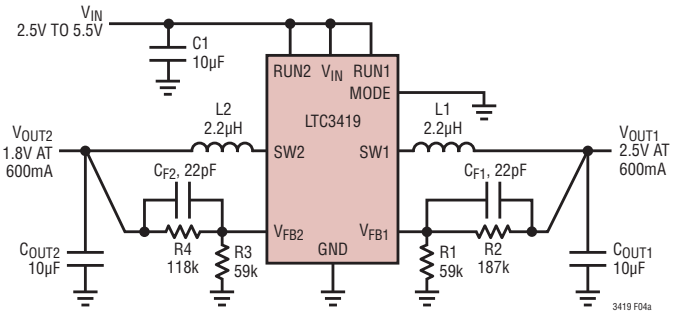
L2 = 1.9µH

R3 = 59k

R4 = 118k

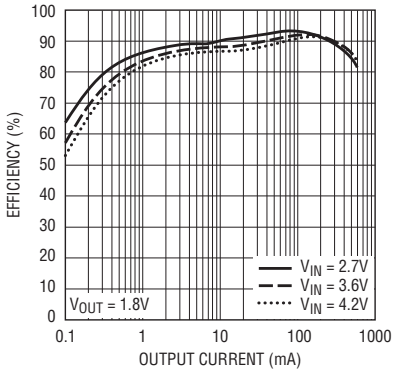
C_{F2} = 22pF

Figure 4 shows the complete schematic for this example, along with the efficiency curve and transient response.



C1, C2, C3: TAIYO YUDEN JMK316BJ106ML L1, L2: TDK VLF3010AT2R2M1RD

Figure 4a. Design Example Circuit



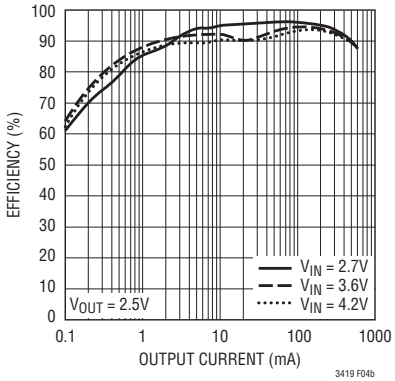
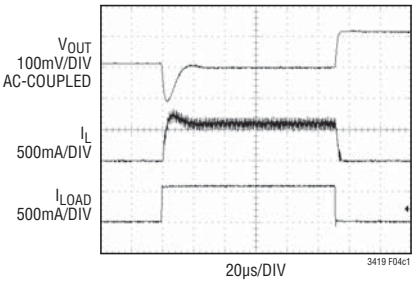


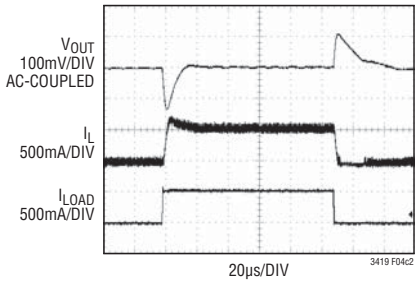
Figure 4b. Efficiency vs Output Current

Load Step



VIN = 3.6V
VOUT = 1.8V
ILOAD = 40mA TO 600mA

Transient Response

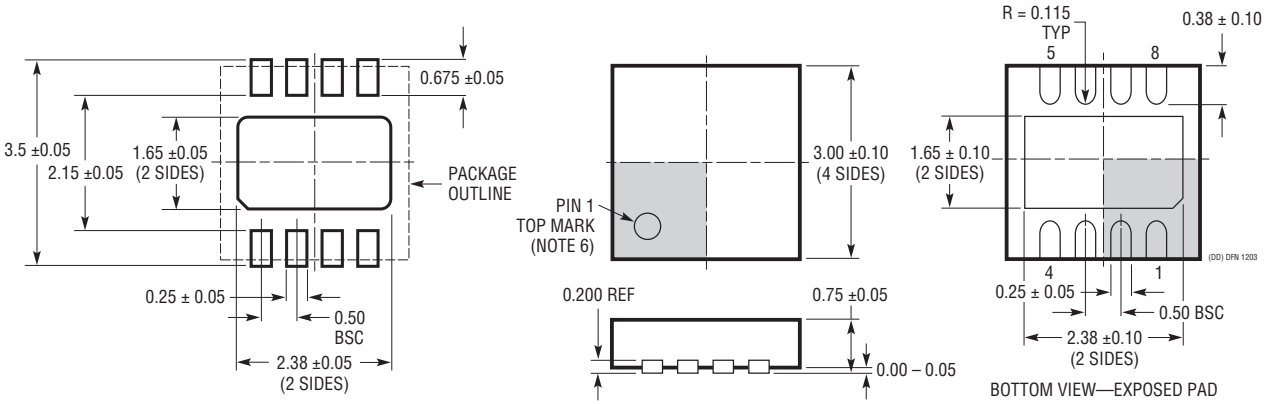


VIN = 3.6V
VOUT = 2.5V
ILOAD = 40mA TO 600mA

Figure 4c. Transient Response

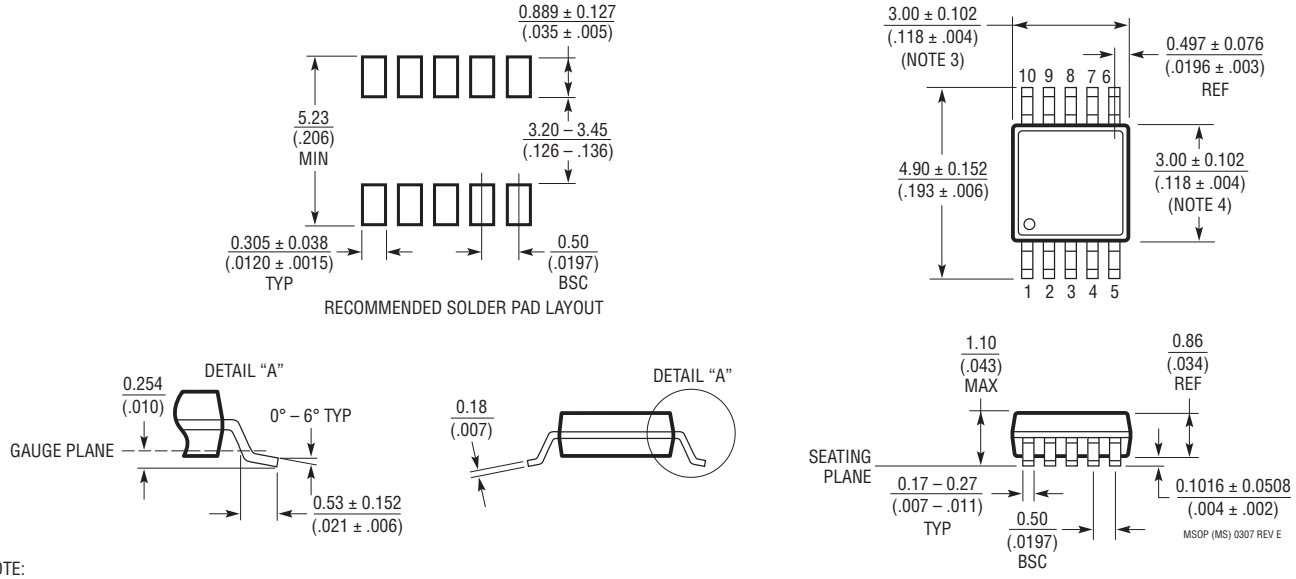
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

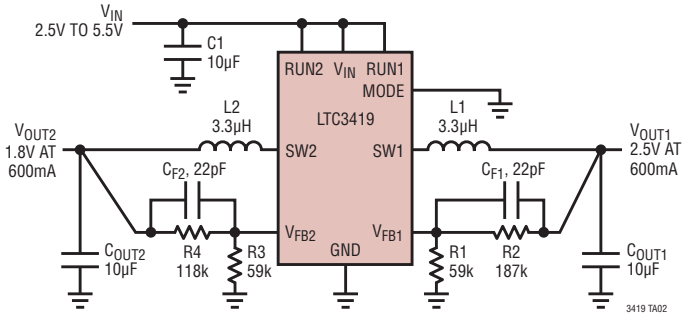
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

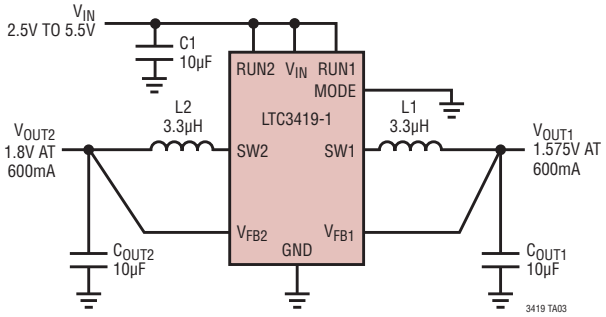
TYPICAL APPLICATIONS

Dual 600mA Buck Converter



C1, C2, C3: TAIYO YUDEN JMK316BJ106ML L1, L2: TDK VLF3010AT3R3M1RD

1.8V/1.575V Dual 600mA Buck Converter



C1, C2, C3: TAIYO YUDEN JMK316BJ106ML L1, L2: TDK VLF3010AT3R3M1RD

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A	300mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converters	96% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/ 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10E and DFN Packages
LTC3409	600mA I_{OUT}, 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$ = 1.6V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} = <1µA, DFN Package
LTC3410/LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} = <1µA, SC70 Package
LTC3411	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS10 and DFN Packages
LTC3412	2.5A I_{OUT} 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3441/LTC3442, LTC3443	1.2A I_{OUT} 2MHz, Synchronous Buck-Boost DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.4V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 50µA, I_{SD} = <1µA, DFN Package
LTC3531/LTC3531-3/ LTC3531-3.3	200mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 1.8V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} = <1µA, ThinSOT and DFN Packages
LTC3532	500mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.4V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} = <1µA, MS10 and DFN Packages
LTC3547/LTC3547B	Dual 300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q = 40µA, I_{SD} = <1µA, DFN-8 Package
LTC3548/LTC3548-1/ LTC3548-2	Dual 400mA and 800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10E and DFN Packages
LTC3561	1.25A I_{OUT}, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q = 240µA, I_{SD} = <1µA, DFN Package

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