THE DATASHEET OF

LT1424IS8-9#PBF

Isolated Flyback Switching Regulator with 9V Output

FEATURES

- **No Transformer "Third Winding" or Optoisolator Required**
- **Application Circuit Meets PCMCIA Type II Height Requirement**
- Fixed, Application Specific 9V Output Voltage
- **Regulation Maintained Well into Discontinuous Mode (Light Load)**
- Load Compensation Provides Excellent Load Regulation
- Available in 8-Pin PDIP and SO Packages
- Operating Frequency: 285kHz

APPLICATIONS

- Ethernet Isolated 5V to –9V Converter

DESCRIPTION

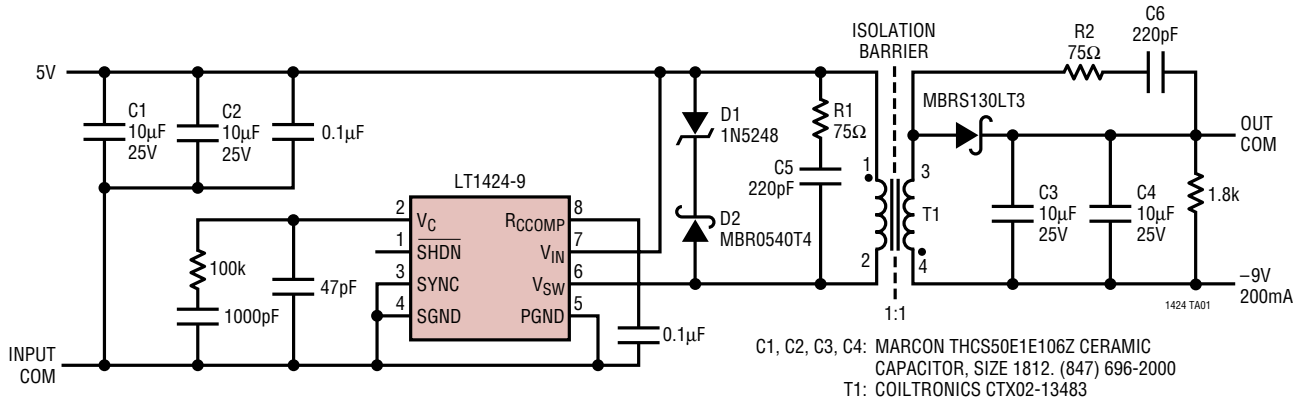
The LT®1424-9 is a monolithic high power switching regulator specifically designed for the isolated flyback topology. No "third winding" or optoisolator is required; the integrated circuit senses the isolated output voltage directly from the primary side flyback waveform. A high current, high efficiency switch is included on the die along with all oscillator, control and protection circuitry.

The LT1424-9 operates with input supply voltages from 3V to 20V and draws only 7mA quiescent current. It can deliver up to 200mA at 9V with no external power devices. By utilizing current mode switching techniques, it provides excellent AC and DC line regulation.

The LT1424-9 has a number of features not found on other switching regulator ICs. Its unique control circuitry can maintain regulation well into discontinuous mode. Load compensation circuitry allows for improved load regulation. An externally activated shutdown mode reduces total supply current to 20µA typical for standby operation.

TYPICAL APPLICATION

–9V PCMCIA Type II Isolated LAN Supply
(2.41mm Maximum Component Height)



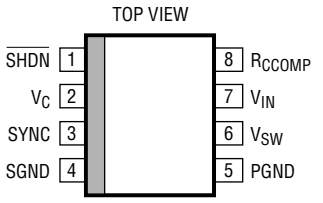
C1, C2, C3, C4: MARCON THCS50E1E106Z CERAMIC CAPACITOR, SIZE 1812. (847) 696-2000
T1: COILTRONICS CTX02-13483

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 20V
Switch Voltage 35V
$\overline{\text{SHDN}}$, SYNC Pin Voltage 7V
Operating Junction Temperature Range
  Commercial ..... 0°C to 125°C
  Industrial ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 145°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 145°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LT1424CN8-9 LT1424CS8-9 LT1424IN8-9 LT1424IS8-9
S8 PART MARKING
14249 1424I9

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{SW} Open, V_C = 1.4V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
$V_{IN(MIN)}$	Minimum Input Voltage		●		2.8	3.1	V
I_{CC}	Supply Current		●		7.0	9.5	mA
	Shutdown Mode Supply Current		●		15	40	µA
	Shutdown Mode Threshold		●	0.3	0.9	1.3	V
Feedback Amplifier							
V_{REF}	Reference Voltage	Measured at V_{SW} Pin (Note 2)	 ●	9.00 8.90	9.15 9.15	9.30 9.40	V V
g_m	Feedback Amplifier Transconductance	ΔI_C = ±10µA (Note 2)	●	400	1000	1600	µmho
I_{SOURCE}, I_{SINK}	Feedback Amplifier Source or Sink Current		●	30	50	80	µA
V_{CL}	Feedback Amplifier Clamp Voltage				1.9		V
	Reference Voltage/Current Line Regulation	5V ≤ V_{IN} ≤ 18V	●		0.01	0.04	%/V
	Voltage Gain	(Note 3)			500		V/V
Output Switch							
BV	Output Switch Breakdown Voltage	I_C = 5mA	●	35	50		V
V(V_{SW})	Output Switch ON Voltage	I_{SW} = 1A	●		0.55	0.85	V
I_{LIM}	Switch Current Limit	Duty Cycle = 50%, 0°C ≤ T_J ≤ 125°C Duty Cycle = 50%, –40°C ≤ T_J ≤ 125°C Duty Cycle = 80%	● ● 	1.35 1.20 	1.6 1.6 1.3	1.95 1.95 	A A A
Current Amplifier							
	Control Pin Threshold	Duty Cycle = Minimum	 ●	0.95 0.85	1.2 1.2	1.3 1.4	V V
	Control Voltage to Switch Transconductance				2		A/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{SW} Open, V_C = 1.4V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing							
f	Switching Frequency		 ●	260 240	285 285	300 320	kHz kHz
t_{ON}	Minimum Switch ON Time			170	200	260	ns
t_{ED}	Flyback Enable Delay Time				150		ns
t_{EN}	Minimum Flyback Enable Time				180		ns
	Maximum Switch Duty Cycle		●	85	90		%
Load Compensation							
	$\Delta V_{REF}/\Delta I_{SW}$				1.5		Ω
SYNC Function							
	Minimum SYNC Amplitude		●		1.5	2.2	V
	Synchronization Range		●	330		450	kHz
	SYNC Pin Input Resistance				40		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

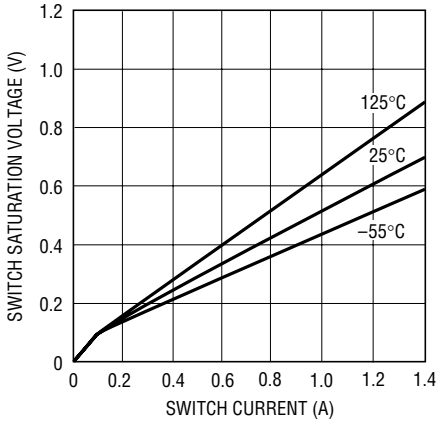
Note 2: V_{REF} is a parameter which is measured at the V_{SW} pin. It differs from the output voltage because it accounts for output diode drop, transformer leakage inductance, etc. Nominal output voltage is 9V in the intended application circuit.

Note 3: Feedback amplifier transconductance is R_{REF} referred.

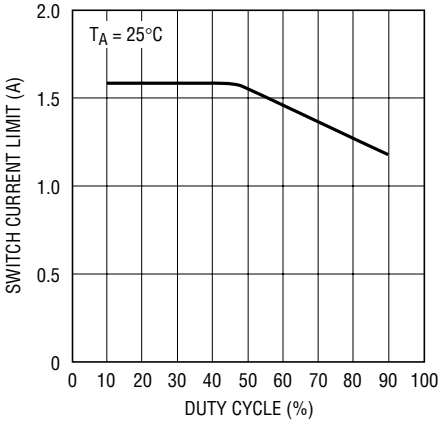
Note 4: Voltage gain is R_{REF} referred.

TYPICAL PERFORMANCE CHARACTERISTICS

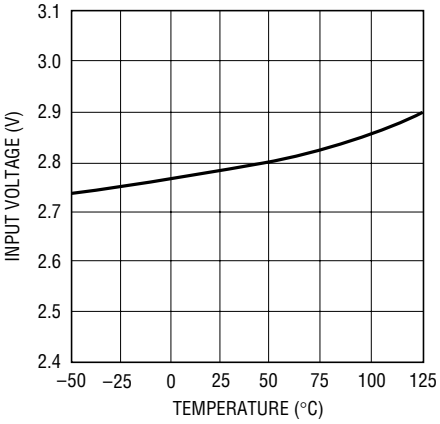
Switch Saturation Voltage vs Switch Current



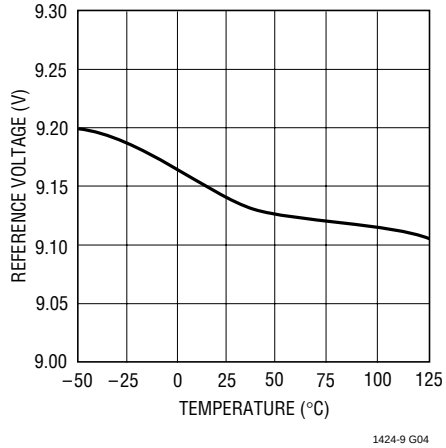
Switch Current Limit vs Duty Cycle



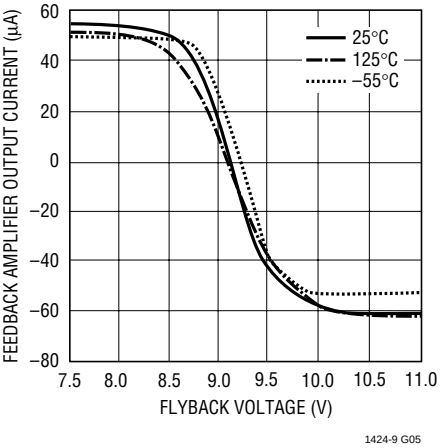
Minimum Input Voltage vs Temperature



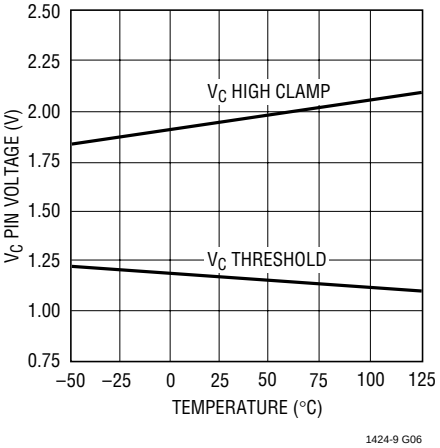
Reference Voltage vs Temperature



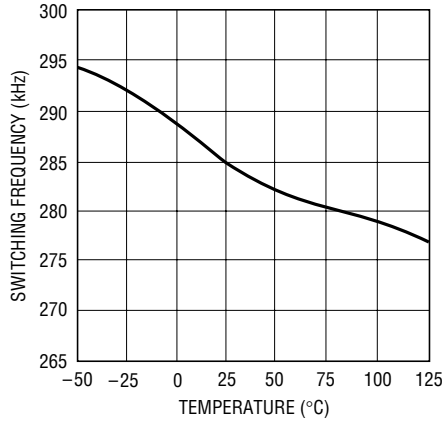
Feedback Amplifier Output Current vs Flyback Voltage



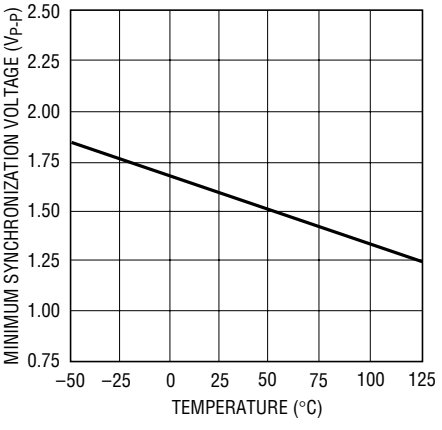
V_C Pin Threshold and High Clamp Voltage vs Temperature



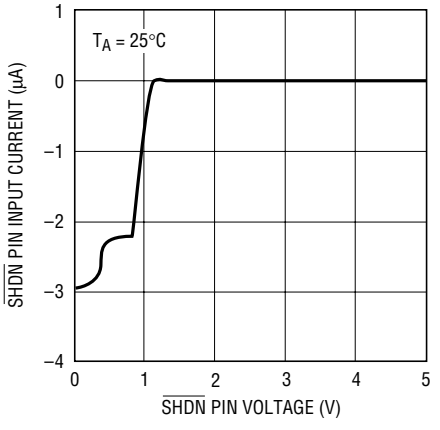
Switching Frequency vs Temperature



Minimum Synchronization Voltage vs Temperature

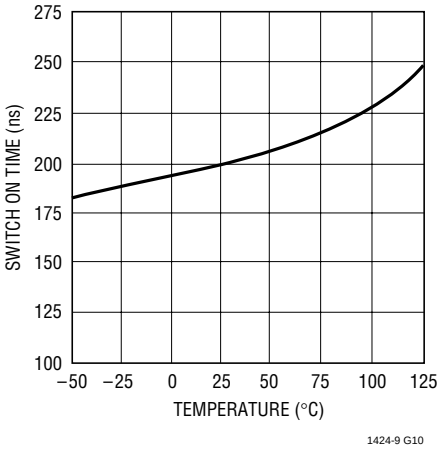


$\overline{SHDN}$ Pin Input Current vs Voltage

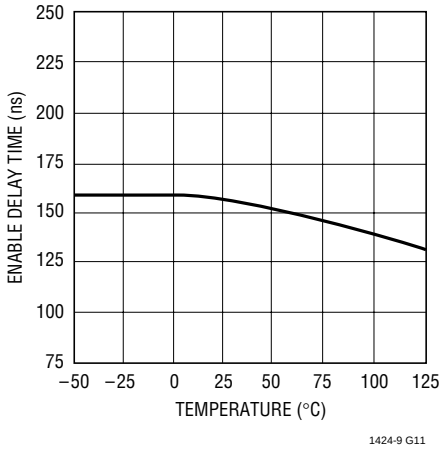


TYPICAL PERFORMANCE CHARACTERISTICS

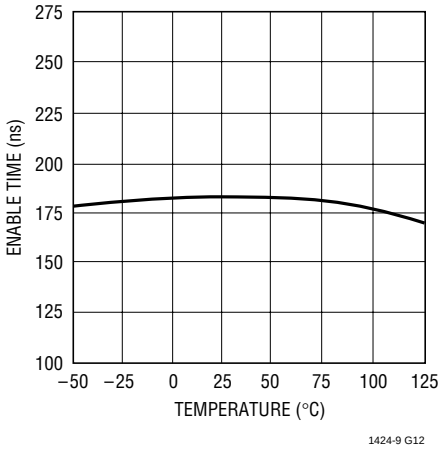
Minimum Switch On Time vs Temperature



Flyback Enable Delay Time vs Temperature



Minimum Flyback Enable Time vs Temperature



PIN FUNCTIONS

$\overline{\text{SHDN}}$ (Pin 1): Shutdown. This pin is used to turn off the regulator and reduce V_{IN} input current to a few tens of microamperes. The $\overline{\text{SHDN}}$ pin can be left floating when unused.

V_C (Pin 2): Control Voltage. This pin is the output of the feedback amplifier and the input of the current comparator. Frequency compensation of the overall loop is effected by placing a capacitor between this node and ground.

SYNC (Pin 3): Pin to synchronize internal oscillator to external frequency reference. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. If unused, this pin should be tied to ground.

SGND (Pin 4): Signal Ground. This pin is a clean ground. The internal reference and feedback amplifier are referred to it. Keep the ground path connection to the V_C compensation capacitor free of large ground currents.

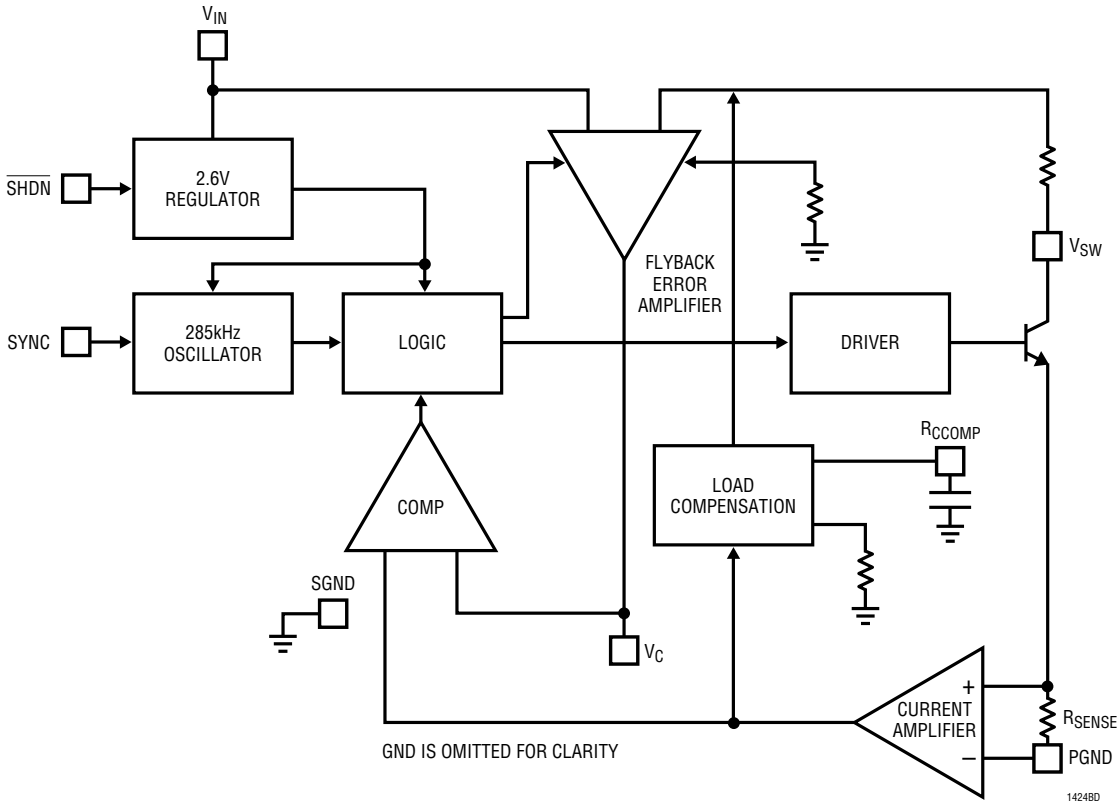
PGND (Pin 5): Power Ground. This pin is the emitter of the power switch device and has large currents flowing through it. It should be connected directly to a good quality ground plane.

V_{SW} (Pin 6): This is the collector node of the output switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize electromagnetic radiation and voltage spikes.

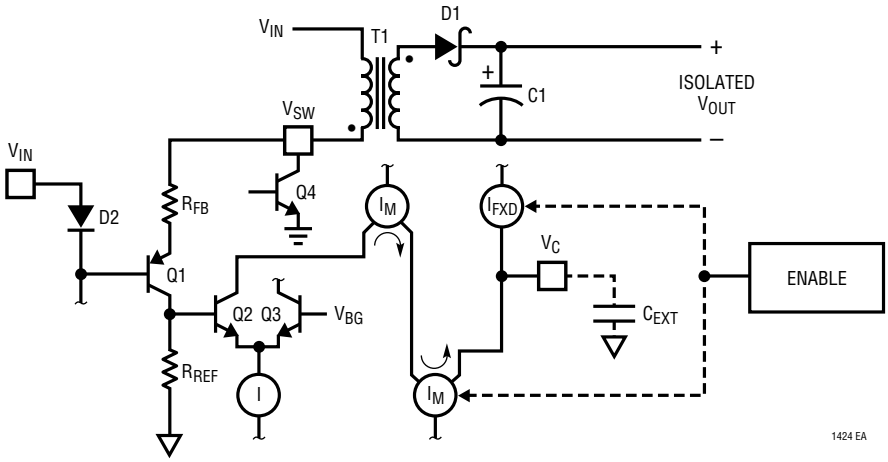
V_{IN} (Pin 7): Supply Voltage. Bypass input supply pin with 10µF or more. The part goes into undervoltage lockout when V_{IN} drops below 2.8V. Undervoltage lockout stops switching and pulls the V_C pin low.

R_{CCOMP} (Pin 8): Pin for the External Filter Capacitor for Load Compensation Function. A common 0.1µF ceramic capacitor will suffice.

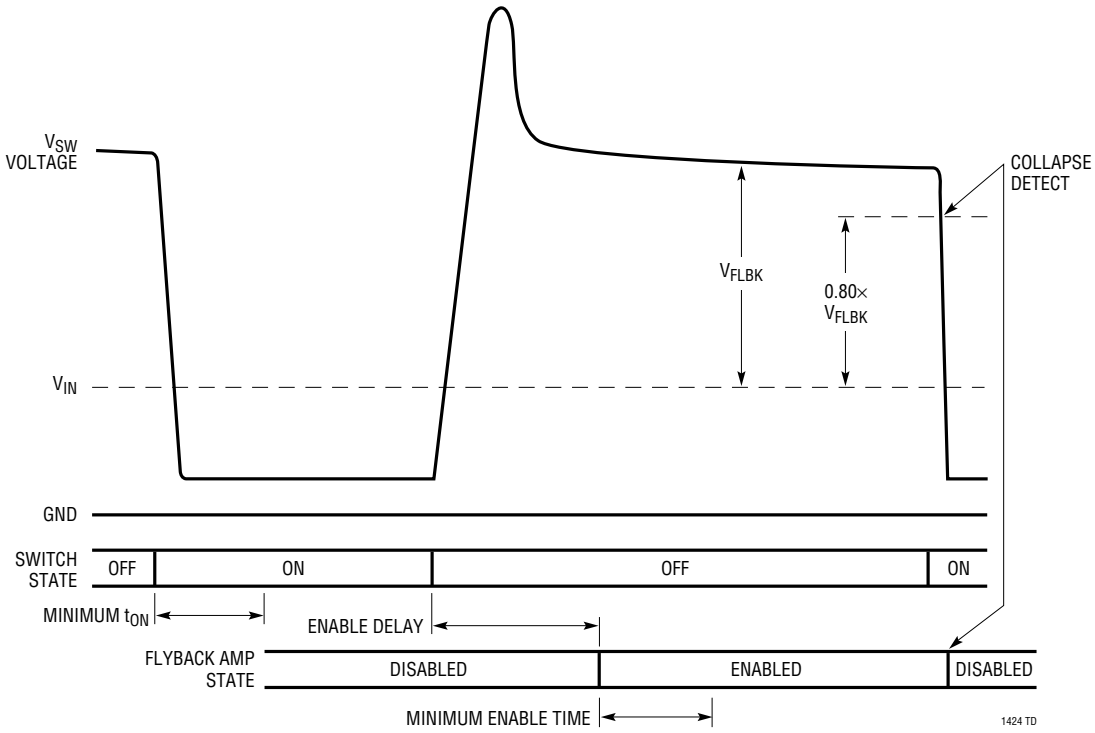
BLOCK DIAGRAM



FLYBACK ERROR AMPLIFIER DIAGRAM



TIMING DIAGRAM



OPERATION

The LT1424-9 is a current mode switching regulator IC that has been designed specifically for the isolated flyback topology. The special problem normally encountered in such circuits is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated to the primary side in order to maintain regulation. Historically, this has been done with optoisolators or extra transformer windings. Optoisolator circuits waste output power and the extra components they require increase the cost and physical volume of the power supply. Optoisolators can also exhibit trouble due to limited dynamic response (temporal), nonlinearity, unit-to-unit variation and aging over life. Circuits employing extra transformer windings also exhibit deficiencies. The extra winding adds to the transformer's physical size and cost. Dynamic response is often mediocre. There is usually no method for maintaining load regulation versus load.

The LT1424-9 derives its information about the isolated output voltage by examining the primary side flyback pulse waveform. In this manner no optoisolator nor extra transformer winding is required. This IC is a quantum improvement over previous approaches because: target output voltage is directly resistor programmable, regulation is maintained well into discontinuous mode and optional load compensation is available.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional designs including: internal bias regulator, oscillator, logic, current amplifier and comparator, driver and output switch. The novel sections include a special flyback error amplifier and a load compensation mechanism. Also, due to the special dynamic requirements of flyback control, the logic system contains additional functionality not found in conventional designs.

The R_{REF}, R_{RFB} and R_{OCOMP} resistors in the Block Diagram are application-specific thin-film resistors internal to the LT1424-9. The capacitor connected to the R_{CCOMP} pin is external.

The LT1424-9 operates much the same as traditional current mode switchers, the major difference being a different type of error amplifier which derives its feedback information from the flyback pulse. Due to space constraints, this discussion will not reiterate the basics of current mode switcher/controllers and isolated flyback converters. A good source of information on these topics is LTC's Application Note 19.

ERROR AMPLIFIER—PSEUDO DC THEORY

Please refer to the simplified diagram of the Flyback Error Amplifier. Operation is as follows: when output switch Q4 turns off, its collector voltage rises above the V_{IN} rail. The amplitude of this flyback pulse, i.e., the difference between it and V_{IN}, is given as:

$$V_{FLBK} = \frac{V_{OUT} + V_F + (I_{SEC})(ESR)}{N_{SP}}$$

V_F = D1 forward voltage
I_{SEC} = Transformer secondary current
ESR = Total impedance of secondary circuit
N_{SP} = Transformer effective secondary-to-primary turns ratio

The flyback voltage is then converted to a current by the action of R_{FB} and Q1. Nearly all of this current flows through resistor R_{REF} to form a ground-referred voltage. This is then compared to the internal bandgap reference by the differential transistor pair Q2/Q3. The collector current from Q2 is mirrored around and subtracted from fixed current source I_{FXD} at the V_C pin. An external capacitor integrates this net current to provide the control voltage to set the current mode trip point.

The relatively high gain in the overall loop will then cause the voltage at the R_{REF} resistor to be nearly equal to the bandgap reference V_{BG}. The relationship between V_{FLBK} and V_{BG} may then be expressed as:

$$\alpha\frac{V_{FLBK}}{R_{FB}} = \frac{V_{BG}}{R_{REF}} \text{ or,}$$

$$V_{FLBK} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{\alpha}\right)$$

α = Ratio of Q1 I_C to I_E
V_{BG} = Internal bandgap reference

OPERATION

Combination with the previous V_{FLBK} expression yields an expression for V_{OUT}, in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{N_{SP}}{\alpha}\right) - V_F - I_{SEC}\,(ESR)$$

Additionally, it includes the effect of nonzero secondary output impedance. See Load Compensation for details. The practical aspects of applying this equation for V_{OUT} are found in the Applications Information section.

So far, this has been a pseudo-DC treatment of flyback error amplifier operation. But the flyback signal is a pulse, not a DC level. Provision must be made to enable the flyback amplifier only when the flyback pulse is present. This is accomplished by the dashed line connections to the block labeled "ENABLE". Timing signals are then required to enable and disable the flyback amplifier.

ERROR AMPLIFIER—DYNAMIC THEORY

There are several timing signals that are required for proper LT1424-9 operation. Please refer to the Timing Diagram.

Minimum Output Switch ON Time

The LT1424-9 effects output voltage regulation via flyback pulse action. If the output switch is not turned on at all, there will be no flyback pulse, and output voltage information is no longer available. This would cause irregular loop response and start-up/latchup problems. The solution chosen is to require the output switch to be on for an absolute minimum time per each oscillator cycle. This in turn establishes a minimum load requirement to maintain regulation. See Applications Information section for further details.

Enable Delay

When the output switch shuts off, the flyback pulse appears. However, it takes a finite time until the transformer primary side voltage waveform approximately represents the output voltage. This is partly due to rise time on the V_{SW} node, but more importantly due to transformer leakage inductance. The latter causes a voltage spike on the primary side not directly related to output voltage. (Some time is also required for internal settling of the feedback amplifier circuitry.)

In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the enabling of the feedback amplifier. This is termed "enable delay". In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See Applications Information section for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, that compares the flyback voltage (R_{REF} referred) to a fixed reference, nominally 80% of V_{BG}. When the flyback waveform drops below this level, the feedback amplifier is disabled. This action accommodates both continuous and discontinuous mode operation.

Minimum Enable Time

The feedback amplifier, once enabled, stays enabled for a fixed minimum time period termed "minimum enable time". This prevents lock-up, especially when the output voltage is abnormally low, e.g., during start-up. The minimum enable time period ensures that the V_C node is able to "pump up" and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. The "minimum enable time" often determines the low load level at which output voltage regulation is lost. See Applications Information section for details.

Effects of Variable Enable Period

It should now be clear that the flyback amplifier is enabled only during a portion of the cycle time. This can vary from the fixed "minimum enable time" described to a maximum of roughly the OFF switch time minus the enable delay

OPERATION

time. Certain parameters of flyback amp behavior will then be directly affected by the variable enable period. These include effective transconductance and V_C node slew rate.

LOAD COMPENSATION THEORY

The LT1424-9 uses the flyback pulse to obtain information about the isolated output voltage. A potential error source is caused by transformer secondary current flow through the real life nonzero impedances of the output rectifier, transformer secondary and output capacitor. This has been represented previously by the expression $(I_{SEC})(ESR)$. However, it is generally more useful to convert this expression to an effective output impedance. Because the secondary current only flows during the off portion of the duty cycle, the effective output impedance equals the lumped secondary impedance times the inverse of the OFF duty cycle. That is,

$$R_{OUT} = ESR\left(\frac{1}{DC\ OFF}\right) \text{ where,}$$

R_{OUT} = Effective supply output impedance
ESR = Lumped secondary impedance
DC OFF = OFF duty cycle

Expressing this in terms of the ON duty cycle, remembering DC OFF = 1 – DC,

$$R_{OUT} = ESR\left(\frac{1}{1 - DC}\right)$$

DC = ON duty cycle

In less critical applications, or if output load current remains relatively constant, this output impedance error may be judged acceptable and the external R_{FB} resistor value adjusted to compensate for nominal expected error. In more demanding applications, output impedance error may be minimized by the use of the load compensation function.

To implement the load compensation function, a voltage is developed that is proportional to average output switch current. This voltage is then impressed across the external R_{OCOMP} resistor and the resulting current is then subtracted from the R_{FB} node. As output loading increases, average switch current increases to maintain rough output voltage regulation. This causes an increase in R_{OCOMP} resistor current subtracted from the R_{FB} node, through which feedback loop action causes a corresponding increase in target output voltage.

Assuming a relatively fixed power supply efficiency, Eff

Power Out = (Eff)(Power In)

$(V_{OUT})(I_{OUT}) = (Eff)(V_{IN})(I_{IN})$

Average primary side current may be expressed in terms of output current as follows:

$$I_{IN} = \left(\frac{V_{OUT}}{(V_{IN})(Eff)}\right) I_{OUT}$$

combining the efficiency and voltage terms in a single variable,

$$I_{IN} = K1(I_{OUT}) \text{ where,}$$

$$K1 = \left(\frac{V_{OUT}}{(V_{IN})(Eff)}\right)$$

Switch current is converted to voltage by a sense resistor and amplified by the current sense amplifier with associated gain G. This voltage is then impressed across the external R_{OCOMP} resistor to form a current that is subtracted from the R_{FB} node. So the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = K1(\Delta I_{OUT})\left(\frac{(R_{SENSE})(G)}{R_{OCOMP}}\right) R_{FB}$$

Expressing the product of R_{SENSE} and G as the data sheet value of $\Delta V_{RCCOMP}/\Delta I_{SW}$,

$$R_{OUT} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OCOMP}}\right) \text{ and,}$$

$$R_{OCOMP} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OUT}}\right) \text{ where,}$$

K1 = Dimensionless variable related to V_{IN}, V_{OUT} and efficiency as above

OPERATION

$\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)$ = Data sheet value for R_{CCOMP} pin action vs switch current

R_{FB} = External "feedback" resistor value

R_{OUT} = Uncompensated output impedance

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OCOMP}}\right)$$

Nominal output impedance cancellation is obtained by equating this expression with R_{OUT}.

APPLICATIONS INFORMATION

The LT1424-X is an application-specific 8-pin part which implements an isolated flyback switcher/controller. Three on-chip thin-film resistors are used to "program" the part for a specific application including mainly desired output voltage, transformer turns ratio and secondary circuit ESR behavior. As of Initial Release, the LT1424-9 is available which implements the "–9V PCMCIA II Isolated LAN Supply" as described in the Typical Application section.

Potential users with a high volume requirement for other applications are advised as follows: general experimentation/breadboarding may be done with the LT1425. This is a general purpose 16-pin part whose functionality is similar to the LT1424-X, with the exception that the three application resistors are external user-supplied components. Application information relating to the proper selection of these resistor values is contained within the LT1425 data sheet. Once technical feasibility is demonstrated, the potential user may discuss the possibility of an additional LT1424-X version with the factory.

OUTPUT VOLTAGE ERROR SOURCES

Conventional nonisolated switching power supply ICs typically have only two substantial sources of output voltage error—the internal or external resistor divider network that connects to V_{OUT} and the internal IC reference. The LT1424-9, which senses the output voltage in both a dynamic and an isolated manner, exhibits additional potential error sources to contend with. Some of these errors are proportional to output voltage, others are fixed in an absolute millivolt sense. Here is a list of possible error sources and their effective contribution:

Internal Voltage Reference

The internal bandgap voltage reference is, of course, imperfect. Its error, both at 25°C and over temperature is already included in the specifications for Reference Voltage.

Schottky Diode Drop

The LT1424-9 senses the output voltage from the transformer primary side during the flyback portion of the cycle. This sensed voltage therefore includes the forward drop, V_F, of the rectifier (usually a Schottky diode). Lot-to-lot and ambient temperature variations will show up as output voltage shift/drift.

Secondary Leakage Inductance

Leakage inductance on the transformer secondary reduces the effective primary-to-secondary turns ratio (N_P/N_S) from its ideal value. This increases the output voltage target by a similar percentage and has been nominally taken into account in the design of the LT1424-9. To the extent that secondary leakage inductance varies from part-to-part, the output voltage will be affected.

Output Impedance Error

The LT1424-9 contains a load compensation function to provide a nominal, first-order cancellation of the effects of secondary circuit ESR. Unit-to-unit variation plus some inherent nonlinearity in the cancellation results in some residual V_{OUT} variation with load.

APPLICATIONS INFORMATION

MINIMUM LOAD CONSIDERATIONS

The LT1424-9 generally provides better low load performance than previous generation switcher/controllers utilizing indirect output voltage sensing techniques. Specifically, it contains circuitry to detect flyback pulse "collapse," thereby supporting operation well into discontinuous mode. In general, there are two possible constraints to ultimate low load operation, minimum switch ON time which sets a minimum level of delivered power, and minimum flyback enable time, which deals with the ability of the feedback system to derive valid output voltage information from the flyback pulse. In the application for which the LT1424-9 is designed, the minimum flyback enable time is more restrictive.

The LT1424-9 derives its output voltage information from the flyback pulse. If the internal minimum enable time pulse extends beyond the flyback pulse, loss of regulation will occur. The onset of this condition can be determined by setting the width of the flyback pulse equal to the sum of the flyback enable delay, t_{ED}, plus the minimum enable time, t_{EN}. Minimum power delivered to the load is then:

$$\text{Min Power} = \left(\frac{1}{2}\right)\left(\frac{f}{L_{SEC}}\right)[V_{OUT} \bullet (t_{EN} + t_{ED})]^2$$
$$= (V_{OUT})(I_{OUT})$$

Which yields a minimum output constraint:

$$I_{OUT(MIN)} = \left(\frac{1}{2}\right)\left(\frac{f(V_{OUT})}{L_{SEC}}\right)(t_{ED} + t_{EN})^2, \text{ where}$$

f = Switching frequency (nominally 285kHz)
L_{SEC} = Transformer secondary side inductance
V_{OUT} = Output voltage
t_{ED} = Enable delay time
t_{EN} = Minimum enable time

In reality, the previously derived expression is a conservative one, as it assumes perfectly "square" waveforms, which is not the case at light load. Furthermore, the equation was set up to yield just the *onset* of control error. In other words, while the equation suggests a minimum load current of perhaps 7mA, laboratory observations suggest operation down to 2mA to 3mA before significant output voltage rise is observed. Nevertheless, this situation is addressed in the application by the use of a fixed 1.8k load resistor, which preloads the supply with a nominal 5mA.

MAXIMUM LOAD/SHORT-CIRCUIT CONSIDERATIONS

The LT1424-9 is a current mode controller. It uses the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 1.9V, then acts as an output switch peak current limit. This action becomes the switch current limit specification. The maximum available output power is then determined by the switch current limit, which is somewhat duty cycle dependent due to internal slope compensation action.

Short-circuit conditions are handled by the same mechanism. The output switch turns on, peak current is quickly reached and the switch is turned off. Because the output switch is only on for a small fraction of the available period, internal power dissipation is controlled. (The LT1424-9 contains an internal overtemperature shutdown circuit, that disables switch action, just in case.)

THERMAL CONSIDERATIONS

Care should be taken to ensure that the worst-case input voltage and load current conditions do not cause excessive die temperatures. The packages are rated at 110°C/W for SO-8 and 130°C/W for N8.

Average supply current (including driver current) is:

$$I_{IN} = 7mA + DC\left(\frac{I_{SW}}{35}\right) \text{ where,}$$

I_{SW} = Switch current
DC = On switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2(R_{SW})(DC)$$

R_{SW} = Output switch ON resistance

APPLICATIONS INFORMATION

Total power dissipation of the die is the sum of supply current times supply voltage plus switch power:

$$P_{D(TOTAL)} = (I_{IN} \bullet V_{IN}) + P_{SW}$$

FREQUENCY COMPENSATION

Loop frequency compensation is performed by connecting a capacitor from the output of the error amplifier (V_C pin) to ground. An additional series resistor, often required in traditional current mode switcher controllers is usually not required; and can even prove detrimental. The phase margin improvement traditionally offered by this extra resistor will usually be already accomplished by the nonzero secondary circuit impedance, which adds a "zero" to the loop response.

In further contrast to traditional current mode switchers, V_C pin ripple is generally not an issue with the LT1424-9. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_C voltage changes during the flyback pulse, but is then "held" during the subsequent "switch ON" portion of the next cycle. This action naturally holds the V_C voltage stable during the current comparator sense action (current mode switching).

PCB LAYOUT CONSIDERATIONS

For maximum efficiency, switch rise and fall times are made as short as practical. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths (primary *and* secondary). B field (magnetic) radiation is minimized by keeping output diode, switch pin and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current paths are shown schematically in Figure 1. Minimum lead length in these paths are essential to ensure clean switching and minimal EMI. The path containing the input capacitor, transformer primary, output switch, the path containing the transformer secondary, output diode and output capacitor are the only ones containing nanosecond rise and fall times. Keep these paths as short as possible.

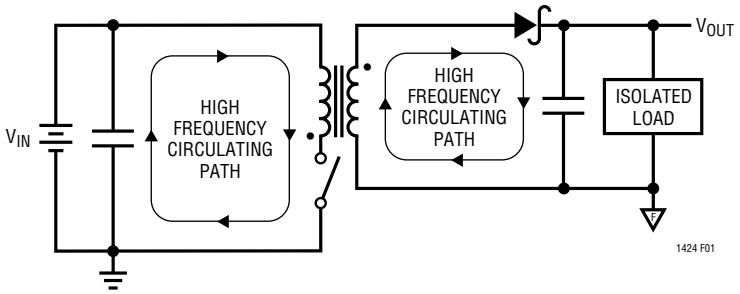
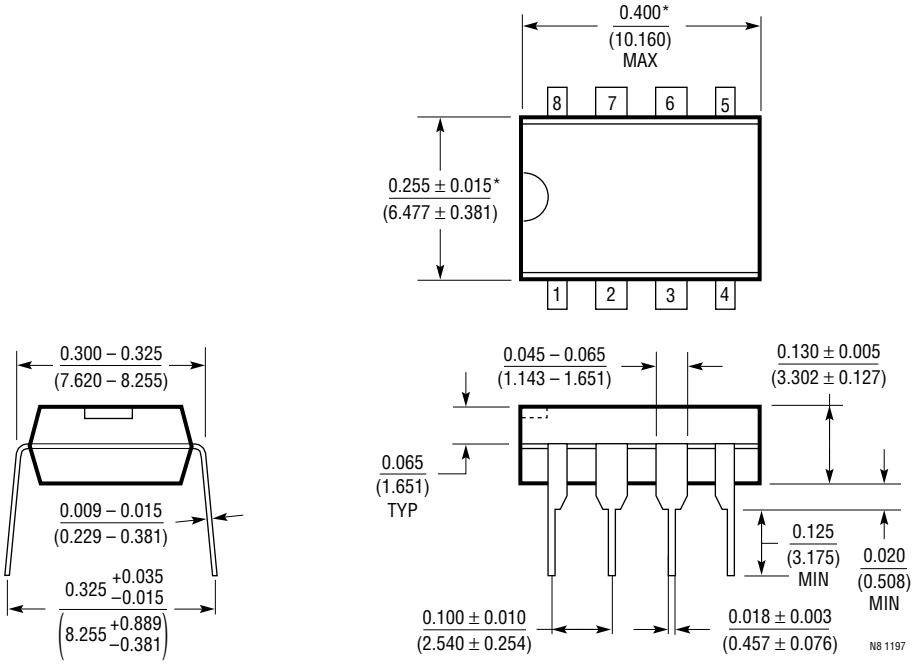


Figure 1

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

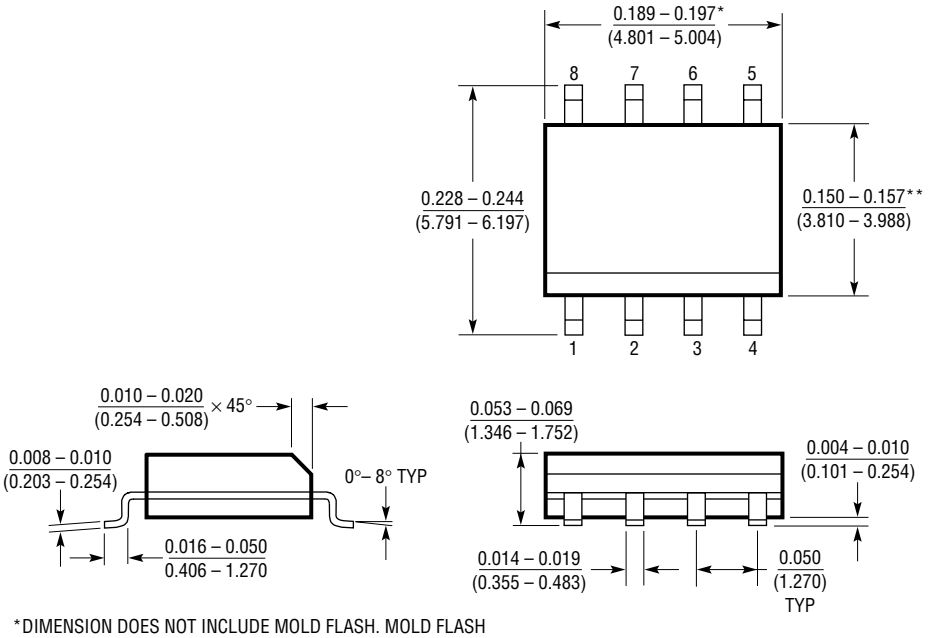


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



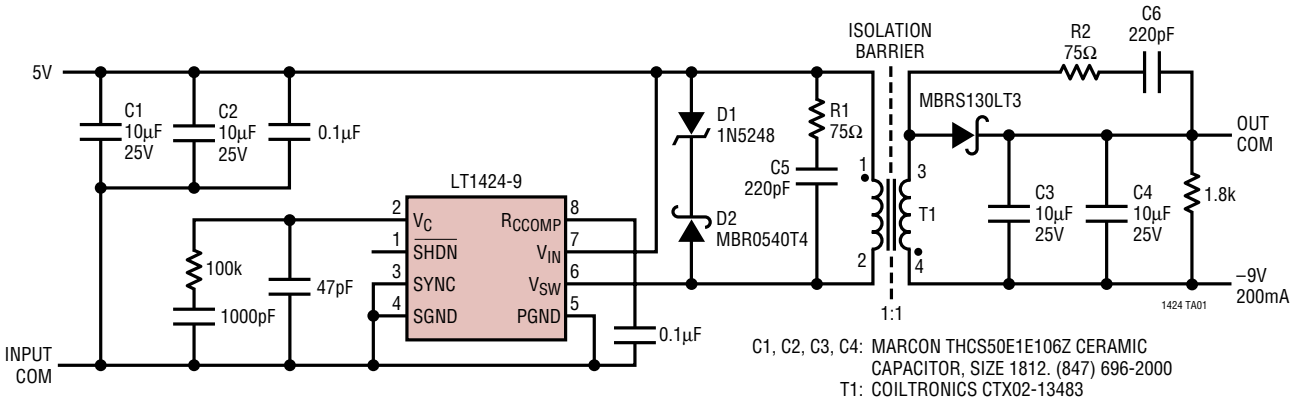
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

TYPICAL APPLICATION

–9V PCMCIA Type II Isolated LAN Supply



C1, C2, C3, C4: MARCON THCS50E1E106Z CERAMIC CAPACITOR, SIZE 1812. (847) 696-2000
T1: COILTRONICS CTX02-13483

Transformer T1

	LPRI	RATIO	ISOLATION	(L × W × H)	I_{OUT}	EFFICIENCY
COILTRONICS CTX02-13483	27µH	1:1	500VAC	14 × 14 × 2.2mm	200mA	70%

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1105	Off-Line Switching Regulator	Built-In Isolated Regulation Without Optoisolator
LTC®1145/46	Isolated Digital Data Transceivers	Up to 200kbps Data Rate, UL Listed
LT1170/71/72	5A/3A/1.25A Flyback Regulators	Isolated Flyback Mode for Higher Currents
LT1370/71	6A/3A Flyback Regulators	Uses Small Magnetics
LT1372/77	500kHz/1MHz Boost/Flyback Regulators	Uses Ultrasmall Magnetics
LT1424-5	Isolated Flyback Switching Regulator	Same as LT1424-9 But with 5V Output
LT1425	Isolated Flyback Switching Regulator	General Purpose with External Application Resistors

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