THE DATASHEET OF

AD9714BCPZRL7

www.win-source.net 0086-755-83957316

Data Sheet

AD9714/AD9715/AD9716/AD9717

Dual, 8-/10-/12-/14-Bit Low Power Digital-to-Analog Converters

FEATURES

- Power dissipation @ 3.3 V, 2 mA output
  - 37 mW @ 10 MSPS
  - 86 mW @ 125 MSPS
- Sleep mode: <3 mW @ 3.3 V
- Supply voltage: 1.8 V to 3.3 V
- SFDR to Nyquist
  - 84 dBc @ 1 MHz output
  - 75 dBc @ 10 MHz output
- AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: −151 dBc/Hz
- Differential current outputs: 1 mA to 4 mA
- 2 on-chip auxiliary DACs
- CMOS inputs with single-port operation
- Output common mode: adjustable 0 V to 1.2 V
- Small footprint 40-lead LFCSP RoHS-compliant package

APPLICATIONS

- Wireless infrastructures
  - Picocell, femtocell base stations
- Medical instrumentation
  - Ultrasound transducer excitation
- Portable instrumentation
  - Signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The AD9714/AD9715/AD9716/AD9717 are pin-compatible, dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC® converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.

The AD9714/AD9715/AD9716/AD9717 offer exceptional ac and dc performance and support update rates up to 125 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9714/AD9715/AD9716/AD9717 make them well-suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. Low Power. DACs operate on a single 1.8 V to 3.3 V supply; total power consumption reduces to 35 mW at 125 MSPS with a 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. LVCMOS Clock Input. High speed, single-ended LVCMOS clock input supports a 125 MSPS conversion rate.
3. Easy Interfacing to Other Components. Adjustable output common mode from 0 V to 1.2 V allows easy interfacing to other components that accept common-mode levels greater than 0 V.

Rev. D

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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8/2022—Rev. B to Rev. C

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FUNCTIONAL BLOCK DIAGRAM

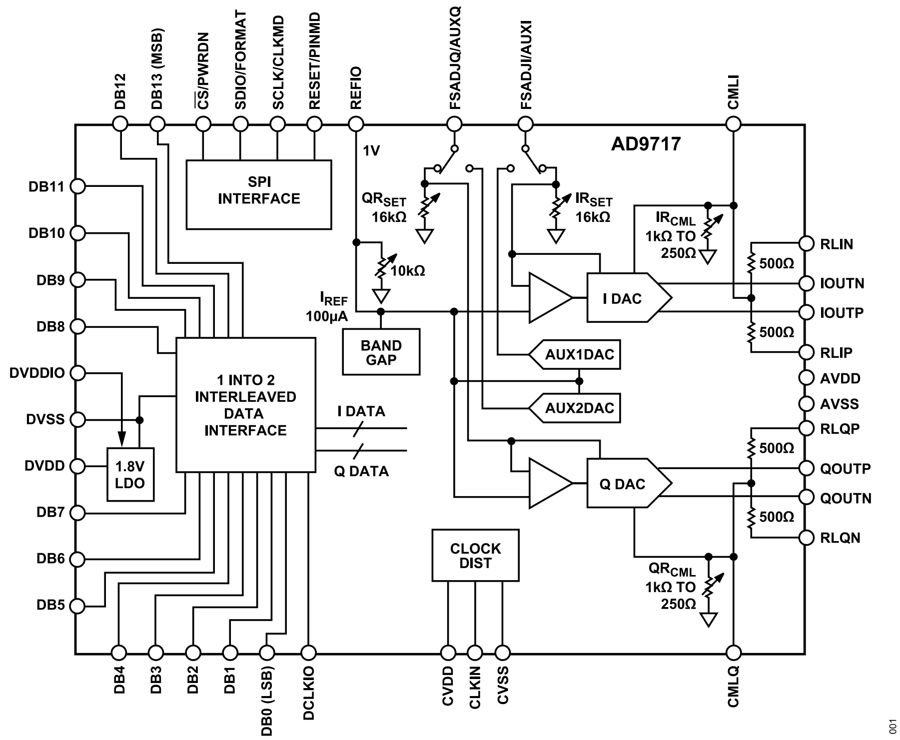


Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9714			AD9715			AD9716			AD9717			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
RESOLUTION		8			10			12			14		Bits
ACCURACY, AVDD = DVDDIO = CVDD = 3.3 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.7		LSB
Postcalibration		±0.003			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.13			±0.4			±1.8		LSB
Postcalibration		±0.01			±0.05			±0.3			±1.3		LSB
ACCURACY, AVDD = DVDDIO = CVDD = 1.8 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.2		LSB
Postcalibration		±0.005			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.12			±0.4			±1.5		LSB
Postcalibration		±0.02			±0.05			±0.25			±1.1		LSB
MAIN DAC OUTPUTS													
Offset Error	−1	0	+1	−1	0	+1	−1	0	+1	−1	0	+1	mV
Gain Error													
Internal Reference	−2		+2	−2		+2	−2		+2	−2		+2	% of FSR
Full-Scale Output Current[1]													
AVDD = 3.3 V	1	2	4	1	2	4	1	2	4	1	2	4	mA
AVDD = 1.8 V	1	2	2.5	1	2	2.5	1	2	2.5	1	2	2.5	mA
Output Compliance Range	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	V
Output Resistance		200			200			200			200		MΩ
Crosstalk, Q DAC to I DAC													
f_{OUT} = 30 MHz		97			97			97			97		dB
f_{OUT} = 60 MHz		78			78			78			78		dB
MAIN DAC TEMPERATURE DRIFT													
Offset		0			0			0			0		ppm/°C
Gain		±40			±40			±40			±40		ppm/°C
Reference Voltage		±25			±25			±25			±25		ppm/°C
AUXDAC OUTPUTS													
Resolution		10			10			10			10		Bits
Full-Scale Output Current (Current Sourcing Mode)		125			125			125			125		μA
Voltage Output Mode	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V
Output Compliance Range (Sourcing 1 mA)	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V

SPECIFICATIONS

Table 1. (Continued)

Parameter	AD9714 Min	AD9714 Typ	AD9714 Max	AD9715 Min	AD9715 Typ	AD9715 Max	AD9716 Min	AD9716 Typ	AD9716 Max	AD9717 Min	AD9717 Typ	AD9717 Max	Unit
Output Compliance Range (Sinking 1 mA)	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V
Output Resistance in Current Output Mode, AV_{SS} to 1 V		1			1			1			1		MΩ
AUX DAC Monotonicity Guaranteed		10			10			10			10		Bits
REFERENCE OUTPUT													
Internal Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Output Resistance		10			10			10			10		kΩ
REFERENCE INPUT													
Voltage Compliance													
AVDD = 3.3 V	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
AVDD = 1.8 V	0.1		1.0	0.1		1.0	0.1		1.0	0.1		1.0	V
Input Resistance External Reference Mode		1			1			1			1		MΩ
DAC MATCHING													
Gain Matching	−1		+1	−1		+1	−1		+1	−1		+1	% FSR
ANALOG SUPPLY VOLTAGES													
AVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
CVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
DIGITAL SUPPLY VOLTAGES													
DVDD	1.7		1.9	1.7		1.9	1.7		1.9	1.7		1.9	V
DVDDIO	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 3.3 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		86			86			86			86		mW
I_{AVDD}		10			10			10			10		mA
I_{DVDD} + I_{DVDDIO}		11			11			11			11		mA
I_{CVDD}		3			3			3			3		mA
Power-Down Mode with Clock		50			50			50			50		mW
Power-Down Mode, No Clock		1.5			1.5			1.5			1.5		mW
Power Supply Rejection Ratio		−0.04			−0.04			−0.04			−0.04		% FSR/V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 1.8 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		35			35			35			35		mW
I_{AVDD}		10			10			10			10		mA
I_{DVDD} + I_{DVDDIO}		8			8			8			8		mA
I_{CVDD}		1.5			1.5			1.5			1.5		mA
Power-Down Mode with Clock		12			12			12			12		mW
Power-Down Mode, No Clock		850			850			850			850		μW
Power Supply Rejection Ratio		−0.001			−0.001			−0.001			−0.001		% FSR/V
OPERATING RANGE	–40	+25	+85	–40	+25	+85	–40	+25	+85	–40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

SPECIFICATIONS

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
Maximum Clock Rate			125	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)		25		MHz
Minimum Pulse Width High		20		ns
Minimum Pulse Width Low		20		ns
INPUT DATA				
1.8 V Q Channel or DCLKIO Falling Edge				
Setup Time, t_S		0.25		ns
Hold Time, t_H		1.2		ns
1.8 V I Channel or DCLKIO Rising Edge				
Setup Time, t_S		0.13		ns
Hold Time, t_H		1.1		ns
3.3 V Q Channel or DCLKIO Falling Edge				
Setup Time, t_S		−0.2		ns
Hold Time, t_H		1.5		ns
3.3 V I Channel or DCLKIO Rising Edge				
Setup Time, t_S		−0.2		ns
Hold Time, t_H		1.6		ns
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9714			AD9715			AD9716			AD9717			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			82			83			84		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		60			61			62			63		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		86			87			88			89		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		71			71			71			71		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−129			−141			−149			−152		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−123			−135			−137			−141		dBc/Hz

SPECIFICATIONS

Table 3. (Continued)

Parameter	AD9714 Min	AD9714 Typ	AD9714 Max	AD9715 Min	AD9715 Typ	AD9715 Max	AD9716 Min	AD9716 Typ	AD9716 Max	AD9717 Min	AD9717 Typ	AD9717 Max	Unit
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−71			−71			−71			−71		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−72			−72			−72			−72		dBc

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, DVDDIO = 1.8 V, CVDD = 1.8 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 4.

Parameter	AD9714 Min	AD9714 Typ	AD9714 Max	AD9715 Min	AD9715 Typ	AD9715 Max	AD9716 Min	AD9716 Typ	AD9716 Max	AD9717 Min	AD9717 Typ	AD9717 Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			78			79			80		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		55			56			57			58		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		79			80			84			85		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		53			53			53			53		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−132			−141			−146			−148		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−126			−131			−131			−132		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−68			−68			−68			−68		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−68			−68			−68			−68		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DVDDIO, CVDD to AVSS, DVSS, CVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.1 V
AVSS to DVSS, CVSS	−0.3 V to +0.3 V
DVSS to AVSS, CVSS	−0.3 V to +0.3 V
CVSS to AVSS, DVSS	−0.3 V to +0.3 V
REFIO, FSADJQ, FSADJI, CMLQ, CMLI to AVSS	−0.3 V to AVDD + 0.3 V
QOUTP, QOUTN, IOUTP, IOUTN, RLQP, RLQN, RLIP, RLIN to AVSS	−1.0 V to AVDD + 0.3 V
DBn[1] (MSB) to DB0 (LSB), $\overline{CS}$, SCLK, SDIO, RESET to DVSS	−0.3 V to DVDDIO + 0.3 V
CLKIN to CVSS	−0.3 V to CVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

1 n stands for 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

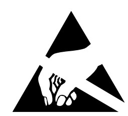
THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	θ_{JB}[1]	θ_{JC}[1]	Unit
40-Lead LFCSP (with No Airflow Movement)	29.8	19.0	3.4	°C/W

1 These calculations are intended to represent the thermal performance of the indicated packages using a JEDEC multilayer test board. Do not assume the same level of thermal performance in actual applications without a careful inspection of the conditions in the application to determine that they are similar to those assumed in these calculations.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

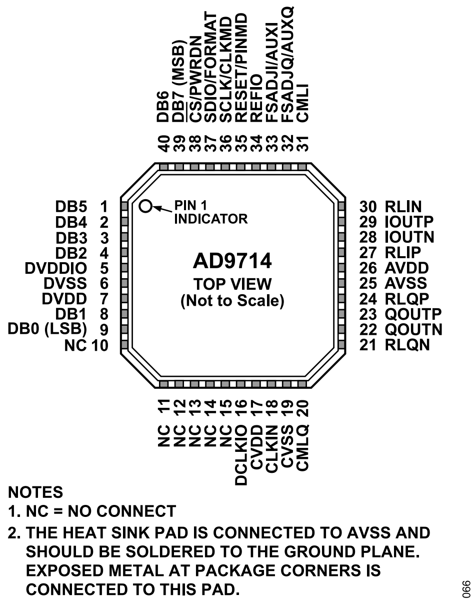


Figure 2. AD9714 Pin Configuration

Table 7. AD9714 Pin Function Descriptions

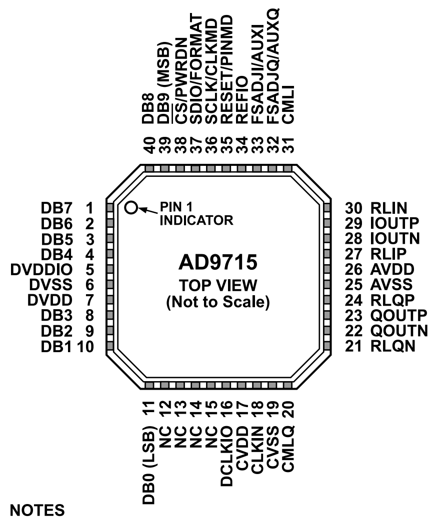
Pin No.	Mnemonic	Description
1 to 4	DB[5:2]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). If DVDDIO is 1.8 V, strap DVDD to DVDDIO. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor. Do not connect external loads to DVDD.
8	DB1	Digital Inputs.
9	DB0 (LSB)	Digital Input (LSB).
10 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 7. AD9714 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 μF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the two complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port. Power-Down (PWRDN). In pin mode, PWRDN powers down the device except for the SPI port.
39	DB7 (MSB)	Digital Input (MSB).
40	DB6	Digital Input.
41	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT
2. THE HEAT SINK PAD IS CONNECTED TO AVSS AND SHOULD BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

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Figure 3. AD9715 Pin Configuration

Table 8. AD9715 Pin Function Descriptions

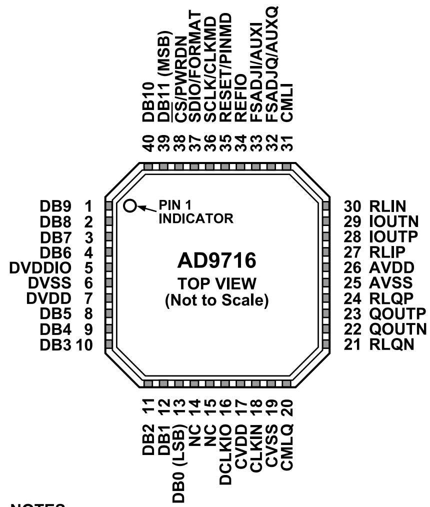
Pin No.	Mnemonic	Description
1 to 4	DB[7:4]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). If DVDDIO is 1.8 V, strap DVDD to DVDDIO. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μF capacitor. Do not connect external loads to DVDD.
8 to 10	DB[3:1]	Digital Inputs.
11	DB0 (LSB)	Digital Input (LSB).
12 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 8. AD9715 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB9 (MSB)	Digital Input (MSB).
40	DB8	Digital Input.
41	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT
2. THE HEAT SINK PAD IS CONNECTED TO AVSS AND SHOULD BE SOLDERED TO THE GROUND PLANE. EXPOSED METAL AT PACKAGE CORNERS IS CONNECTED TO THIS PAD.

003

Figure 4. AD9716 Pin Configuration

Table 9. AD9716 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[9:6]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). If DVDDIO is 1.8 V, strap DVDD to DVDDIO. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μF capacitor. Do not connect external loads to DVDD.
8 to 12	DB[5:1]	Digital Inputs.
13	DB0 (LSB)	Digital Input (LSB).
14, 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 9. AD9716 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current.
		Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current.
		Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 μF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values.
		A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port.
		Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port.
		Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select.
		Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB11 (MSB)	Digital Input (MSB).
40	DB10	Digital Input.
41	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

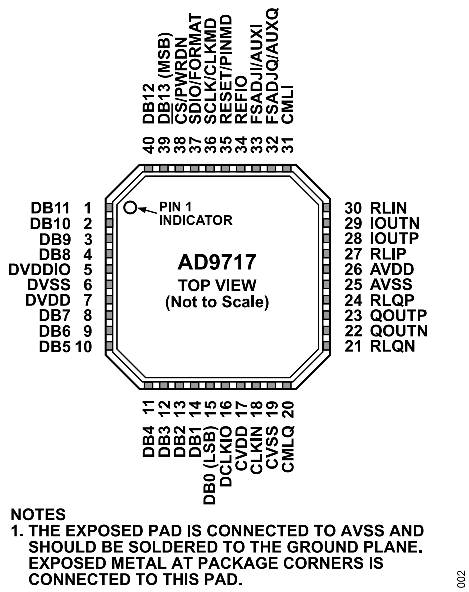


Figure 5. AD9717 Pin Configuration

Table 10. AD9717 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[11:8]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). If DVDDIO is 1.8 V, strap DVDD to DVDDIO. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 μF capacitor. Do not connect external loads to DVDD.
8 to 14	DB[7:1]	Digital Inputs.
15	DB0 (LSB)	Digital Input (LSB).
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 10. AD9717 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current.
		Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current.
		Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 μF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values.
		A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port.
		Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port.
		Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select.
		Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB13 (MSB)	Digital Input (MSB).
40	DB12	Digital Input.
41	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

TYPICAL PERFORMANCE CHARACTERISTICS

I_{xOUTFS} = 2 mA, maximum sample rate (125 MSPS), unless otherwise noted. DVDD is always at 1.8 V.

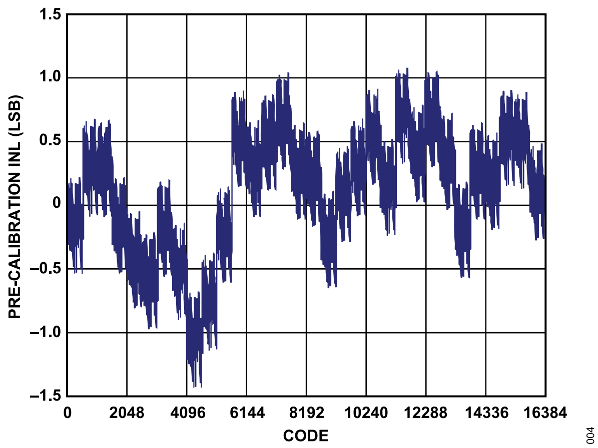


Figure 6. AD9717 Precalibration INL at 1.8 V (DVDD = 1.8 V)

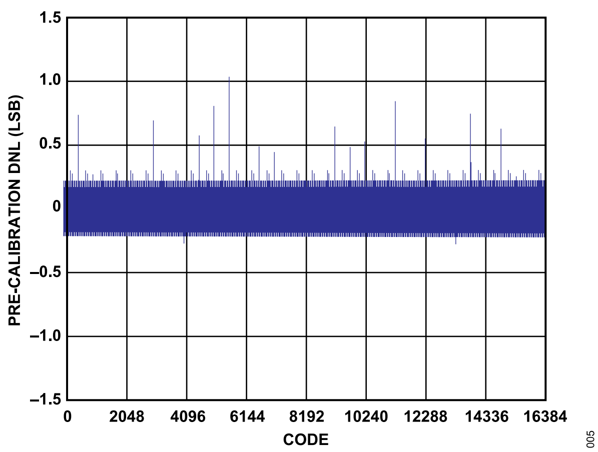


Figure 7. AD9717 Precalibration DNL at 1.8 V (DVDD = 1.8 V)

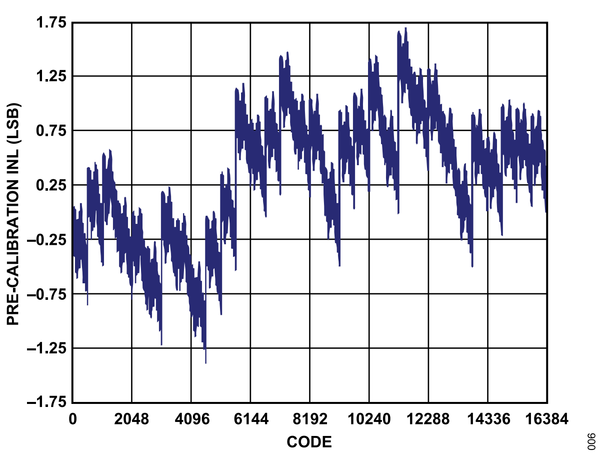


Figure 8. AD9717 Precalibration INL at 3.3 V (DVDD = 1.8 V)

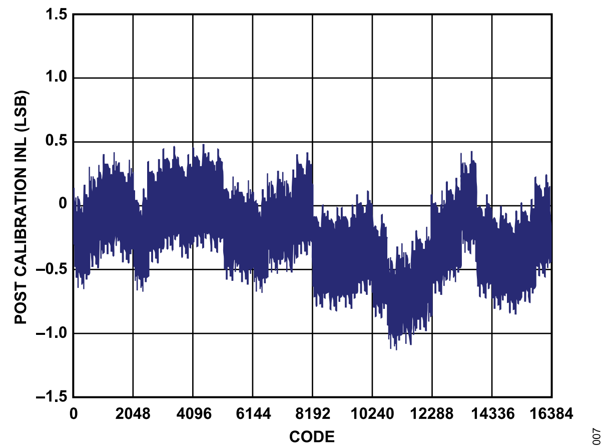


Figure 9. AD9717 Postcalibration INL at 1.8 V (DVDD = 1.8 V)

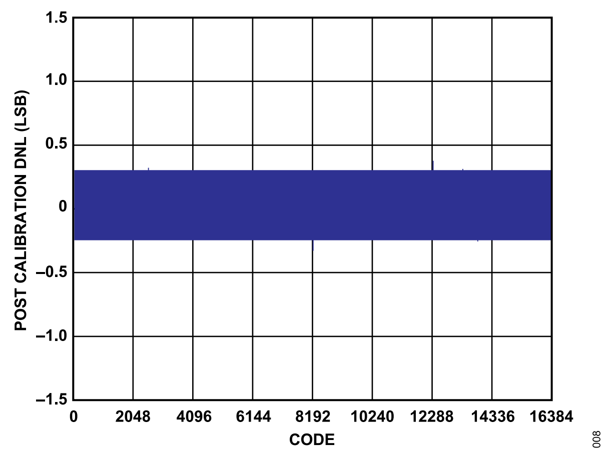


Figure 10. AD9717 Postcalibration DNL at 1.8 V (DVDD = 1.8 V)

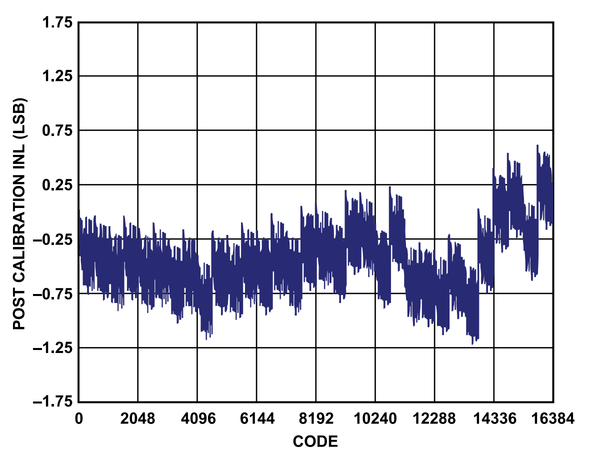


Figure 11. AD9717 Postcalibration INL at 3.3 V (DVDD = 1.8 V)

TYPICAL PERFORMANCE CHARACTERISTICS

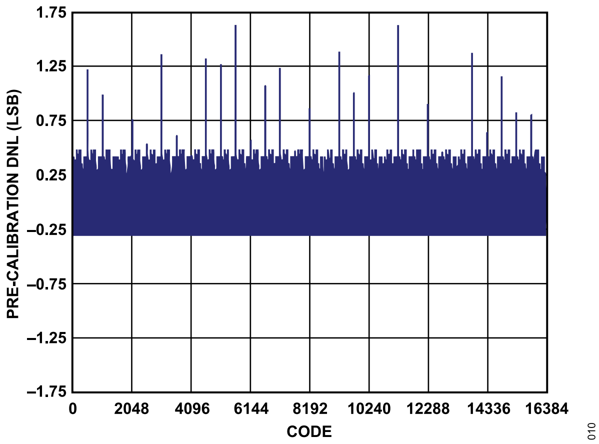


Figure 12. AD9717 Precalibration DNL at 3.3 V

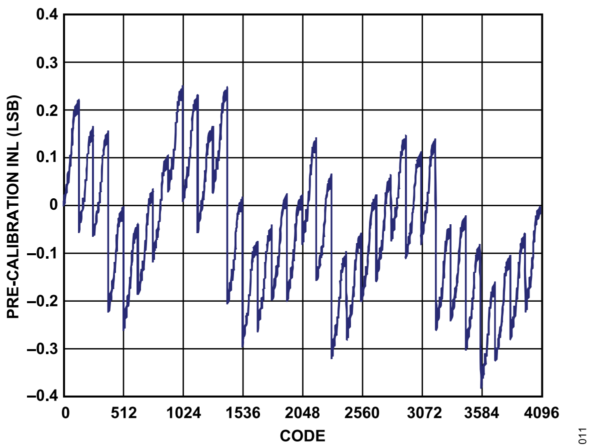


Figure 13. AD9716 Precalibration INL at 1.8 V

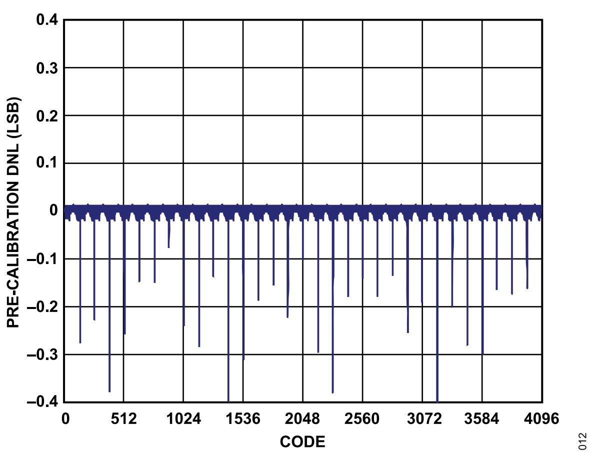


Figure 14. AD9716 Precalibration DNL at 1.8 V

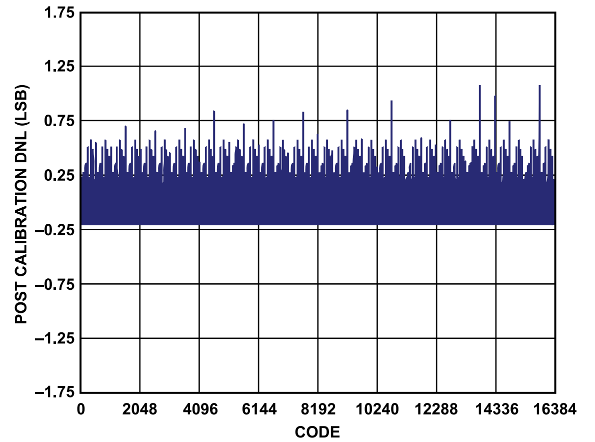


Figure 15. AD9717 Postcalibration DNL at 3.3 V

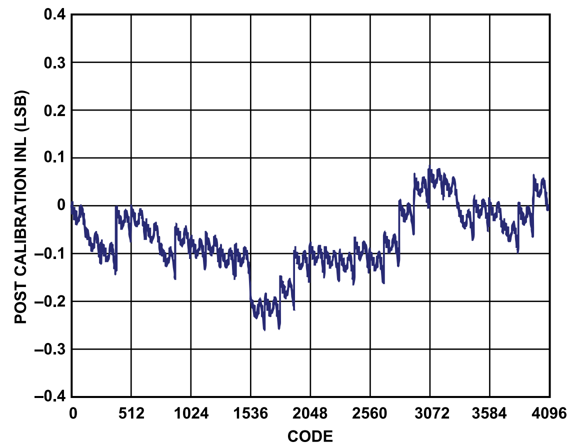


Figure 16. AD9716 Postcalibration INL at 1.8 V

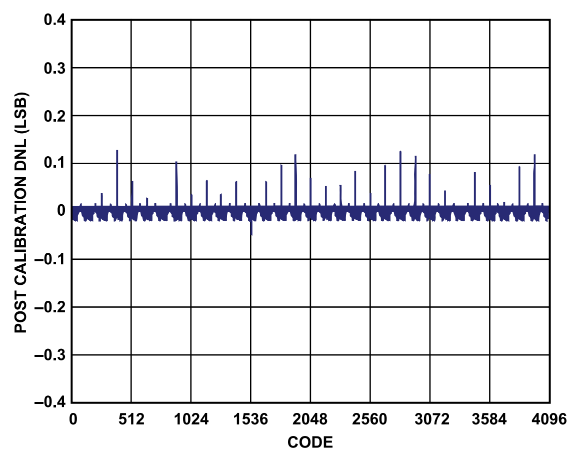


Figure 17. AD9716 Postcalibration DNL at 1.8 V

TYPICAL PERFORMANCE CHARACTERISTICS

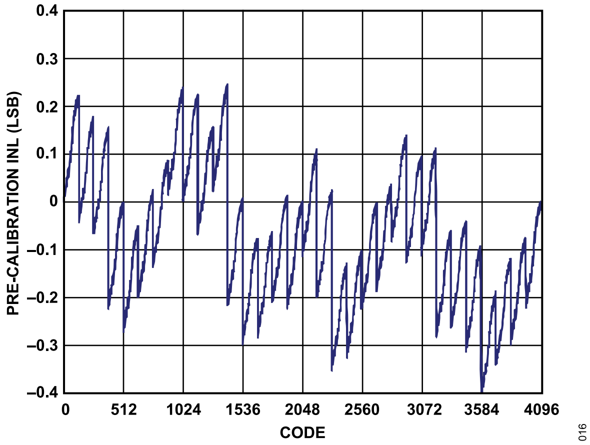


Figure 18. AD9716 Precalibration INL at 3.3 V

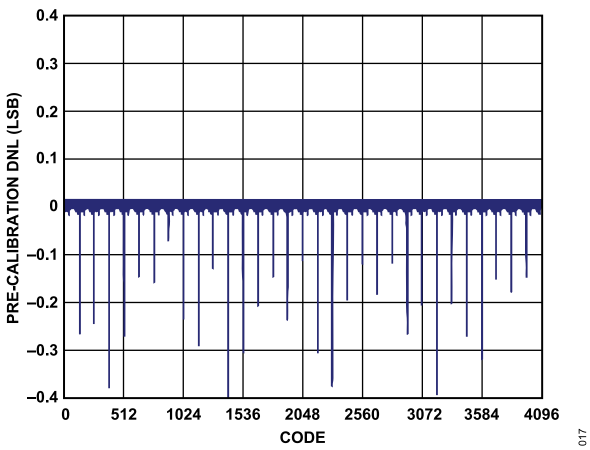


Figure 19. AD9716 Precalibration DNL at 3.3 V

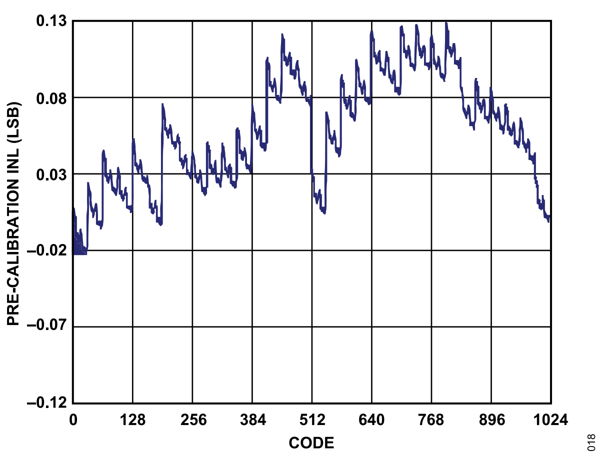


Figure 20. AD9715 Precalibration INL at 1.8 V

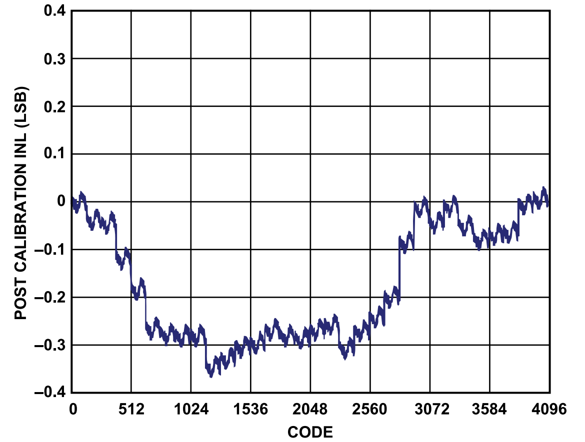


Figure 21. AD9716 Postcalibration INL at 3.3 V

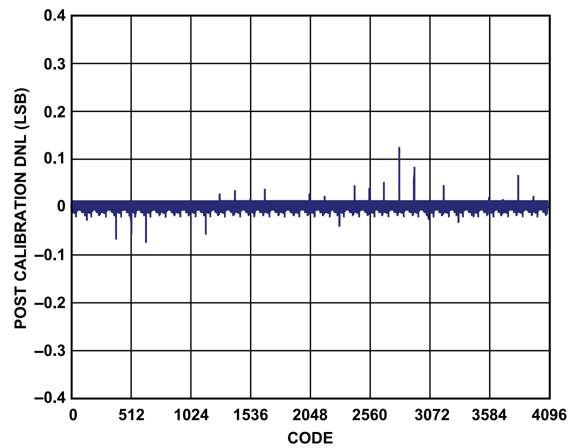


Figure 22. AD9716 Postcalibration DNL at 3.3 V

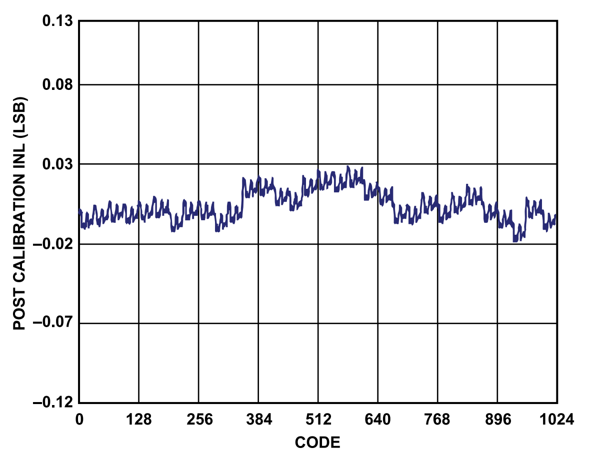


Figure 23. AD9715 Postcalibration INL at 1.8 V

TYPICAL PERFORMANCE CHARACTERISTICS

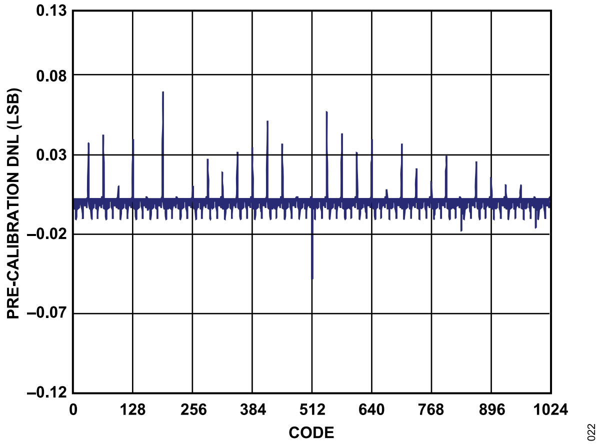


Figure 24. AD9715 Precalibration DNL at 1.8 V

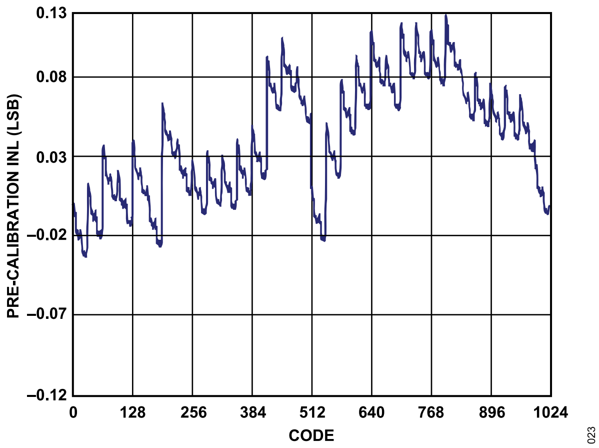


Figure 25. AD9715 Precalibration INL at 3.3 V

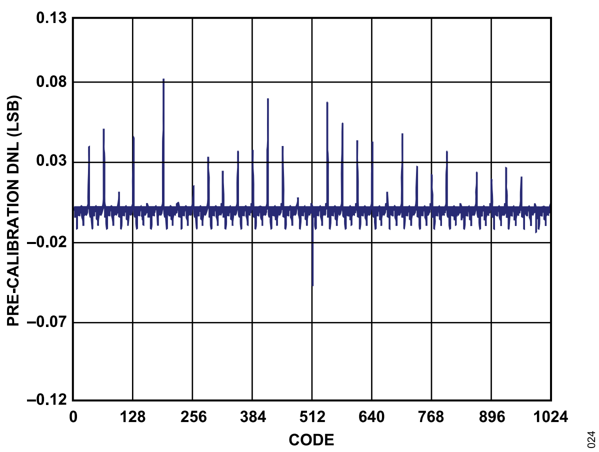


Figure 26. AD9715 Precalibration DNL at 3.3 V

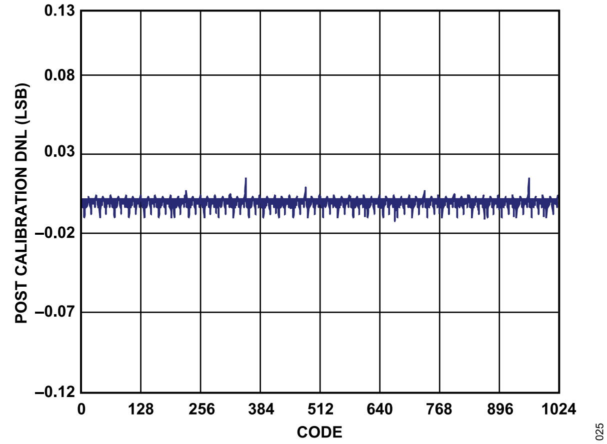


Figure 27. AD9715 Postcalibration DNL at 1.8 V

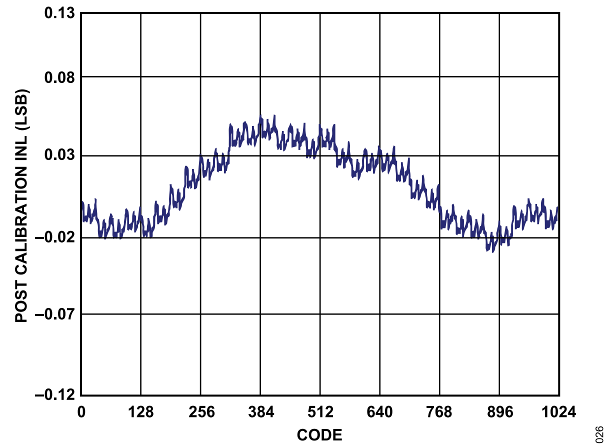


Figure 28. AD9715 Postcalibration INL at 3.3 V

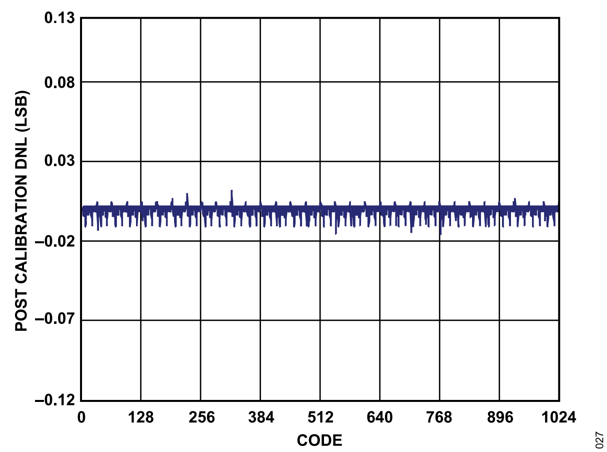


Figure 29. AD9715 Postcalibration DNL at 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

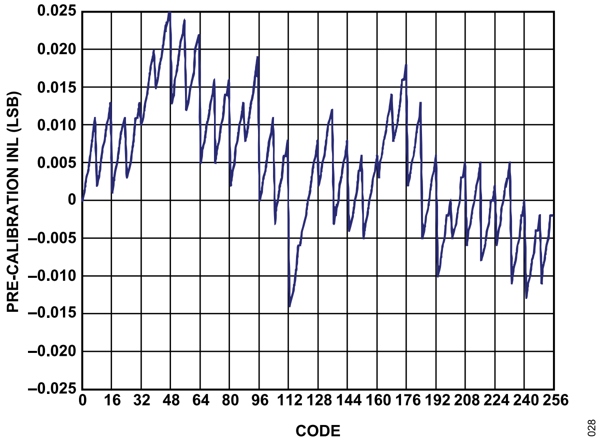


Figure 30. AD9714 Precalibration INL at 1.8 V

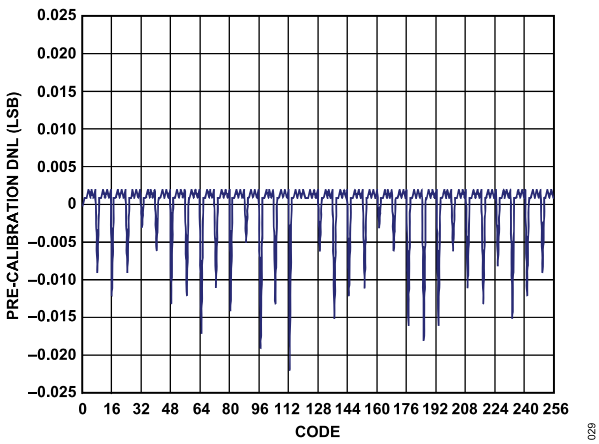


Figure 31. AD9714 Precalibration DNL at 1.8 V

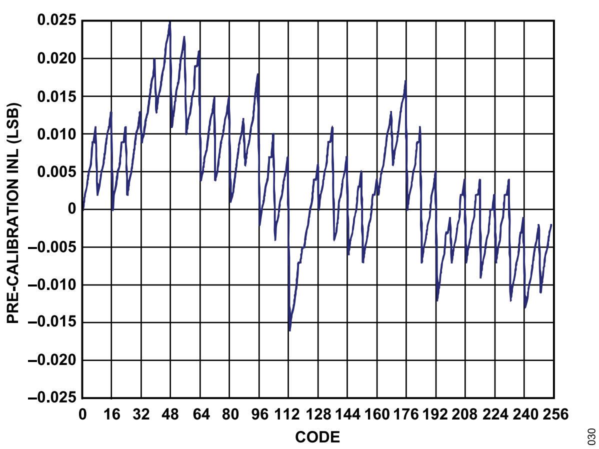


Figure 32. AD9714 Precalibration INL at 3.3 V

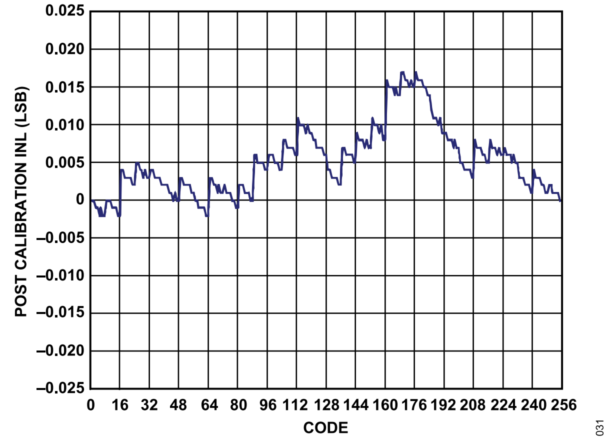


Figure 33. AD9714 Postcalibration INL at 1.8 V

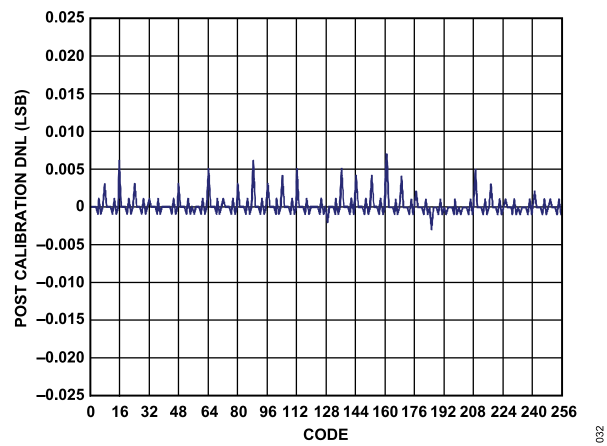


Figure 34. AD9714 Postcalibration DNL at 1.8 V

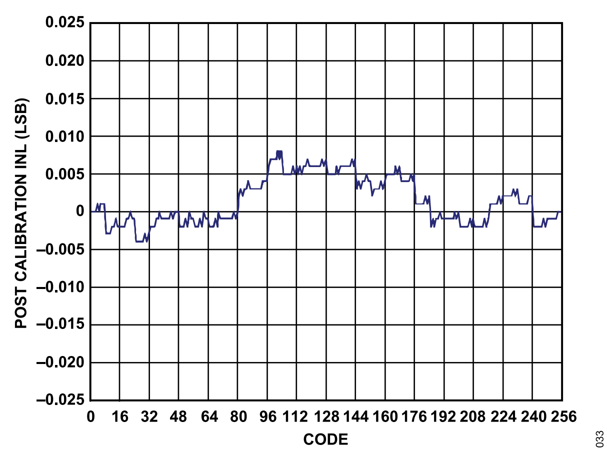


Figure 35. AD9714 Postcalibration INL at 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

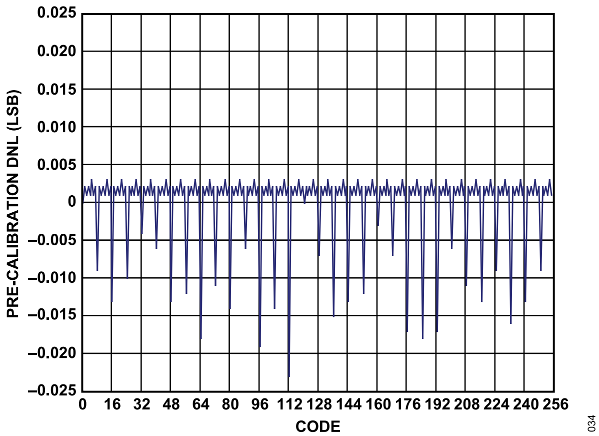


Figure 36. AD9714 Precalibration DNL at 3.3 V

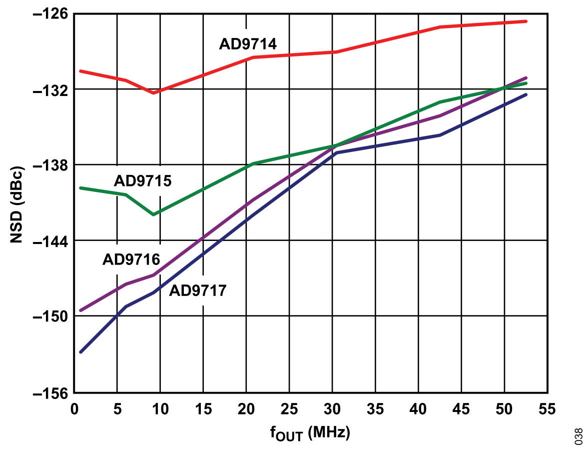


Figure 37. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 1.8 V

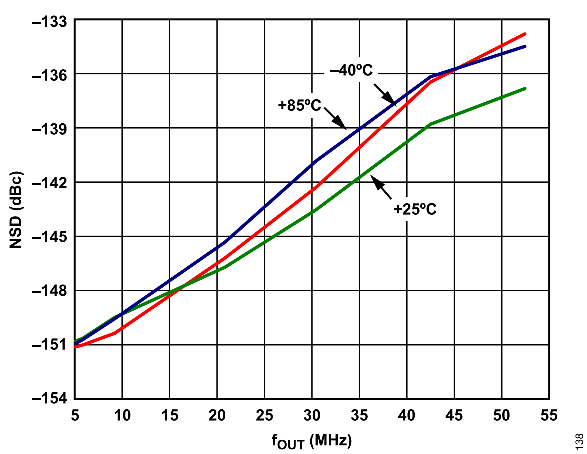


Figure 38. AD9717 Noise Spectral Density at Three Temperatures, 1.8 V

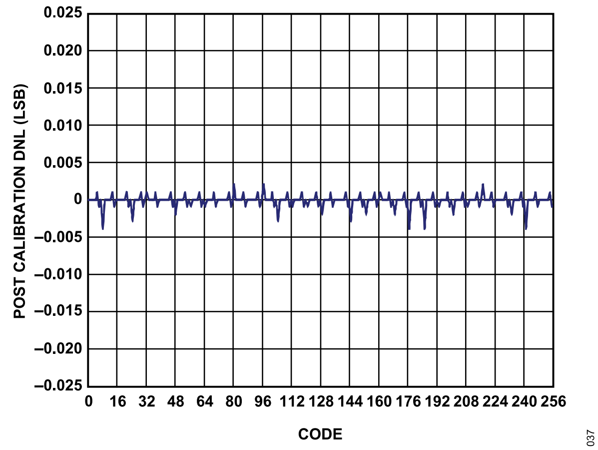


Figure 39. AD9714 Postcalibration DNL at 3.3 V

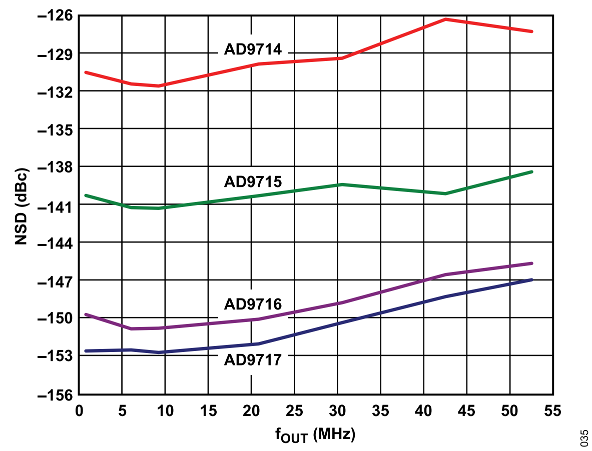


Figure 40. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 3.3 V

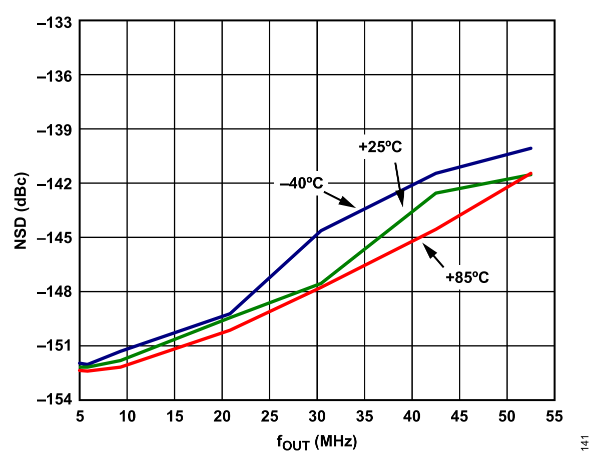


Figure 41. AD9717 Noise Spectral Density at Three Temperatures, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

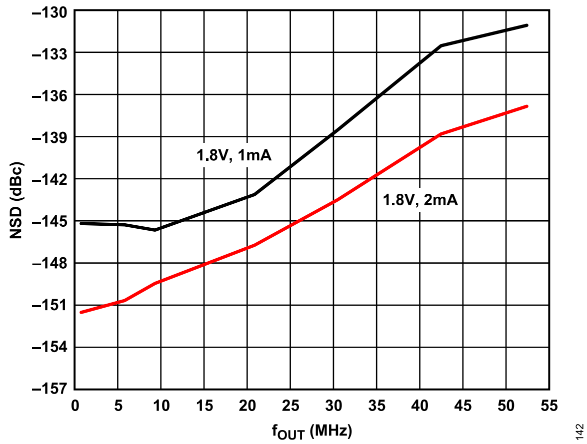


Figure 42. AD9717 Noise Spectral Density at Two Output Currents, 1.8 V

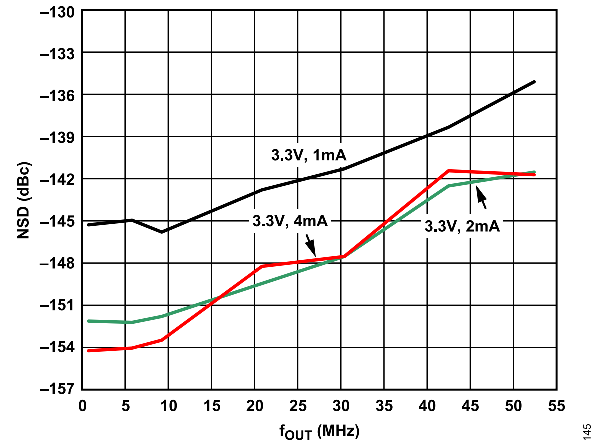


Figure 45. AD9717 Noise Spectral Density at Three Output Currents, 3.3 V

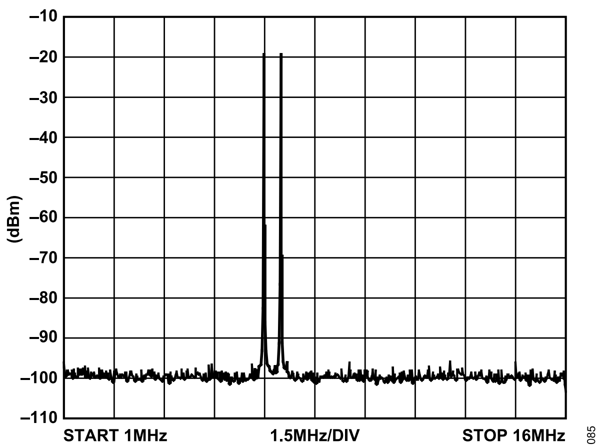


Figure 43. AD9717 Two Tone Spectrum, 1.8 V

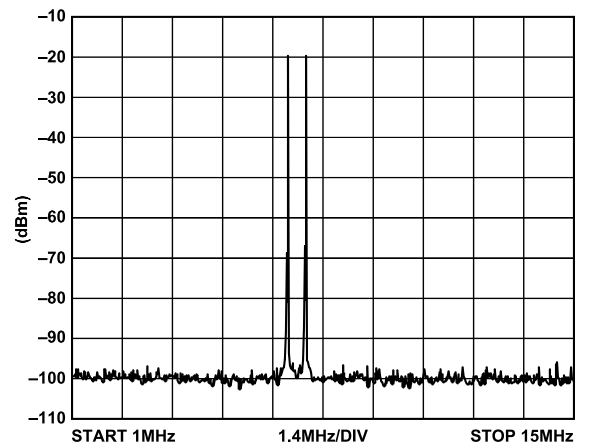


Figure 46. AD9717 Two Tone Spectrum, 3.3 V

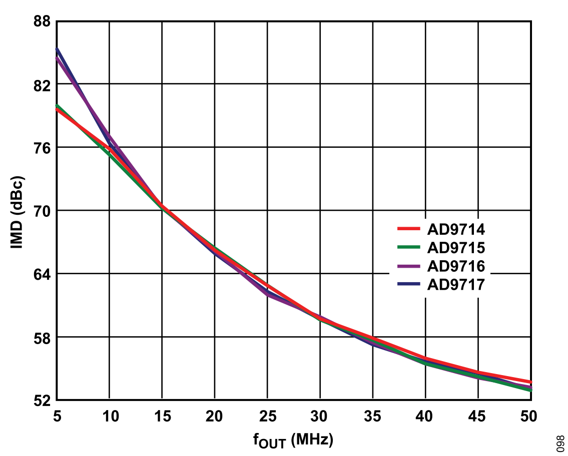


Figure 44. AD9714/AD9715/AD9716/AD9717 IMD at 1.8 V

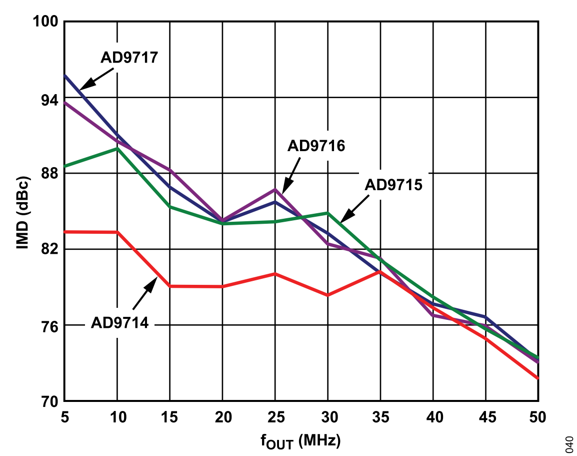


Figure 47. AD9714/AD9715/AD9716/AD9717 IMD at 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

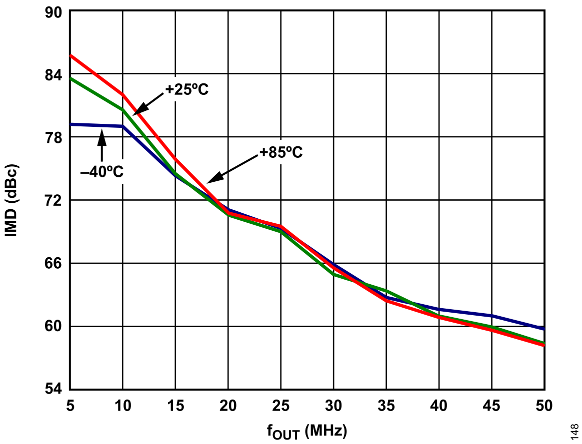


Figure 48. AD9717 IMD at Three Temperatures, 1.8 V

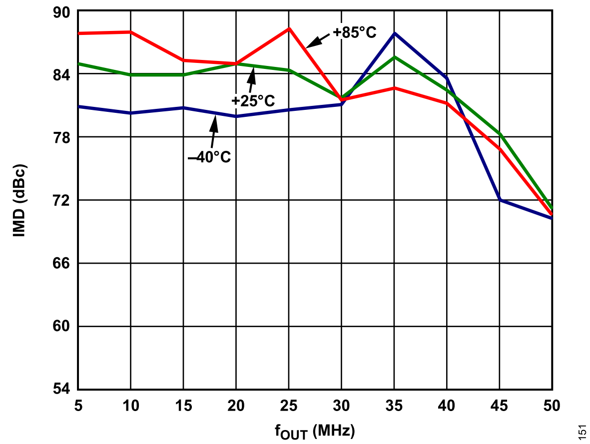


Figure 51. AD9717 IMD at Three Temperatures, 3.3 V

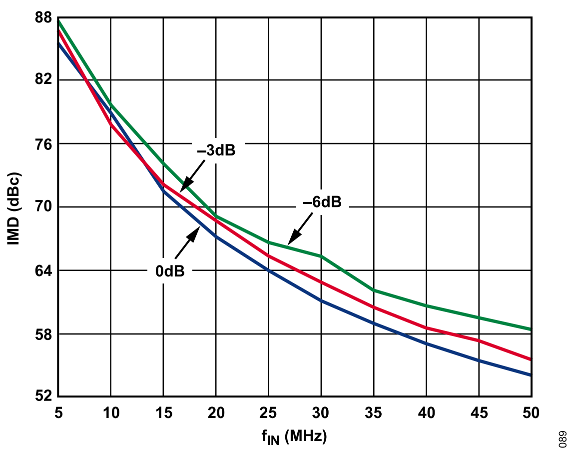


Figure 49. AD9717 IMD at Three Digital Input Levels, 1.8 V

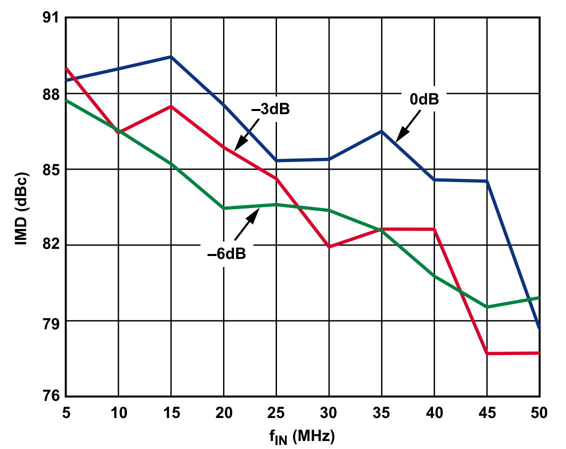


Figure 52. AD9717 IMD at Three Digital Input Levels, 3.3 V

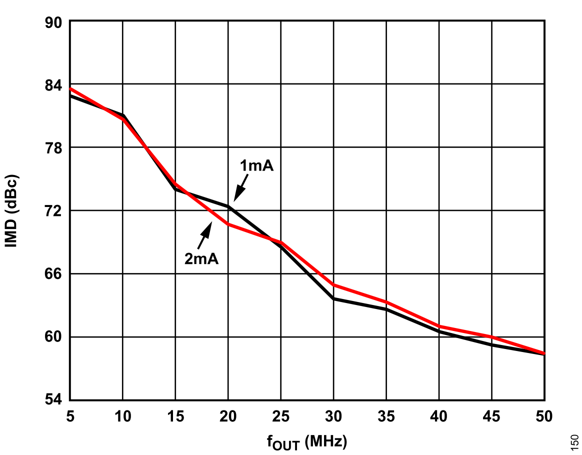


Figure 50. AD9717 IMD at Two Output Currents, 1.8 V

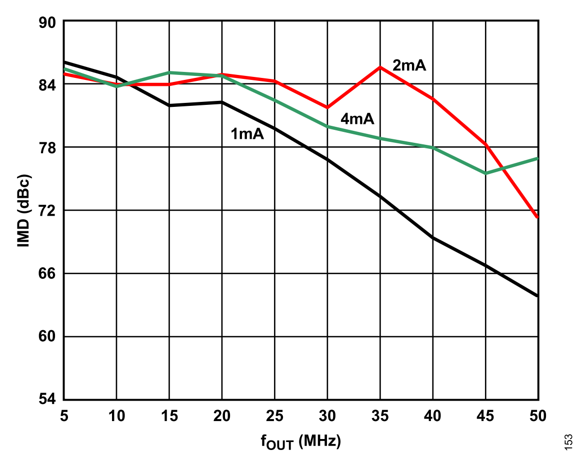


Figure 53. AD9717 IMD at Three Output Currents, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

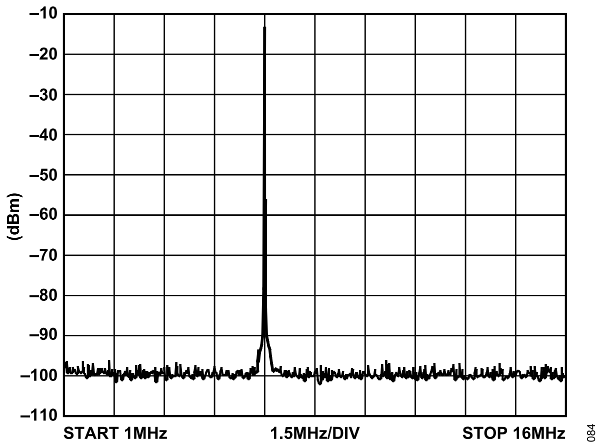


Figure 54. AD9717 Single-Tone Spectrum, 1.8 V

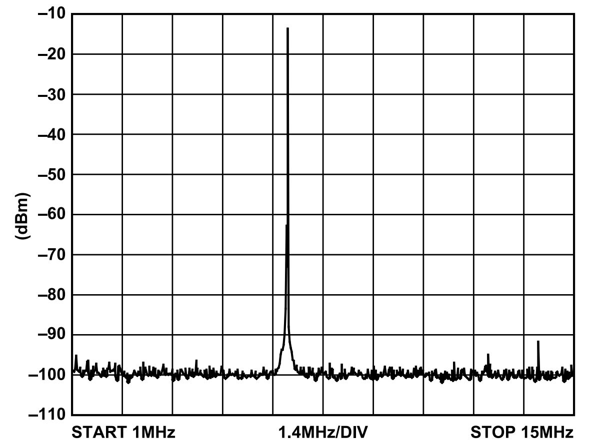


Figure 57. AD9717 Single-Tone Spectrum, 3.3 V

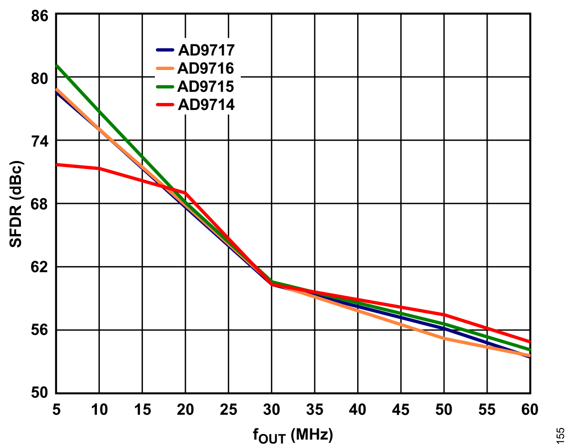


Figure 55. AD9714/AD9715/AD9716/AD9717 SFDR at 1.8 V

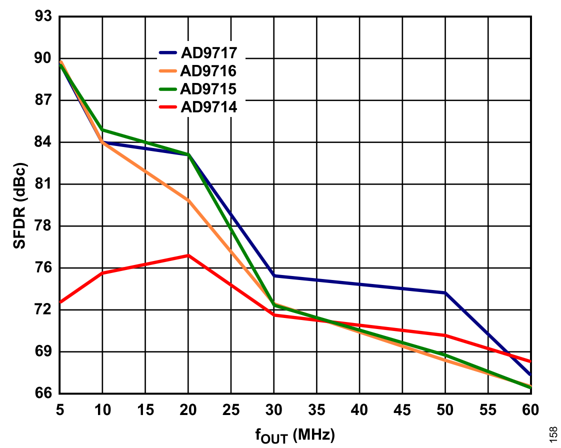


Figure 58. AD9714/AD9715/AD9716/AD9717 SFDR at 3.3 V

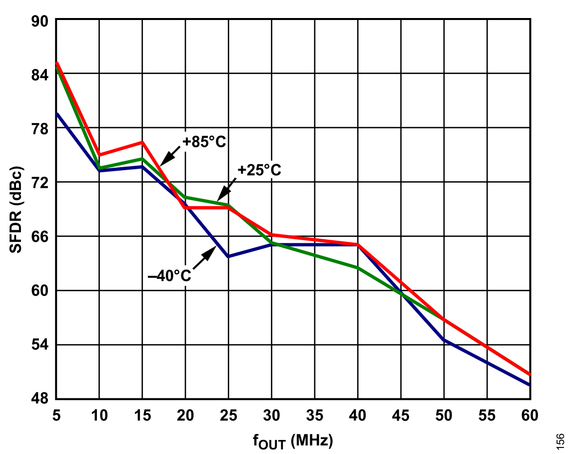


Figure 56. AD9717 SFDR at Three Temperatures, 1.8 V

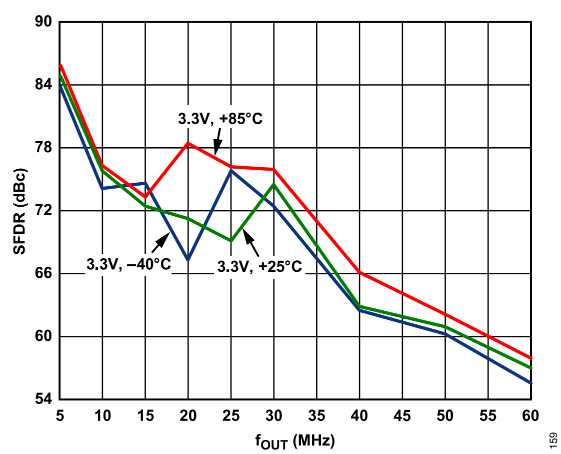


Figure 59. AD9717 SFDR at Three Temperatures, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

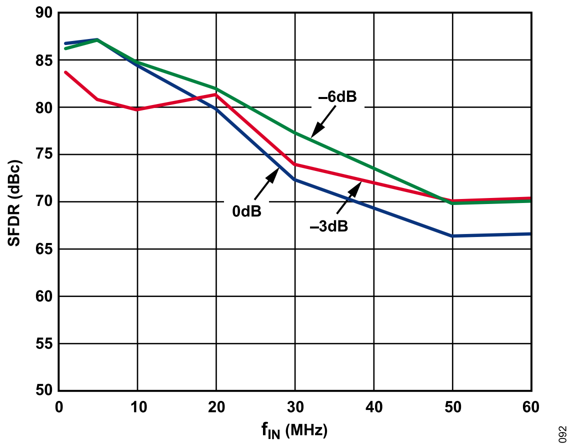


Figure 60. SFDR at Three Digital Input Levels vs. f_{IN}, 1.8 V

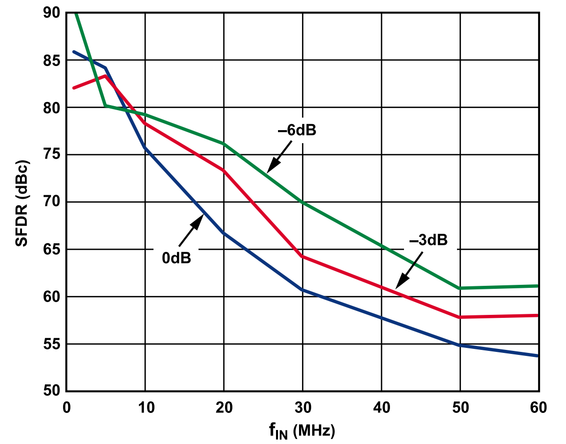


Figure 63. SFDR at Three Digital Input Levels vs. f_{IN}, 3.3 V

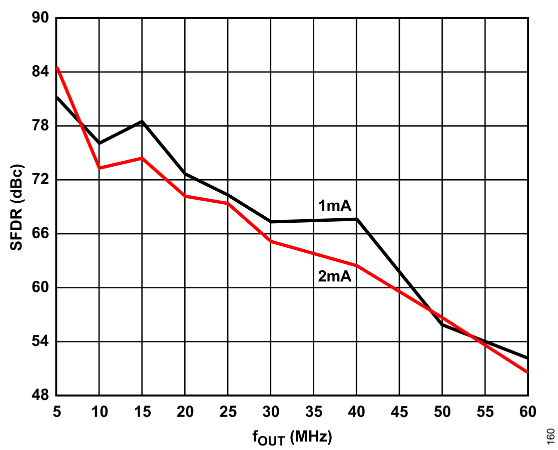


Figure 61. SFDR at Two Output Currents, 1.8 V

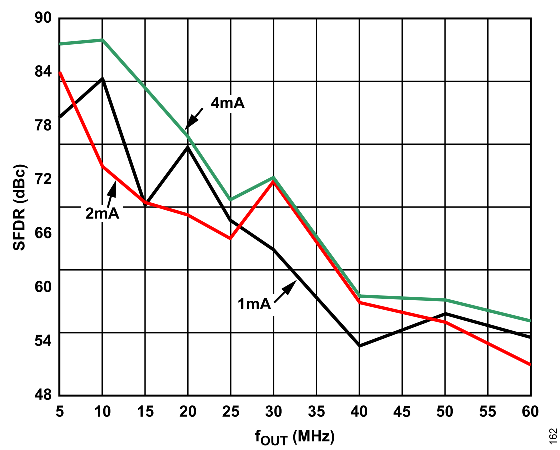


Figure 64. SFDR at Three Output Currents, 3.3 V

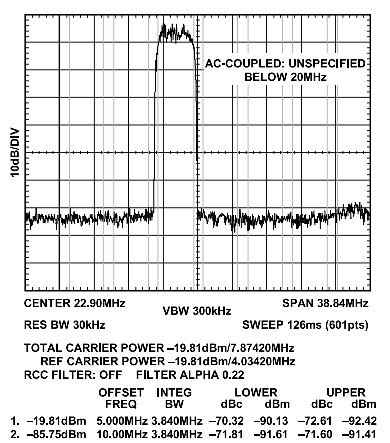


Figure 62. AD9717 One-Carrier ACLR, 1.8 V

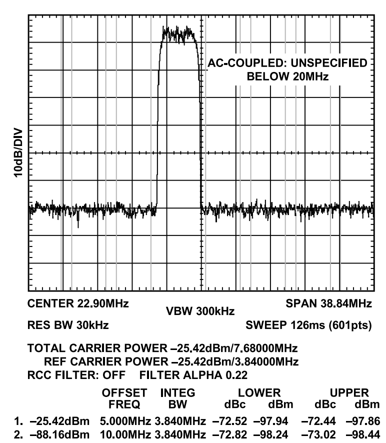


Figure 65. AD9717 One-Carrier ACLR, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

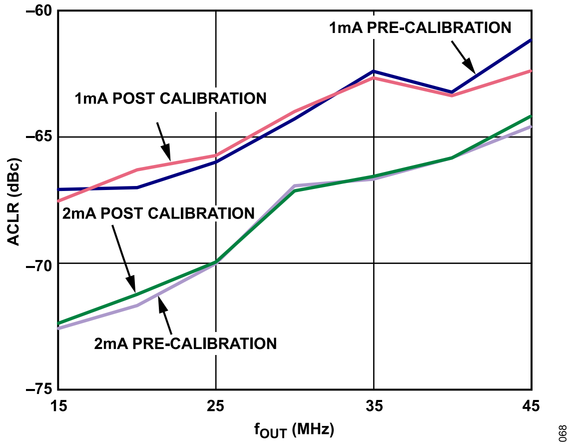


Figure 66. AD9717 One-Carrier W-CDMA First ACLR, 1.8 V

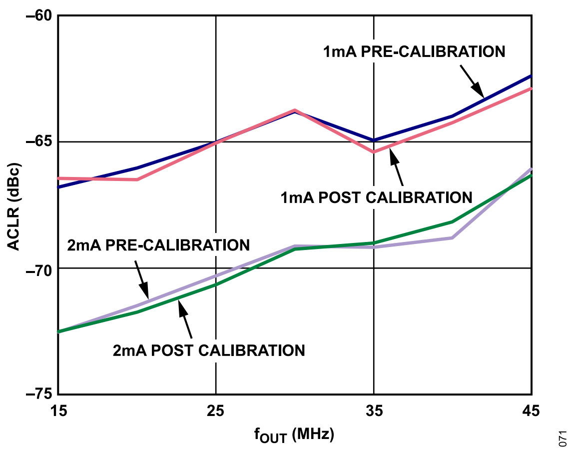


Figure 67. AD9717 One-Carrier W-CDMA Second ACLR, 1.8 V

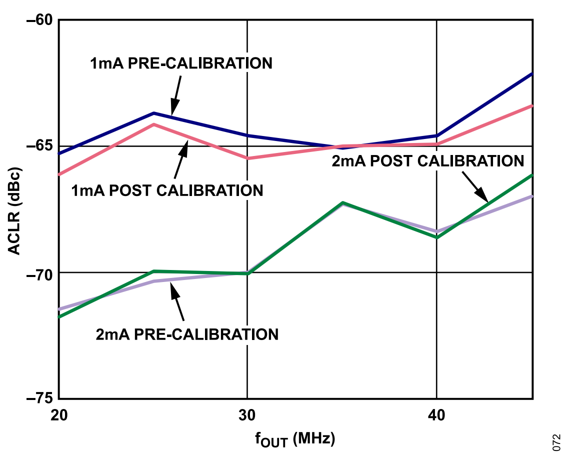


Figure 68. AD9717 One-Carrier W-CDMA Third ACLR, 1.8 V

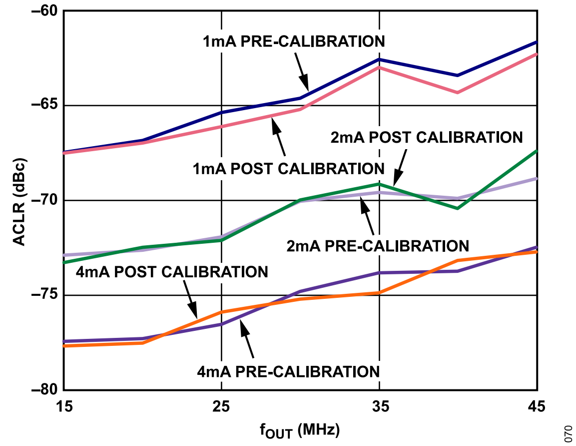


Figure 69. AD9717 One-Carrier W-CDMA First ACLR, 3.3 V

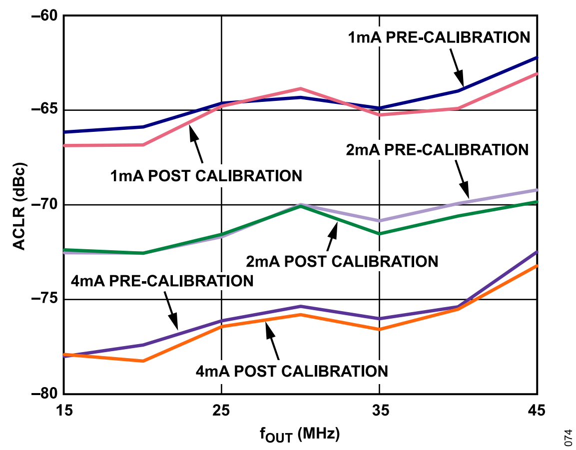


Figure 70. AD9717 One-Carrier W-CDMA Second ACLR, 3.3 V

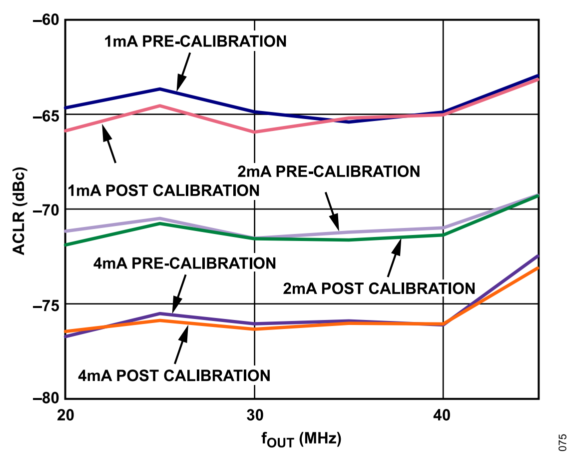


Figure 71. AD9717 One-Carrier W-CDMA Third ACLR, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

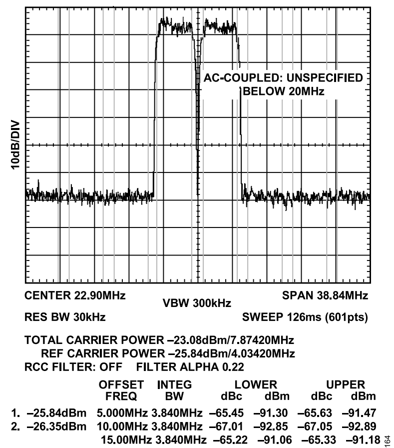


Figure 72. AD9717 Two-Carrier ACLR, 1.8 V

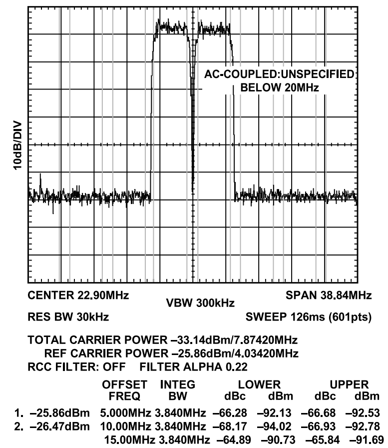


Figure 75. AD9717 Two-Carrier ACLR, 3.3 V

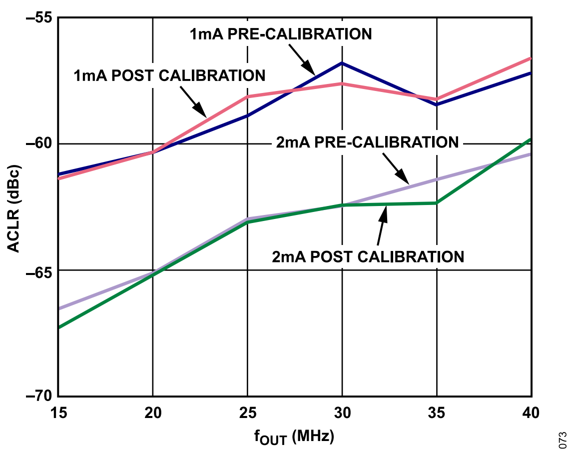


Figure 73. AD9717 Two-Carrier W-CDMA First ACLR, 1.8 V

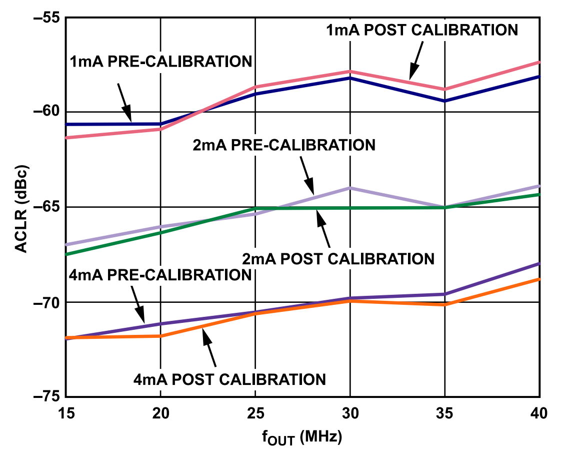


Figure 76. AD9717 Two-Carrier W-CDMA First ACLR, 3.3 V

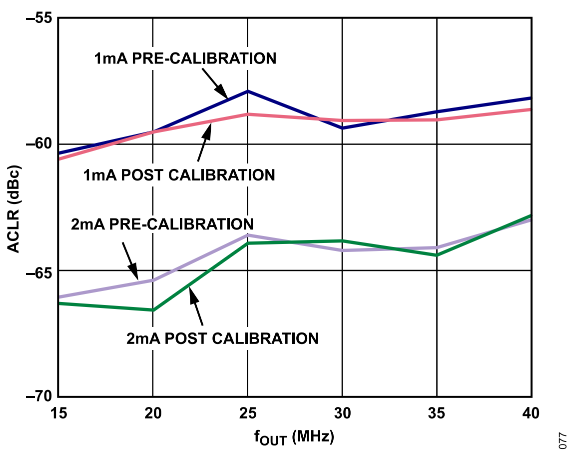


Figure 74. AD9717 Two-Carrier W-CDMA Second ACLR, 1.8 V

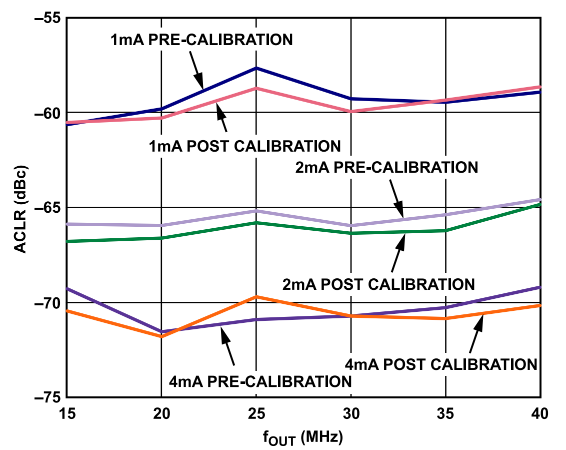


Figure 77. AD9717 Two-Carrier W-CDMA Second ACLR, 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

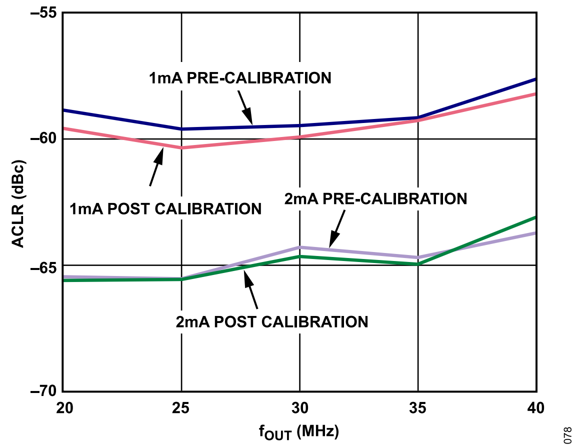


Figure 78. AD9717 Two-Carrier W-CDMA Third ACLR, 1.8 V

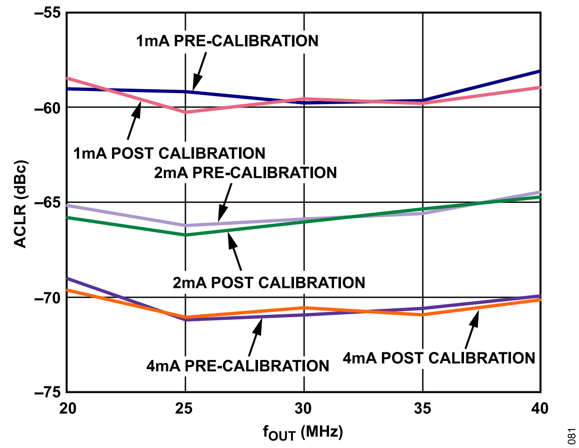


Figure 81. AD9717 Two-Carrier W-CDMA Third ACLR, 3.3 V

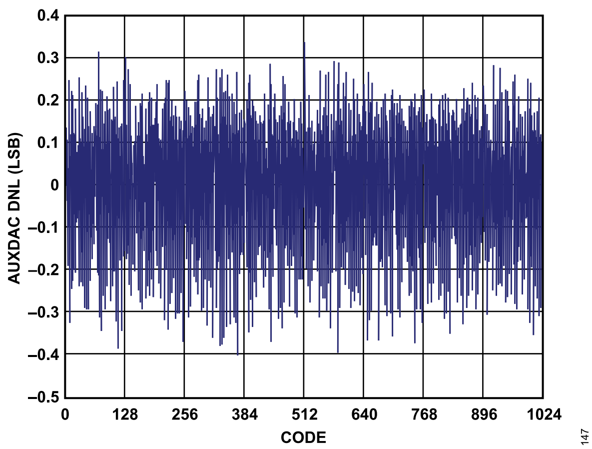


Figure 79. AUXDAC DNL

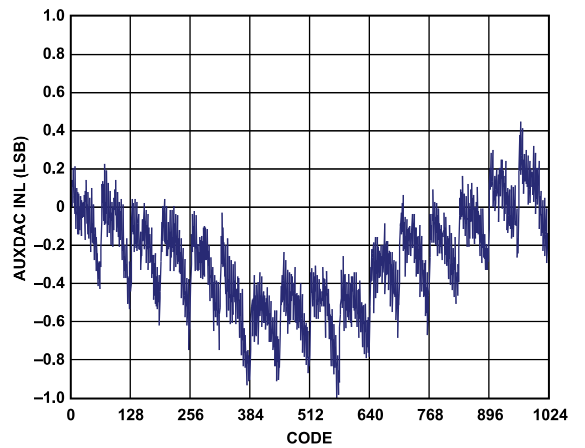


Figure 82. AUXDAC INL

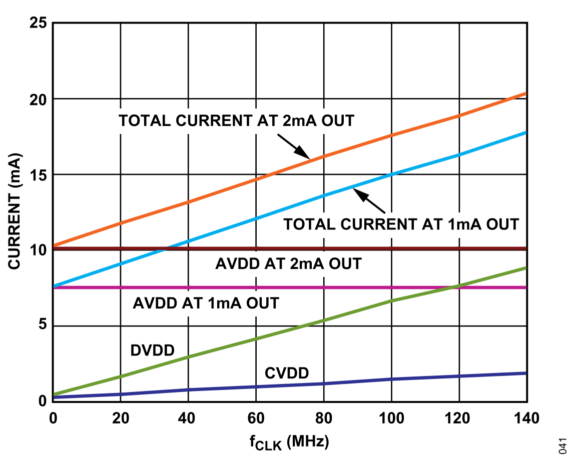


Figure 80. Supply Current vs. Clock Frequency at 1.8 V

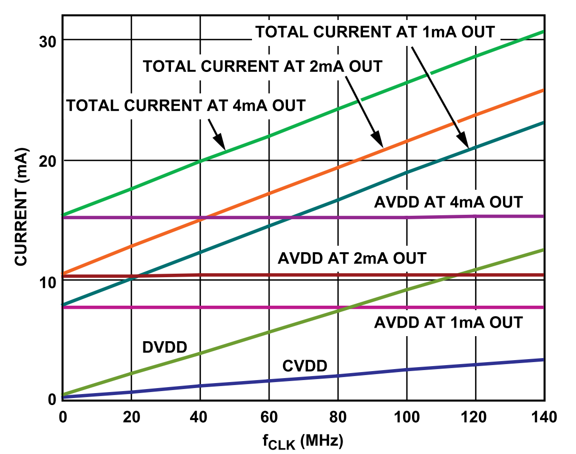


Figure 83. Supply Current vs. Clock Frequency at 3.3 V

TERMINOLOGY

Linearity Error or Integral Nonlinearity (INL)

Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

Offset error is the deviation of the output current from the ideal of zero. For I_{OUTP}, 0 mA output is expected when the inputs are all 0. For I_{OUTN}, 0 mA output is expected when all inputs are set to 1.

Gain Error

Gain error is the difference between the actual and the ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range

Output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient value (25°C) to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range per degree Celsius (ppm FSR/°C). For reference drift, the drift is reported in parts per million per degree Celsius (ppm/°C).

Power Supply Rejection

Power supply rejection is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time

Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels (dB).

Adjacent Channel Leakage Ratio (ACLR)

ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection

In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

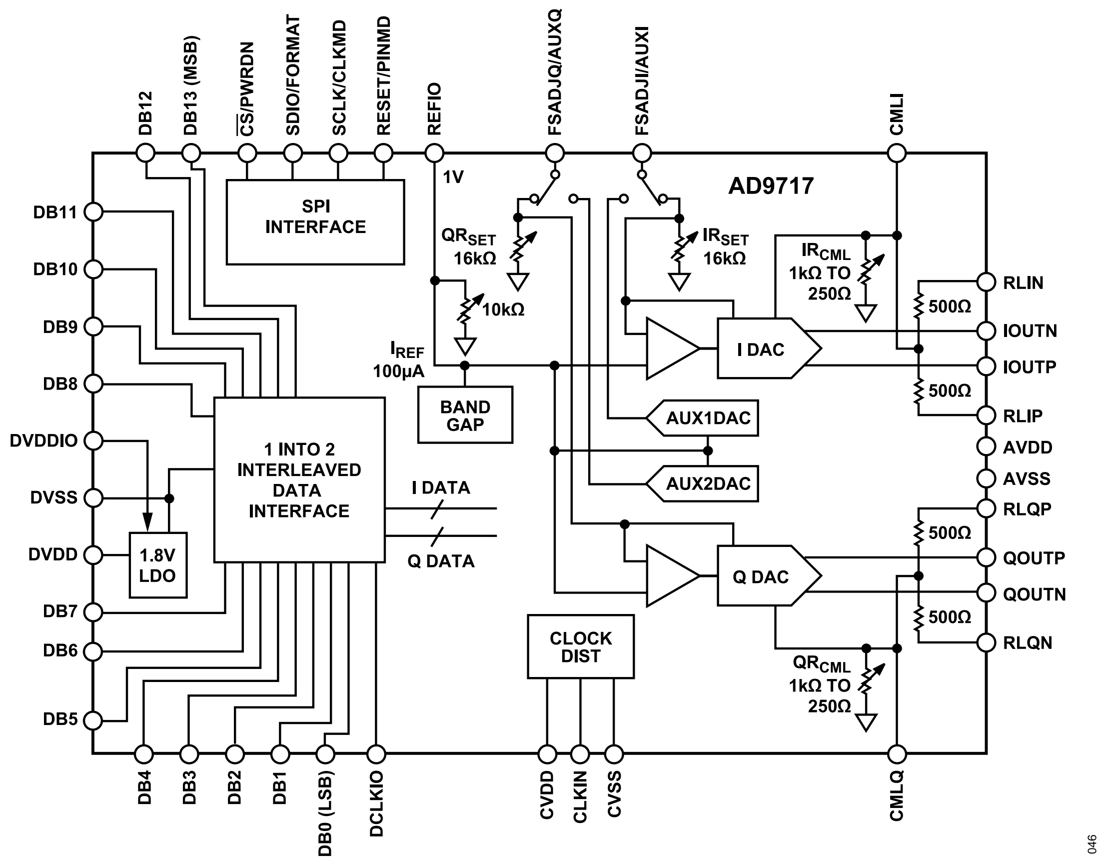


Figure 84. Simplified Block Diagram

Figure 84 shows a simplified block diagram of the AD9714/AD9715/AD9716/AD9717 that consists of two DACs, digital control logic, and a full-scale output current control. Each DAC contains a PMOS current source array capable of providing a nominal full-scale current (I_{xOUTFS}) of 2 mA and a maximum of 4 mA. The arrays are divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16 of an MSB current source. The remaining LSBs are binary weighted fractions of the current sources of the middle bits. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of the DACs (that is, >200 MΩ).

The current sources are switched to one or the other of the two output nodes (I_{OUTP} or I_{OUTN}) via PMOS differential current switches. The switches are based on the architecture that was pioneered in the AD976x family, with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital I/O sections of the AD9714/AD9715/AD9716/AD9717 have separate power supply inputs (AVDD, DVDDIO, and CVDD) that can operate independently over a 1.8 V to 3.3 V range. The core digital section (DVDD) requires 1.8 V. For an operating supply voltage of 1.8 V at DVDDIO, DVDD can be strapped to DVDDIO. Otherwise, for an operating supply voltage of >1.8 V at DVDDIO, the on-chip LDO for the digital block must be enabled and DVDD pin must be bypassed with a 0.1 µF capacitor. To ensure proper operation of the device, the RESET/PINMD pin must be pulsed high after applying power to all supplies. If operating the device in SPI mode, the minimum duration before setting the pin low is 50 ns. If operating the device in pin mode, there is no need to set RESET/PINMD low after pulsing it high and, alternatively, the pin can be pulled up to DVDDIO.

The core is capable of operating at a rate of up to 125 MSPS. It consists of edge-triggered latches and the segment decoding logic circuitry. The analog section includes PMOS current sources, associated differential switches, a 1.0 V band gap voltage reference, and a reference control amplifier.

Each DAC full-scale output current is regulated by the reference control amplifier and can be set from 1 mA to 4 mA via an external resistor, xR_{SET}, connected to its full-scale adjust pin (FSADJx).

The external resistor, in combination with both the reference control amplifier and voltage reference, V_{REFIO}, sets the reference current, I_{xREF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{xOUTFS}, is 32 × I_{xREF}.

THEORY OF OPERATION

Optional on-chip xR_{SET} resistors are provided that can be programmed between a nominal value of 8 kΩ to 32 kΩ (4 mA to 1 mA I_{xOUTFS}, respectively).

The AD9714/AD9715/AD9716/AD9717 provide the option of setting the output common mode to a value other than AVSS via the output common-mode pins (CMLI and CMLQ). This facilitates directly interfacing the output of the AD9714/AD9715/AD9716/AD9717 to components that require common-mode levels greater than 0 V.

SERIAL PERIPHERAL INTERFACE (SPI)

The serial port of the AD9714/AD9715/AD9716/AD9717 is a flexible, synchronous serial communications port that allows easy interfacing to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9714/AD9715/AD9716/AD9717. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial interface port of the AD9714/AD9715/AD9716/AD9717 is configured as a single I/O pin on the SDIO pin.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communications cycle on the AD9714/AD9715/AD9716/AD9717. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9714/AD9715/AD9716/AD9717, coinciding with the first eight SCLK rising edges. In Phase 2, the instruction byte provides the serial port controller of the AD9714/AD9715/AD9716/AD9717 with information regarding the data transfer cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9714/AD9715/AD9716/AD9717.

To ensure that SPI registers are set to default after power up, a Logic 1 with a minimum pulse width of 50 ns, followed by a Logic 0 must be applied on Pin 35 (RESET/PINMD). This also resets the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9714/AD9715/AD9716/AD9717 and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes, as determined by the instruction byte. Using one multi-byte transfer is the preferred method. Single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

INSTRUCTION BYTE

The instruction byte contains the information shown in Table 11.

Table 11.

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{\text{W}}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{\text{W}}$ (Bit 7 of the instruction byte) determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation. N1 and N0 (Bit 6 and Bit 5 of the instruction byte) determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 12.

Table 12. Byte Transfer Count

N1	N0	Description
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

A4, A3, A2, A1, and A0 (Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle. For multi-byte transfers, this address is the starting byte address. The following register addresses are generated internally by the AD9714/AD9715/AD9716/AD9717, based on the LSBFIRST bit (Register 0x00, Bit 6).

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9714/AD9715/AD9716/AD9717 and to run the internal state machines. The SCLK maximum frequency is 20 MHz. All data input to the AD9714/AD9715/AD9716/AD9717 is registered on the rising edge of SCLK. This is shown in Figure 85 and Figure 87 for write instructions where the SCLK rising edges are lined up in the middle of the data. All data is driven out of the AD9714/AD9715/AD9716/AD9717 on the falling edge of SCLK. This is shown in Figure 86 and Figure 88 for read cycles where the falling edges are lined up with the beginning of the data in the data transfer cycle.

$\overline{\text{CS}}$—Chip Select

An active low input starts and gates a communications cycle. It allows more than one device to be used on the same serial communications lines. The SDIO/FORMAT pin reaches a high impedance state when this input is high. Chip select should stay low during the entire communications cycle.

SDIO—Serial Data I/O

The SDIO pin is used as a bidirectional data line to transmit and receive data.

MSB/LSB TRANSFERS

The serial port of the AD9714/AD9715/AD9716/AD9717 can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the LSBFIRST bit (Register 0x00, Bit 6). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first), the instruction and data bytes must be written from the most significant bit to the least significant

SERIAL PERIPHERAL INTERFACE (SPI)

bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from a high address to a low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communications cycle.

When LSBFIRST = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address of the AD9714/AD9715/AD9716/AD9717 decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

SERIAL PORT OPERATION

The serial port configuration of the AD9714/AD9715/AD9716/AD9717 is controlled by Register 0x00. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register can occur during the middle of the communications cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communications cycle.

The same considerations apply to setting the software reset bit (Register 0x00, Bit 5). All registers are set to their default values except Register 0x00, which remains unchanged.

Use of single-byte transfers or initiating a software reset is recommended when changing serial port configurations to prevent unexpected device behavior.

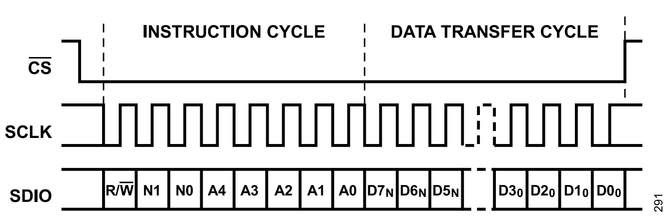


Figure 85. Serial Register Interface Timing, MSB First Write

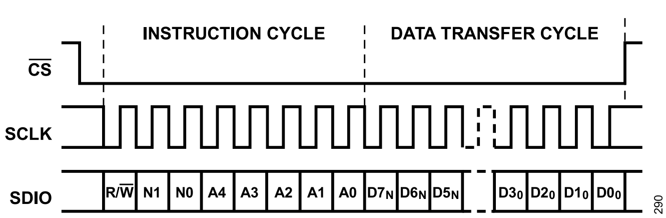


Figure 86. Serial Register Interface Timing, MSB First Read

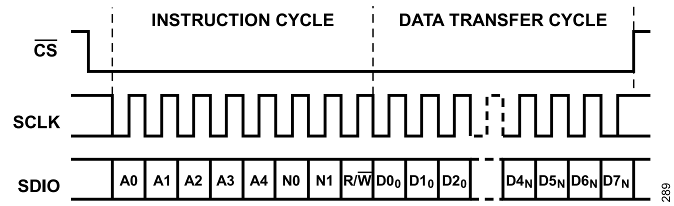


Figure 87. Serial Register Interface Timing, LSB First Write

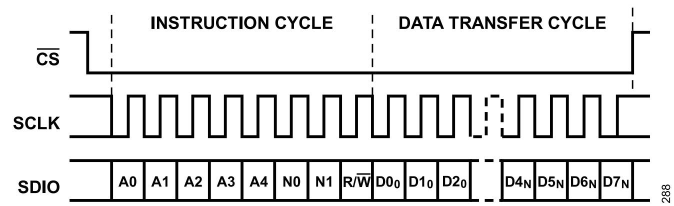


Figure 88. Serial Register Interface Timing, LSB First Read

PIN MODE

The AD9714/AD9715/AD9716/AD9717 can also be operated without ever writing to the serial port. With the RESET/PINMD pin tied high, the SCLK pin becomes CLKMD to provide for clock mode control (see the Retimer section), the SDIO pin becomes FORMAT and selects the input data format, and the $\overline{\text{CS}}$/PWRDN pin serves to power down the device. If the data format is changed, it is required to wait 1 µs after power up to ensure proper function.

Operation is otherwise exactly as defined by the default register values in Table 13; therefore, external resistors at FSADJI and FSADJQ are needed to set the DAC currents, and both DACs are active. This is also a convenient quick checkout mode.

DAC currents can be externally adjusted in pin mode by sourcing or sinking currents at the FSADJI/AUXI and FSADJQ/AUXQ pins as desired with the fixed resistors installed. An op amp output with appropriate series resistance is one of many possibilities. This has the same effect as changing the resistor value. Place at least 10 kΩ resistors in series right at the DAC to guard against accidental short circuits and noise modulation. The REFIO pin can be adjusted ±25% in a similar manner, if desired.

SPI REGISTER MAP

Table 13.

Name	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00	Reserved	LSBFIRST	Reset	LNGINS	Reserved			
Power-Down	0x01	0x40	LDOOFF	LDOSTAT	PWRDN	Q DACOFF	I DACOFF	QCLKOFF	ICLKOFF	EXTREF
Data Control	0x02	0x34	TWOS	Reserved	IFIRST	IRISING	SIMULBIT	DCI_EN	DCOSGL	DCODBL
I DAC Gain	0x03	0x00	Reserved		I DACGAIN[5:0]					
IRSET	0x04	0x00	IRSETEN	Reserved	IRSET[5:0]					
IRCML	0x05	0x00	IRCMLEN	Reserved	IRCML[5:0]					
Q DAC Gain	0x06	0x00	Reserved		Q DACGAIN[5:0]					
QRSET	0x07	0x00	QRSETEN	Reserved	QRSET[5:0]					
QRCML	0x08	0x00	QRCMLEN	Reserved	QRCML[5:0]					
AUXDAC I	0x09	0x00	IAUXDAC[7:0]							
AUX CTL I	0x0A	0x00	IAUXEN	IAUXRNG[1:0]		IAUXOFS[2:0]			IAUXDAC[9:8]	
AUXDAC Q	0x0B	0x00	QAUXDAC[7:0]							
AUX CTL Q	0x0C	0x00	QAUXEN	QAUXRNG[1:0]		QAUXOFS[2:0]			QAUXDAC[9:8]	
Reference Resistor	0x0D	0x00	Reserved		RREF[5:0]					
Cal Control	0x0E	0x00	PRELDQ	PRELDI	CALSELQ	CALSELI	CALCLK	DIVSEL[2:0]		
Cal Memory	0x0F	0x00	CALSTATQ	CALSTATI	Reserved		CALMEMQ[1:0]		CALMEMI[1:0]	
Memory Address	0x10	0x00	Reserved		MEMADDR[5:0]					
Memory Data	0x11	0x3F	Reserved		MEMDATA[5:0]					
Memory R/W	0x12	0x00	CALRSTQ	CALRSTI		CALEN	SMEMWR	SMEMRD	UNCALQ	UNCALI
CLKMODE	0x14	0x00	CLKMODEQ[1:0]			Searching	Reacquire	CLKMODEN	CLKMODEI[1:0]	
Version	0x1F	0x03	Version[7:0]							

SPI REGISTER DESCRIPTIONS

Reading these registers returns previously written values for all defined register bits, unless otherwise noted.

Table 14.

Register	Address	Bit	Name	Description
SPI Control	0x00	6	LSBFIRST	0 (default): MSB first, per SPI standard.
				1: LSB first, per SPI standard.
				Note that the user must always change the LSB/MSB order in single-byte instructions to avoid erratic behavior due to bit order errors.
		5	Reset	Execute software reset of SPI and controllers, reload default register values except Register 0x00.
				1: sets software reset; write 0 on the next (or any following) cycle to release reset.
		4	LNGINS	0 (default): the SPI instruction word uses a 5-bit address.
				1: the SPI instruction word uses a 13-bit address.
Power-Down	0x01	7	LDOOFF	0 (default): LDO voltage regulator on.
				1: turns core LDO voltage regulator off.
		6	LDOSTAT	0: indicates that the core LDO voltage regulator is off.
				1 (default): indicates that the core LDO voltage regulator is on.
		5	PWRDN	0 (default): all analog and digital circuitry and SPI logic are powered on.
				1: powers down all analog and digital circuitry except for SPI logic.
		4	Q DACOFF	0 (default): turns on Q DAC output current.
				1: turns off Q DAC output current.
		3	I DACOFF	0 (default): turns on I DAC output current.
				1: turns off I DAC output current.
		2	QCLKOFF	0 (default): turns on Q DAC clock.
				1: turns off Q DAC clock.
		1	ICLKOFF	0 (default): turns on I DAC clock.
				1: turns off I DAC clock.
		0	EXTREF	0 (default): turns on internal voltage reference.
				1: powers down internal voltage reference (external reference required).
Data Control	0x02	7	TWOS	0 (default): unsigned binary input data format.
				1: twos complement input data format.
		5	IFIRST	0: pairing of data—Q first of pair on data input pads.
				1 (default): pairing of data—I first of pair on data input pads.
		4	IRISING	0: Q data latched on DCLKIO rising edge.
				1 (default): I data latched on DCLKIO rising edge.
		3	SIMULBIT	0 (default): allows simultaneous input and output enable on DCLKIO.
				1: disallows simultaneous input and output enable on DCLKIO.
		2	DCI_EN	Controls the use of the DCLKIO pad for data clock input.
				0: data clock input disabled.
				1 (default): data clock input enabled.
		1	DCOSGL	Controls the use of the DCLKIO pad for data clock output.
				0 (default): data clock output disabled.
				1: data clock output enabled; regular strength driver.
		0	DCODBL	Controls the use of the DCLKIO pad for data clock output.
				0 (default): DCODBL data clock output disabled.
				1: DCODBL data clock output enabled; paralleled with DCOSGL for 2× drive current.
I DAC Gain	0x03	5:0	I DACGAIN[5:0]	DAC I fine gain adjustment; alters the full-scale current as shown in Figure 101. Default IDACGAIN = 0x00.

SPI REGISTER DESCRIPTIONS

Table 14. (Continued)

Register	Address	Bit	Name	Description
IRSET	0x04	7	IRSETEN	0 (default): disables on-chip IR_{SET} resistor for I channel. IR_{SET} is set by an external resistor connected to the FADJI/AUXI pin. Nominal value for this external resistor is 16 kΩ.
				1: enables the on-chip IR_{SET} and allows value to be changed for I channel.
		5:0	IRSET[5:0]	Changes the value of the on-chip IR_{SET} resistor for I channel; this scales the full-scale current of the DAC in ~0.25 dB steps twos complement (nonlinear); see Figure 100.
				000000 (default): IR_{SET} = 16 kΩ.
				011111: IR_{SET} = 32 kΩ.
				100000: IR_{SET} = 8 kΩ.
				111111: IR_{SET} = 16 kΩ.
IRCML	0x05	7	IRCMLEN	0 (default):disables on-chip IR_{CML} resistor value for the I channel. IR_{CML} is set by an external resistor connected to the CMLI pin. Recommended value for this external resistor is 0 Ω.
				1: enables on-chip IR_{CML} and allows adjustment for I channel.
		5:0	IRCML[5:0]	Changes the value of the on-chip IR_{CML} resistor for I channel; this adjusts the common-mode level of the DAC output stage.
				000000 (default): IR_{CML} = 250 Ω.
				100000: IR_{CML}= 625 Ω.
				111111: IR_{CML} = 1 kΩ.
Q DAC Gain	0x06	5:0	Q DACGAIN[5:0]	DAC Q fine gain adjustment; alters the full-scale current as shown in Figure 101. Default QDACGAIN = 0x00.
QRSET	0x07	7	QRSETEN	0 (default):disables on-chip QR_{SET} resistor value for Q channel. QR_{SET} is set by an external resistor connected to the FADJQ/AUXQ pin. Recommended value for this external resistor is 16 kΩ.
				1: enables on-chip QR_{SET} and allows adjustment for Q channel.
		5:0	QRSET[5:0]	Changes the value of the on-chip QR_{SET} resistor for Q channel; this scales the full-scale current of the DAC in ~0.25 dB steps twos complement (nonlinear); see Figure 100.
				000000 (default): QR_{SET} = 16 kΩ.
				011111: QR_{SET} = 32 kΩ.
				100000: QR_{SET} = 8 kΩ.
				111111: QR_{SET} = 16 kΩ.
QRCML	0x08	7	QRCMLEN	0 (default): disables on-chip QR_{CML} resistor value for the Q channel. QR_{CML} is set by an external resistor connected to CMLQ pin. Recommended value for this external resistor is 0 Ω.
				1: enables on-chip QR_{CML} adjustment for Q channel.
		5:0	QRCML[5:0]	Changes the value of the on-chip QR_{CML} resistor for Q channel; this adjusts the common-mode level of the DAC output stage.
				000000 (default): QR_{CML} = 250 Ω.
				100000: QR_{CML} = 625 Ω.
				111111: QR_{CML} = 1 kΩ.
AUXDAC I	0x09	7:0	IAUXDAC[7:0]	8 LSBs for 10-bit AUXDAC I output voltage adjustment word. Set MSBs in Register 0x0A.
				0x3FF: sets AUXDAC I output to full scale.
				0x200: sets AUXDAC I output to midscale.
				0x000 (default): sets AUXDAC I output to bottom of scale.
AUX CTL I	0x0A	7	IAUXEN	0 (default): AUXDAC I output disabled.
				1: enables AUXDAC I output.
		6:5	IAUXRNG[1:0]	00 (default): sets AUXDAC I output voltage range to 2 V.
				01: sets AUXDAC I output voltage range to 1.5 V.
				10: sets AUXDAC I output voltage range to 1.0 V.

SPI REGISTER DESCRIPTIONS

Table 14. (Continued)

Register	Address	Bit	Name	Description
				11: sets AUXDAC I output voltage range to 0.5 V.
		4:2	IAUXOFS[2:0]	000 (default): sets AUXDAC I top of range to 1.0 V.
				001: sets AUXDAC I top of range to 1.5 V.
				010: sets AUXDAC I top of range to 2.0 V.
				011: sets AUXDAC I top of range to 2.5 V.
				100: sets AUXDAC I top of range to 2.9 V.
		1:0	IAUXDAC[9:8]	2 MSBs for 10-bit AUXDAC I output voltage adjustment word (default = 00). Set LSBs in Register 0x09.
AUXDAC Q	0x0B	7:0	QAUXDAC[7:0]	8 LSBs for 10-bit AUXDAC Q output voltage adjustment word. Set MSBs in Register 0x0C.
				0x3FF: sets AUXDAC Q output to full scale.
				0x200: sets AUXDAC Q output to midscale.
				0x000 (default): sets AUXDAC Q output to bottom of scale.
AUX CTL Q	0x0C	7	QAUXEN	0 (default): AUXDAC Q output disabled.
				1: enables AUXDAC Q output.
		6:5	QAUXRNG[1:0]	00 (default): sets AUXDAC Q output voltage range to 2 V.
				01: sets AUXDAC Q output voltage range to 1.5 V.
				10: sets AUXDAC Q output voltage range to 1.0 V.
				11: sets AUXDAC Q output voltage range to 0.5 V.
		4:2	QAUXOFS[2:0]	000 (default): sets AUXDAC Q top of range to 1.0 V.
				001: sets AUXDAC Q top of range to 1.5 V.
				010: sets AUXDAC Q top of range to 2.0 V.
				011: sets AUXDAC Q top of range to 2.5 V.
				100: sets AUXDAC Q top of range to 2.9 V.
		1:0	QAUXDAC[9:8]	2 MSBs for 10-bit AUXDAC Q output voltage adjustment word (default = 00). Set LSBs in Register 0x0B.
Reference Resistor	0x0D	5:0	RREF[5:0]	Permits an adjustment of the on-chip reference voltage and output at REFIO (see Figure 99) twos complement.
				000000 (default): sets the value of R_{REF} to 10 kΩ, V_{REF} = 1.0 V.
				011111: sets the value of R_{REF} to 12 kΩ, V_{REF} = 1.2 V.
				100000: sets the value of R_{REF} to 8 kΩ, V_{REF} = 0.8 V.
				111111: sets the value of R_{REF} to 10 kΩ, V_{REF} = 1.0 V.
Cal Control	0x0E	7	PRELDQ	0 (default): preload Q DAC calibration reference set to 32.
				1: preload Q DAC calibration reference set by user (Cal Address 1).
		6	PRELDI	0 (default): preload I DAC calibration reference set to 32.
				1: preload I DAC calibration reference set by user (Cal Address 1).
		5	CALSELQ	0 (default): Q DAC self-calibration done.
				1: select Q DAC self-calibration.
		4	CALSELI	0 (default): I DAC self-calibration done.
				1: select I DAC self-calibration.
		3	CALCLK	0 (default): calibration clock disabled.
				1: calibration clock enabled.
		2:0	DIVSEL[2:0]	Calibration clock divide ratio from DAC clock rate.
				000 (default): divide by 256.
				001: divide by 128.
				…

SPI REGISTER DESCRIPTIONS

Table 14. (Continued)

Register	Address	Bit	Name	Description
				110: divide by 4. 111: divide by 2.
Cal Memory	0x0F	7	CALSTATQ	0 (default): Q DAC calibration in progress. 1: calibration of Q DAC complete.
		6	CALSTATI	0 (default): I DAC calibration in progress. 1: calibration of I DAC complete.
		3:2	CALMEMQ[1:0]	Status of Q DAC calibration memory. 00 (default): uncalibrated. 01: self-calibrated. 10: user calibrated.
		1:0	CALMEMI[1:0]	Status of I DAC calibration memory. 00 (default): uncalibrated. 01: self-calibrated. 10: user calibrated.
Memory Address	0x10	5:0	MEMADDR[5:0]	Address of static memory to be accessed.
Memory Data	0x11	5:0	MEMDATA[5:0]	Data for static memory access.
Memory R/W	0x12	7	CALRSTQ	0 (default): no action. 1: clear CALSTATQ.
		6	CALRSTI	0 (default): no action. 1: clear CALSTATI.
		4	CALEN	0 (default): no action. 1: initiate device self-calibration.
		3	SMEMWR	0 (default): no action. 1: write to static memory (calibration coefficients).
		2	SMEMRD	0 (default): no action. 1: read from static memory (calibration coefficients).
		1	UNCALQ	0 (default): no action. 1: reset Q DAC calibration coefficients to default (uncalibrated).
		0	UNCALI	0 (default): no action. 1: reset I DAC calibration coefficients to default (uncalibrated).
CLKMODE	0x14	7:6	CLKMODEQ[1:0]	Depending on the CLKMODEN bit setting, these two bits reflect the phase relationship between DCLKIO and CLKIN, as described in Table 16. If CLKMODEN = 0, read only; reports the clock phase chosen by the retimer. If CLKMODEN = 1, read/write; value in this register sets Q clock phases; force if needed to better synchronize the DACs (see the Retimer section).
		4	Searching	Data path retimer status bit. 0 (default): clock relationship established. 1: indicates that the internal data path retimer is searching for clock relationship (device output is not usable while this bit is high).
		3	Reacquire	Edge triggered, 0 to 1 causes the retimer to reacquire the clock relationship.
		2	CLKMODEN	0 (default): CLKMODEI/CLKMODEQ values computed by the two retimers and read back in CLKMO-DEI[1:0] and CLKMODEQ[1:0]. 1: CLKMODE values set in CLKMODEI[1:0] override both I and Q retimers.
		1:0	CLKMODEI[1:0]	Depending on CLKMODEN bit setting, these two bits reflect the phase relationship between DCLKIO and CLKIN as described in Table 16.

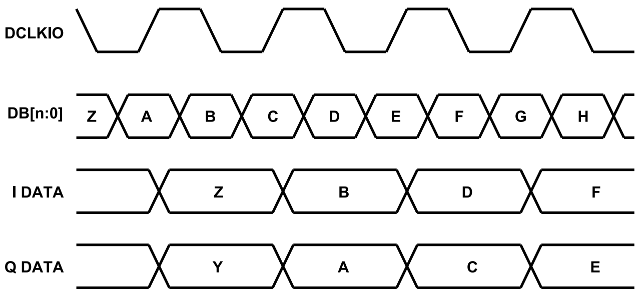
SPI REGISTER DESCRIPTIONS

Table 14. (Continued)

Register	Address	Bit	Name	Description
				If CLKMODEN = 0, read only; reports the clock phase chosen by the retimer. If CLKMODEN = 1, read/write; value in this register sets I clock phases; force if needed to better synchronize the DACs (see the Retimer section).
Version	0x1F	7:0	Version[7:0]	Hardware version of the device. This register is set to 0x03 for the latest version of the device.

DIGITAL INTERFACE OPERATION

Digital data for the I and Q DACs is supplied over a single parallel bus (DB[n:0], where n is 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717) accompanied by a qualifying clock (DCLKIO). The I and Q data are provided to the chip in an interleaved double data rate (DDR) format. The maximum guaranteed data rate is 250 MSPS with a 125 MHz clock. The order of data pairing and the sampling edge selection is user programmable using the IFIRST and IRISING data control bits, resulting in four possible timing diagrams. These are shown in Figure 89, Figure 90, Figure 91, and Figure 92.



NOTES:
1. DB[n:0], WHERE n IS 7 FOR THE AD9714, 9 FOR THE AD9715, 11 FOR THE AD9716, AND 13 FOR THE AD9717.

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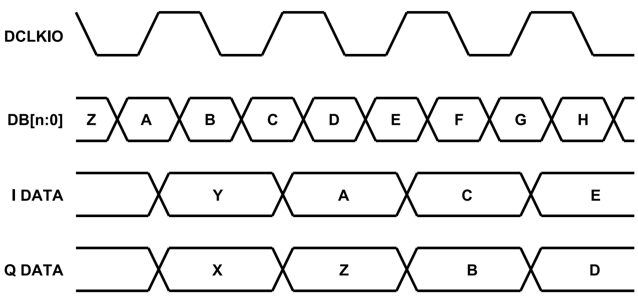
Figure 89. Timing Diagram with IFIRST = 0, IRISING = 0



NOTES:
1. DB[n:0], WHERE n IS 7 FOR THE AD9714, 9 FOR THE AD9715, 11 FOR THE AD9716, AND 13 FOR THE AD9717.

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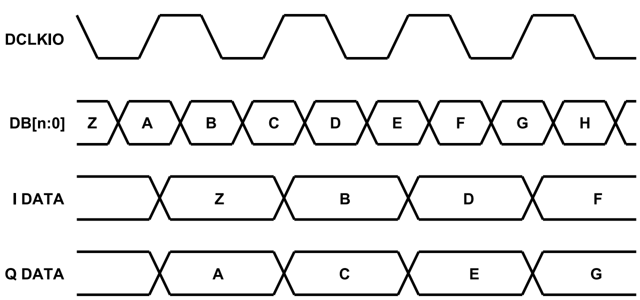
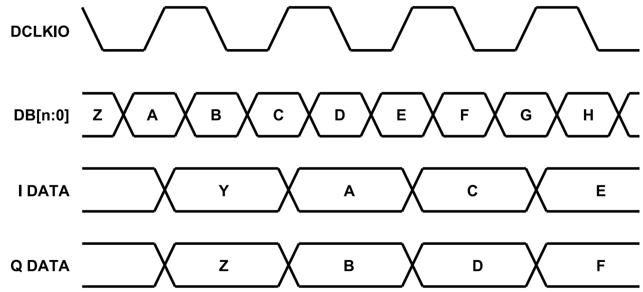
Figure 90. Timing Diagram with IFIRST = 0, IRISING = 1



NOTES:
1. DB[n:0], WHERE n IS 7 FOR THE AD9714, 9 FOR THE AD9715, 11 FOR THE AD9716, AND 13 FOR THE AD9717.

049

Figure 91. Timing Diagram with IFIRST = 1, IRISING = 0

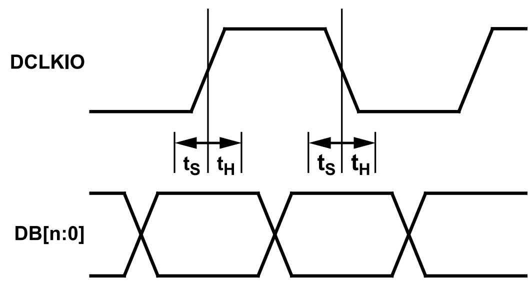


NOTES:
1. DB[n:0], WHERE n IS 7 FOR THE AD9714, 9 FOR THE AD9715, 11 FOR THE AD9716, AND 13 FOR THE AD9717.

050

Figure 92. Timing Diagram with IFIRST = 1, IRISING = 1

Ideally, the rising and falling edges of the clock fall in the center of the keep-in-window formed by the setup and hold times, t_S and t_H. Refer to Table 2 for setup and hold times. A detailed timing diagram is shown in Figure 93.



NOTES:
1. DB[n:0], WHERE n IS 7 FOR THE AD9714, 9 FOR THE AD9715, 11 FOR THE AD9716, AND 13 FOR THE AD9717.

051

Figure 93. Setup and Hold Times for All Input Modes

In addition to the different timing modes listed in Table 2, the input data can also be presented to the device in either unsigned binary or twos complement format. The format type is chosen via the TWOS data control bit.

DIGITAL INTERFACE OPERATION

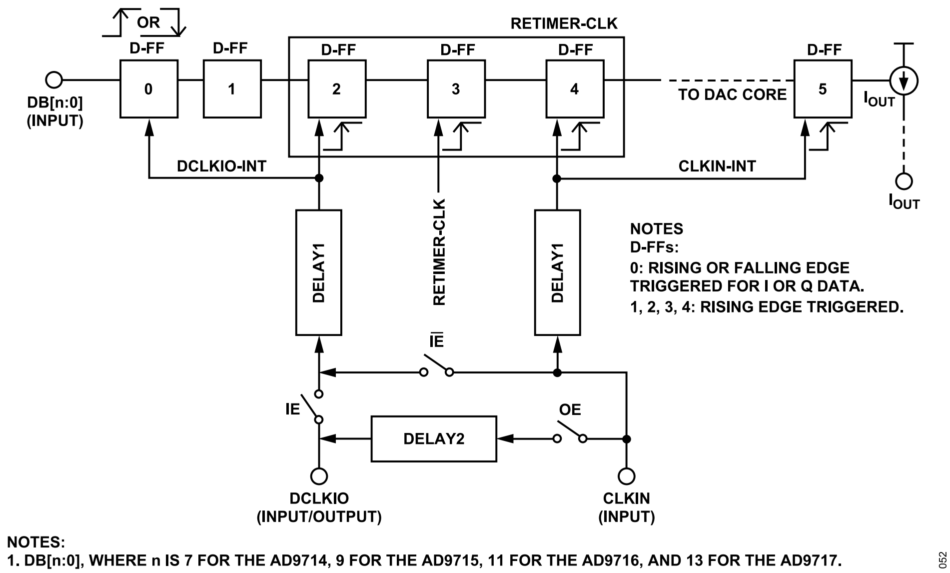


Figure 94. Simplified Diagram of AD9714/AD9715/AD9716/AD9717 Timing

DIGITAL DATA LATCHING AND RETIMER BLOCK

The AD9714/AD9715/AD9716/AD9717 have two clock inputs, DCLKIO and CLKIN. The CLKIN is the analog clock whose jitter affects DAC performance, and the DCLKIO is a digital clock from an FPGA that needs to have a fixed relationship with the input data to ensure that the data is picked up correctly by the flip-flops on the pads.

Figure 94 is a simplified diagram of the entire data capture system in the AD9714/AD9715/AD9716/AD9717. The double data rate input data (DB[n:0], where n is 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717) is latched at the pads/pins either on the rising edge or the falling edge of the DCLKIO-INT clock, as determined by IRISING, Bit 4 of SPI Address 0x02. Bit 5 of SPI Address 0x02, IFIRST, determines which channel data is latched first (that is, I or Q). The captured data is then retimed to the internal clock (CLKIN-INT) in the retimer block before being sent to the final analog DAC core (D-FF 4), which controls the current steering output switches. All delay blocks depicted in Figure 94 are noninverting, and any wires without an explicit delay block can be assumed to have no delay.

Only one channel is shown in Figure 94 with the data pads (DB[n:0], where n is 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717) serving as double data rate pads for both channels.

The default PINMD and SPI settings are IE = high (closed) and OE = low (open). These settings are enabled when RESET/ PINMD (Pin 35) is held high. In this mode, the user has to supply both DCLKIO and CLKIN. In PINMD, it is also recommended that the DCLKIO and the CLKIN be in phase for proper functioning of the DAC, which can easily be ensured by tying the pins together on the PCB. If the user can access the SPI, setting Bit 2 of SPI Address 0x02, DCI_EN, to logic low causes the CLKIN to be used as the DCLKIO also.

Setting Bit 1 or Bit 0 of SPI Address 0x02, DCOSGL or DCODBL, respectively, to logic high allows the user to obtain a DCLKIO output from the CLKIN input for use in the user's PCB system.

It is strongly recommended that DCI_EN = DCOSGL = high or DCI_EN = DCODBL = high not be used even though the device may appear to function correctly. Similarly, do not set DCOSGL and DCODBL to logic high simultaneously.

Retimer

The AD9714/AD9715/AD9716/AD9717 have an internal data retimer circuit that compares the CLKIN-INT and DCLKIO-INT clocks and, depending on their phase relationship, selects a retimer clock (RETIMER-CLK) to safely transfer data from the DCLKIO used at the chip's input interface to the CLKIN used to clock the analog DAC cores (D-FF 4).

The retimer selects one of the three phases shown in Figure 95. The retimer is controlled by the CLKMODE SPI bits, as shown in Table 15.

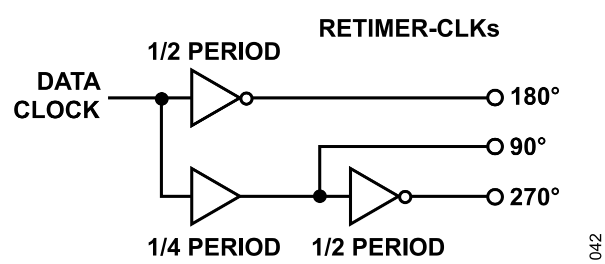


Figure 95. RETIMER-CLK Phases

DIGITAL INTERFACE OPERATION

Note that, in most cases, more than one retimer phase works and, in such cases, the retimer arbitrarily picks one phase that works. The retimer cannot pick the best or safest phase. If the user has a working knowledge of the exact phase relationship between DCLKIO and CLKIN (and thus DCLKIO-INT and CLKIN-INT because the delay is approximately the same for both clocks and equal to DELAY1), then the retimer can be forced to this phase with CLKMODEN = 1, as described in Table 15 and the following paragraphs.

Table 15. Timer Register List

Bit Name	Description
CLKMODEQ[1:0]	Q data path retimer clock selected output. Valid after the searching bit goes low.
Searching	High indicates that the internal data path retimer is searching for the clock relationship (DAC is not usable until it is low again).
Reacquire	Changing this bit from 0 to 1 causes the data path retimer circuit to reacquire the clock relationship.
CLKMODEN	0: uses CLKMODEI/CLKMODEQ values (as computed by the two internal retimers) for I and Q clocking.
	1: uses the CLKMODE value set in CLKMODEI[1:0] to override the bits for both I and Q retimers (that is, force the retimer).
CLKMODEI[1:0]	I data path retimer clock selected output. Valid after searching goes low.
	If CLKMODEN = 1, a value written to this register overrides both the I and Q automatic retimer values.

Table 16. CLKMODEI/CLKMODEQ Details

CLKMODEI[1:0]/CLKMODEQ[1:0]	DCLKIO-to-CLKIN Phase Relationship	RETIMER-CLK Selected
00	0° to 90°	Phase 2
01	90° to 180°	Phase 3
10	180° to 270°	Phase 3
11	270° to 360°	Phase 1

DIGITAL INTERFACE OPERATION

When RESET is pulsed high and then returns low (the part is in SPI mode), the retimer runs and automatically selects a suitable clock phase for the RETIMER-CLK within 128 clock cycles. The SPI searching bit, Bit 4 of SPI Address 0x14, returns to low, indicating that the retimer has locked and the part is ready for use. The reacquire bit, Bit 3 of SPI Address 0x14, can be used to reinitiate phase detection in the I and Q retimers at any time. CLKMODEQ[1:0] and CLKMODEI[1:0] of SPI Address 0x14 provide readback for the values picked by the internal phase detectors in the retimer (see Table 16).

To force the two retimers (I and Q) to pick a particular phase for the retimer clock (they must both be forced to the same value), CLKMODEN, Bit 2 of SPI Address 0x14, should be set high and the required phase value is written into CLKMODEI[1:0] and CLKMODEQ[1:0]. For example, if the DCLKIO and the CLKIN are in phase to the first order, the user can safely force the retimers to pick Phase 2 for the RETIMER-CLK. This forcing function may be useful for synchronizing multiple devices.

In pin mode, it is expected that the user tie CLKIN and DCLKIO together. The device has a small amount of programmable functionality using the unused SPI pins (SCLK, SDIO, and $\overline{\text{CS}}$). If the two chip clocks are tied together, the SCLK pin can be tied to ground, and the chip uses a clock for the retimer that is 180° out of phase with the two input clocks (that is, Phase 2, which is the safest and best option). The chip has an additional option in pin mode when the redefined SCLK pin is high. Use this mode if using pin mode, but CLKIN and DCLKIO are not tied together (that is, not in phase). Holding SCLK high causes the internal clock detector to use the phase detector output to determine which clock to use in the retimer (that is, select a suitable RETIMER-CLK phase). The action of taking SCLK high causes the internal phase detector to reexamine the two clocks and determine the relative phase. Whenever the user wants to reevaluate the relative phase of the two clocks, the SCLK pin can be taken low and then high again.

ESTIMATING THE OVERALL DAC PIPELINE DELAY

DAC pipeline latency is affected by the phase of the RETIMER-CLK that is selected. If latency is critical to the system and must be constant, the retimer should be forced to a particular phase and not be allowed to automatically select a phase each time.

Consider the case in which DCLKIO = CLKIN (that is, in phase), and the RETIMER-CLK is forced to Phase 2. Assume that IRISING is 1 (that is, I data is latched on the rising edge and Q data is latched on the falling edge). Then the latency to the output for the I channel is four clock cycles total; one clock cycle from the input interface (D-FF 1, not D-FF0, as it latches data on either edge and does not cause any delay); two clock cycles from the retimer (D-FF 2 and D-FF 4, but not D-FF 3, because it is latched on the half clock cycle or 180°); and one clock cycle going through the analog core (D-FF 5). The latency to the output for the Q channel from the time the falling edge latches it at the pads in D-FF 0 is 3.5 clock cycles (no delay due to D-FF0, 1 clock cycle due to D-FF 1, ½ clock cycle to D-FF 2, 1 clock cycle to D-FF 4, and 1 clock cycle to D-FF 5). This latency for the AD9714/AD9715/AD9716/AD9717 is case specific and needs to be calculated based on the RETIMER-CLK phase that is automatically selected or manually forced.

REFERENCE OPERATION

The AD9714/AD9715/AD9716/AD9717 contain an internal 1.0 V band gap reference. The internal reference can be disabled by setting Bit 0 (EXTREF) of the power-down register (Address 0x01) through the SPI interface. To use the internal reference, decouple the REFIO pin to AVSS with a 0.1 µF capacitor, enable the internal reference, and clear Bit 0 of the power-down register (Address 0x01) through the SPI interface. Note that this is the default configuration. The internal reference voltage is present at REFIO and ramps up for around 2 ms when the proper power-up conditions in the Power Supply section are followed. If the voltage at REFIO is to be used anywhere else in the circuit, an external buffer amplifier with an input bias current of less than 100 nA must be used to avoid loading the reference. An example of the use of the internal reference is shown in Figure 96.

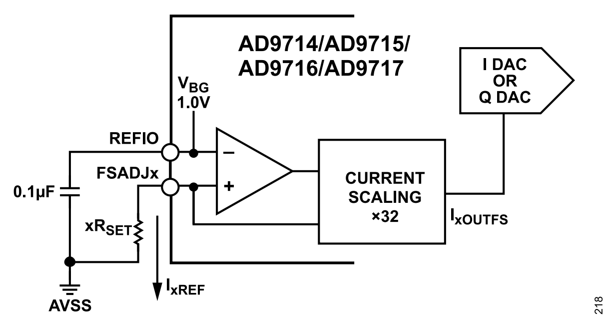


Figure 96. Internal Reference Configuration

REFIO serves as either an input or an output, depending on whether the internal or an external reference is used. Table 17 summarizes the reference operation.

Table 17. Reference Operation

Reference Mode	REFIO Pin	Register Setting
Internal	Connect 0.1 µF capacitor	Register 0x01, Bit 0 = 0 (default)
External	Apply external capacitor	Register 0x01, Bit 0 = 1 (for power saving)

An external reference is recommended in applications requiring tighter gain tolerances or lower temperature drift. Also, a variable external voltage reference can be used to implement a method for gain control of the DAC output.

DIGITAL INTERFACE OPERATION

Recommendations When Using an External Reference

Apply the external reference to the REFIO pin. The internal reference can be directly overdriven by the external reference, or the internal reference can be powered down to save power consumption.

The external 0.1 μF compensation capacitor on REFIO is not required unless specified by the external voltage reference manufacturer. The input impedance of REFIO is 10 kΩ when the internal reference is powered up and 1 MΩ when it is powered down.

The ADR130 precision voltage reference or equivalent is recommended with the analog supply connected to AVDD, as shown in Figure 97.

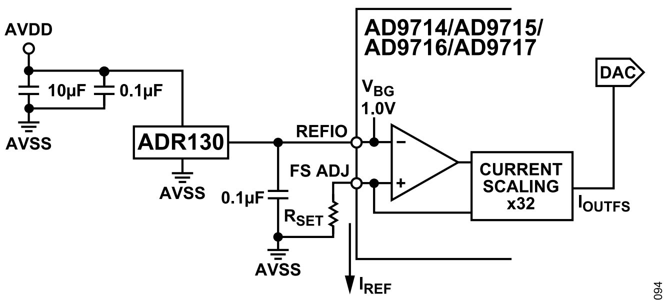


Figure 97. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9714/AD9715/AD9716/AD9717 contain a control amplifier that regulates the full-scale output current, I_{xOUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 96. The output current, I_{xREF}, is determined by the ratio of the V_{REFIO} and an external resistor, xR_{SET}, as stated in Equation 4 (see the DAC Transfer Function section). I_{xREF}, is mirrored to the segmented current sources with the proper scale factor to set I_{xOUTFS}, as stated in Equation 3.

The control amplifier allows a 2.5:1 adjustment span of I_{xOUTFS} from 1 mA to 4 mA by setting I_{xREF} between 125 μA and 31.25 μA (set xR_{SET} between 8 kΩ and 32 kΩ). The wide adjustment span of I_{xOUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9714/AD9715/AD9716/AD9717, which is proportional to I_{xOUTFS} (see the DAC Transfer Function section). The second benefit relates to the ability to adjust the output over a 8 dB range with 0.25 dB steps, which is useful for controlling the transmitted power. The small signal bandwidth of the reference control amplifier is approximately 500 kHz. This allows the device to be used for low frequency, small signal multiplying applications.

When an external resistor greater than 16 kΩ is used on the FSADJx pins, care must be taken to maintain the high frequency equivalent circuit to an impedance lower than 16 kΩ by splitting the resistor into two resistors in series with a 10 nF capacitor in parallel with the resistor to AVSS (see Figure 98).

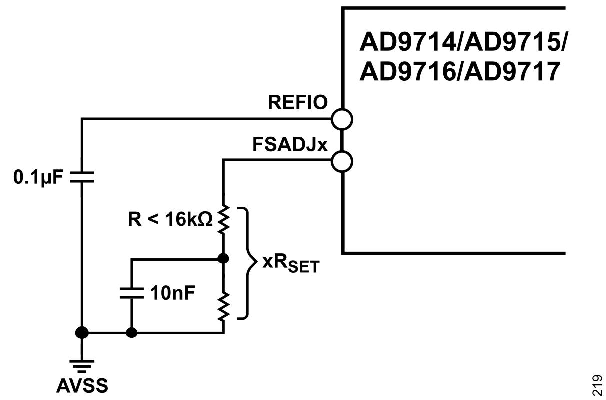


Figure 98. xR_{SET} Configuration for Values > 16 kΩ

DAC TRANSFER FUNCTION

The AD9714/AD9715/AD9716/AD9717 provide two differential current outputs, IOUTP/IOUTN and QOUTP/QOUTN. IOUTP and QOUTP provide a near full-scale current output, I_{xOUTFS}, when all bits are high (that is, DAC CODE = $2^N - 1$, where N = 8, 10, 12, or 14 for the AD9714, AD9715, AD9716, and AD9717, respectively), while IOUTN and QOUTN, the complementary outputs, provide no current. The current outputs appearing at the positive DAC outputs, IOUTP and QOUTP, and at the negative DAC outputs, IOUTN and QOUTN, are a function of both the input code and I_{xOUTFS} and can be expressed as follows:

$$IOUTP = (IDAC\ CODE/2^N) \times I_{IOUTFS} \quad (1)$$

$$QOUTP = (QDAC\ CODE/2^N) \times I_{QOUTFS}$$

$$IOUTN = ((2^N - 1) - IDAC\ CODE)/2^N \times I_{IOUTFS} \quad (2)$$

$$QOUTN = ((2^N - 1) - QDAC\ CODE)/2^N \times I_{QOUTFS}$$

where:
IDAC CODE and *QDAC CODE* = 0 to $2^N - 1$ (that is, decimal representation).
I_{IOUTFS} and I_{QOUTFS} are functions of the reference currents, I_{IREF} and I_{QREF}, respectively, which are nominally set by a reference voltage, V_{REFIO}, and external resistors, IR_{SET} and QR_{SET}, respectively. I_{IOUTFS} and I_{QOUTFS} can be expressed as follows:

$$I_{IOUTFS} = 32 \times I_{IREF} \quad (3)$$

$$I_{QOUTFS} = 32 \times I_{QREF}$$

where:

$$I_{IREF} = V_{REFIO}/IR_{SET} \quad (4)$$

$$I_{QREF} = V_{REFIO}/QR_{SET}$$

or

$$I_{IOUTFS} = 32 \times V_{REFIO}/IR_{SET} \quad (5)$$

$$I_{QOUTFS} = 32 \times V_{REFIO}/QR_{SET}$$

DIGITAL INTERFACE OPERATION

A differential pair (IOUTP/IOUTN or QOUTP/QOUTN) typically drives a resistive load directly or via a transformer. If dc coupling is required, the differential pair (IOUTP/IOUTN or QOUTP/QOUTN) must be connected to matching resistive loads, xR_{LOAD}, that are tied to analog common, AVSS. The single-ended voltage output appearing at the positive and negative nodes is

$$V_{IOUTP} = IOUTP \times IR_{LOAD} \quad (6)$$

$$V_{QOUTP} = QOUTP \times QR_{LOAD}$$

$$V_{IOUTN} = IOUTN \times IR_{LOAD} \quad (7)$$

$$V_{QOUTN} = QOUTN \times QR_{LOAD}$$

To achieve 1 V p-p at the nominal 4 mA output current, IR_{LOAD} = QR_{LOAD} must be set to 250 Ω.

Substituting the values of IOUTP, IOUTN, and I_{xREF}, V_{IDIFF} can be expressed as

$$V_{IDIFF} = \{(2 \times IDAC\ CODE - (2^N - 1))/2^N\} \times (32 \times V_{REFIO}/IR_{SET}) \times IR_{LOAD} \quad (8)$$

Equation 8 highlights some of the advantages of operating the AD9714/AD9715/AD9716/AD9717 differentially. First, the differential operation helps cancel common-mode error sources associated with IOUTP and IOUTN, such as noise, distortion, and dc offsets. Second, the differential code-dependent current and subsequent voltage, V_{IDIFF}, is twice the value of the single-ended voltage output (that is, V_{IOUTP} or V_{IOUTN}), thus providing twice the signal power to the load. Note that the gain drift temperature performance for a single-ended output (V_{IOUTP} and V_{IOUTN}) or differential output (V_{IDIFF}) of the AD9714/AD9715/AD9716/AD9717 can be enhanced by selecting temperature-tracking resistors for xR_{LOAD} and xR_{SET} because of their ratiometric relationship, as shown in Equation 8.

ANALOG OUTPUT

The complementary current outputs in each DAC, IOUTP/ IOUTN and QOUTP/QOUTN, can be configured for single-ended or differential operation. IOUTP/IOUTN and QOUTP/ QOUTN can be converted into complementary single-ended voltage outputs, V_{IOUTP} and V_{IOUTN}, as well as V_{QOUTP} and V_{QOUTN} via a load resistor, xR_{LOAD}, as described in the DAC Transfer Function section by Equation 6 through Equation 8. The differential voltages, V_{IDIFF} and V_{QDIFF}, existing between V_{IOUTP} and V_{IOUTN}, and V_{QOUTP} and V_{QOUTN}, can also be converted to a single-ended voltage via a transformer or a differential amplifier configuration. The ac performance of the AD9714/AD9715/AD9716/AD9717 is optimum and is specified using a differential transformer-coupled output in which the voltage swing at IOUTP and IOUTN is limited to ±0.5 V. The distortion and noise performance of the AD9714/AD9715/AD9716/ AD9717 can be enhanced when it is configured for differential operation. The common-mode error sources of both IOUTP/IOUTN and QOUTP/QOUTN can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first-order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise. Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (assuming no source termination). Because the output currents of IOUTP/IOUTN and QOUTP/QOUTN are complementary, they become additive when processed differentially.

SELF-CALIBRATION

The AD9714/AD9715/AD9716/AD9717 have a self-calibration feature that improves the DNL of the device. Performing a self-calibration on the device improves device performance in low frequency applications. The device performance in applications where the analog output frequencies are above 5 MHz are generally influenced more by dynamic device behavior than by DNL and, in these cases, self-calibration is unlikely to provide much benefit. The calibration clock frequency is equal to the DAC clock divided by the division factor chosen by the DIVSEL value. Each calibration clock cycle is between 32 and 2048 DAC input clock cycles, depending on the value of DIVSEL[2:0] (Register 0x0E, Bits[2:0]). The frequency of the calibration clock should be between 0.5 MHz and 4 MHz for reliable calibrations. Best results are obtained by setting DIVSEL[2:0] (Register 0x0E, Bits[2:0]) to produce a calibration clock frequency between these values. Separate self-calibration hardware is included for each DAC. The DACs can be self-calibrated individually or simultaneously.

To perform a device self-calibration, the following procedure can be used:

1. Write 0x00 to Register 0x12. This ensures that the UNCALI and UNCALQ bits are reset.
2. Set up a calibration clock between 0.5 MHz and 4 MHz using DIVSEL[2:0], and then enable the calibration clock by setting the CALCLK bit (Register 0x0E, Bit 3).
3. Select the DAC(s) to self-calibrate by setting either Bit 4 (CALSELI) for the I DAC and/or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E. Note that each DAC contains independent calibration hardware so that they can be calibrated simultaneously.
4. Start self-calibration by setting the CALEN bit (Register 0x12, Bit 4). Wait approximately 300 calibration clock cycles.
5. Check if the self-calibration has completed by reading the CALSTATI bit (Bit 6) and CALSTATQ bit (Bit 7) in Register 0x0F. Logic 1 indicates that the calibration has completed.
6. When the self-calibration has completed, write 0x00 to Register 0x12.
7. Disable the calibration clock by clearing the CALCLK bit (Register 0x0E, Bit 3).

The AD9714/AD9715/AD9716/AD9717 allow reading and writing of the calibration coefficients. There are 32 coefficients in total. The read/write feature of the coefficients can be useful for improving the results of the self-calibration routine by averaging the results

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of several self-calibration cycles and loading the averaged results back into the device.

To read the calibration coefficients, use the following steps:

1. Select which DAC core to read by setting either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E. Write the address of the first coefficient (0x01) to Register 0x10.
2. Set the SMEMRD bit (Register 0x12, Bit 2) by writing 0x04 to Register 0x12.
3. Read the 6-bit value of the first coefficient by reading the contents of Register 0x11.
4. Clear the SMEMRD bit by writing 0x00 to Register 0x12.
5. Repeat Step 2 through Step 4 for each of the remaining 31 coefficients by incrementing the address by 1 for each read.
6. Deselect the DAC core by clearing either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.

To write the calibration coefficients to the device, use the following steps:

1. Select which DAC core to write to by setting either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.
2. Set the SMEMWR bit (Register 0x12, Bit 3) by writing 0x08 to Register 0x12.
3. Write the address of the first coefficient (0x01) to Register 0x10.
4. Write the value of the first coefficient to Register 0x11.
5. Repeat Step 2 through Step 4 for each of the remaining 31 coefficients by incrementing the address by one for each write.
6. Clear the SMEMWR bit by writing 0x00 to Register 0x12.
7. Deselect the DAC core by clearing either Bit 4 (CALSELI) for the I DAC or Bit 5 (CALSELQ) for the Q DAC in Register 0x0E.

COARSE GAIN ADJUSTMENT

Option 1

A coarse full-scale output current adjustment can be achieved using the lower six bits in Register 0x0D. This adds or subtracts up to 20% from the band gap voltage on Pin 34 (REFIO), and the voltage on the FSADJx resistors tracks this change. As a result, the DAC full-scale current varies by the same amount. A secondary effect to changing the REFIO voltage is that the full-scale voltage in the AUXDAC also changes by the same magnitude. The register uses twos complement format, in which 011111 maximizes the voltage on the REFIO node and 100000 minimizes the voltage.

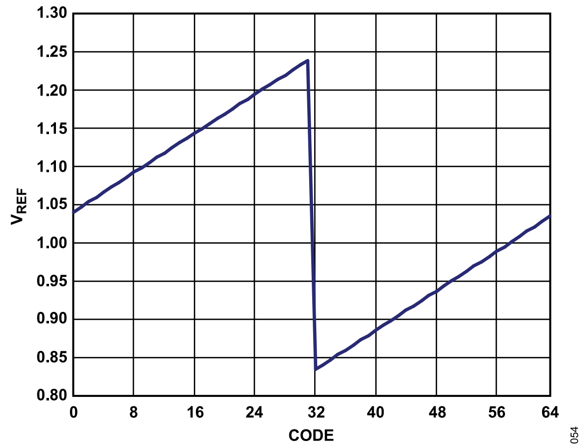

Figure 99. Typical V_{REF} Voltage vs. Code

Option 2

While using the internal FSADJx resistors, each main DAC can achieve independently controlled coarse gain using the lower six bits of Register 0x04 (IRSET[5:0]) and Register 0x07 (QRSET[5:0]). Unlike Coarse Gain Option 1, this impacts only the main DAC full-scale output current. The register uses twos complement format and allows the output current to be changed in approximately 0.25 dB steps.

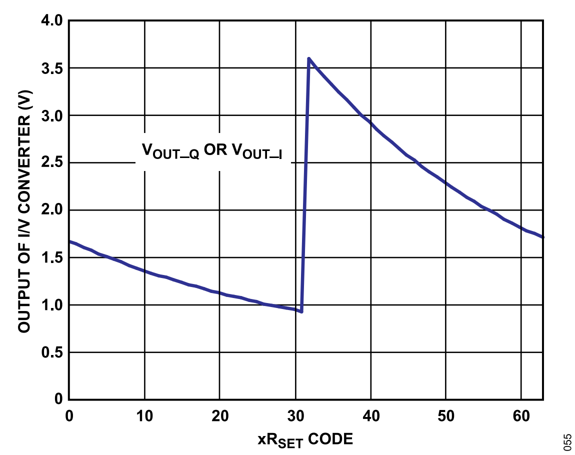

Figure 100. Effect of xR_{SET} Code

For applications requiring tighter gain tolerances or lower temperature drift, external temperature tracking resistors for FSADJx, xR_{LOAD}, and xR_{SET} are recommended.

Option 3

Even when the device is in pin mode, full-scale values can be adjusted by sourcing or sinking current from the FSADJx pins. Any noise injected here appears as amplitude modulation of the output. Thus, a portion of the required series resistance (at least 20 kΩ) must be installed right at the pin. A range of ±10% is quite practical using this method.

DIGITAL INTERFACE OPERATION

Option 4

As in Option 3, when the device is in pin mode, both full-scale values can be adjusted by sourcing or sinking current from the REFIO pin. Noise injected here appears as amplitude modulation of the output; therefore, a portion of the required series resistance (at least 10 kΩ) must be installed at the pin. A range of ±25% is quite practical when using this method.

Fine Gain

Each main DAC has independent fine gain control using the lower six bits in Register 0x03 (I DAC gain) and Register 0x06 (Q DAC gain). Unlike Coarse Gain Option 1, this impacts only the main DAC full-scale output current. These registers use straight binary format. One application in which straight binary format is critical is for side-band suppression while using a quadrature modulator. This is described in more detail in the Applications Information section.

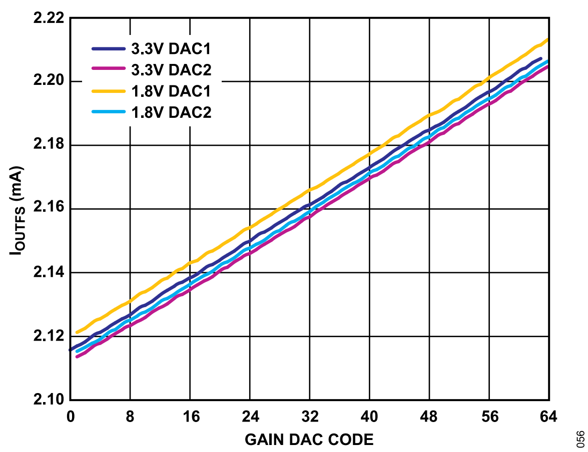

Figure 101. Typical DAC Gain Characteristics

USING THE INTERNAL TERMINATION RESISTORS

The AD9714/AD9715/AD9716/AD9717 have four 500 Ω termination internal resistors (two for each DAC output). To use these resistors to convert the DAC output current to a voltage, connect each DAC output pin to the adjacent load pin. For example, on the I DAC, IOUTP must be shorted to RLIP and IOUTN must be shorted to RLIN. In addition, the CMLI or CMLQ pin must be connected to ground directly or through a resistor. If the output current is at the nominal 2 mA and the CMLI or CMLQ pin is tied directly to ground, this produces a dc common-mode bias voltage on the DAC output equal to 0.5 V. If the DAC dc bias must be higher than 0.5 V, an external resistor can be connected between the CMLI or CMLQ pin and ground. This part also has an internal common-mode resistor that can be enabled. This is explained in the Using the Internal Common-Mode Resistor section.

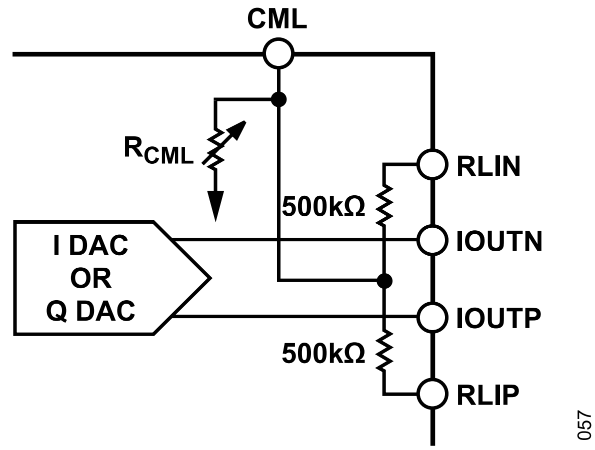

Figure 102. Simplified Internal Load Options

Using the Internal Common-Mode Resistor

These devices contain an adjustable internal common-mode resistor that can be used to increase the dc bias of the DAC outputs. By default, the common-mode resistor is not connected. When enabled, it can be adjusted from ~250 Ω to ~1 kΩ. Each main DAC has an independent adjustment using the lower six bits in Register 0x05 (IRCML[5:0]) and Register 0x08 (QRCML[5:0]).

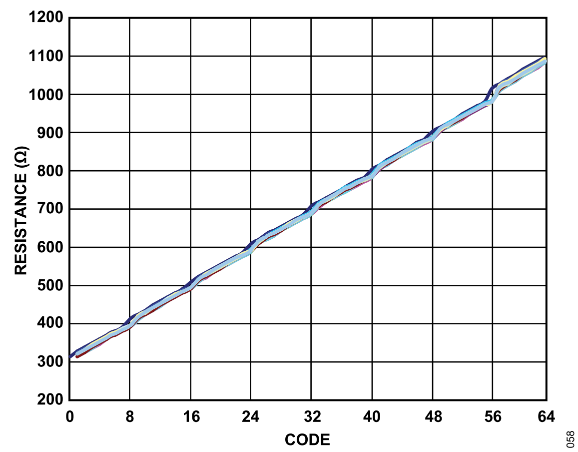

Figure 103. Typical CML Resistor Value vs. Register Code

Using the CMLx Pins for Optimal Performance

The CMLx pins also serve to change the DAC bias voltages in the parts allowing them to run at higher dc output bias voltages. When running the bias voltage below 0.9 V and an AVDD of 3.3 V, the parts perform optimally when the CMLx pins are tied to ground. When the dc bias increases above 0.9 V, set the CMLx pins at 0.5 V for optimal performance. The maximum dc bias on the DAC output should be kept at or below 1.2 V when the supply is 3.3 V. When the supply is 1.8 V, keep the dc bias close to 0 V and connect the CMLx pins directly to ground.

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OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9714/AD9715/AD9716/AD9717. Unless otherwise noted, it is assumed that I_{xOUTFS} is set to a nominal 2 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, signal gain, and/or a low output impedance.

A single-ended output is suitable for applications in which low cost and low power consumption are primary concerns.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion, as shown in Figure 104. The distortion performance of a transformer typically exceeds that available from standard op amps, particularly at higher frequencies. Transformer coupling provides excellent rejection of common-mode distortion (that is, even-order harmonics) over a wide frequency range. It also provides electrical isolation and can deliver voltage gain without adding noise. Transformers with different impedance ratios can also be used for impedance matching purposes. The main disadvantages of transformer coupling are low frequency roll-off, lack-of-power gain, and high output impedance.

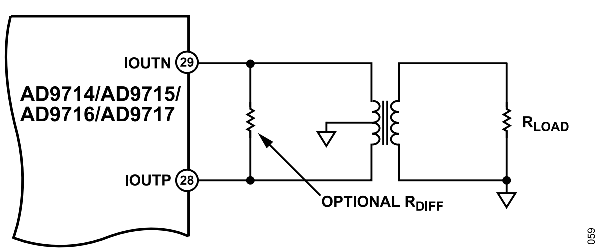

Figure 104. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to a voltage that keeps the voltages on IOUTP and IOUTN within the output common-mode voltage range of the device. Note that the dc component of the DAC output current is equal to I_{xOUTFS} and flows out of both IOUTP and IOUTN. The center tap of the transformer should provide a path for this dc current. In most applications, AGND provides the most convenient voltage for the transformer center tap. The complementary voltages appearing at IOUTP and IOUTN (that is, V_{IOUTP} and V_{IOUTN}) swing symmetrically around AGND and should be maintained with the specified output compliance range of the AD9714/AD9715/AD9716/AD9717.

A differential resistor, R_{DIFF}, can be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF}, as reflected by the transformer, is chosen to provide a source termination that results in a low voltage standing wave ratio (VSWR). Note that approximately half the signal power is dissipated across R_{DIFF}.

SINGLE-ENDED BUFFERED OUTPUT USING AN OP AMP

Figure 105 shows a buffered single-ended output configuration in which the op amp ADA4899-1 performs a current to voltage (I-V) conversion on the AD9714/AD9715/AD9716/AD9717 output current. The ADA4899-1 maintains IOUTN (or IOUTP) at a virtual ground, minimizing the nonlinear output impedance effect on the INL performance of the DAC as described in the Analog Output section. Although this single-ended configuration typically provides optimal dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by the slew rate capabilities of the op amp. The ADA4899-1 provides a negative unipolar output voltage, and its full-scale output voltage is simply the product of R_{FB} (250 Ω) and I_{OUTFS}. Set the full-scale output within the voltage output swing capabilities of the AD9714/AD9715/AD9716/AD9717 by scaling I_{OUTFS} and/or the feedback resistor, R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} because the signal current at the op amp is required to sink less signal current.

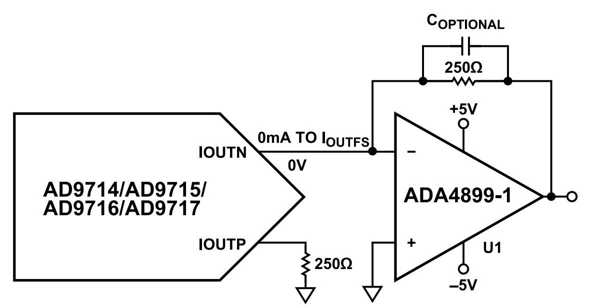

Figure 105. Unipolar Buffered Voltage Output

DIFFERENTIAL BUFFERED OUTPUT USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion, as shown in Figure 106. The AD9714/AD9715/AD9716/AD9717 is configured with two equal load resistors, R_{LOAD}, of 250 Ω. The differential voltage developed across IOUTN and IOUTP is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTN and IOUTP, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the distortion performance of the op amp by preventing the high slewing output of the DAC from overloading the op amp input.

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the ADA4899-1 is configured to provide some additional signal gain. The op amp must operate from a dual supply because its output is approximately ±1 V. A high speed

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amplifier capable of preserving the differential performance of the AD9714/AD9715/AD9716/AD9717 while meeting other system level objectives (such as cost or power) must be selected. The differential gain, gain setting resistor values, and full-scale output swing capabilities of the op amp must all be considered when optimizing this circuit.

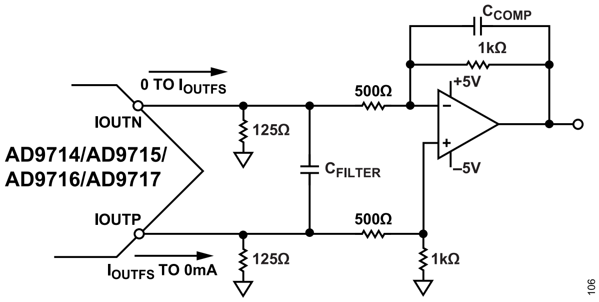

Figure 106. Differential Buffered Voltage Output

AUXILIARY DACS

The DACs of the AD9714/AD9715/AD9716/AD9717 feature two versatile and independent 10-bit auxiliary DACs suitable for dc offset correction and similar tasks.

Because the AUXDACs are driven through the SPI port, they should never be used in timing-critical applications, such as inside analog feedback loops.

To keep the pin count reasonable, these auxiliary DACs each share a pin with the corresponding FSADJx resistor. They are, therefore, usable only when enabled and when that DAC is operated on its internal full-scale resistors. A simple I-to-V converter is implemented on chip with selectable shunt resistors (3.2 kΩ to 16 kΩ) such that if REFIO is set to exactly 1 V, REFIO/2 equals 0.5 V, and the following equation describes the no load output voltage:

$$V_{OUT} = 0.5\ \text{V} - \left(I_{DAC} - \frac{1.5}{R_S}\right)16\ \text{k}\Omega \tag{9}$$

Figure 107 illustrates the function of all the SPI bits controlling these DACs with the exception of the QAUXEN (Register 0x0C, Bit 7) and IAUXEN (Register 0x0A, Bit 7) bits and gating to prohibit R_S < 3.2 kΩ.

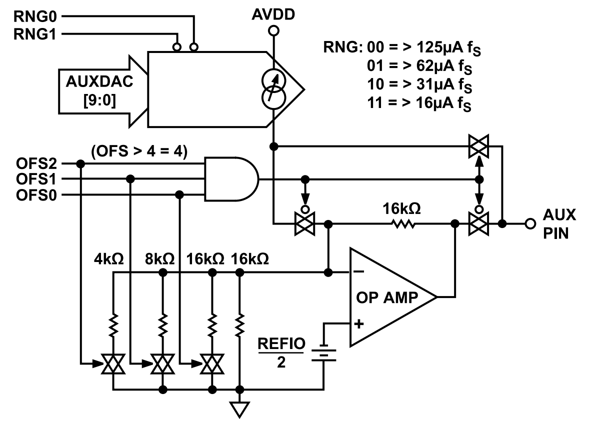

Figure 107. AUXDAC Simplified Circuit Diagram

The SPI speed limits the update rate of the auxiliary DACs. The data is inverted such that I_{AUXDAC} is full scale at 0x000 and zero at 0x1FF, as shown in Figure 108.

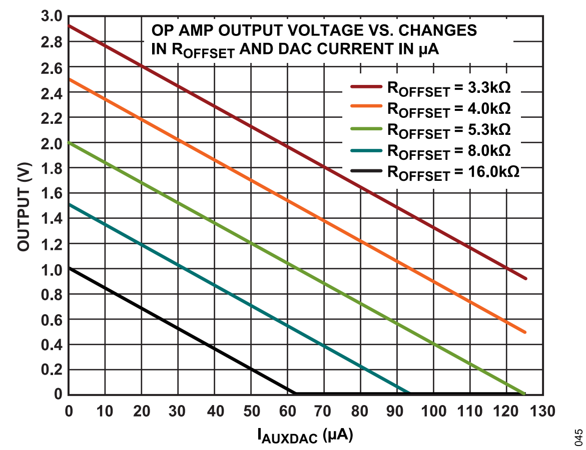

Figure 108. AUXDAC Op Amp Output vs. Current, AVDD = 3.3 V, No Load, AUXDAC 0x1FF to 0x000

Two registers are assigned to each DAC with 10 bits for the actual DAC current to be generated, a 3-bit offset (and gain) adjustment, a 2-bit current range adjustment, and an enable/disable bit. Setting the IAUXOFS (Register 0x0A, Bits[4:2]) and QAUXOFS (Register 0x0C, Bits[4:2]) bits to all 1s disables the respective op amp and routes the DAC current directly to the respective FSADJI/AUXI or FSADJQ/AUXQ pins. This is especially useful when the loads to be driven are beyond the limited capability of the on-chip amplifier.

When not enabled (QAUXEN or IAUXEN = 0), the respective DAC output is in open circuit.

DAC-TO-MODULATOR INTERFACING

The auxiliary DACs can be used for local oscillator (LO) cancellation when the DAC output is followed by a quadrature modulator. This LO feedthrough is caused by the input referred dc offset voltage of the quadrature modulator (and the DAC output offset voltage mismatch) and can degrade system performance. Typical

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DAC-to-quadrature modulator interfaces are shown in Figure 109 and Figure 110, with the series resistor value chosen to give an appropriate adjustment range. Figure 109 also shows external load resistors in use. Often, the input common-mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling or a dc level shift is necessary. If the required common-mode input voltage on the quadrature modulator matches that of the DAC, the dc blocking capacitors in Figure 109 can be removed and the on-chip resistors can be connected.

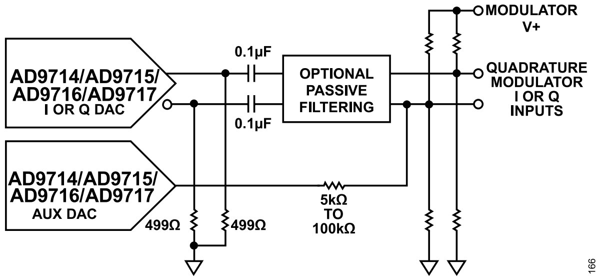

Figure 109. Typical Use of Auxiliary DACs and External Components for Coupling to Quadrature Modulators

Figure 110 shows a greatly simplified circuit that takes full advantage of the internal components supplied in the DAC. A low-pass or band-pass passive filter is recommended when spurious signals from the DAC (distortion and DAC images) at the quadrature modulator inputs can affect the system performance. In the example shown in Figure 109, the filter must be able to pass dc to properly bias the modulator. Placing the filter at the location shown in Figure 109 and Figure 110 allows easy design of the filter because the source and load impedances can easily be designed close to 500 Ω for a 2 mA full-scale output. Once the resistance at the modulator inputs is known, the user can easily look up the range of input offsets that may be encountered and compute a value for the series resistor on the AUXDAC output.

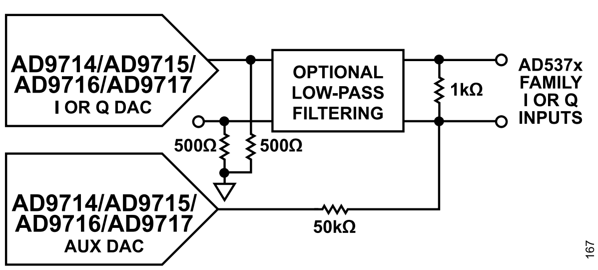

Figure 110. Simplified DC Coupling to Quadrature Modulator ADL537x Family or Equivalent Is Enabled By Using Internal Components

CORRECTING FOR NONIDEAL PERFORMANCE OF QUADRATURE MODULATORS ON THE IF-TO-RF CONVERSION

Analog quadrature modulators make it very easy to realize single sideband radios. However, there are several nonideal aspects of quadrature modulator performance. Among these analog degradations are gain mismatch and LO feedthrough.

Gain Mismatch

The gain in the real and imaginary signal paths of the quadrature modulator may not be matched perfectly. This leads to less than optimal image rejection because the cancellation of the negative frequency image is less than perfect.

LO Feedthrough

The quadrature modulator has a finite dc referred offset, as well as coupling from its LO port to the signal inputs. These can lead to a significant spectral spur at the frequency of the quadrature modulator LO.

The AD9714/AD9715/AD9716/AD9717 have the capability to correct for both of these analog degradations. However, understand that these degradations drift over temperature; therefore, if close to optimal single sideband performance is desired, a scheme for sensing these degradations over temperature and correcting them may be necessary.

I/Q-CHANNEL GAIN MATCHING

Fine gain matching is achieved by adjusting the values in the DAC fine gain adjustment registers. For the I DAC, these values are in the I DAC gain register (Register 0x03). For the Q DAC, these values are in the Q DAC gain register (Register 0x06). These are 6-bit values that cover ±2% of full scale. To perform gain compensation starting from the default values of zero, raise the value of one of these registers a few steps until it can be determined if the amplitude of the unwanted image is increased or decreased. If the unwanted image increases in amplitude, remove the step and try the same adjustment on the other DAC control register. Iterate register changes until the rejection cannot be improved further. If the fine gain adjustment range is not sufficient to find a null (that is, the register goes full scale with no null apparent), adjust the course gain settings of the two DACs accordingly and try again. Variations on this simple method are possible.

Note that LO feedthrough compensation is independent of phase compensation. However, gain compensation can affect the LO compensation because the gain compensation may change the common-mode level of the signal. The dc offset of some modulators is common-mode level dependent. Therefore, it is recommended that the gain adjustment be performed prior to LO compensation.

LO FEEDTHROUGH COMPENSATION

To achieve LO feedthrough compensation in a circuit, each output of the two AUXDACs must be connected through a 100 kΩ resistor to one side of the differential DAC output. See the Auxiliary DACs section for details of how to use AUXDACs. The purpose of these connections is to drive a very small amount of current into the nodes at the quadrature modulator inputs, thereby adding a slight

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dc bias to one or the other of the quadrature modulator signal inputs.

To achieve LO feedthrough compensation, the user should start with the default conditions of the AUXDAC registers, and then increment the magnitude of one or the other AUXDAC output voltages. While this is being done, the amplitude of the LO feedthrough at the quadrature modulator output should be sensed. If the LO feedthrough amplitude increases, try either decreasing the output voltage of the AUXDAC being adjusted, or try adjusting the output voltage of the other AUXDAC. It may take practice before an effective algorithm is achieved. The AD9714/AD9715/AD9716/AD9717 evaluation board can be used to adjust the LO feedthrough down to the noise floor, although this is not stable over temperature.

RESULTS OF GAIN AND OFFSET CORRECTION

The results of gain and offset correction can be seen in Figure 111 and Figure 112. Figure 111 shows the output spectrum of the quadrature demodulator before gain and offset correction. Figure 112 shows the output spectrum after correction. The LO feedthrough spur at 450 MHz has been suppressed to the noise level. This result can be achieved by applying the correction, but the correction must be repeated after a large change in temperature.

Note that gain matching improves the negative frequency image rejection, but it is also related to the phase mismatch in the quadrature modulator. It can be improved by adjusting the relative phase between the two quadrature signals at the digital side or properly designing the low-pass filter between the DACs and quadrature modulators. Phase mismatch is frequency dependent; therefore, routines must be developed to adjust it if wideband signals are desired.

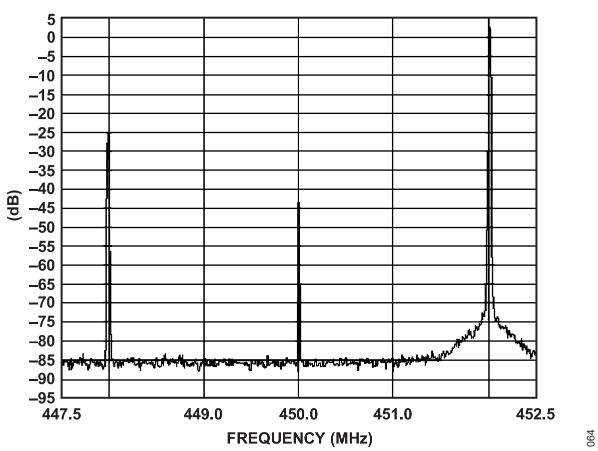

Figure 111. AD9714/AD9715/AD9716/AD9717 and ADL5370 with a Single-Tone Signal at 450 MHz, No Gain or LO Compensation

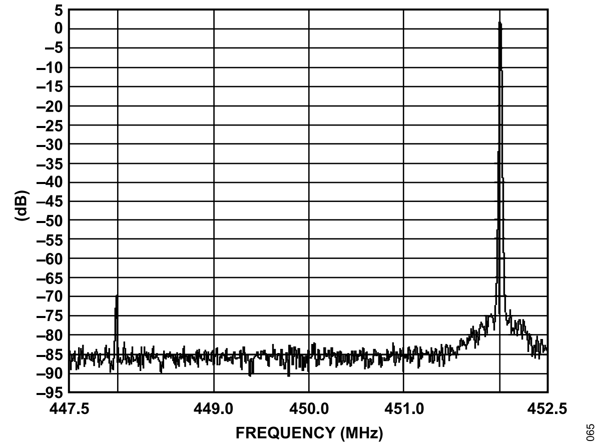

Figure 112. AD9714/AD9715/AD9716/AD9717 and ADL5370 with a Single-Tone Signal at 450 MHz, Gain and LO Compensation Optimized

POWER SUPPLY

Requirements

The analog and digital I/O sections of the AD9714/AD9715/AD9716/AD9717 have separate power supply inputs (AVDD, DVDDIO, and CVDDIO) that can operate from 1.8 V to 3.3 V. The core digital section (DVDD) requires 1.8 V.

To ensure proper operation of the device, the RESET/PINMD pin must be pulsed high after applying power to all supplies. If operating the device in SPI mode, the minimum duration before setting the pin low is 50 ns. If operating the device in pin mode, there is no need to set RESET/PINMD low after pulsing it high and, alternatively, the pin can be pulled up to DVDDIO.

Recommendation

The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths. Recommended decoupling capacitor values for each supply pin are one of each of the following: 10 nF, 0.1 µF, and 10 µF. The smallest value capacitor must be placed nearest to the supply pin.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-40-1	LFCSP	40-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: August 05, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9714BCPZ	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)		CP-40-1
AD9714BCPZRL7	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 750	CP-40-1
AD9715BCPZ	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)		CP-40-1
AD9715BCPZRL7	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 750	CP-40-1
AD9716BCPZ	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)		CP-40-1
AD9716BCPZRL7	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 750	CP-40-1
AD9717BCPZ	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)		CP-40-1
AD9717BCPZRL7	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 750	CP-40-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
AD9714-DPG2-EBZ	Evaluation Board
AD9715-DPG2-EBZ	Evaluation Board
AD9716-DPG2-EBZ	Evaluation Board
AD9717-DPG2-EBZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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