



# THE DATASHEET OF DAC8812IBPW



## DAC8812 Dual, Serial-Input 16-Bit Multiplying Digital-to-Analog Converter

### 1 Features

- Relative Accuracy: 1 LSB Max
- Differential Nonlinearity: 1 LSB Max
- 2-mA Full-Scale Current  $\pm 20\%$ , With  $V_{REF} = \pm 10\text{ V}$
- 0.5- $\mu\text{s}$  Settling Time
- Midscale or Zero-Scale Reset
- Separate 4Q Multiplying Reference Inputs
- Reference Bandwidth: 10 MHz
- Reference Dynamics:  $-105\text{-dB THD}$
- SPI™-Compatible 3-Wire Interface: 50 MHz
- Double Buffered Registers to Enable Simultaneous Multichannel Update
- Internal Power-On Reset
- Industry-Standard Pin Configuration

### 2 Applications

- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration

### 3 Description

The DAC8812 is a dual, 16-bit, current-output digital-to-analog converter (DAC) designed to operate from a single 2.7-V to 5.5-V supply.

The applied external reference input voltage  $V_{REF}$  determines the full-scale output current. An internal feedback resistor ( $R_{FB}$ ) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

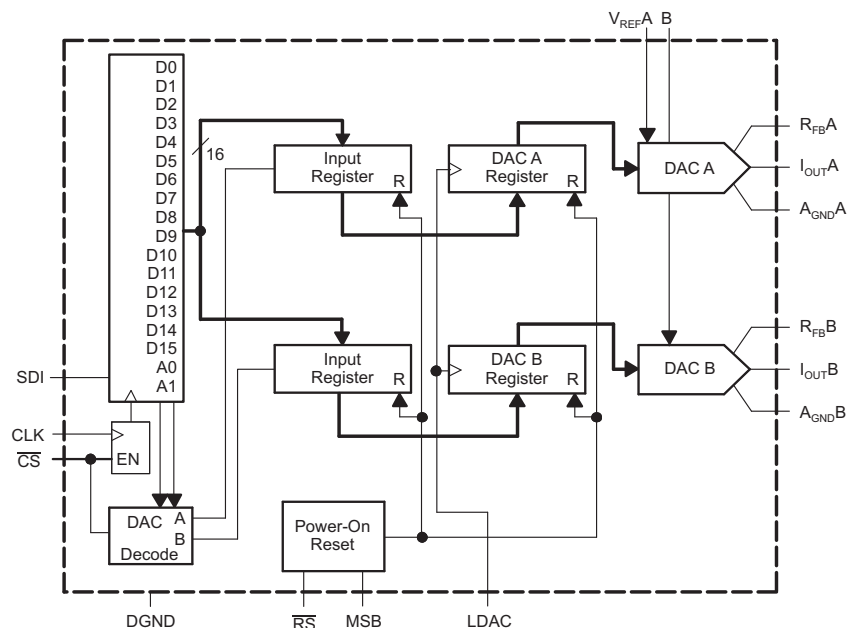
A double-buffered, serial data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using serial data in (SDI), clock (CLK), and a chip-select ( $\overline{CS}$ ). A common level-sensitive load DAC strobe (LDAC) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to zero at system turnon. An MSB pin allows system reset assertion ( $\overline{RS}$ ) to force all registers to zero code when  $MSB = 0$ , or to midscale code when  $MSB = 1$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC8812	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Functional Block Diagram



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.3 Feature Description .....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	8.4 Device Functional Modes .....	<b>15</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>18</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information .....	<b>18</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	9.2 Typical Application .....	<b>18</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>19</b>
<b>7 Specifications</b> .....	<b>4</b>	<b>11 Layout</b> .....	<b>20</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	11.1 Layout Guidelines .....	<b>20</b>
7.2 ESD Ratings .....	<b>4</b>	11.2 Layout Example .....	<b>21</b>
7.3 Recommended Operating Conditions .....	<b>4</b>	<b>12 Device and Documentation Support</b> .....	<b>22</b>
7.4 Thermal Information .....	<b>4</b>	12.1 Documentation Support .....	<b>22</b>
7.5 Electrical Characteristics .....	<b>5</b>	12.2 Receiving Notification of Documentation Updates .....	<b>22</b>
7.6 Timing Requirements .....	<b>6</b>	12.3 Community Resources .....	<b>22</b>
7.7 Switching Characteristics .....	<b>6</b>	12.4 Trademarks .....	<b>22</b>
7.8 Typical Characteristics .....	<b>8</b>	12.5 Electrostatic Discharge Caution .....	<b>22</b>
<b>8 Detailed Description</b> .....	<b>13</b>	12.6 Glossary .....	<b>22</b>
8.1 Overview .....	<b>13</b>	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>22</b>
8.2 Functional Block Diagram .....	<b>13</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (March 2016) to Revision F</b>	<b>Page</b>
• Changed the maximum $T_A$ value from 125°C to 85°C in the <i>Recommended Operating Conditions</i> table .....	<b>4</b>
• Changed the name of the input resistance match parameter to <i>Channel-to-channel input resistance match</i> in the <i>Electrical Characteristics</i> table .....	<b>5</b>
• Made $V_{REF}$ negative in the equation for $V_{OUT}$ .....	<b>14</b>
• Added the <i>Receiving Notification of Documentation Updates</i> section .....	<b>22</b>

<b>Changes from Revision D (January 2016) to Revision E</b>	<b>Page</b>
• Changed the <i>DAC8812 Timing Diagram</i> image .....	<b>7</b>

<b>Changes from Revision C (November 2015) to Revision D</b>	<b>Page</b>
• Changed the <i>DAC8812 Timing Diagram</i> image to show the setup and hold time with respect to rising edge .....	<b>7</b>

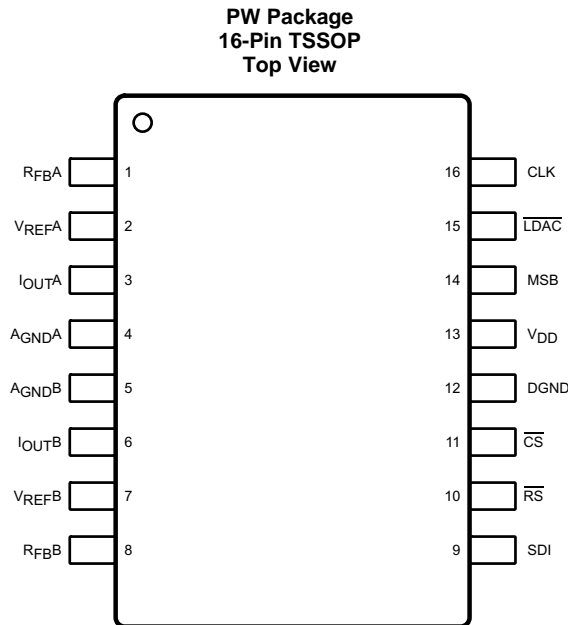
  

<b>Changes from Revision B (February 2007) to Revision C</b>	<b>Page</b>
• Added ESD Ratings table, Timing Requirements and Switching Characteristics tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ....	<b>1</b>
• Replaced Package/Ordering Information table with Device Comparison table .....	<b>3</b>
• Added I/O column to Pin Functions table .....	<b>3</b>

## 5 Device Comparison Table

DEVICE	MAXIMUM RELATIVE ACCURACY (LSB)
DAC8812C	±1
DAC8812B	±2

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	RFB A	I	Establish voltage output for DAC A by connecting to external amplifier output.
2	VREF A	I	DAC A reference voltage input pin. Establishes DAC A full-scale output voltage. Can be tied to V <sub>DD</sub> pin.
3	IOUT A	O	DAC A current output
4	AGND A	—	DAC A analog ground
5	AGND B	—	DAC B analog ground
6	IOUT B	O	DAC B current output
7	VREF B	I	DAC B reference voltage input pin. Establishes DAC B full-scale output voltage. Can be tied to V <sub>DD</sub> pin.
8	RFB B	I	Establish voltage output for DAC B by connecting to external amplifier output.
9	SDI	I	Serial data input; data loads directly into the shift register.
10	RS	I	Reset pin; active-low input. Input registers and DAC registers are set to all 0s or midscale. Register data = 0x0000 when MSB = 0. Register data = 0x8000 when MSB = 1 for DAC8812.
11	CS	I	Chip-select; active-low input. Disables shift register loading when high. Transfers serial register data to input register when CS goes high. Does not affect LDAC operation.
12	DGND	—	Digital ground
13	V <sub>DD</sub>	I	Positive power-supply input. Specified range of operation 2.7 V to 5.5 V.
14	MSB	I	MSB bit sets output to either 0 or midscale during a RESET pulse (RS) or at system power-on. Output equals zero scale when MSB = 0 and midscale when MSB = 1. MSB pin can be permanently tied to ground or V <sub>DD</sub> .
15	LDAC	I	Load DAC register strobe; level-sensitive active-low. Transfers all input register data to the DAC registers. Asynchronous active-low input. See Table 2 for operation.
16	CLK	I	Clock input. Positive edge clocks data into shift register.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>DD</sub> to GND	–0.3	7	V
V <sub>REFX</sub> , R <sub>FBX</sub> to GND	–18	18	V
Digital logic inputs to GND	–0.3	V <sub>DD</sub> + 0.3	V
I <sub>OUTX</sub> to GND	–0.3	V <sub>DD</sub> + 0.3	V
A <sub>GNDX</sub> to DGND	–0.3	0.3	V
Input current to any pin except supplies	–50	50	mA
Package power dissipation		(T <sub>Jmax</sub> – T <sub>A</sub> ) / R <sub>θJA</sub>	W
Maximum junction temperature (T <sub>Jmax</sub> )		150	°C
Operating temperature	–40	85	°C
Storage temperature, T <sub>stg</sub>	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage to GND	2.7		5.5	V
T <sub>A</sub>	Operating ambient temperature	–40		85	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DAC8812	UNIT
		PW (TSSOP)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	100.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	32.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	46.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

$V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $I_{OUTX} = \text{Virtual GND}$ ,  $A_{GNDX} = 0\text{ V}$ ,  $V_{REFA,B} = 10\text{ V}$ ,  $T_A = \text{full operating temperature range}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	
<b>STATIC PERFORMANCE<sup>(1)</sup></b>						
Resolution				16	Bits	
INL	Relative accuracy	DAC8812B		±2	LSB	
		DAC8812C		±1		
DNL	Differential nonlinearity			±1	LSB	
$I_{OUTX}$	Output leakage current	Data = 0000h, $T_A = 25^\circ\text{C}$		10	nA	
		Data = 0000h, $T_A = T_A \text{ max}$		20		
$G_{FSE}$	Full-scale gain error	Data = FFFFh		±0.75	±4	mV
$TCV_{FS}$	Full-scale temperature coefficient <sup>(2)</sup>		1		ppm/°C	
$R_{FBX}$	Feedback resistor	$V_{DD} = 5\text{ V}$		5	kΩ	
<b>REFERENCE INPUT<sup>(2)</sup></b>						
$V_{REFX}$	$V_{REFX}$ range	-15		15	V	
$R_{REFX}$	Input resistance	4	5	6	kΩ	
		Channel-to-channel input resistance match		1%		
$C_{REFX}$	Input capacitance		5		pF	
<b>ANALOG OUTPUT<sup>(2)</sup></b>						
$I_{OUTX}$	Output current	Data = FFFFh		1.6	2.5	mA
$C_{OUTX}$	Output capacitance	Code-dependent		50		pF
<b>LOGIC INPUTS<sup>(2)</sup></b>						
$V_{IL}$	Input low voltage	$V_{DD} = 2.7\text{ V}$		0.6	V	
		$V_{DD} = 5\text{ V}$		0.8		
$V_{IH}$	Input high voltage	$V_{DD} = 2.7\text{ V}$		2.1	V	
		$V_{DD} = 5\text{ V}$		2.4		
$I_{IL}$	Input leakage current			1	μA	
$C_{IL}$	Input capacitance			10	pF	

(1) All static performance tests (except  $I_{OUT}$ ) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8812  $R_{FB}$  pin is tied to the amplifier output. Typical values represent average readings measured at  $25^\circ\text{C}$ .

(2) These parameters are not subject to production testing.

## Electrical Characteristics (continued)

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $I_{OUTX} = \text{Virtual GND}$ ,  $A_{GNDX} = 0\text{ V}$ ,  $V_{REFA,B} = 10\text{ V}$ ,  $T_A = \text{full operating temperature range}$ , unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CHARACTERISTICS</b>						
$V_{DD\text{ RANGE}}$	Power supply range		2.7		5.5	V
$I_{DD}$	Positive supply current	Logic inputs = 0 V, $V_{DD} = 4.5\text{ V to }5.5\text{ V}$		2	5	$\mu\text{A}$
		Logic inputs = 0 V, $V_{DD} = 2.7\text{ V to }3.6\text{ V}$		1	2.5	$\mu\text{A}$
$P_{DISS}$	Power dissipation	Logic inputs = 0 V			0.0275	mW
$P_{SS}$	Power supply sensitivity	$\Delta V_{DD} = \pm 5\%$			0.006%	
<b>AC CHARACTERISTICS<sup>(2) (3)</sup></b>						
$t_s$	Output voltage settling time	To $\pm 0.1\%$ of full-scale, Data = 0000h to FFFFh to 0000h		0.3		$\mu\text{s}$
		To $\pm 0.0015\%$ of full-scale, Data = 0000h to FFFFh to 0000h		0.5		
$Q_G$	DAC glitch impulse	Data = 7FFFh to 8000h to 7FFFh		5		nV-s
BW -3 dB	Reference multiplying BW	$V_{REFX} = 100\text{ mV}_{RMS}$ , Data = FFFFh, $C_{FB} = 3\text{ pF}$		10		MHz
	Feedthrough error	Data = 0000h, $V_{REFX} = 100\text{ mV}_{RMS}$ , $f = 100\text{ kHz}$		-70		dB
	Crosstalk error	Data = 0000h, $V_{REFB} = 100\text{ mV}_{RMS}$ , Adjacent channel, $f = 100\text{ kHz}$		-100		dB
$Q_D$	Digital feedthrough	$\overline{CS} = 1$ and $f_{CLK} = 1\text{ MHz}$		1		nV-s
THD	Total harmonic distortion	$V_{REF} = 5\text{ V}_{PP}$ , Data = FFFFh, $f = 1\text{ kHz}$		-105		dB
$e_n$	Output spot noise voltage	$f = 1\text{ kHz}$ , BW = 1 Hz		12		$\text{nV}/\sqrt{\text{Hz}}$

(3) All ac characteristic tests are performed in a closed-loop system using a THS4011 I-to-V converter amplifier.

## 7.6 Timing Requirements

See [Figure 1](#)

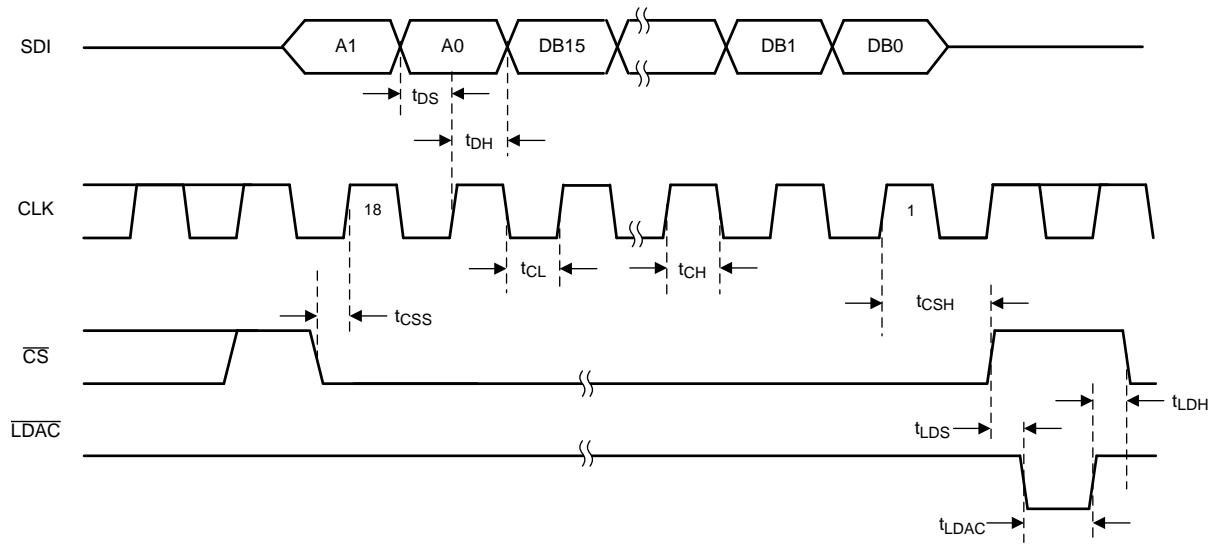
		MIN	NOM	MAX	UNIT
<b>INTERFACE TIMING<sup>(1)</sup></b>					
$t_{CH}$	Clock duration, high	10			ns
$t_{CL}$	Clock duration, low	10			ns
$t_{CSS}$	$\overline{CS}$ to clock setup	0			ns
$t_{CSH}$	Clock to $\overline{CS}$ hold	10			ns
$t_{LDAC}$	Load DAC pulse duration	20			ns
$t_{DS}$	Data setup	10			ns
$t_{DH}$	Data hold	10			ns
$t_{LDS}$	Load setup	5			ns
$t_{LDH}$	Load hold	25			ns

(1) All input control signals are specified with  $t_R = t_F = 2.5\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

## 7.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERFACE TIMING</b>						
$t_{PD}$	Clock to SDO propagation delay		2		20	ns



**Figure 1. DAC8812 Timing Diagram**

## 7.8 Typical Characteristics

### 7.8.1 Channel A—5 V

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise noted

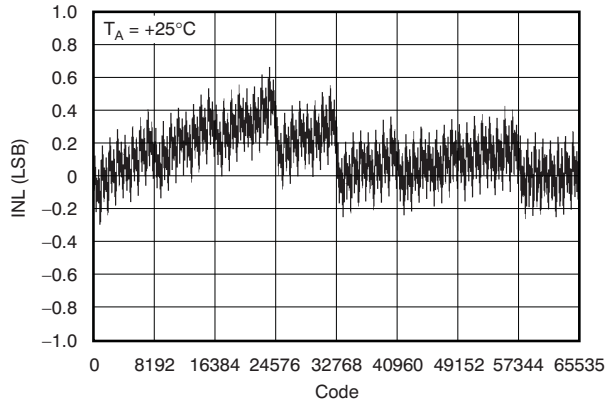


Figure 2. Integral Nonlinearity vs Digital Input Code

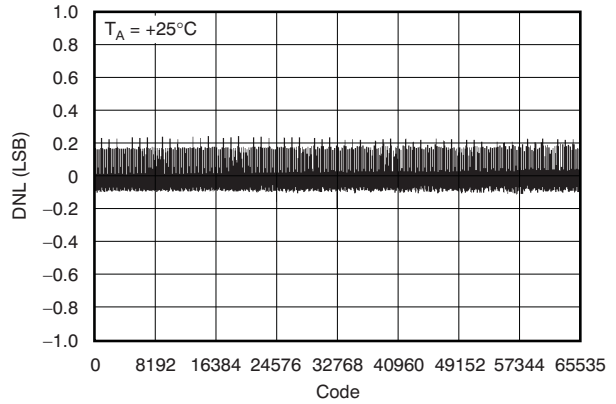


Figure 3. Differential Nonlinearity vs Digital Input Code

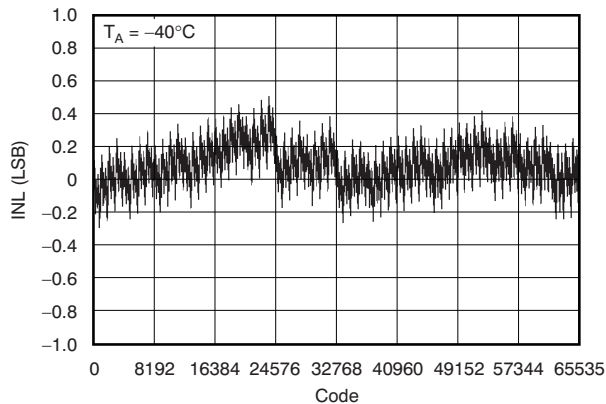


Figure 4. Integral Nonlinearity vs Digital Input Code

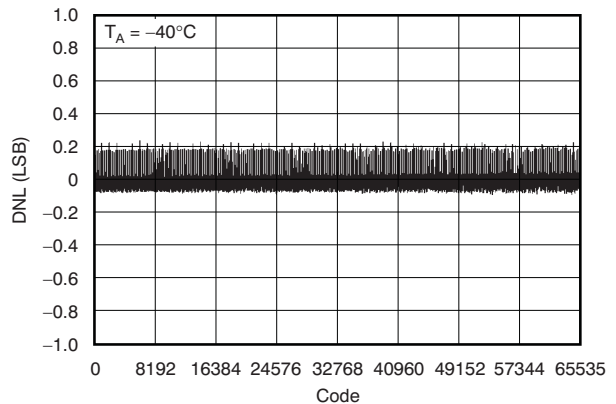


Figure 5. Differential Nonlinearity vs Digital Input Code

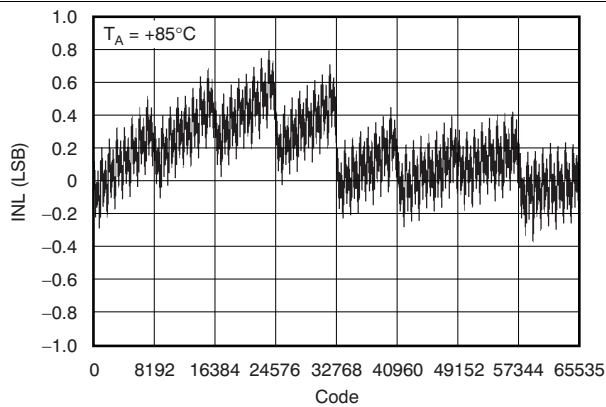


Figure 6. Integral Nonlinearity vs Digital Input Code

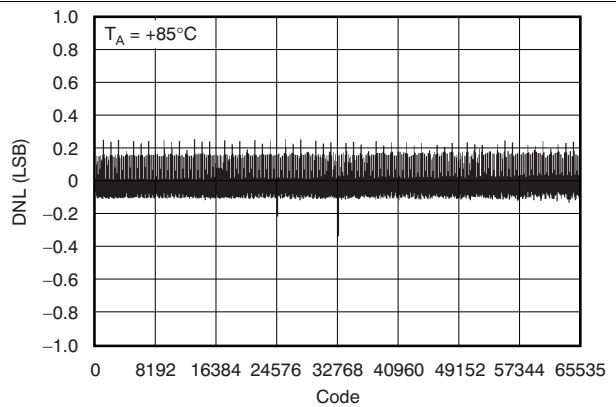
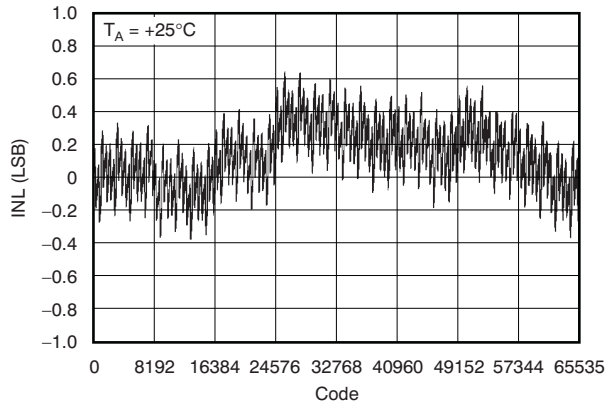


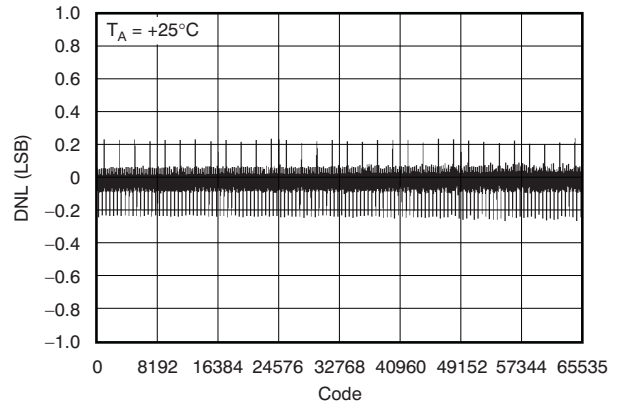
Figure 7. Differential Nonlinearity vs Digital Input Code

### 7.8.2 Channel B—5 V

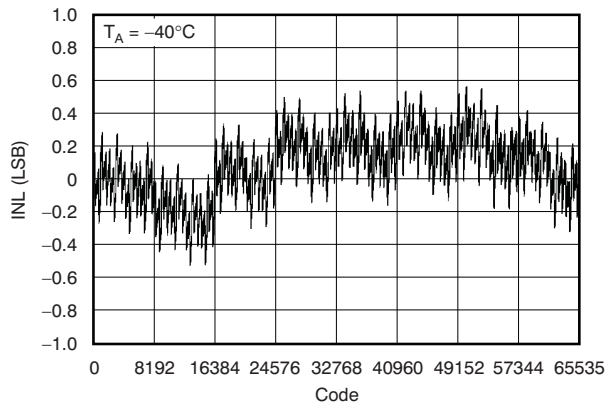
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise noted



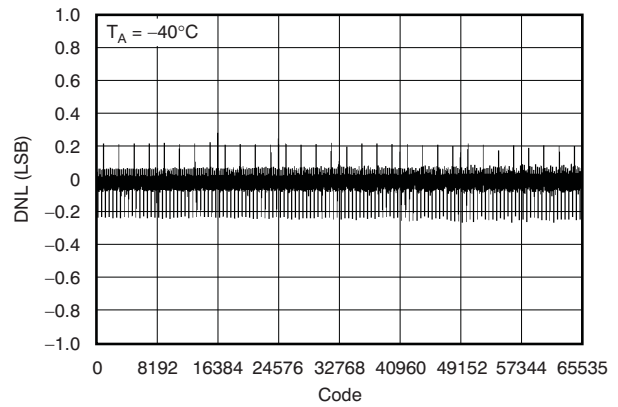
**Figure 8. Integral Nonlinearity vs Digital Input Code**



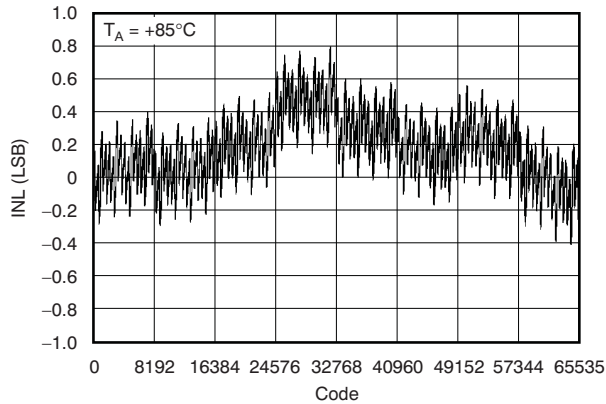
**Figure 9. Differential Nonlinearity vs Digital Input Code**



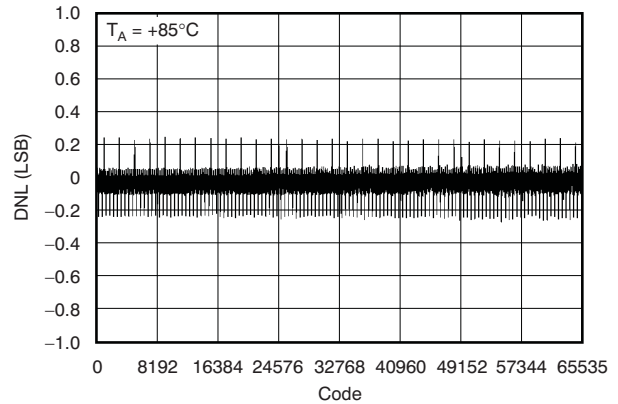
**Figure 10. Integral Nonlinearity vs Digital Input Code**



**Figure 11. Differential Nonlinearity vs Digital Input Code**



**Figure 12. Integral Nonlinearity vs Digital Input Code**



**Figure 13. Differential Nonlinearity vs Digital Input Code**

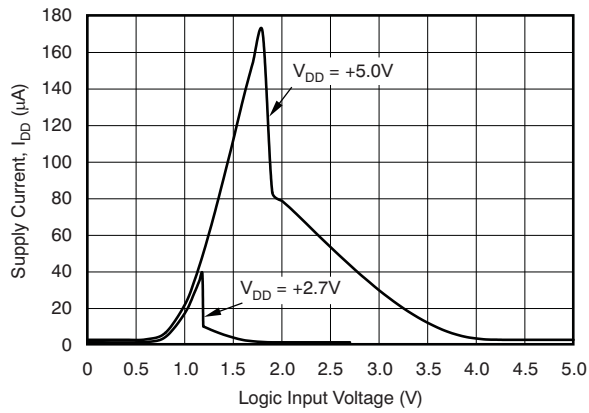
**DAC8812**

SBAS349F – AUGUST 2005 – REVISED JUNE 2016

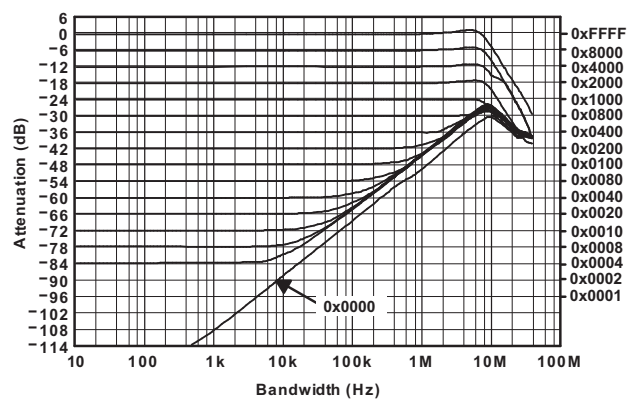
www.ti.com

**7.8.3 Channel A and B—5 V**

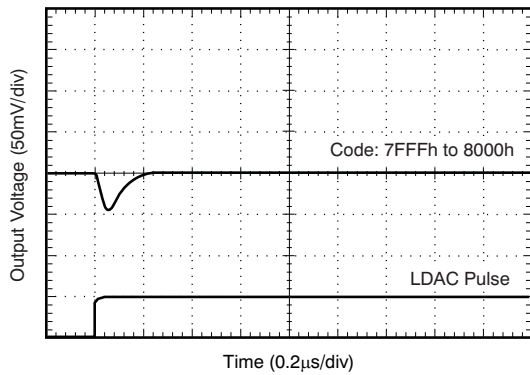
At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise noted



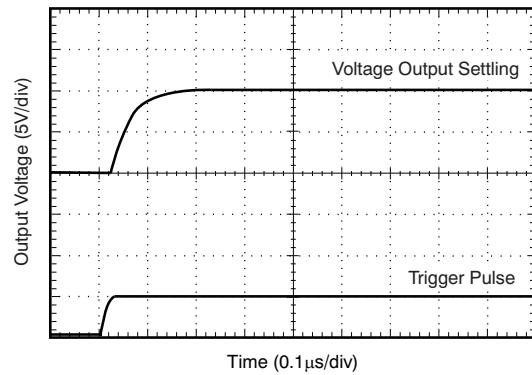
**Figure 14. Supply Current vs Logic Input Voltage**



**Figure 15. Reference Multiplying Bandwidth**



**Figure 16. DAC Glitch**



**Figure 17. DAC Settling Time**

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ , unless otherwise noted

### 7.8.4 Channel A—2.7 V

At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ , unless otherwise noted

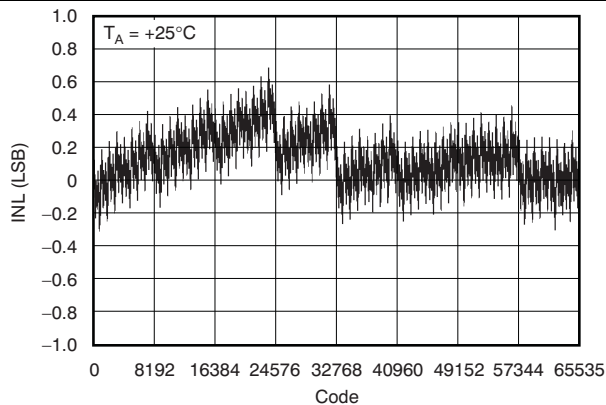


Figure 18. Integral Nonlinearity vs Digital Input Code

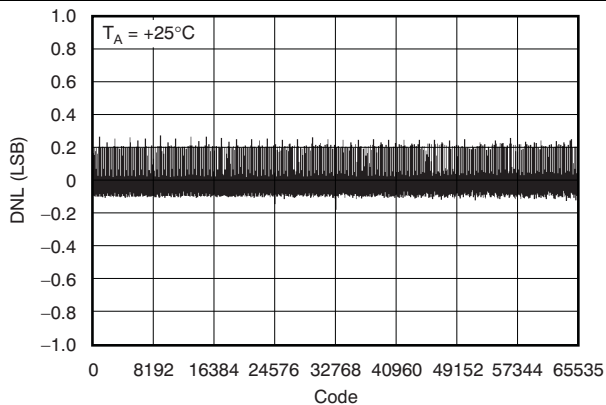


Figure 19. Differential Nonlinearity vs Digital Input Code

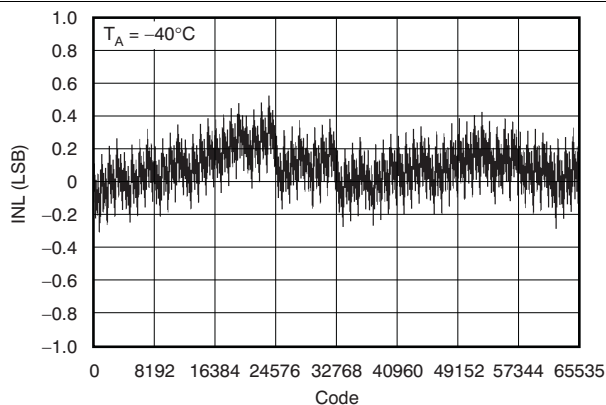


Figure 20. Integral Nonlinearity vs Digital Input Code

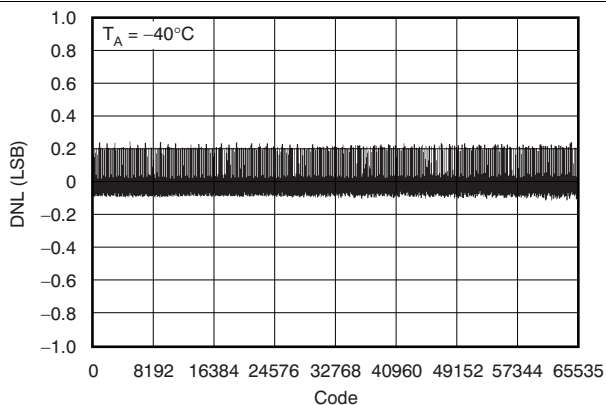


Figure 21. Differential Nonlinearity vs Digital Input Code

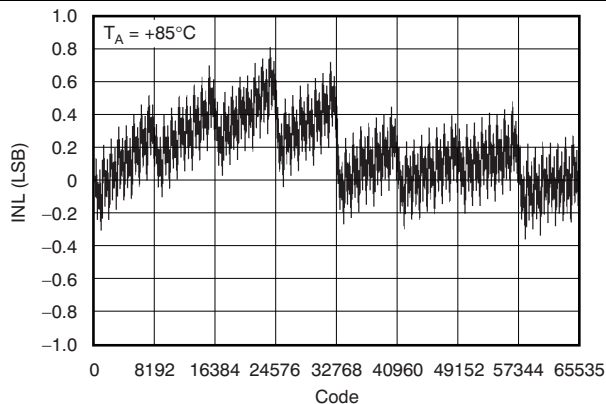


Figure 22. Integral Nonlinearity vs Digital Input Code

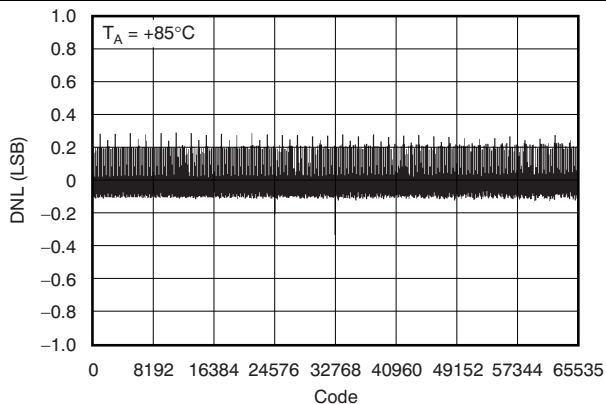
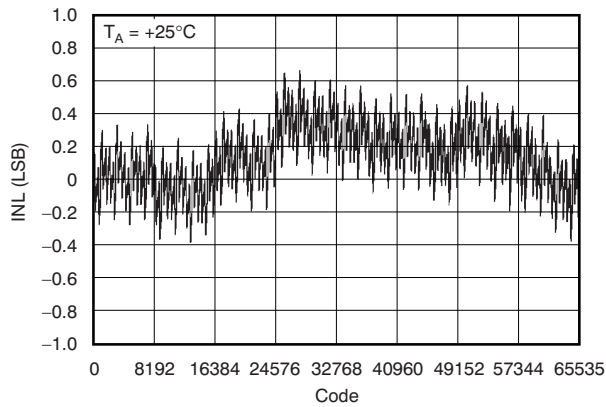
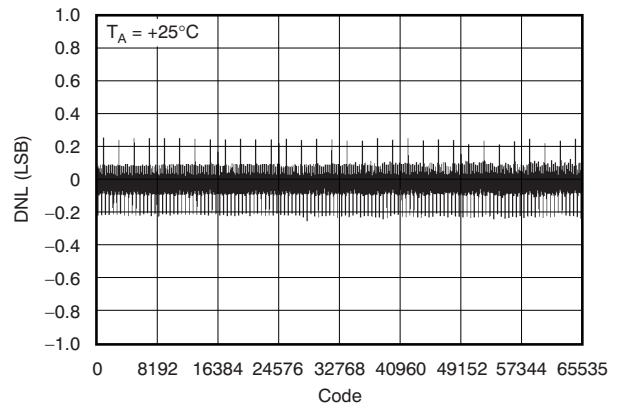
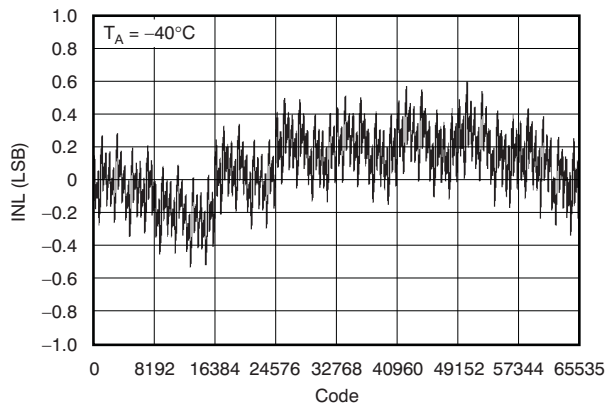
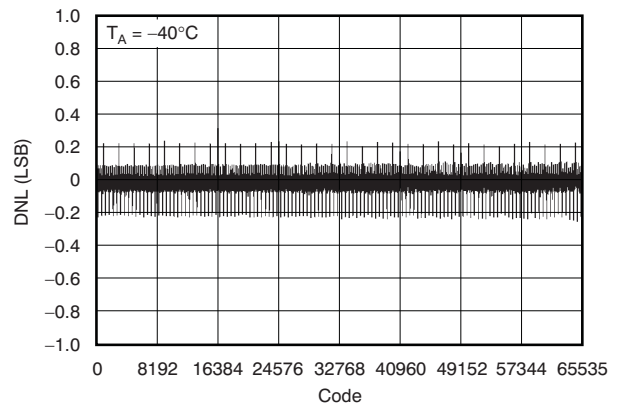
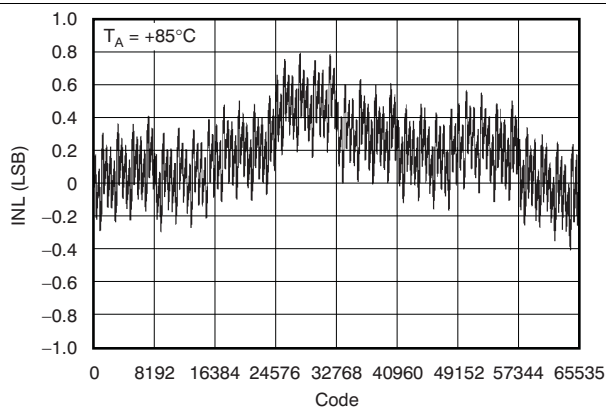
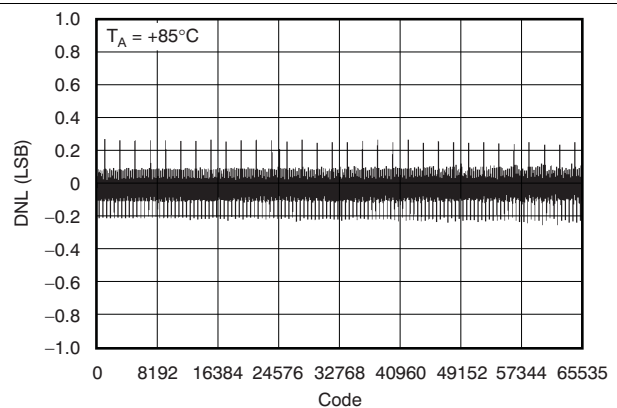


Figure 23. Differential Nonlinearity vs Digital Input Code

### 7.8.5 Channel B—2.7 V

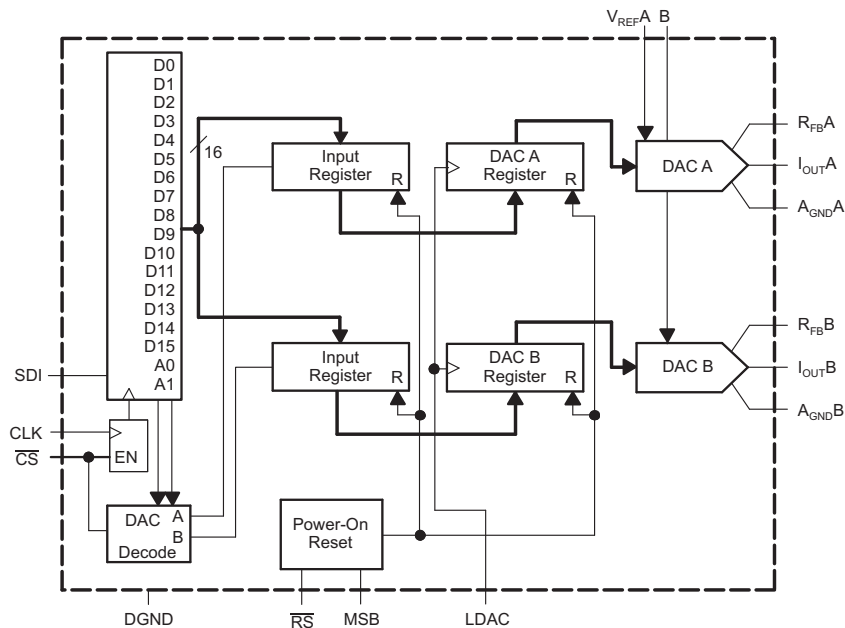
 At  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ , unless otherwise noted

**Figure 24. Integral Nonlinearity vs Digital Input Code**

**Figure 25. Differential Nonlinearity vs Digital Input Code**

**Figure 26. Integral Nonlinearity vs Digital Input Code**

**Figure 27. Differential Nonlinearity vs Digital Input Code**

**Figure 28. Integral Nonlinearity vs Digital Input Code**

**Figure 29. Differential Nonlinearity vs Digital Input Code**

## 8 Detailed Description

### 8.1 Overview

The DAC8812 contains two 16-bit, current-output, digital-to-analog converters (DACs). Each DAC has its own independent multiplying reference input. The DAC8812 uses a 3-wire, SPI-compatible serial data interface, with a configurable asynchronous  $\overline{RS}$  pin for midscale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an  $\overline{LDAC}$  strobe enables two channel simultaneous updates for hardware synchronized output voltage changes.

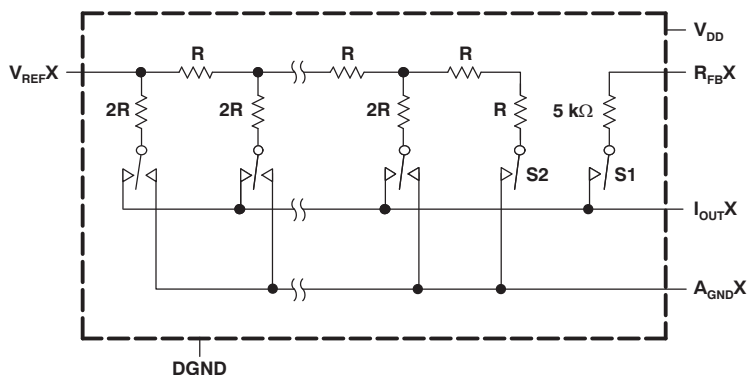
### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Digital-to-Analog Converters

The DAC8812 contains two current-steering R-2R ladder DACs. Figure 30 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The  $R_{FBX}$  pin is connected to the output of the external amplifier. The  $I_{OUTX}$  pin is connected to the inverting input of the external amplifier. The  $A_{GNDX}$  pin should be Kelvin-connected to the load point in the circuit requiring the full 16-bit accuracy.



Digital interface connections omitted for clarity.  
Switches S1 and S2 are closed,  $V_{DD}$  must be powered.

Figure 30. Typical Equivalent DAC Channel

**Feature Description (continued)**

The DAC is designed to operate with both negative or positive reference voltages. The  $V_{DD}$  power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal  $5\text{ k}\Omega$  feedback resistor. If users are attempting to measure the value of  $R_{FB}$ , power must be applied to  $V_{DD}$  in order to achieve continuity. The DAC output voltage is determined by  $V_{REF}$  and the digital data (D) according to Equation 1:

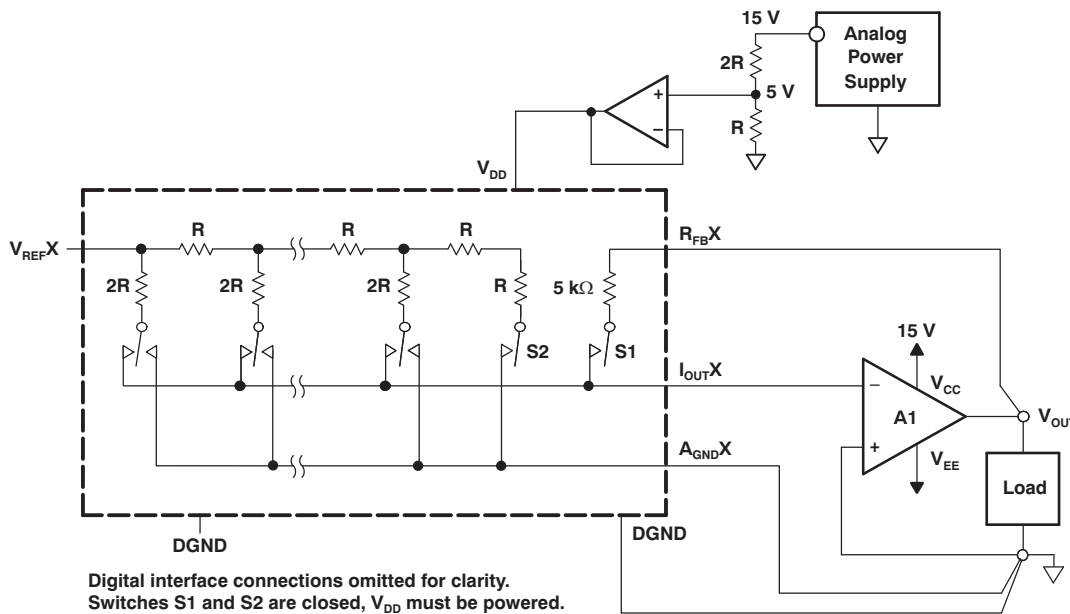
$$V_{OUT} = -V_{REF} \times \frac{D}{65536} \tag{1}$$

Note that the output polarity is opposite of the  $V_{REF}$  polarity for dc reference voltages.

The DAC is also designed to accommodate ac reference input signals. The DAC8812 accommodates input reference voltages in the range of  $-15\text{ V}$  to  $15\text{ V}$ . The reference voltage inputs exhibit a constant nominal input resistance of  $5\text{ k}\Omega$ ,  $\pm 20\%$ . On the other hand, DAC outputs  $I_{OUTA}$  and B are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8812 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor,  $C_{FB}$  ( $4\text{ pF}$  to  $20\text{ pF}$  typical), may be needed to provide a critically damped output response for step changes in reference input voltages.

Figure 15 shows the gain vs frequency performance at various attenuation settings using a  $3\text{ pF}$  external feedback capacitor connected across the  $I_{OUTX}$  and  $R_{FBX}$  pins. In order to maintain good analog performance, power-supply bypassing of  $0.01\text{ }\mu\text{F}$ , in parallel with  $1\text{ }\mu\text{F}$ , is recommended. Under these conditions, clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and  $P_{SS}$  frequency-dependent characteristics. It is best to derive the DAC8812 5-V supply from the system analog supply voltages (do not use the digital 5-V supply); see Figure 31.



**Figure 31. Recommended Kelvin-Sensed Hookup**

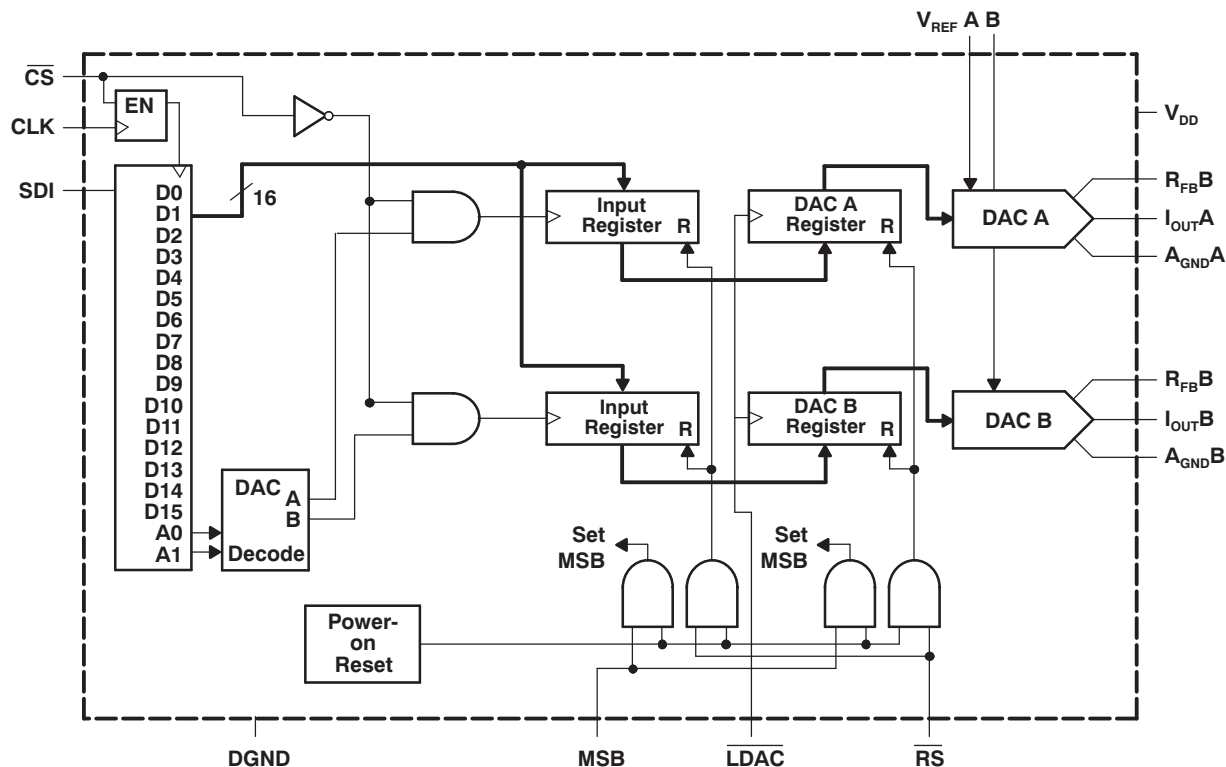


Figure 32. System-Level Digital Interfacing

### 8.3.2 Power-On Reset

When the  $V_{DD}$  power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or midscale, depending on the MSB pin voltage. The  $V_{DD}$  power supply should have a smooth positive ramp without drooping, in order to have consistent results, especially in the region of  $V_{DD} = 1.5$  V to 2.3 V. The DAC register data stays at zero or midscale setting until a valid serial register data load takes place.

#### 8.3.2.1 ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and  $V_{DD}$  as shown in Figure 33.

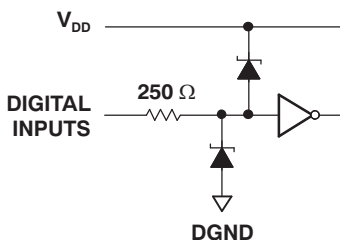


Figure 33. Equivalent ESD Protection Circuits

## 8.4 Device Functional Modes

### 8.4.1 Serial Data Interface

The DAC8812 uses a 3-wire ( $\overline{CS}$ , SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8812 is clocked into the serial input register in an 18-bit data-word format. MSB bits are loaded first. Table 1 defines the 18 data-word bits for the DAC8812.

## Device Functional Modes (continued)

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the *Interface Timing* specifications of the [Electrical Characteristics](#). Data can only be clocked in while the  $\overline{CS}$  chip select pin is active low. For the DAC8812, only the last 18 bits clocked into the serial register are interrogated when the  $\overline{CS}$  pin returns to the logic high state.

Because most microcontrollers output serial data in 8-bit bytes, three right-justified data bytes can be written to the DAC8812. Keeping the  $\overline{CS}$  line low between the first, second, and third byte transfers will result in a successful serial register update.

When the data is properly aligned in the shift register, the positive edge of the  $\overline{CS}$  initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0. For the DAC8812, [Table 1](#), [Table 2](#), [Table 3](#), and [Figure 1](#) define the characteristics of the software serial interface.

**Table 1. Serial Input Register Data Format, Data Loaded MSB First<sup>(1)</sup>**

Bit	B17 (MSB)	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- (1) Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the  $\overline{CS}$  line positive edge returns to logic high. At this point an internally-generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8812 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the LDAC pin can be tied logic low to disable the DAC registers.

**Table 2. Control Logic Truth Table<sup>(1)</sup>**

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
H	X	H	L	H	No effect	Latched data = 8000h	Latched data = 8000h

- (1) ↑+ = Positive logic transition; X = Don't care

**Table 3. Address Decode**

A1	A0	DAC DECODE
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

Figure 34 shows the equivalent logic interface for the key digital control pins for the DAC8812.

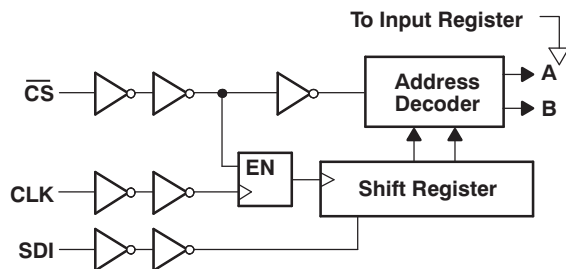


Figure 34. DAC8812 Equivalent Logic Interface

Two additional pins,  $\overline{RS}$  and MSB, provide hardware control over the preset function and DAC register loading. If these functions are not needed, the  $\overline{RS}$  pin can be tied to logic high. The asynchronous input  $\overline{RS}$  pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the midscale state (MSB = 1).

## 9 Application and Implementation

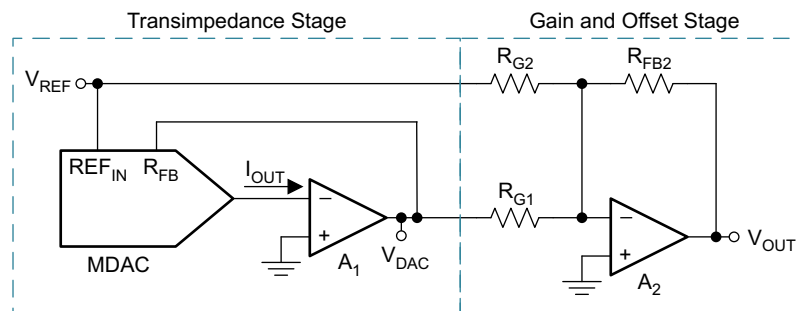
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

This design features one channel of the DAC8812 followed by a four-quadrant circuit for multiplying DACs. The circuit conditions the current output of an MDAC into a symmetrical bipolar voltage. The design uses an op amp in a transimpedance configuration to convert the MDAC current into a voltage, followed by an additional amplifier in a summing configuration to apply an offset voltage.

### 9.2 Typical Application



**Figure 35. Four-Quadrant Multiplying Application Circuit**

#### 9.2.1 Design Requirements

Using a multiplying DAC requires a transimpedance stage using an amplifier with minimal input offset voltage. The tolerance of the external resistors varies depending on the goals of the application, but for optimal performance with the DAC8812 the tolerance should be 0.1% for all of the external resistors. The summing stage amplifier also requires low input-offset voltage and enough slew rate for the output range desired.

#### 9.2.2 Detailed Design Procedure

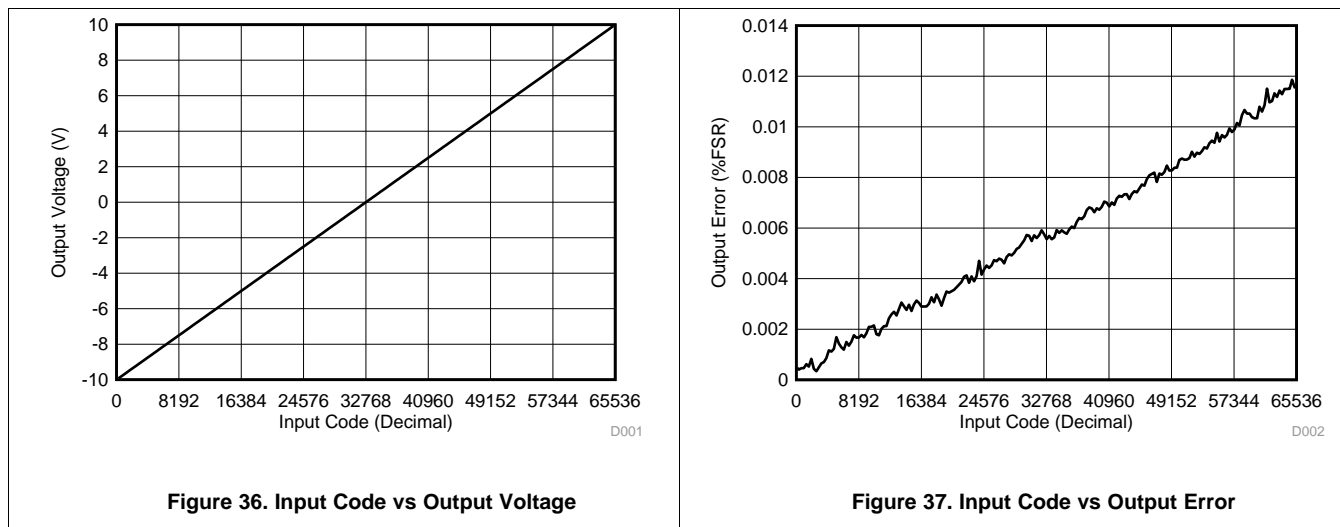
The first stage of the design converts the current output of the MDAC ( $I_{OUT}$ ) to a voltage ( $V_{OUT}$ ) using an amplifier in a transimpedance configuration. A typical MDAC features an on-chip feedback resistor sized appropriately to match the ratio of the resistor values used in the DAC R-2R ladder. This resistor is available using the input shown in Figure 35 called  $R_{FB}$  on the MDAC. The MDAC reference and the output of the transimpedance stage are then connected to the inverting input of the amplifier in the summing stage to produce the output that is defined by Equation 2.

$$V_{OUT}(\text{Code}) = \left( \frac{R_{FB2}}{R_{G1}} \times \frac{V_{REF} \times \text{Code}}{2^{\text{bits}}} \right) - \left( \frac{R_{FB2}}{R_{G2}} \times V_{REF} \right) \quad (2)$$

#### 9.2.3 Application Curves

Figure 36 shows the output voltage vs code of this design, and Figure 37 shows the output error vs code. Notice that the error gets worse as the output code increases because the contribution of the DAC gain error increases with code.

Typical Application (continued)



10 Power Supply Recommendations

This device can operate within the specified supply voltage range of 2.7 V to 5.5 V. The power applied to  $V_{DD}$  should be well-regulated and low-noise. In order to further minimize noise from the power supplies, a strong recommendation is to include a 100-pF to 1-nF capacitor and a 0.1- $\mu$ F to 1- $\mu$ F bypass capacitor very close to the  $V_{DD}$  pin. The current consumption of the  $V_{DD}$  pin, the short-circuit current limit, and the load current for these devices are listed in the [Electrical Characteristics](#) table. Choose a power supply for these devices to meet the aforementioned current requirements.

## 11 Layout

### 11.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC8812 offers single-supply operation, and is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output. This device has three ground pins: two for analog ground ( $A_{GND A}$  and  $A_{GND B}$ ) and one for digital ground (DGND), which are pinned out on opposite sides of the device. Ideally, the analog grounds would be connected directly to an analog ground plane, and similarly the digital ground connected to a digital ground plane. These planes would be separated until they were connected at the power-entry point of the system. The power applied to  $V_{DD}$  should be well-regulated and low-noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.  $V_{DD}$  should be connected to a power-supply plane or trace that is separate from the connection for digital logic until the analog and digital supplies are connected at the power-entry point. In addition, adding both a 100-pF to 1-nF capacitor and a 0.1- $\mu$ F to 1- $\mu$ F bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100- $\mu$ F electrolytic capacitor or even a pi filter made up of inductors and capacitors – all designed essentially to provide low-pass filtering for the supply and remove the high-frequency noise.

The compensation capacitors shown on the layout in [Figure 38](#) are not required for normal operation of the DAC. However, overshoot of the amplifier output voltage on large code changes is possible. This can be mitigated by using a compensation capacitor between the IOUTx and RFBx nodes, as shown implemented here.

Performance of the DAC8812 can be compromised by grounding and PCB lead trace resistance. The 16-bit DAC8812 with a 10-V full-scale range has an LSB size of 153  $\mu$ V. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2-mA current level, a series wiring and connector resistance of only 76 m $\Omega$  causes 1 LSB of voltage drop. The preferred PCB layout for the DAC8812 is to have all AGNDx pins connected directly to an analog ground plane at the device. The noninverting input for the transimpedance amplifier of each channel should also either connect directly to the analog ground plane or have an individual sense trace back to the AGNDx pin connection. The feedback resistor trace to the transimpedance amplifier should also be kept short and have low resistance in order to prevent IR drops from contributing to gain error. Therefore, it is important to place the transimpedance amplifier as close to the DAC as possible. This attention to wiring and placement ensures the optimal performance of the DAC8812.

### 11.2 Layout Example

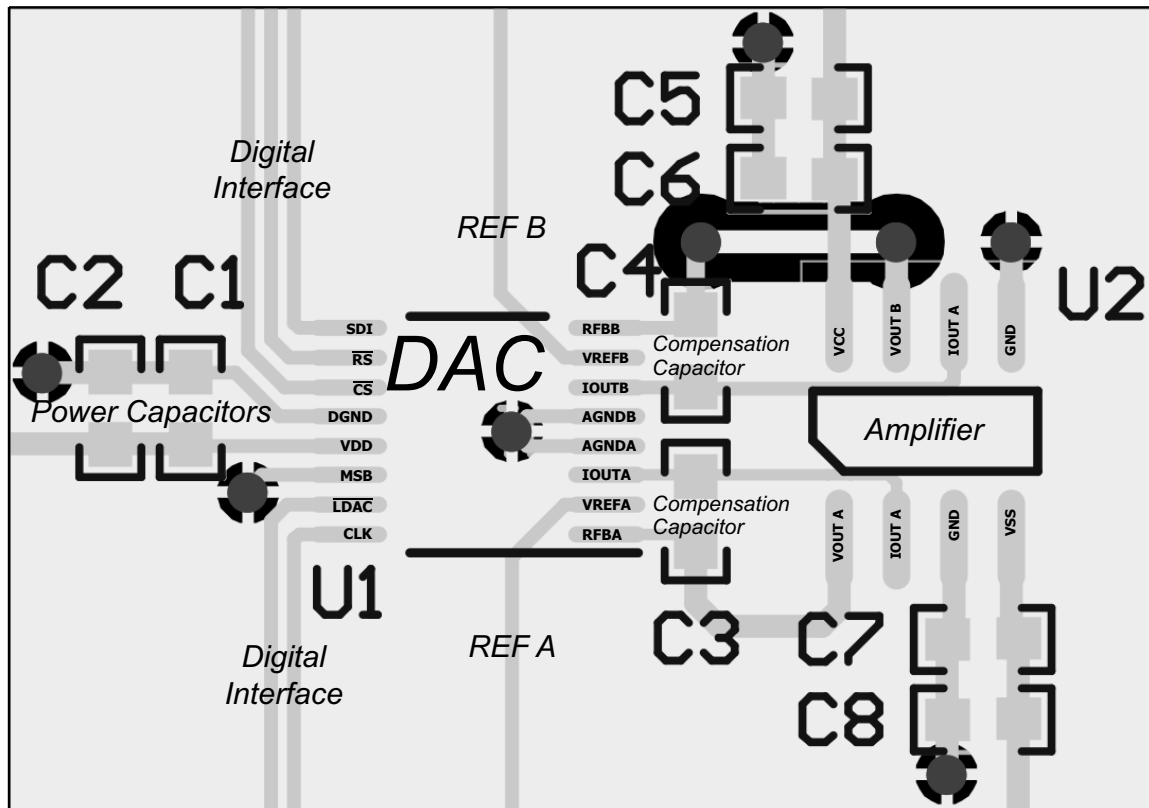


Figure 38. DAC8812 Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[DAC8811 16-Bit, Serial Input Multiplying Digital-to-Analog Converter](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

SPI is a trademark of Motorola, Inc.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8812IBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	<a href="#">Samples</a>
DAC8812IBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	<a href="#">Samples</a>
DAC8812ICPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	<a href="#">Samples</a>
DAC8812ICPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	<a href="#">Samples</a>
DAC8812ICPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8812	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

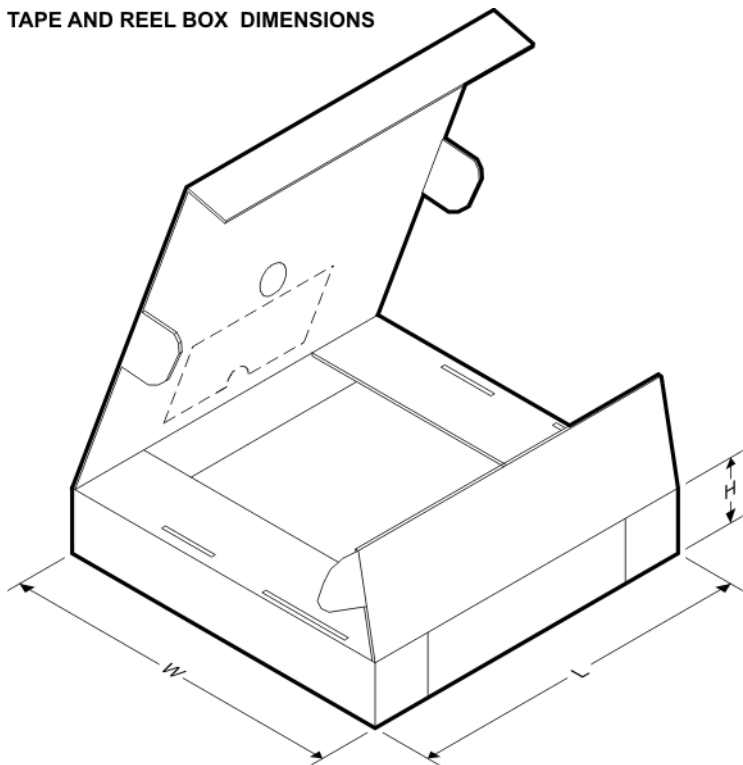


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8812IBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8812ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8812IBPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
DAC8812ICPWR	TSSOP	PW	16	2000	350.0	350.0	43.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View DAC8812IBPW](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management