



**THE DATASHEET OF  
ADA4004-1ARZ-R7**



### FEATURES

**Very low voltage noise: 1.8 nV/ $\sqrt{\text{Hz}}$**   
**Low input bias current: 90 nA maximum**  
**Offset voltage: 125  $\mu\text{V}$  maximum**  
**High gain: 120 dB**  
**Wide bandwidth: 12 MHz**  
 **$\pm 5\text{ V}$  to  $\pm 15\text{ V}$  operation**

### APPLICATIONS

**Precision instrumentation**  
**Filter blocks**  
**Microphone preamplifiers**  
**Industrial control**  
**Thermocouples and RTDs**  
**Reference buffers**

### GENERAL DESCRIPTION

The ADA4004-1/ADA4004-2/ADA4004-4 are 1.8 nV/ $\sqrt{\text{Hz}}$  precision amplifiers featuring 40  $\mu\text{V}$  offset, 0.7  $\mu\text{V}/^\circ\text{C}$  drift, 12 MHz bandwidth, and low 1.7 mA per amplifier supply current.

The ADA4004-1/ADA4004-2/ADA4004-4 are designed on the high performance *iPolar*<sup>™</sup> process, enabling improvements such as reduced noise and power consumption, increased speed and stability, and smaller footprint size. Novel design techniques enable the ADA4004-1/ADA4004-2/ADA4004-4 to achieve 1.8 nV/ $\sqrt{\text{Hz}}$  voltage noise density and a low 6 Hz 1/f noise corner frequency while consuming just 1.7 mA per amplifier. The small package saves board space, reduces cost, and improves layout flexibility.

Applications for these amplifiers include high precision controls, PLL filters, high performance precision filters, medical and analytical instrumentation, precision power supply controls, ATE, and data acquisition systems. Operation is fully specified from  $\pm 5\text{ V}$  to  $\pm 15\text{ V}$  from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

The ADA4004-1, ADA4004-2, and ADA4004-4 are members of a growing series of low noise op amps offered by Analog Devices, Inc., (see Table 1).

Table 1. Voltage Noise

Pkg.	0.9 nV	1.1 nV	1.8 nV	2.8 nV	3.8 nV
Single	AD797	AD8597	ADA4004-1	AD8675	AD8671
Dual		AD8599	ADA4004-2	AD8676	AD8672
Quad			ADA4004-4		AD8674

### PIN CONFIGURATIONS

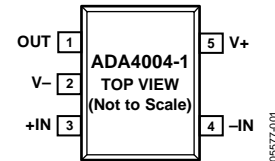


Figure 1. 5-Lead SOT (RJ-5)

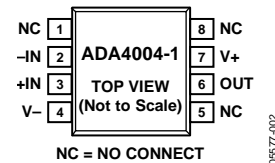


Figure 2. 8-Lead SOIC (R-8)

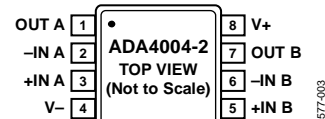


Figure 3. 8-Lead MSOP (RM-8) and 8-Lead SOIC (R-8)

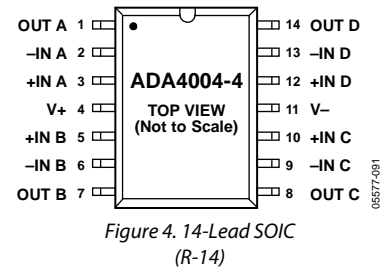
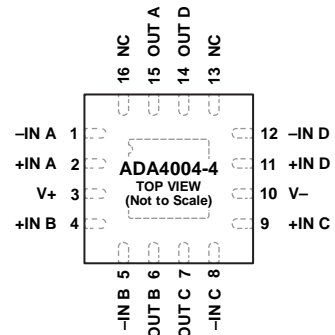


Figure 4. 14-Lead SOIC (R-14)



**NOTES**  
 1. NC = NO CONNECT.  
 2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V-.

Figure 5. 16-Lead LFCSP (CP-16-23)

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**REVISION HISTORY**

**7/15—Rev. G to Rev. H**

Changed CP-16-4 to CP-16-23 and Changed LFCSP\_VQ to LFCSP\_WQ ..... Throughout  
 Changes to Figure 5..... 1  
 Changed Differential Input Voltage Parameter, Table 4..... 5  
 Updated Outline Dimensions ..... 12  
 Changes to Ordering Guide ..... 15

**4/11—Rev. F to Rev. G**

Changes to Figure 1 ..... 1  
 Updated Outline Dimensions ..... 12

**6/10—Rev. E to Rev. F**

Added Differential Input Current to Table 4 ..... 5  
 Changes to Figure 14 and Figure 17 ..... 7

**10/09—Rev. D to Rev. E**

Changes to Product Title, General Description Section, and Figure 5 ..... 1  
 Updated Outline Dimensions (RM-8)..... 13  
 Changes to Ordering Guide ..... 14

**6/09—Rev. C to Rev. D**

Changes to Figure 5..... 1

**10/08—Rev. B to Rev. C**

Added ADA4004-1 and ADA4004-2 ..... Universal  
 Added 5-Lead SOT, 8-Lead SOIC, and 8-Lead MSOP ..... Universal  
 Changes to Features Section ..... 1  
 Added Figure 1 to Figure 3; Renumbered Sequentially..... 1  
 Changes to General Description Section ..... 1

Added Table 1; Renumbered Sequentially ..... 1  
 Change to Output Voltage Low Parameter, Table 2..... 3  
 Changes to Supply Current per Amplifier Parameter, Table 2 ..... 3  
 Added Phase Margin Parameter, Table 2..... 3  
 Change to Output Voltage Low Parameter, Table 3..... 3  
 Changes to Supply Current per Amplifier Parameter, Table 3 ..... 4  
 Added Phase Margin Parameter, Table 3..... 4  
 Changes to Table 4 ..... 5  
 Changes to Thermal Resistance Section..... 5  
 Changes to Table 5 ..... 5  
 Update Outline Dimensions..... 12  
 Changes to Ordering Guide..... 13

**11/07—Rev. A to Rev. B**

Changed  $V_S$  to  $V_{SY}$  ..... Universal  
 Changes to General Description ..... 1  
 Changes to Supply Current per Amplifier ..... 3  
 Changes to Open-Loop Gain ..... 4  
 Changes to Supply Current per Amplifier ..... 4  
 Changes to Figure 10, Figure 11, Figure 13, and Figure 14..... 7  
 Changes to Figure 26..... 9  
 Updated Outline Dimensions ..... 12  
 Changes to Ordering Guide ..... 12

**7/06—Rev. 0 to Rev. A**

Changes to Table 4..... 5  
 Updated Outline Dimensions ..... 12  
 Changes to Ordering Guide ..... 12

**1/06—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{SY} = \pm 5\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	140	$\mu\text{V}$
					300	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
					165	nA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	85	nA
					100	nA
Input Voltage Range	IVR		-3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.0\text{ V to }+3.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		105	111	dB
				95	110	dB
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_{OUT} = -2.5\text{ V to }+2.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		250	400	V/mV
				170		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1	$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		3.7	3.9	V
				3.4	3.6	V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		-3.6	-3.55	V
				-3.6	-3.4	V
Short-Circuit Limit	$I_{SC}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25		mA
Output Current	$I_O$	$V_{OUT} = \pm 3.6\text{ V}$		$\pm 10$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5\text{ V to } \pm 15\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		110	118	dB
				110		dB
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.0	mA
					2.2	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	$\Phi_M$			48		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.1		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		1.8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		3.5		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 200\text{ Hz}$		1.2		pA/ $\sqrt{\text{Hz}}$

$V_{SY} = \pm 15\text{ V}$ ,  $V_{CM} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	125	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	270	$\mu\text{V}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			90	nA
Input Voltage Range	IVR	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			165	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5\text{ V to }+12.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-12.5	113	+12.5	V
Open-Loop Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_{OUT} = -12.0\text{ V to }+12.0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	104		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	250	500		dB
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.4	13.6		V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	13.1	13.3		V
Short-Circuit Limit	$I_{SC}$			25		mA
Output Current	$I_O$	$V_{OUT} = \pm 13.6\text{ V}$		$\pm 10$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5\text{ V to } \pm 15\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	118		dB
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110		2.2	dB
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ to ground		2.7		$\text{V}/\mu\text{s}$
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	$\Phi_M$			48		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_{n,p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		0.15		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		1.8		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		3.5		$\text{pA}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 200\text{ Hz}$		1.2		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$ or $+36\text{ V}$
Input Voltage	$V^- < V_{IN} < V^+$
Differential Input Voltage	$\pm 600\text{ mV}$
Differential Input Current	$\pm 5\text{ mA}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	$300^\circ\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard printed circuit board with zero airflow.

Table 5.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
5-Lead SOT (RJ-5)	230	92	$^\circ\text{C}/\text{W}$
8-Lead SOIC (R-8), <a href="#">ADA4004-1</a>	177	53	$^\circ\text{C}/\text{W}$
8-Lead SOIC (R-8), <a href="#">ADA4004-2</a>	155	45	$^\circ\text{C}/\text{W}$
8-Lead MSOP (RM-8)	186	52	$^\circ\text{C}/\text{W}$
14-Lead SOIC_N (R-14)	115	36	$^\circ\text{C}/\text{W}$
16-Lead LFCSP_VQ (CP-16-4)	44	31.5	$^\circ\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

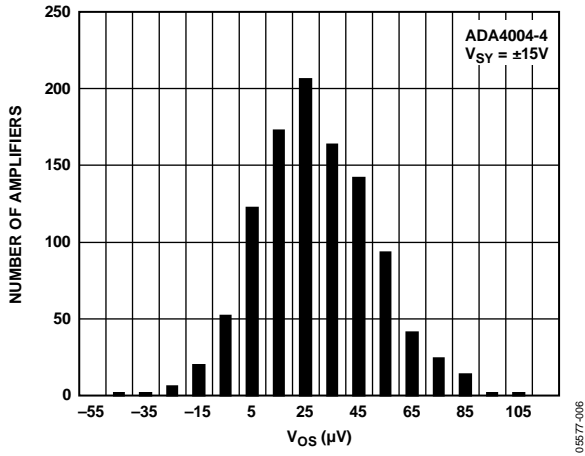


Figure 6. Number of Amplifiers vs. Input Offset Voltage

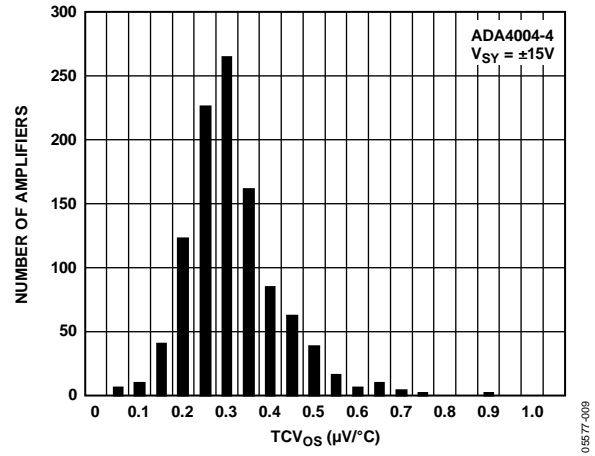


Figure 9. Number of Amplifiers vs. TCV<sub>os</sub>

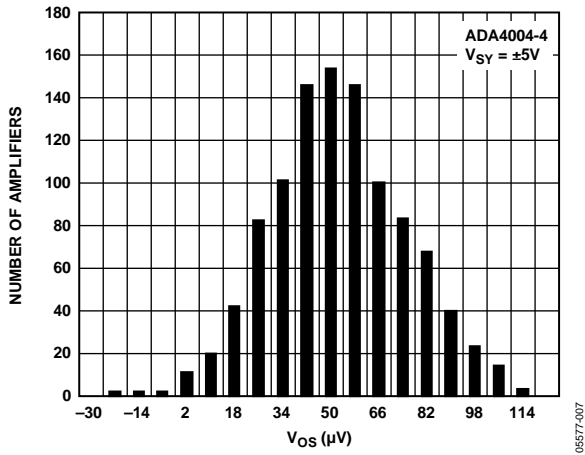


Figure 7. Number of Amplifiers vs. Input Offset Voltage

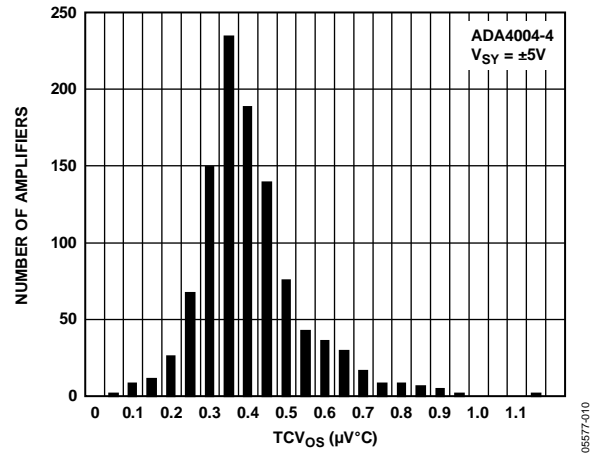


Figure 10. Number of Amplifiers vs. TCV<sub>os</sub>

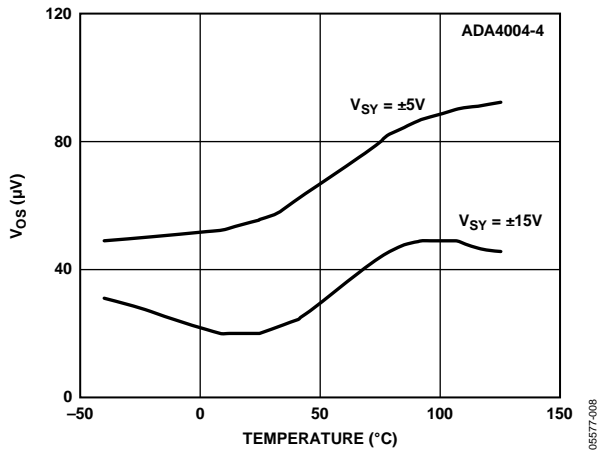


Figure 8. Input Offset Voltage vs. Temperature

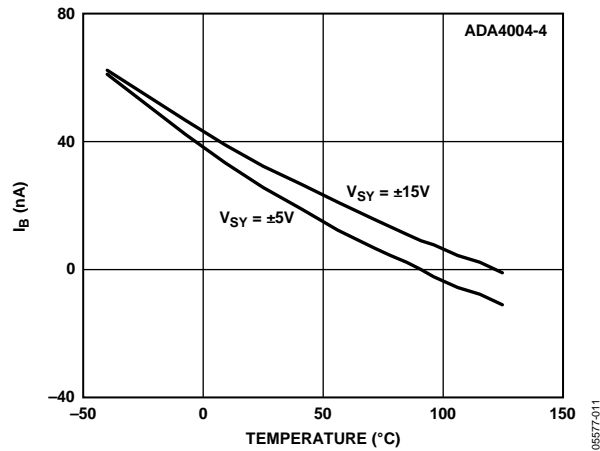


Figure 11. Input Bias Current vs. Temperature

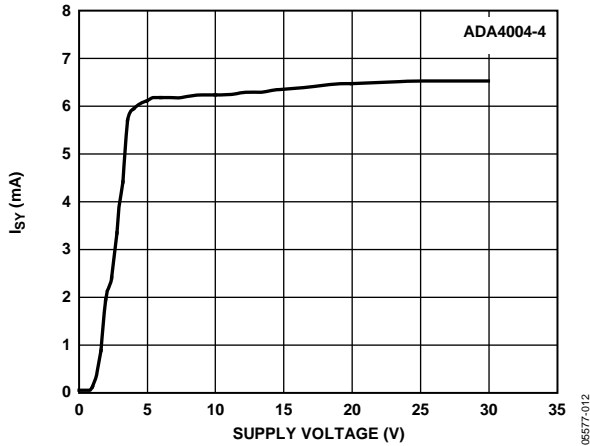


Figure 12. Supply Current vs. Total Supply Voltage

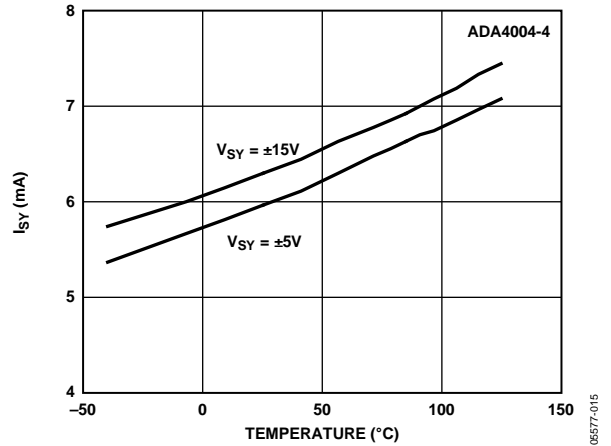


Figure 15. Supply Current vs. Temperature

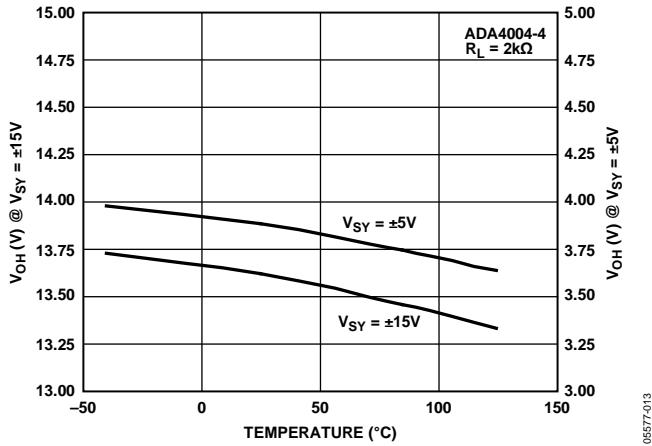


Figure 13.  $V_{OH}$  vs. Temperature

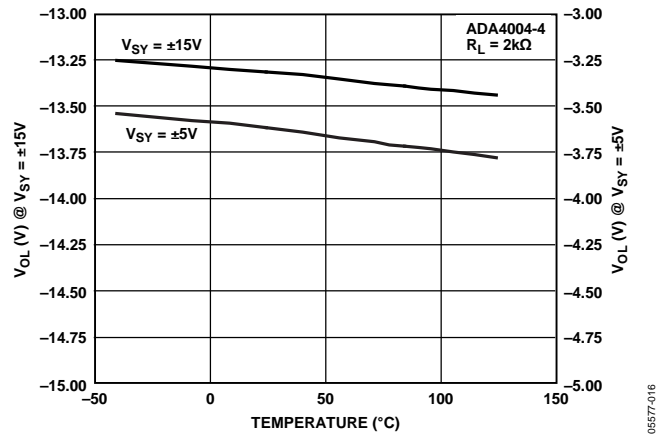


Figure 16.  $V_{OL}$  vs. Temperature

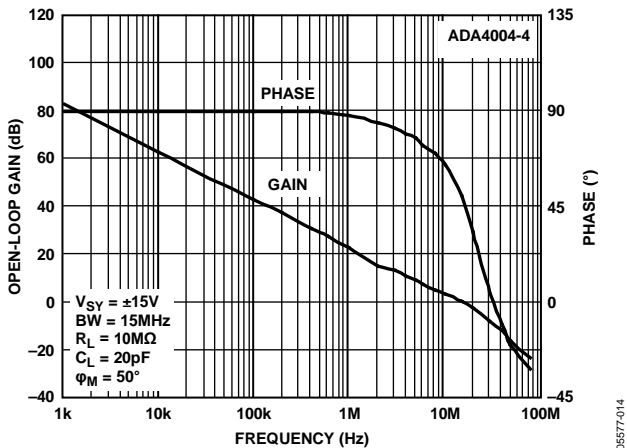


Figure 14. Open-Loop Gain and Phase vs. Frequency

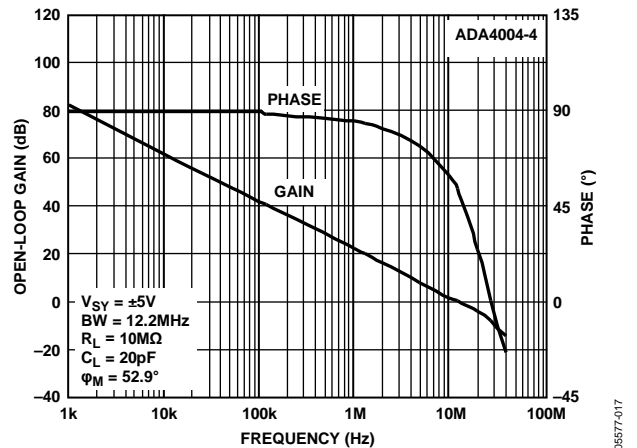


Figure 17. Open-Loop Gain and Phase vs. Frequency

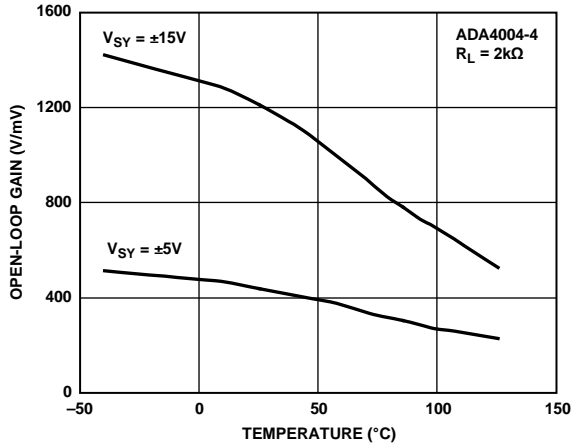


Figure 18. Open-Loop Gain vs. Temperature

06577-018

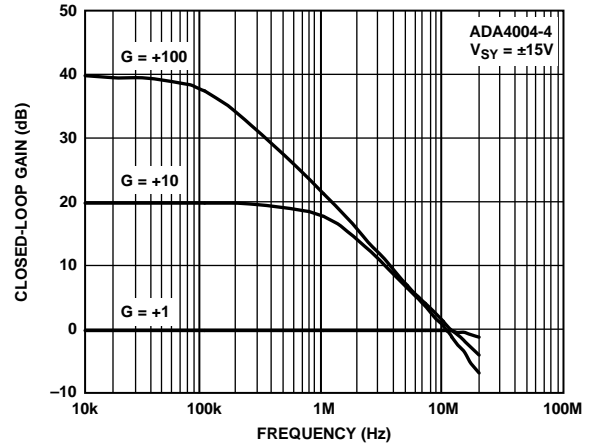


Figure 21. Closed-Loop Gain vs. Frequency

06577-021

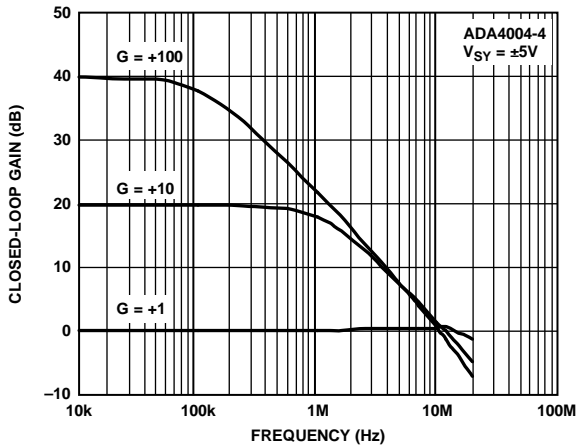


Figure 19. Closed-Loop Gain vs. Frequency

06577-019

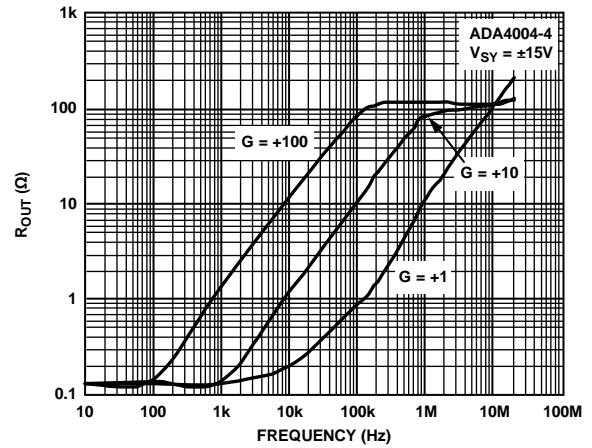


Figure 22. Output Impedance vs. Frequency

06577-022

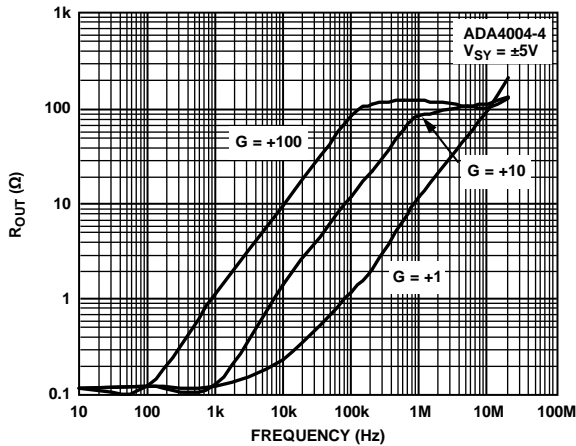


Figure 20. Output Impedance vs. Frequency

06577-020

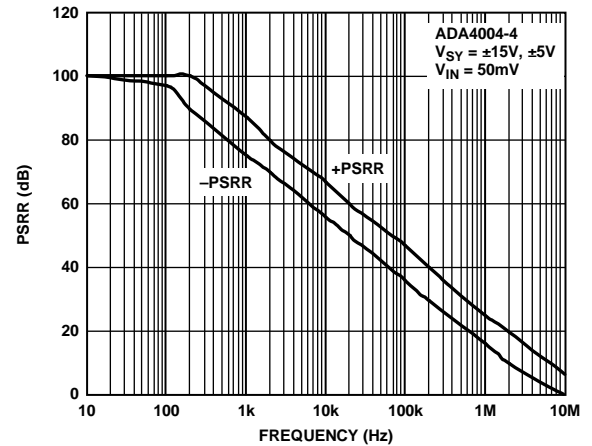


Figure 23. PSRR vs. Frequency

06577-023

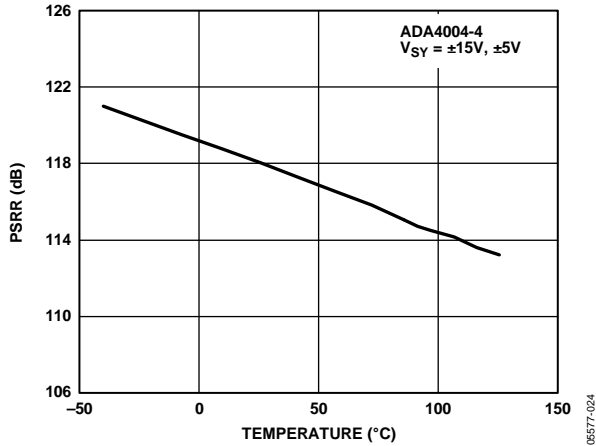


Figure 24. PSRR vs. Temperature

05577-024

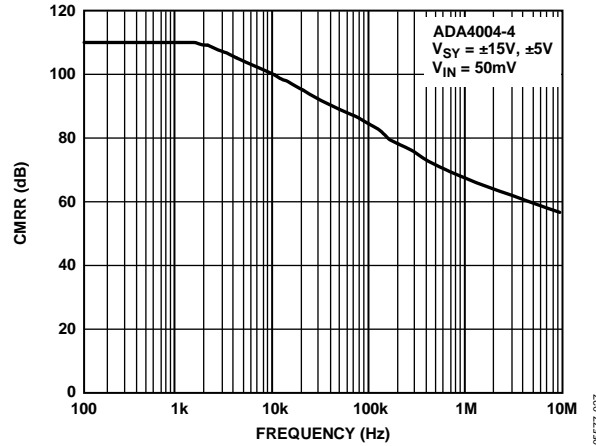


Figure 27. CMRR vs. Frequency

05577-027

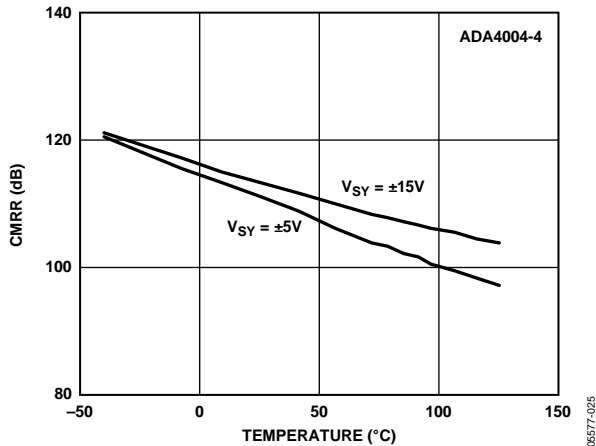


Figure 25. CMRR vs. Temperature

05577-025

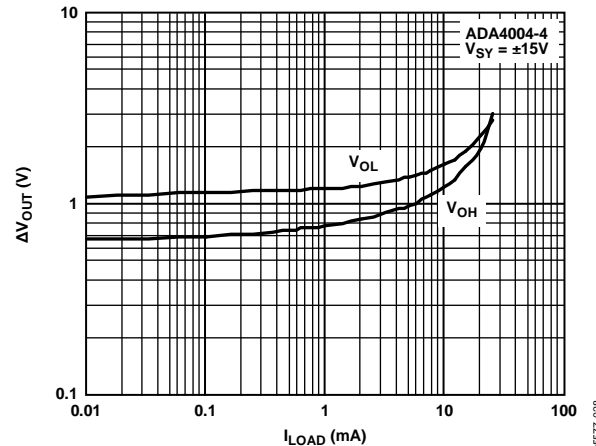


Figure 28. Output Voltage vs. Current Load

05577-028

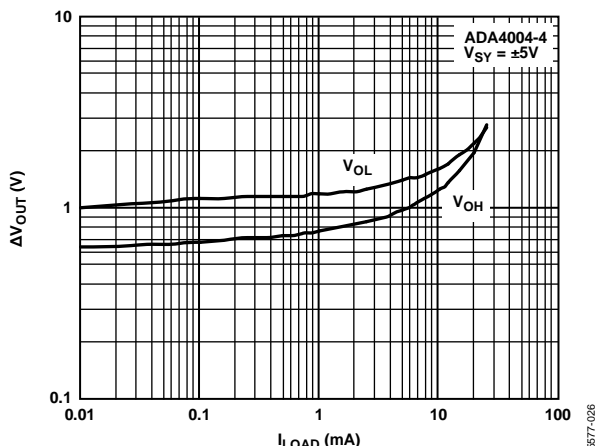


Figure 26. Output Voltage vs. Current Load

05577-026

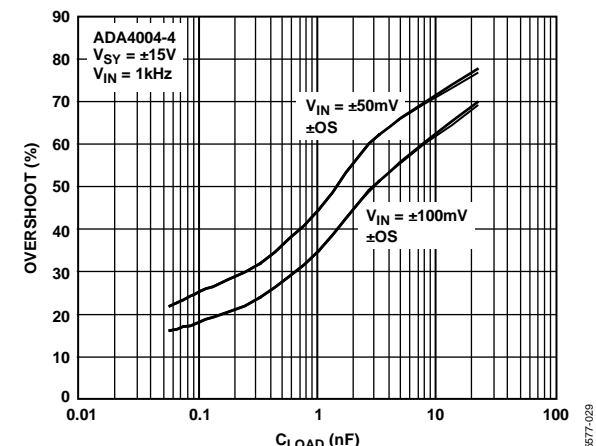


Figure 29. Small-Signal Overshoot vs. Capacitive Load

05577-029

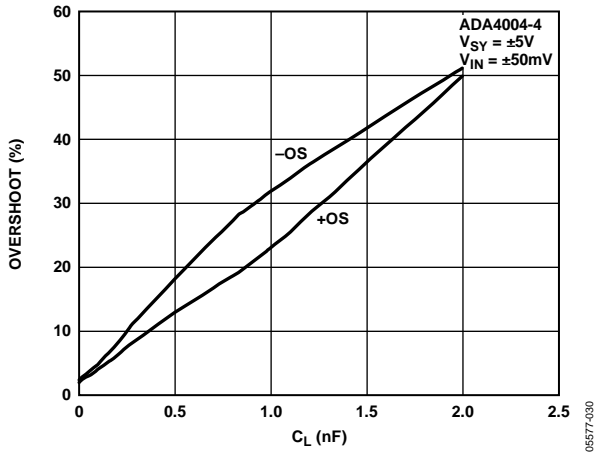


Figure 30. Small-Signal Overshoot vs. Capacitive Load

05577-030

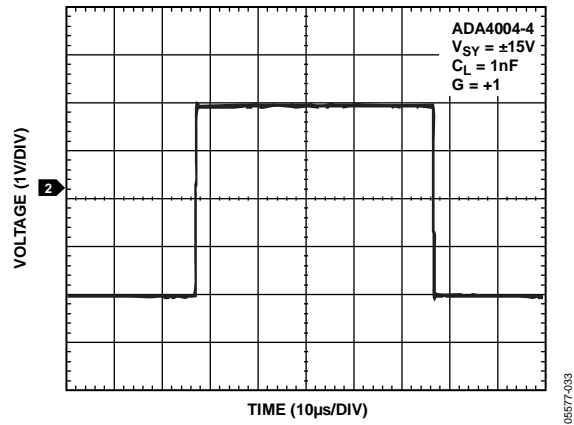


Figure 33. Large-Signal Transient Response

05577-033

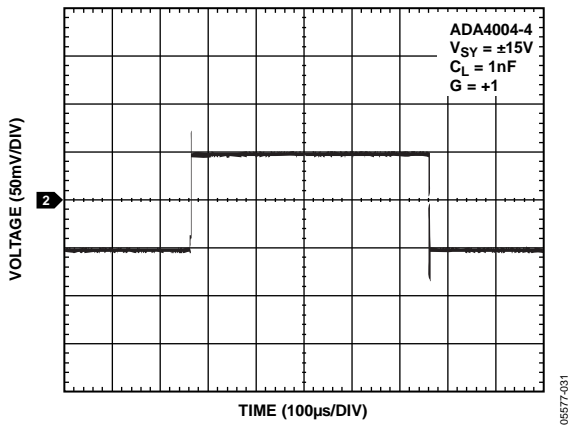


Figure 31. Small-Signal Transient Response

05577-031

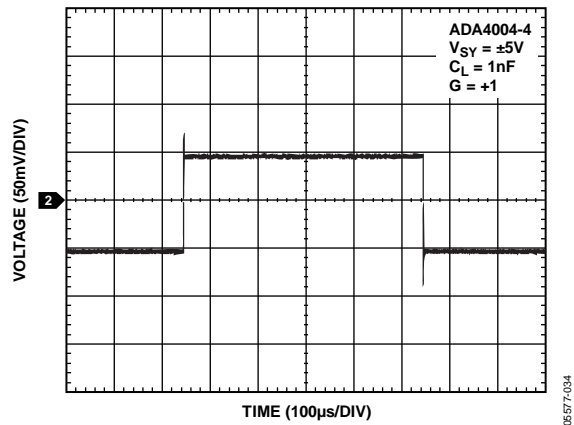


Figure 34. Small-Signal Transient Response

05577-034

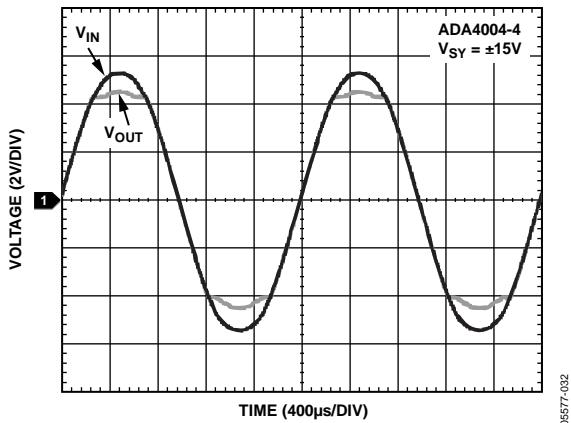


Figure 32. No Phase Reversal

05577-032

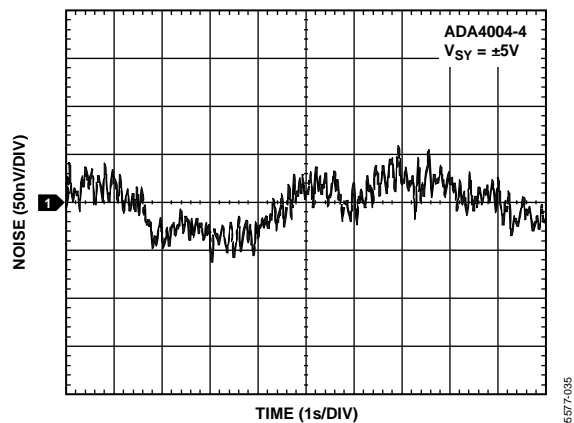


Figure 35. Voltage Noise (0.1 Hz to 10 Hz)

05577-035

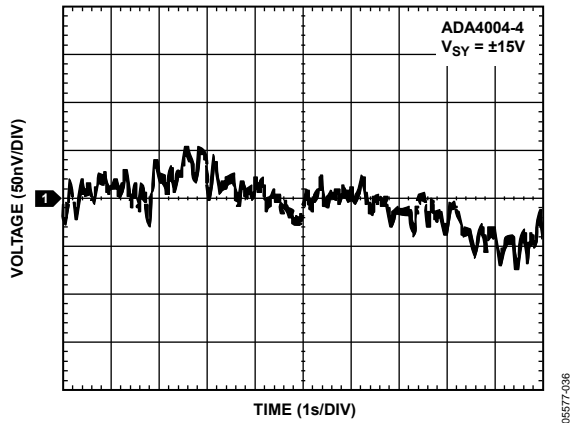


Figure 36. Voltage Noise (0.1 Hz to 10 Hz)

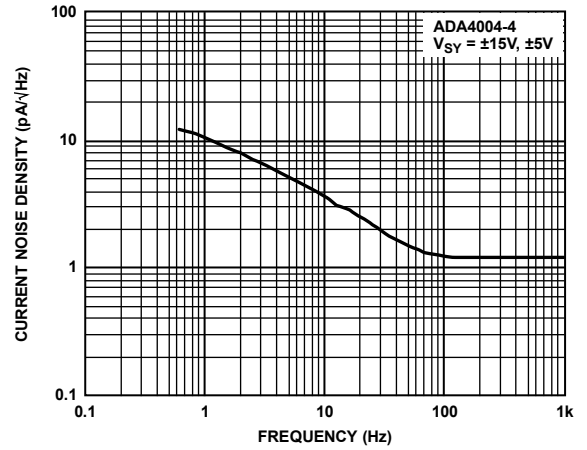


Figure 38. Current Noise Density vs. Frequency

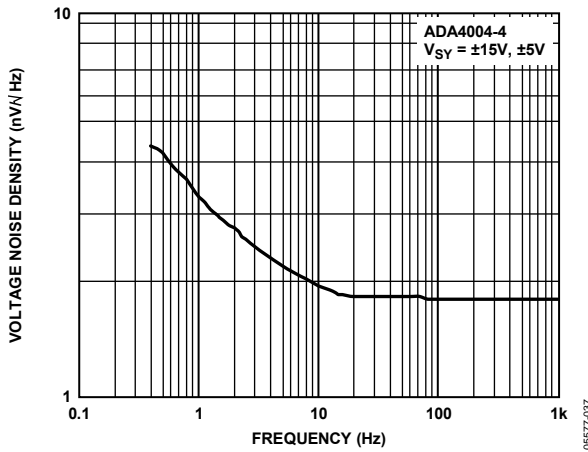


Figure 37. Voltage Noise Density vs. Frequency

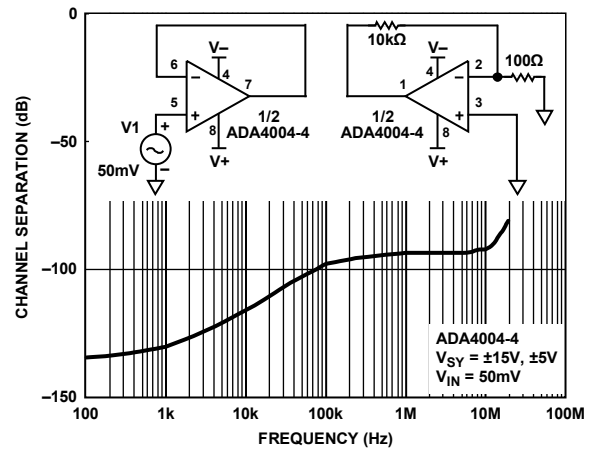
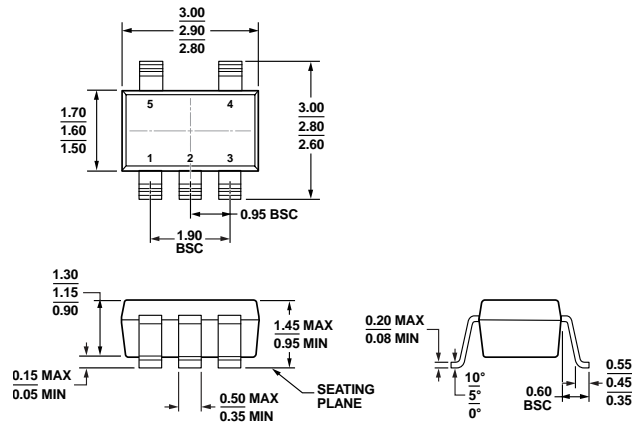


Figure 39. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

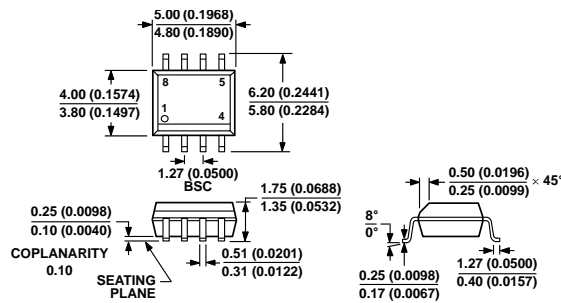


COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 40. 5-Lead Small Outline Transistor Package [SOT-23] (RJ-5)

Dimensions shown in millimeters

11-01-2010-A



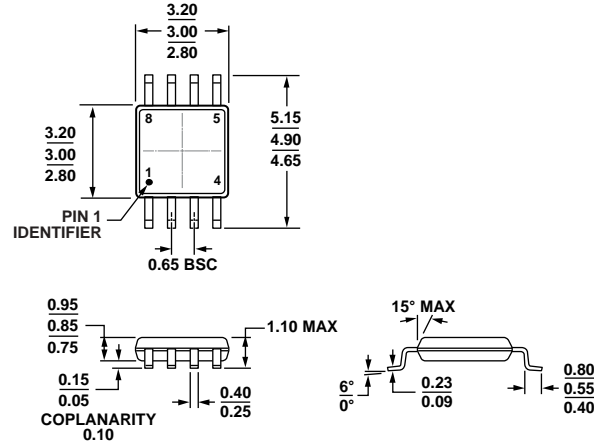
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 41. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012607-A

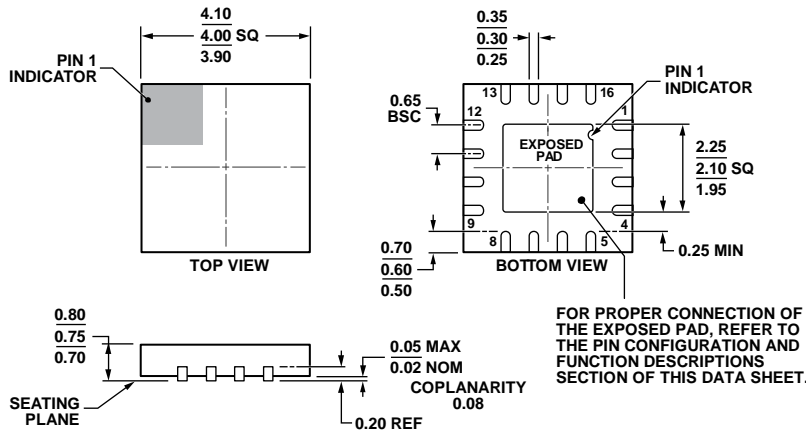


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 42. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B

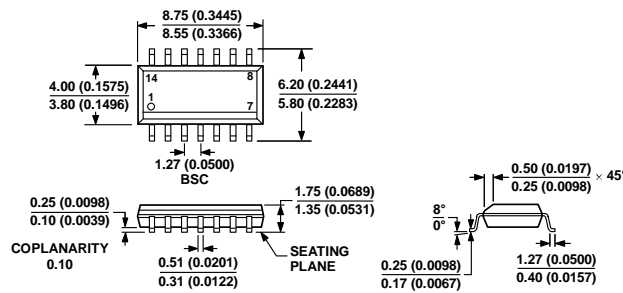


COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 43. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ] 4 mm x 4 mm Body, Very Very Thin Quad (CP-16-23)

Dimensions shown in millimeters

111986-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 44. 14-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

0001006-A

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADA4004-1ARJZ-R2	-40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-R7	-40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-RL	-40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-RL	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARMZ	-40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-RL	-40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-R7	-40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-RL	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-4ACPZ-R2	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ACPZ-R7	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ACPZ-RL	-40°C to +125°C	16-Lead LFCSP_WQ	CP-16-23	
ADA4004-4ARZ	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-R7	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-RL	-40°C to +125°C	14-Lead SOIC_N	R-14	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

NOTES

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View ADA4004-1ARZ-R7 on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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