THE DATASHEET OF

AD8260ACPZ-WP

High Current Driver Amplifier and Digital VGA/Preamplifier with 3 dB Steps

Data Sheet **AD8260**

FEATURES

- **High current driver**
  - **Differential input—direct drive from DAC**
  - **Preset gain: 1.5×**
  - **−3 dB bandwidth: 195 MHz**
  - **Large output drive: >±300 mA**
- **VGA/preamplifier**
  - **Low noise**
    - **Voltage noise: 2.4 nV/√Hz**
    - **Current noise: 5 pA/√Hz**
  - **−3 dB bandwidth: 230 MHz**
  - **Gain range: 30 dB in 3 dB steps**
    - **−6 dB to +24 dB (for preamplifier gain of 6 dB)**
  - **Single-ended preamplifier input and differential VGA output**
- **Supplies: 3.3 V to 10 V (with VMID enabled)**
  - **±3.3 V to ±5 V (with VMID disabled)**
- **Power: 93 mW with 3.3 V supplies**
  - **Power-down for VGA, driver amplifier, and system**

APPLICATIONS

Digital AGC systems
Tx/Rx signal processing
Power line transceivers

FUNCTIONAL BLOCK DIAGRAM

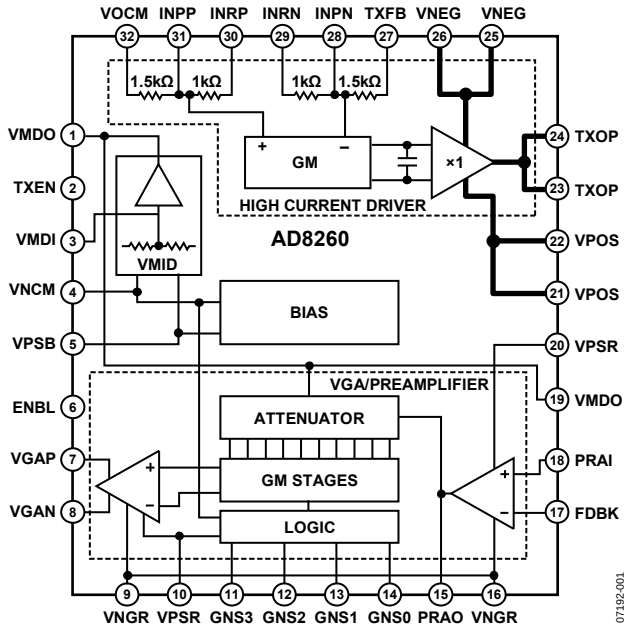

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8260 includes a high current driver, usable as a transmitter, and a low noise digitally programmable variable gain amplifier (DGA), useable as a receiver.

The receiver section consists of a single-ended input preamplifier, and linear-in-dB, differential-output DGA. The receiver has a small signal −3 dB bandwidth of 230 MHz; the driver small signal bandwidth is 195 MHz. The driver delivers ±300 mA, well suited for driving low impedance loads, even when connected to a 3.3 V supply.

The AD8260 DGA is ideal for trim applications and has a gain span of 30 dB, in 3 dB steps. Excellent bandwidth uniformity is maintained across the entire frequency range. The low output-referred noise of the DGA is advantageous in driving high speed ADCs. The differential output facilitates the interface to modern low voltage high speed ADCs.

Single-supply and dual-supply operation makes the part versatile and enables gain control of negative-going pulses, such as those generated by photodiodes or photo-multiplier tubes, as well as processing band-pass signals on a single supply. For maximum dynamic range, it is essential that the part be ac-coupled when operating on a single supply.

The AD8260 preamplifier (PrA) is configured with external resistors for gains greater than 6 dB and can be inverting or noninverting. The DGA is characterized with a noninverting preamplifier gain of 2×. The attenuator has a range of 30 dB and the output amplifier has a gain of 8× (18.06 dB). The lowest noninverting gain range is −6 dB to +24 dB and shifts up with increased preamplifier gain. The gain is controlled via a parallel port (Pin GNS0 to Pin GNS3) with 10 gain steps of 3 dB per code. The preamplifier and DGA are disabled for any code that is not assigned a gain step.

The AD8260 can operate with single or dual supplies from 3.3 V to ±5 V. An internal buffer normally provides a split supply reference for single-supply operation; an external reference can also be used when the VMID buffer is shut down.

The operating temperature range is −40°C to +105°C. The AD8260 is available in a 5 mm × 5 mm, 32-lead LFCSP.

Rev. B **Document Feedback**

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5/08—Revision 0: Initial Version

SPECIFICATIONS

V_S (supply voltage) = 3.3 V, T_A = 25°C, preamplifier gain = 2× (R_{FB1} = R_{FB2} = 100 Ω), V_{VMDO} = V_S/2, f = 10 MHz, C_L = 5 pF, R_{LOAD} = 500 Ω, DGA differential output. All dBm values are referenced to 50 Ω, gain code 1011, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DRIVER AMPLIFIER—GENERAL PARAMETERS					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p, R_{LOAD} = 500 Ω		195		MHz
	V_{OUT} = 10 mV p-p, R_{LOAD} = 50 Ω		120		MHz
	V_{OUT} = 10 mV p-p, R_{LOAD} = 10 Ω		85		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p		195		MHz
	V_{OUT} = 2 V p-p		190		MHz
	V_{OUT} = 2 V p-p, R_{LOAD} = 50 Ω		180		MHz
Slew Rate	V_{OUT} = 1 V p-p		730		V/µs
	V_{OUT} = 2 V p-p		725		V/µs
	V_{OUT} = 2 V p-p, R_{LOAD} = 50 Ω		620		V/µs
Gain	Nominal gain with internal gain setting resistors	3.0	3.52		dB
Input Voltage Noise	f = 10 MHz		9.5		nV/√Hz
Noise Figure	R_S = 100 Ω (differential, 2 × 50 Ω that convert differential DAC output currents to differential voltage)		17.6		dB
Output-Referred Noise	Gain = 3.52 dB (1.5×), includes internal gain setting resistors		14.3		nV/√Hz
Output Impedance	DC to 10 MHz, V_S = ±3.3 V		≤1.7		Ω
Output Current	R_{LOAD} = 1 Ω, V_{IN} = ±0.5 V		±310		mA
Output Signal Range	R_{LOAD} ≥ 500 Ω		V_{MDO} ± 1.5		V
	V_S = +5 V		V_{MDO} ± 2.3		V
	V_S = ±5 V		±4.7		V
Input Signal Range	Differential input signal		2		V p-p
Output Offset Voltage	Gain = 3.52 dB (1.5×), maximum and minimum limits are 3σ	−20	±5	+20	mV
DRIVER AMPLIFIER—DYNAMIC PERFORMANCE					
Harmonic Distortion	V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−84		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−83		dBc
HD3			−70		dBc
Harmonic Distortion	V_{OUT} = 2 V p-p				
HD2	f = 1 MHz		−78		dBc
HD3			−76		dBc
HD2	f = 10 MHz		−70		dBc
HD3			−58		dBc
Input 1 dB Compression Point			13		dBm
Multitone Power Ratio (MTPR, In-Band)	R_{LOAD} = 50 Ω, V_{OUT} = 1.4 V p-p max, 10 tones, 2 MHz to 22 MHz with missing tone at 12 MHz (spacing 2 MHz)		−49		dBc
	R_{LOAD} = 50 Ω, V_{OUT} = 1.4 V p-p max, 16 tones, 2 MHz to 38 MHz with missing tones at 10 MHz, 20 MHz, 30 MHz, and 40 MHz (spacing 2 MHz)		−43		dBc
Two-Tone Intermodulation Distortion (IMD3)	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−90		dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−71		dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−60		dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−48		dBc
Output Third-Order Intercept	V_{OUT} = 1 V p-p, f = 10 MHz		43		dBm
	V_{OUT} = 2 V p-p, f = 10 MHz		40		dBm
	V_{OUT} = 1 V p-p, f = 45 MHz		28		dBm
	V_{OUT} = 2 V p-p, f = 45 MHz		28		dBm
Two-Tone Intermodulation Distortion (IMD3), R_{LOAD} = 50 Ω	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−69		dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−72		dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−51		dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−48		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Third-Order Intercept, R_{LOAD} = 50 Ω	V_{OUT} = 1 V p-p, f = 10 MHz		33		dBm
	V_{OUT} = 2 V p-p, f = 10 MHz		40		dBm
	V_{OUT} = 1 V p-p, f = 45 MHz		23		dBm
	V_{OUT} = 2 V p-p, f = 45 MHz		28		dBm
PREAMPLFIER AND VGA—GENERAL PARAMETERS					
−3 dB Small Signal Bandwidth	V_{OUT} = 10 mV p-p, gain code = 0110		230		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p, gain code = 0110		165		MHz
	V_{OUT} = 2 V p-p, gain code = 0110		135		MHz
Slew Rate	V_{OUT} = 1 V p-p, gain code = 0110		330		V/µs
	V_{OUT} = 1.6 V p-p, gain code = 0110		335		V/µs
Input Voltage Noise	f = 10 MHz (shorted input)		2.4		nV/√Hz
	f = 10 MHz (input open)		6.2		nV/√Hz
Noise Figure	Maximum gain (gain code = 1011), R_S = 50 Ω, unterminated		10.2		dB
	Maximum gain (gain code = 1011), R_S = 50 Ω, shunt terminated with 50 Ω		15.5		dB
Output-Referred Noise	Maximum gain (gain code = 1011), gain = 24 dB (input short)		38		nV/√Hz
	Maximum gain (gain code = 1011), gain = 24 dB (input open)		98.1		nV/√Hz
	Minimum gain (gain code = 0001), gain = −6 dB		25		nV/√Hz
Output Impedance	DC to 10 MHz		≤3		Ω
Output Signal Range (per Pin)	R_{LOAD} ≥ 500 Ω		V_{MDO} ± 0.7		V
	V_S = +5 V		V_{MDO} ± 1.4		V
	V_S = ±5 V		±3.6		V
Input Signal Range	Preamplifier input		V_{MDO} ± 0.3		V
Output Offset Voltage	Maximum gain (gain code = 1011), gain = 24 dB, 3 σ limits	−50	±20	+50	mV
PREAMPLIFIER AND VGA—DYNAMIC PERFORMANCE					
Harmonic Distortion	Gain code = 0110, gain = 9 dB, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−90		dBc
HD3			−87		dBc
HD2	f = 10 MHz		−75		dBc
HD3			−58		dBc
Harmonic Distortion	Gain code = 1011, gain = 24 dB, V_{OUT} = 2 V p-p				
HD2	f = 1 MHz		−94		dBc
HD3			−90		dBc
HD2	f = 10 MHz		−61		dBc
HD3			−84		dBc
Input 1 dB Compression Point	Minimum gain (gain code = 0001), gain = −6 dB (preamplifier limited)		1.9		dBm
	Maximum gain (gain code = 1011), gain = 24 dB (VGA limited)		−9.2		dBm
MTPR (In-Band)	V_{OUT} = 1.4 V p-p maximum, 10 tones, 2 MHz to 22 MHz with missing tone at 12 MHz (spacing 2 MHz), gain code = 1011, gain = 24 dB		−68		dBc
	V_{OUT} = 1.4 V p-p maximum, 16 tones, 2 MHz to 38 MHz with missing tones at 10 MHz, 20 MHz, 30 MHz, and 40 MHz (spacing 2 MHz)		−61		dBc
Two-Tone Intermodulation Distortion (IMD3)	Gain code = 1011, gain = 24 dB				
	V_{OUT} = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−92		dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−77		dBc
	V_{OUT} = 1 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−50		dBc
	V_{OUT} = 2 V p-p, f_1 = 45 MHz, f_2 = 46 MHz		−36		dBc
Output Third-Order Intercept	Gain code = 1011, gain = 24 dB				
	V_{OUT} = 1 V p-p, f = 10 MHz		44		dBm
	V_{OUT} = 2 V p-p, f = 10 MHz		43		dBm
	V_{OUT} = 1 V p-p, f = 45 MHz		27		dBm
	V_{OUT} = 2 V p-p, f = 45 MHz		22		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Overload Recovery	Maximum gain (gain code = 1011), gain = 24 dB, V_{IN} = 50 mV p-p to 500 mV p-p		50		ns
Group Delay Variation	1 MHz < f < 50 MHz, full gain range		2		ns
ACCURACY					
Absolute Gain Error	All gain codes, limits are 3σ	−0.5	±0.15	+0.5	dB
Gain Law Conformance (DNL)	Differential gain error, code to code	−0.3	±0.15	+0.3	dB
GAIN CONTROL					
Gain Step per Code			3.0		dB
Gain Range	Default = −6 dB to +24 dB		30		dB
Response Time	30 dB gain change (gain code stepped from 0001 to 1011)		50		ns
LOGIC INTERFACES					
High Level Input Voltage		1.4		V_S	V
Low Level Input Voltage		0		0.8	V
Logic Input Bias Current	Logic high, V_{LOGIC} = 3.3 V		0.2		µA
	Logic low		18		nA
POWER SUPPLY					
Supply Voltage	Single supply	3.3		10	V
	Dual supply	±3.3		±5	V
Quiescent Current	Full chip enabled (TXEN = 1, ENBL = 1, gain code = 0001)		28.3		mA
	TXEN = 0, ENBL = 1, gain code = 0001, driver off, DGA on		19.1		mA
	TXEN = 1, ENBL = 1, gain code = 0000, driver on, DGA off		10.8		mA
	Chip disabled (TXEN = 0, ENBL = 0, gain code = 0000)		35		µA
	V_S = ±5 V, no signal		34.2		mA
PSRR	Maximum gain (gain code = 1011), gain = 24 dB, 1 MHz		−30		dB
	Driver amplifier, 1 MHz		−48		dB
Power Dissipation	No signal		93		mW
	No signal, $V_{POS} - V_{NEG}$ = 10 V		342		mW
ENABLE TIMES					
Chip Enable Time	Bias only, TXEN = 0, gain code = 0000, ENBL = 0 to 1		0.4		µs
	All at once, TXEN = 0 to 1, gain code = 0000 to 0001, ENBL = 0 to 1		0.3		µs
Preamplifier and DGA Enable Time	ENBL = 1, TXEN = 0, gain code = 0000 to 0001		0.3		µs
Driver Enable Time	ENBL = 1, gain code = 0001, TXEN stepped from 0 to 1		0.2		µs
DISABLE TIMES					
Chip Disable Time	TXEN = 1 to 0, gain code = 0001 to 0000, ENBL = 1 to 0, I_{SUPPLY} = 100 µA		20		µs
	All at once, TXEN = 1 to 0, gain code = 0001 to 0000, ENBL = 1 to 0, I_{SUPPLY} = 35 µA		50		µs
Preamplifier and DGA Disable Time	ENBL = 1, TXEN = 0, gain code = 0001 to 0000		0.4		µs
Driver Disable Time	ENBL = 1, gain code = 0000, TXEN = 1 to 0		2.2		µs

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6 V
Input Voltage (INxx, PRAI, FDBK, VMDI, VOCM)	VPOS, VNEG
Logic Voltages	VPOS, ground
Temperature	
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Thermal Data[1]	
Maximum Junction Temperature	125°C
θ_{JA}	47.3°C/W
θ_{JC}	6.9°C/W
θ_{JB}	28.6°C/W
Ψ_{JT}	0.6°C/W
Ψ_{JB}	27.4°C/W

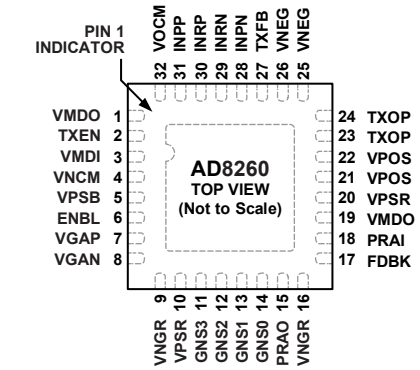
[1] Thermal data at zero airflow with exposed pad soldered to four-layer JEDEC board with vias per JESD51-5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE. THE GROUND PLANE PATTERN SHOULD INCLUDE A PATTERN OF VIAS TO INNER LAYERS.

07192-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 19[1]	VMDO	VMID Buffer Output. Requires robust ac decoupling with a capacitance of 0.1 µF capacitor or greater.
2	TXEN	Driver Enable. Logic threshold = 1.1 V with ±0.2 V hysteresis.
3	VMDI	VMID Input Voltage. Normally decoupled with a 0.1 µF capacitor. When pulled to VNCM, the VMID buffer shuts down. This can be useful when using the part with dual supplies or when an external midpoint generator is used.
4	VNCM	Negative Supply for Bias Cell, VMID Cell, and Logic Inputs. (Ground this pin in applications.)
5	VPSB	Positive Supply for Bias Cell and VMID Cell.
6	ENBL	Enable. Logic threshold = 1.1 V. When low, the AD8260 is disabled and the supply current is 35 µA when TXEN and all GNSx pins are also low.
7	VGAP	Positive VGA Output (Needs to Be Ac-Coupled for Single Supply).
8	VGAN	Negative VGA Output (Needs to Be Ac-Coupled for Single Supply).
9, 16[1]	VNGR	Negative Supply for Preamplifier and DGA (Set to −VPOS for Dual Supply; GND for Single Supply).
10, 20[1]	VPSR	Positive Supply for Preamplifier, DGA, and GNSx Logic Decoder.
11	GNS3	MSB for Gain Control. Logic threshold = 1.1 V.
12	GNS2	Gain Control Bit. Logic threshold = 1.1 V.
13	GNS1	Gain Control Bit. Logic threshold = 1.1 V.
14	GNS0	LSB for Gain Control. Logic threshold = 1.1 V.
15	PRAO	Preamplifier Output.
17	FDBK	Negative Input of Preamplifier.
18	PRAI	Positive Input of Preamplifier.
21, 22[1]	VPOS	Positive Supply for Driver Amplifier.
23, 24[1]	TXOP	Driver Output.
25, 26[1]	VNEG	Negative Supply for Driver Amplifier (Set to −VPOS for Dual Supply; GND for Single Supply).
27	TXFB	Feedback for Driver Amplifier.
28	INPN	Negative Driver Amplifier Input.
29	INRN	Negative Gain Resistor Input for Driver Amplifier.
30	INRP	Positive Gain Resistor Input for Driver Amplifier.
31	INPP	Positive Driver Amplifier Input.
32	VOCM	Output Common Mode Pin. Normally connected to Pin VMDO.
	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and maximum thermal capability it is recommended that the pad be soldered to the ground plane. The ground plane pattern should include a pattern of vias to inner layers.

[1] Pins with the same name are connected internally.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S (supply voltage) = 3.3 V, T_A = 25°C, C_L = 5 pF, f = 10 MHz, preamplifier gain = 2×, R_{FB1} and R_{FB2} of the preamplifier = 100 Ω, R_{LOAD} of the driver amplifier = 500 Ω, T_X and R_X enabled, unless otherwise specified.

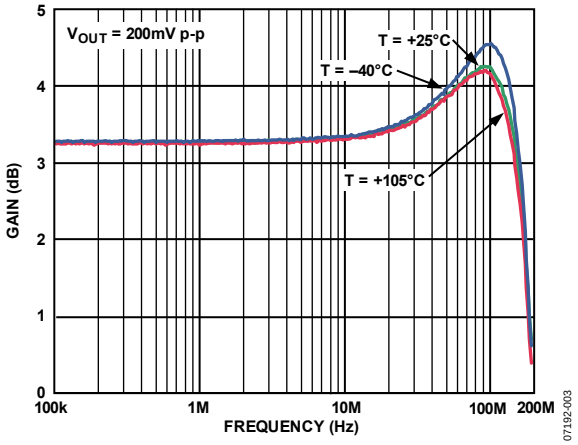


Figure 3. Small-Signal Frequency Response at Three Temperatures of the High Current Driver—See Figure 51

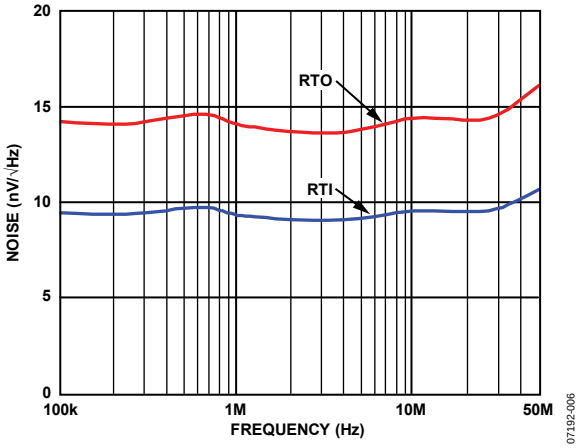


Figure 6. Input-Referred and Output-Referred Noise of the High Current Driver—See Figure 52

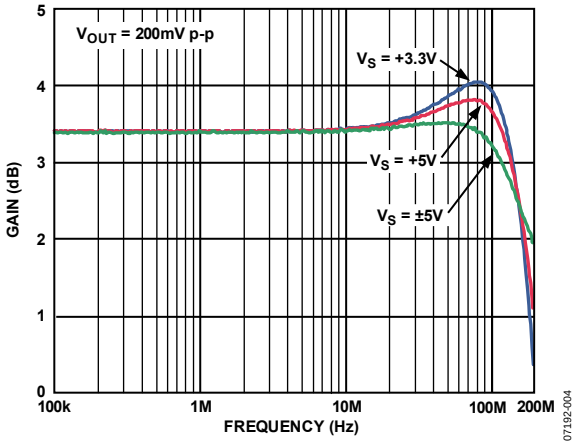


Figure 4. Small-Signal Frequency Response of the High Current Driver for Three Supply Voltages—See Figure 51

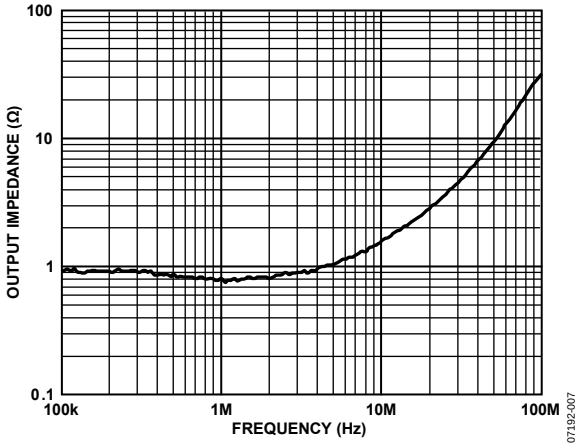


Figure 7. Output Impedance of the High Current Driver See Figure 53

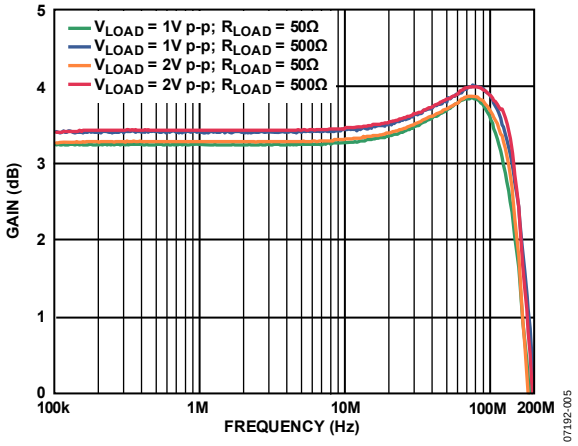


Figure 5. Large-Signal Frequency Response of the High Current Driver for Two Values of Output Voltage and Two Values of Load Resistance—See Figure 51

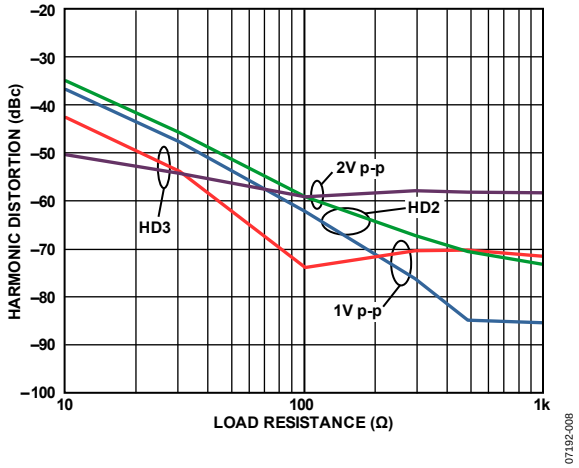


Figure 8. Harmonic Distortion (HD2, HD3) vs. Load Resistance for the High Current Driver—See Figure 54

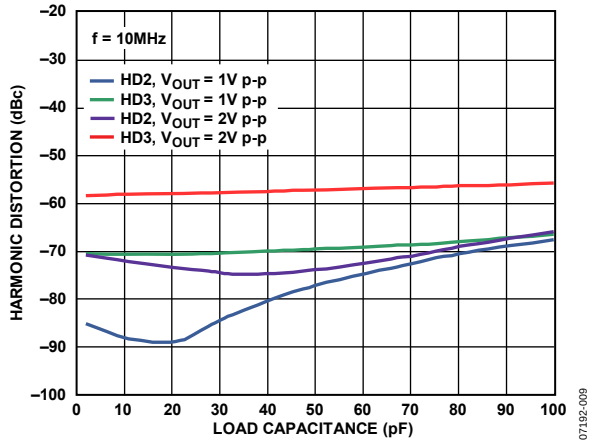


Figure 9. Harmonic Distortion (HD2, HD3) vs. Load Capacitance at Two Values of Output Voltage for the High Current Driver—See Figure 54

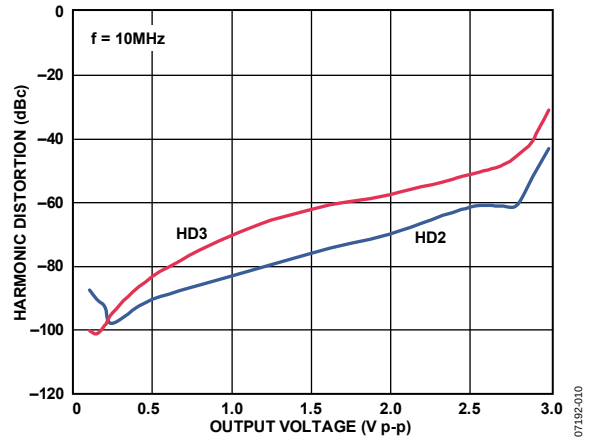


Figure 10. Harmonic Distortion (HD2, HD3) vs. Output Voltage for the High Current Driver—See Figure 54

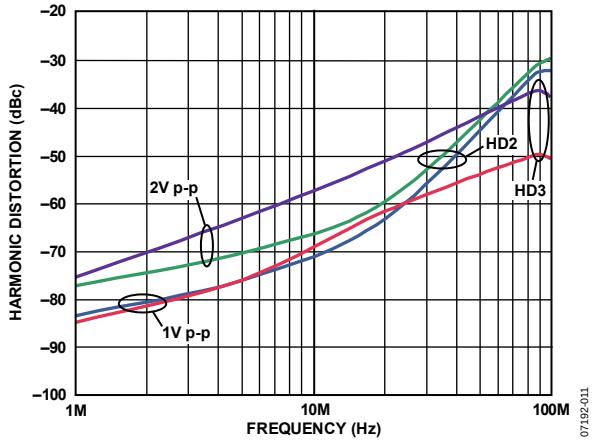


Figure 11. Harmonic Distortion (HD2, HD3) vs. Frequency of the High Current Driver at Two Values of Output Voltage—See Figure 54

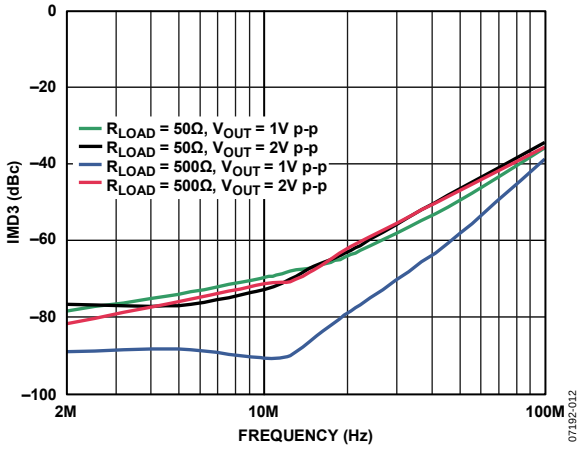


Figure 12. IMD3 vs. Frequency for Two Values of Output Voltage and Two Values of Load Resistance for the High Current Driver—See Figure 55

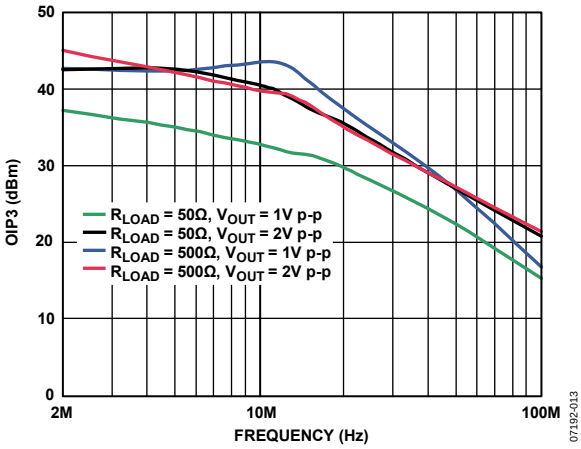


Figure 13. Third-Order Intercept (OIP3) vs. Frequency for the High Current Driver See Figure 55

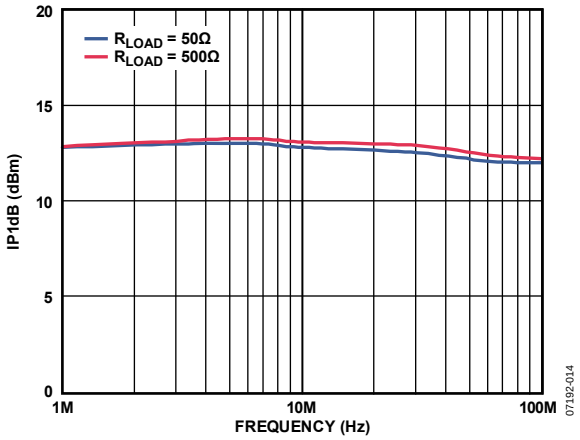


Figure 14. Input-Referred 1 dB Compression (IP1dB) vs. Frequency for Two Values of Load Resistance for the High Current Driver

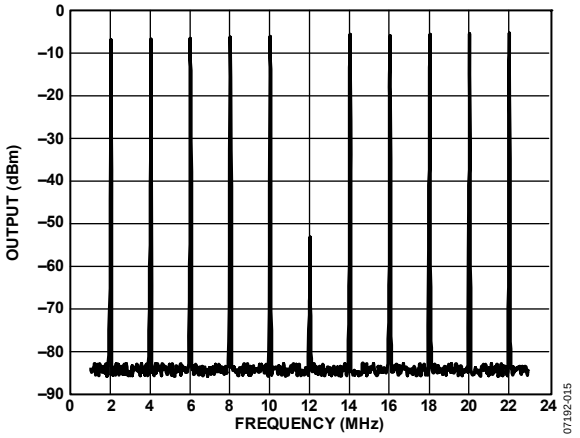


Figure 15. Missing Tone Power Ratio for the High Current Driver

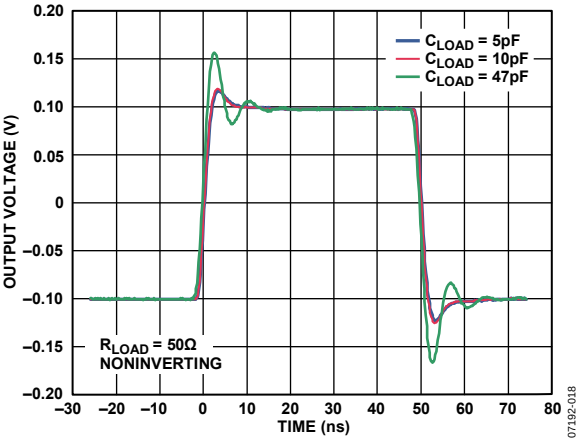


Figure 18. Small-Signal Pulse Response of the High Current Driver for Various Values of Load Capacitance, C_{LOAD}, and 50 Ω Load—See Figure 56

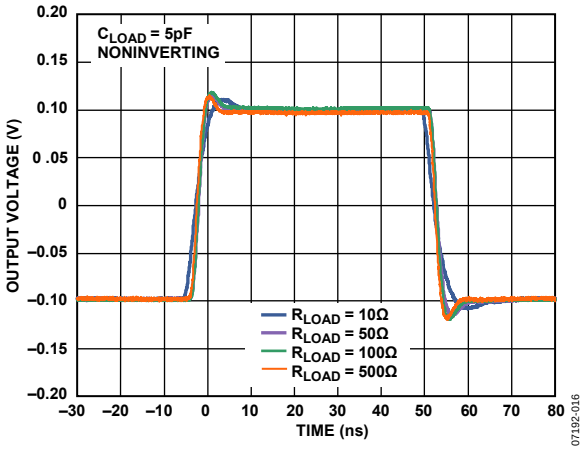


Figure 16. Small-Signal Pulse Response of the High Current Driver for Various Values of Load Resistance, R_{LOAD}—See Figure 56

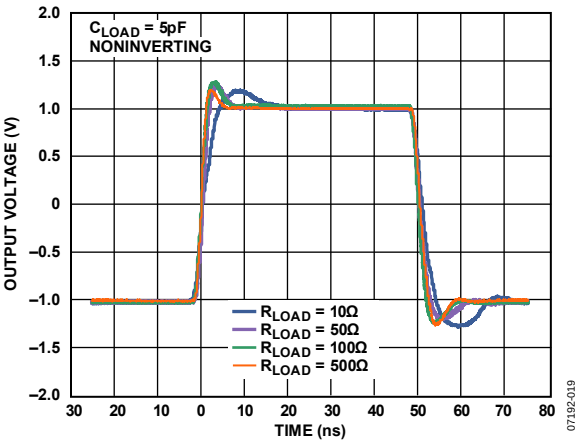


Figure 19. Large-Signal Pulse Response of the High Current Driver for Various Values of Load Resistance, R_{LOAD}—See Figure 56

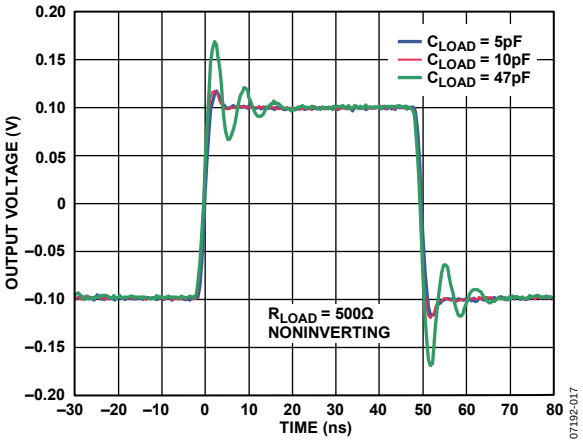


Figure 17. Small-Signal Pulse Response of the High Current Driver for Various Values of Load Capacitance, C_{LOAD}, and R_{LOAD} = 500 Ω—See Figure 56

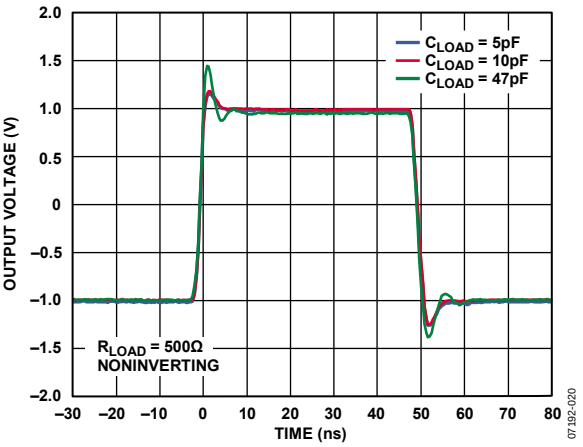


Figure 20. Large-Signal Pulse Response of the High Current Driver for Various Values of Load Capacitance, C_{LOAD}, and R_{LOAD} = 500 Ω—See Figure 56

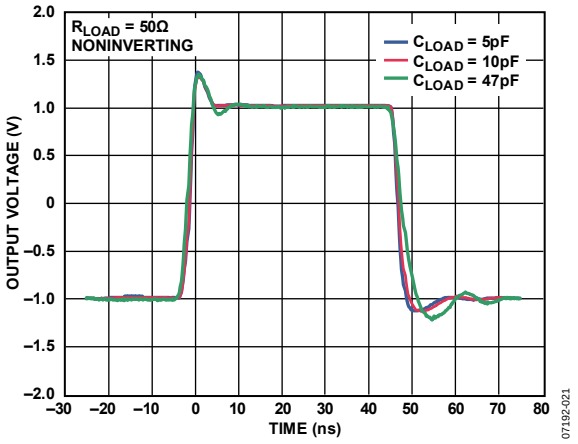


Figure 21. Large-Signal Pulse Response of the High Current Driver for Various Values of Load Capacitance, C_{LOAD}, and 50 Ω Load—See Figure 56

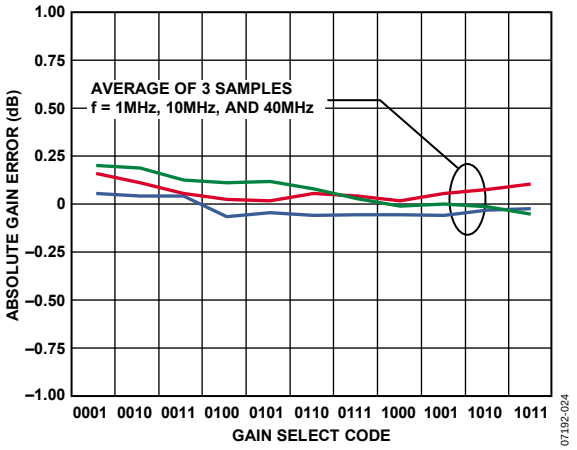


Figure 24. Absolute Gain Error vs. Gain Select Code for Three Samples for the VGA/Preamplifier at Three Frequencies Normalized to 1 MHz and Code 0110 See Figure 57

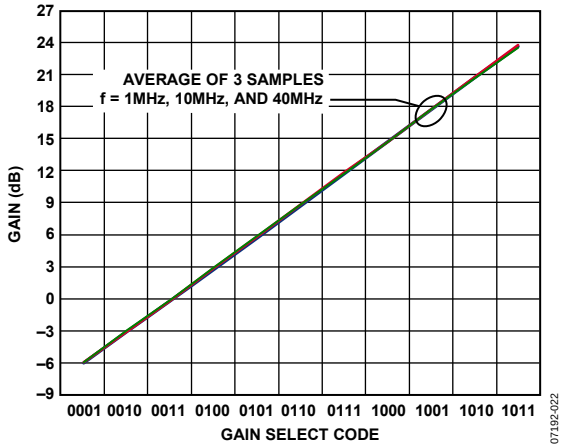


Figure 22. Gain vs. Gain Select Code for Three Samples for the VGA/Preamplifier at Three Frequencies—See Figure 57

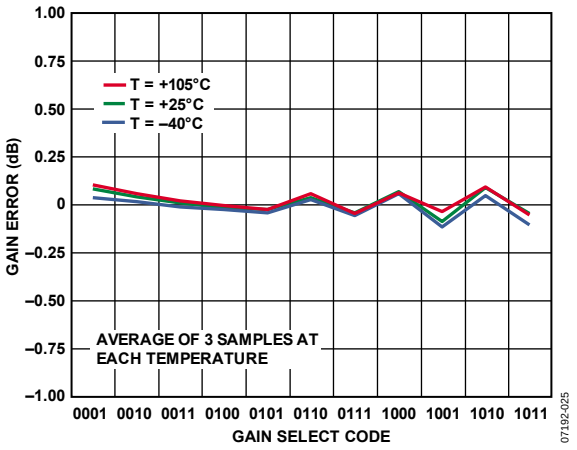


Figure 25. Gain Error vs. Gain Select Code at Three Temperatures for the VGA/Preamplifier—See Figure 57

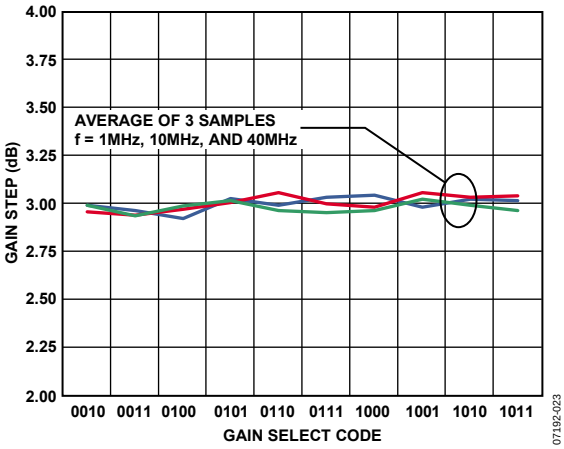


Figure 23. Gain Step vs. Gain Select Code for Three Samples for the VGA/Preamplifier at Three Frequencies—See Figure 57

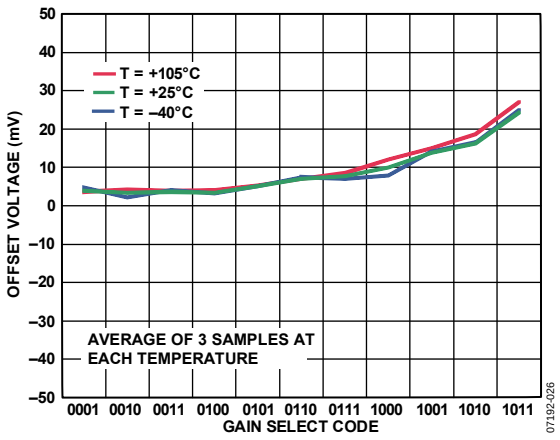


Figure 26. Output Offset Voltage vs. Gain Select Code at Three Temperatures for the VGA/Preamplifier—See Figure 58

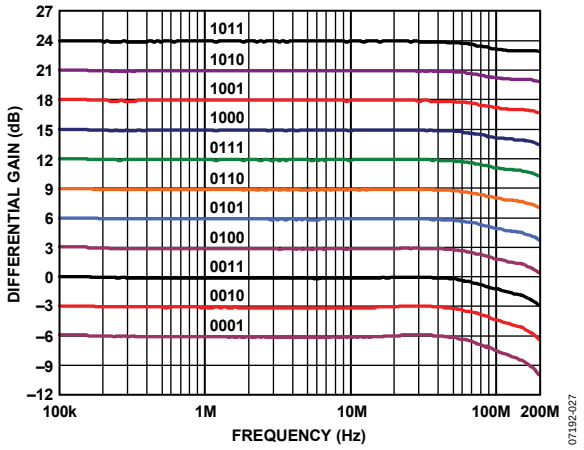


Figure 27. Frequency Response for a Supply Voltage (V_S) of 3.3 V for all Codes of the VGA/Preamplifier—See Figure 59

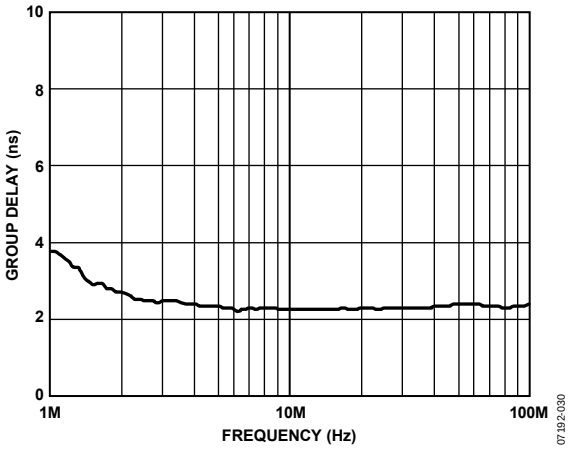


Figure 30. Group Delay vs. Frequency for the VGA/Preamplifier See Figure 59

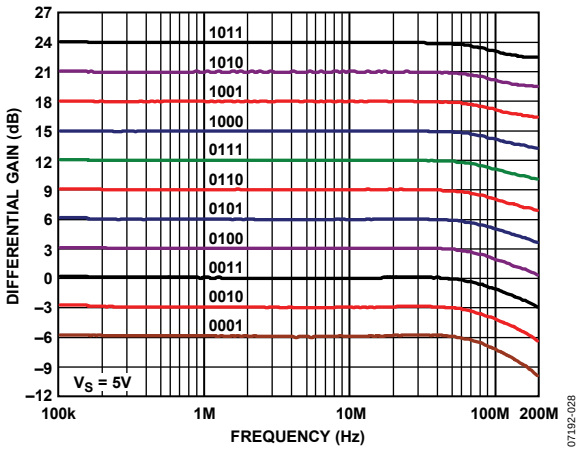


Figure 28. Frequency Response for a Supply Voltage (V_S) of 5 V for All Codes for the VGA/Preamplifier—See Figure 59

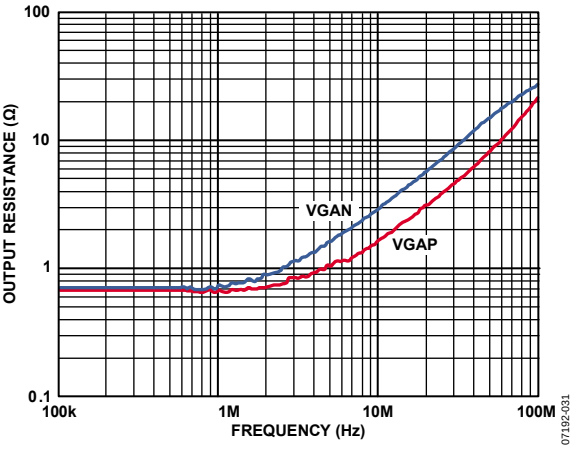


Figure 31. Output Resistance vs. Frequency for the VGA/Preamplifier See Figure 60

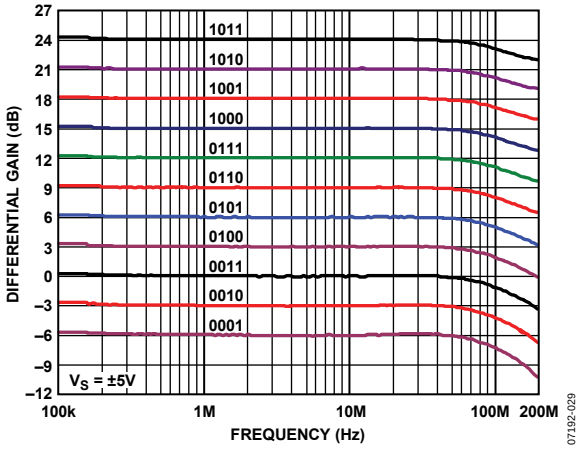


Figure 29. Frequency Response for a Dual Supply (V_S) = ±5 V for All Codes for the VGA/Preamplifier—See Figure 59

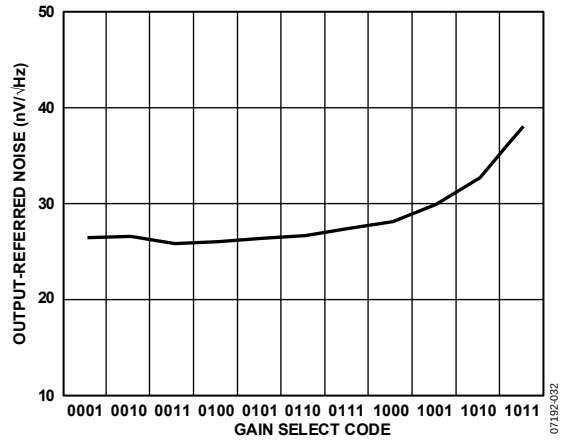


Figure 32. Output-Referred Noise vs. Gain Select Code for the VGA/Preamplifier—See Figure 61

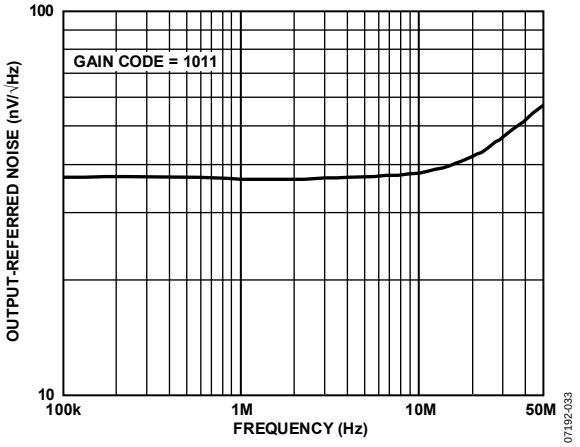


Figure 33. Output-Referred Noise vs. Frequency for the VGA/Preamplifier at Maximum Gain—See Figure 61

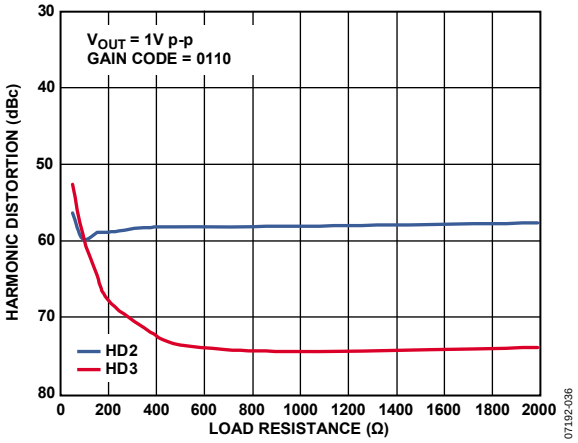


Figure 36. Harmonic Distortion (HD2, HD3) vs. Load Resistance for the VGA/Preamplifier—See Figure 62

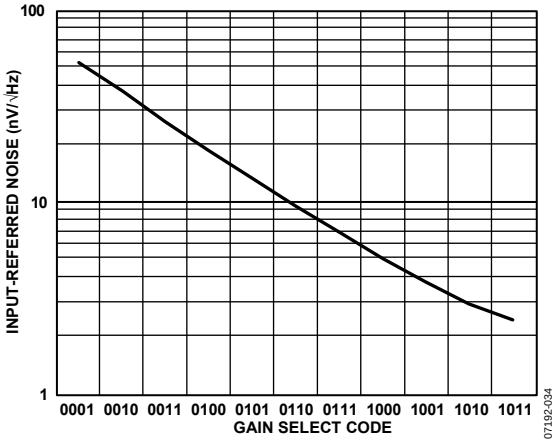


Figure 34. Input-Referred Noise vs. Gain Select Code for the VGA/Preamplifier See Figure 61

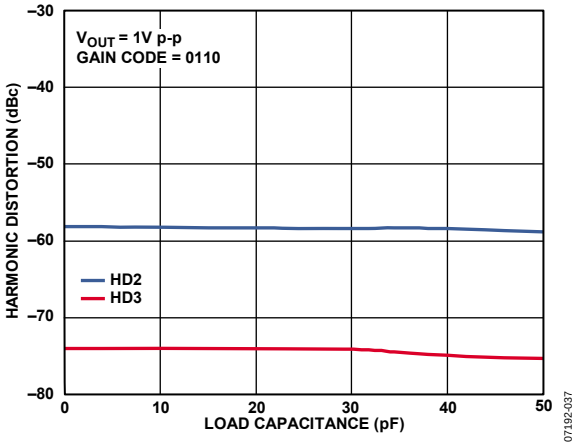


Figure 37. Harmonic Distortion (HD2, HD3) vs. Load Capacitance for the VGA/Preamplifier—See Figure 62

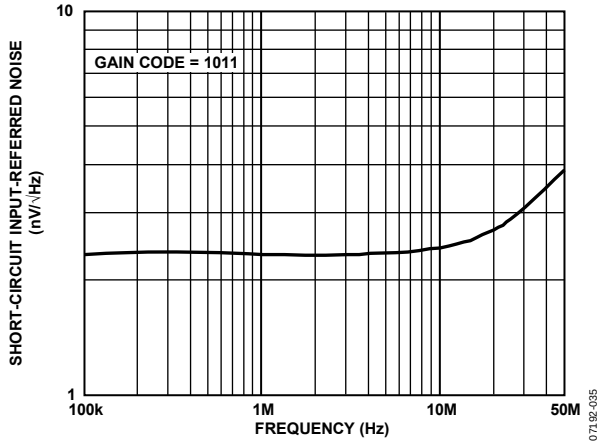


Figure 35. Short-Circuit Input Noise vs. Frequency for the VGA/Preamplifier See Figure 61

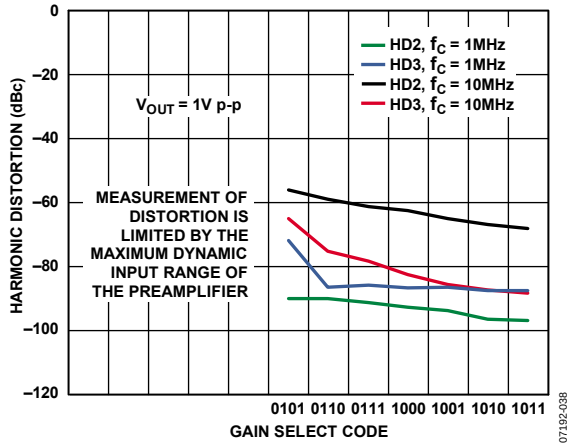


Figure 38. Harmonic Distortion (HD2, HD3) vs. Gain Select Code at 1 MHz and 10 MHz for the VGA/Preamplifier—See Figure 62

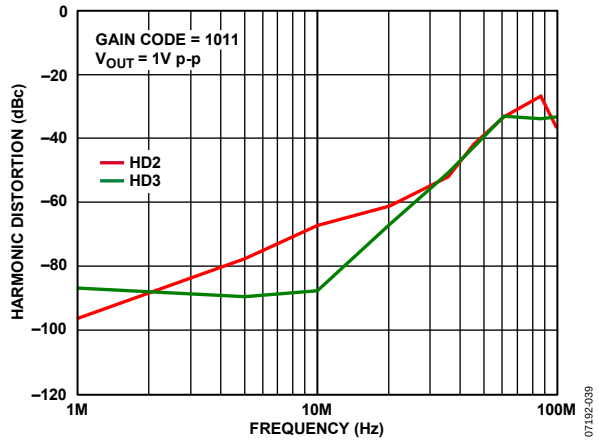


Figure 39. Harmonic Distortion (HD2, HD3) vs. Frequency for the VGA/Preamplifier—See Figure 62

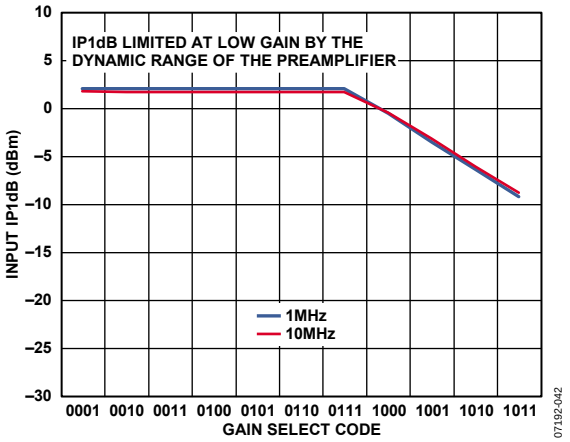


Figure 42. Input 1 dB Compression (IP1dB) vs. Gain Select Code at 1 MHz and 10 MHz for the VGA/Preamplifier

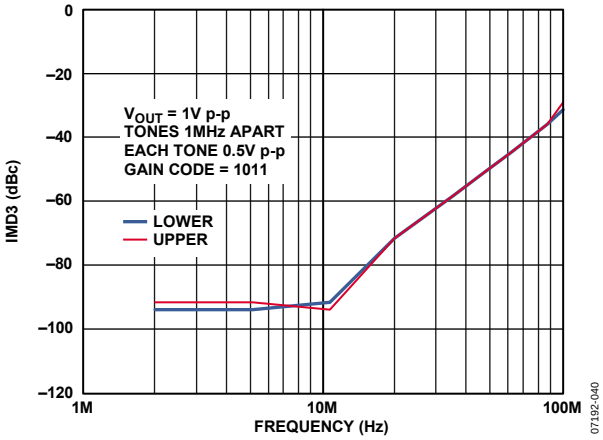


Figure 40. Third-Order Intermodulation Distortion (IMD3) vs. Frequency for the VGA/Preamplifier

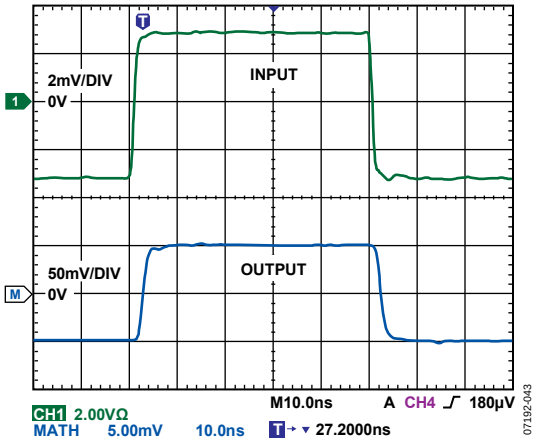


Figure 43. Small-Signal Pulse Response for the VGA/Preamplifier

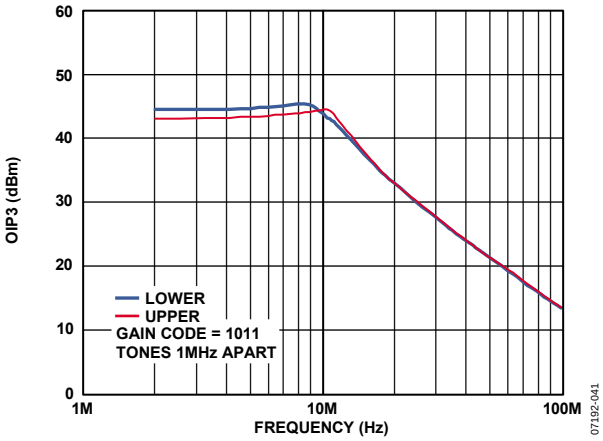


Figure 41. OIP3 vs. Frequency for the VGA/Preamplifier

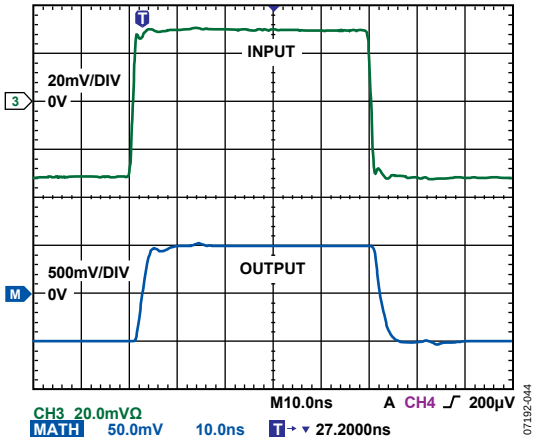


Figure 44. Large-Signal Pulse Response for the VGA/Preamplifier

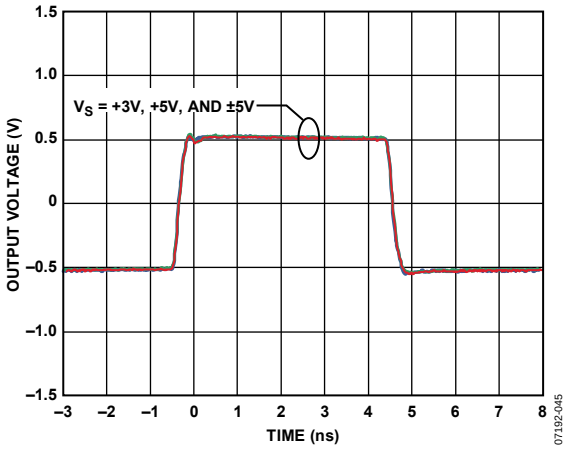


Figure 45. Large-Signal Pulse Response for Various Values of Supply Voltage for the VGA/Preamplifier

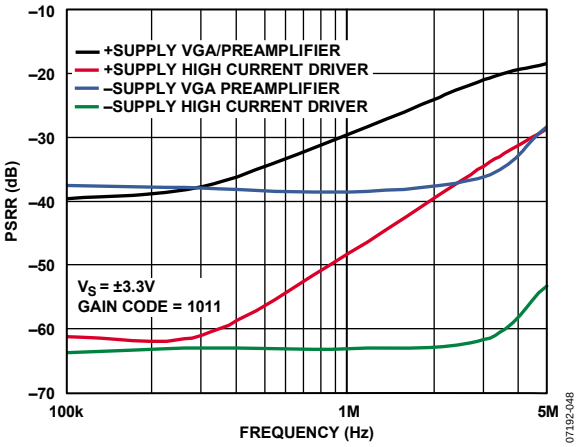


Figure 48. PSRR vs. Frequency for Dual Supplies for the High Current Driver and the VGA/Preamplifier

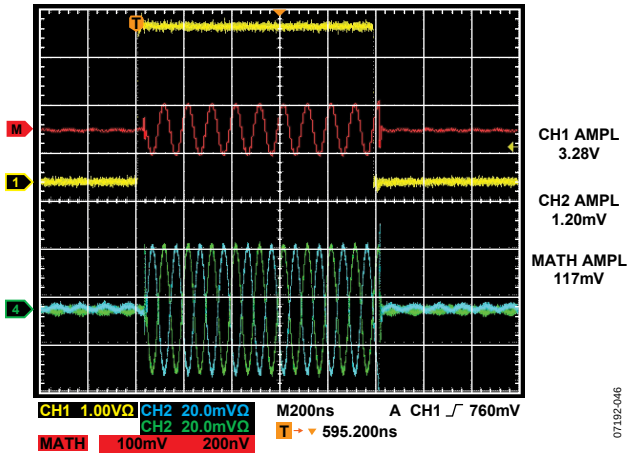


Figure 46. Gain Response for the VGA/Preamplifier, Yellow: Gain Code Select, Red: VGA Differential Output, Blue/Green: VGAP and VGAN

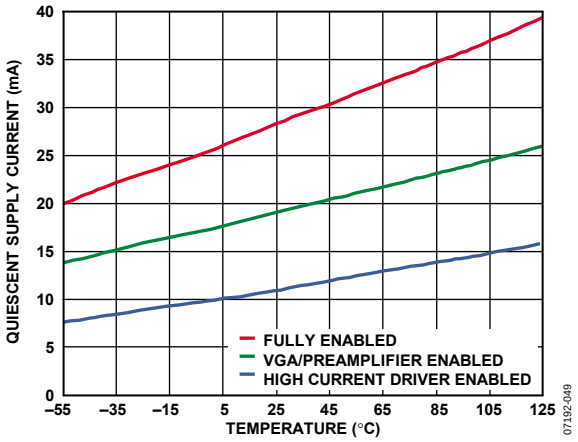


Figure 49. Quiescent Supply Current vs. Temperature for Three Operating States

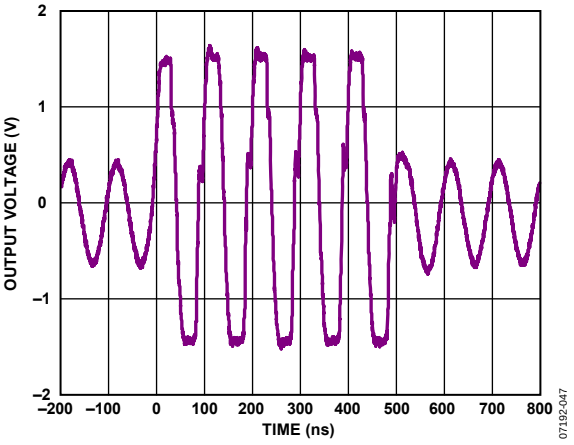


Figure 47. Overdrive Recovery of the VGA/Preamplifier—Gain Code = 1011

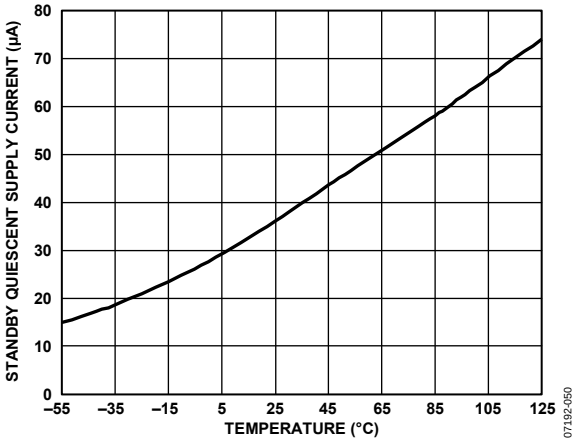


Figure 50. Standby Quiescent Supply Current vs. Temperature

TEST CIRCUITS

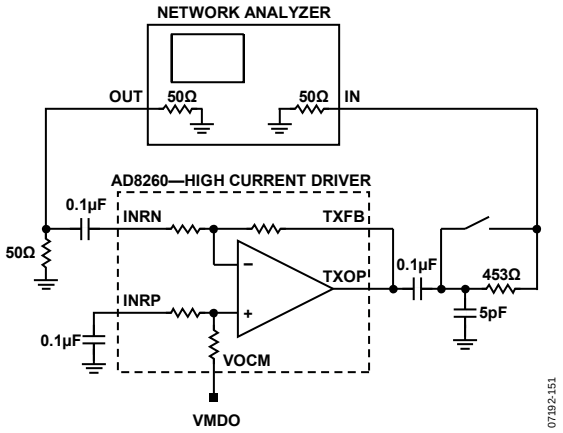


Figure 51. Test Circuit for Frequency Response of the High Current Driver

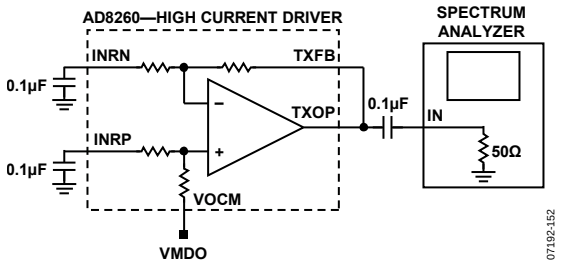


Figure 52. Test Circuit for Input-Referred and Output-Referred Noise of the High Current Driver

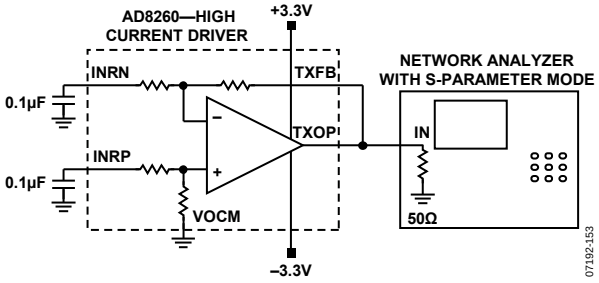


Figure 53. Test Circuit for Output Impedance of the High Current Driver

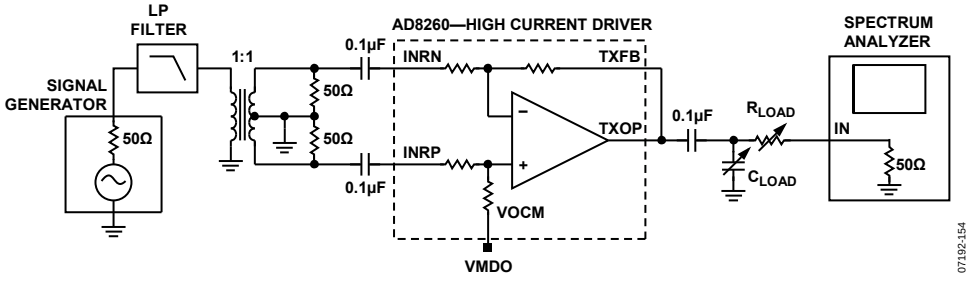


Figure 54. Test Circuit for Harmonic Distortion of the High Current Driver

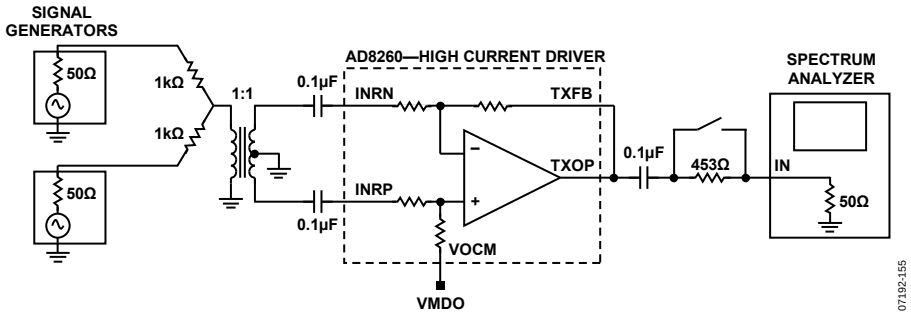


Figure 55. Test Circuit for IMD3 and OIP3 of the High Current Driver

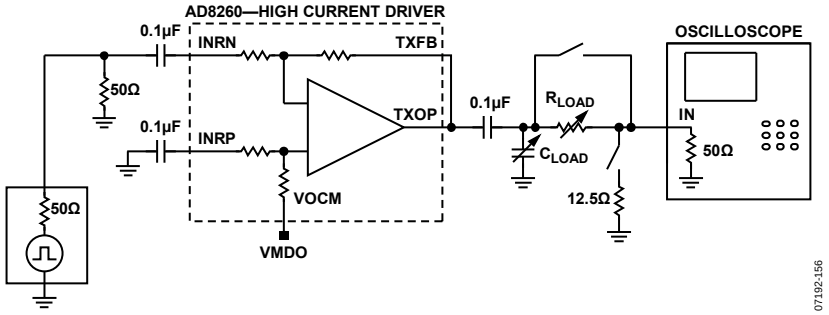


Figure 56. Test Circuit for Pulse Response of the High Current Driver

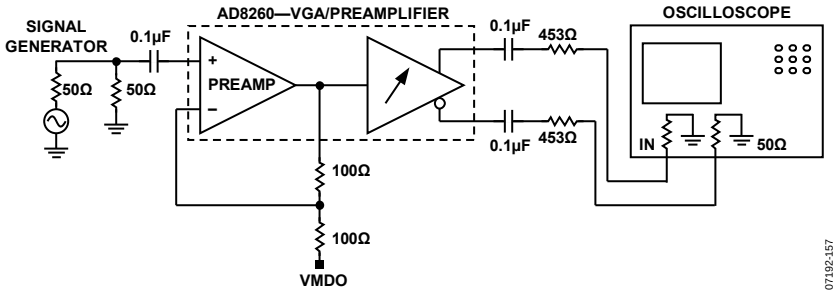


Figure 57. Test Circuit for Gain Step Size and Error of the VGA/Preamplifier

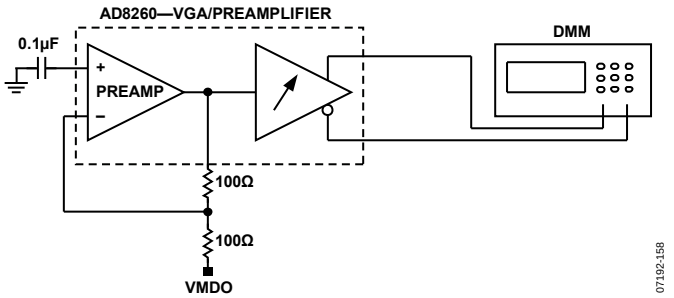


Figure 58. Test Circuit for Output-Referred Offset Voltage of the VGA/Preamplifier

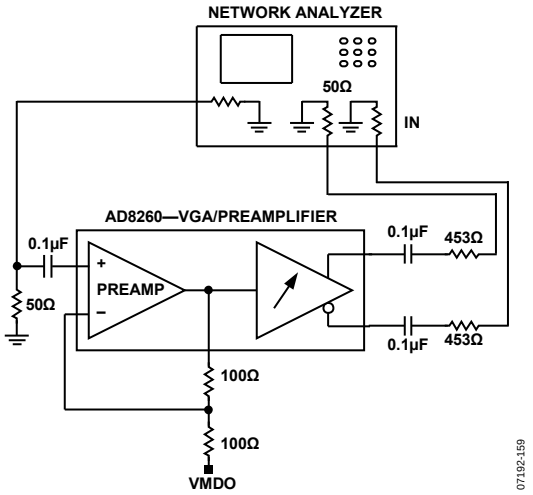


Figure 59. Test Circuit for Frequency Response and Group Delay of the VGA/Preamplifier

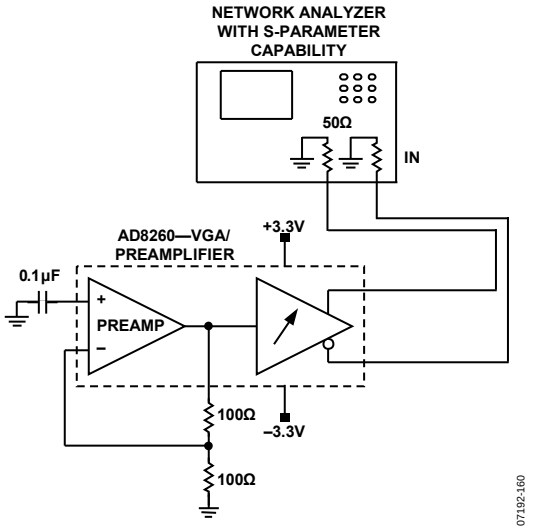


Figure 60. Test Circuit for Output Resistance of the VGA/Preamplifier

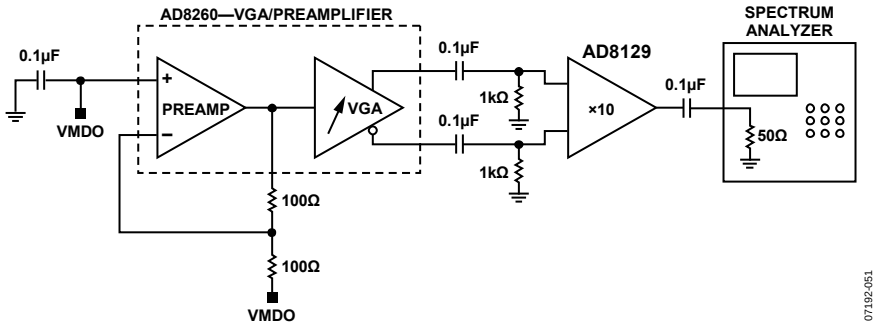


Figure 61. Test Circuit for Input-Referred and Output-Referred Noise Measurements of the VGA/Preamplifier

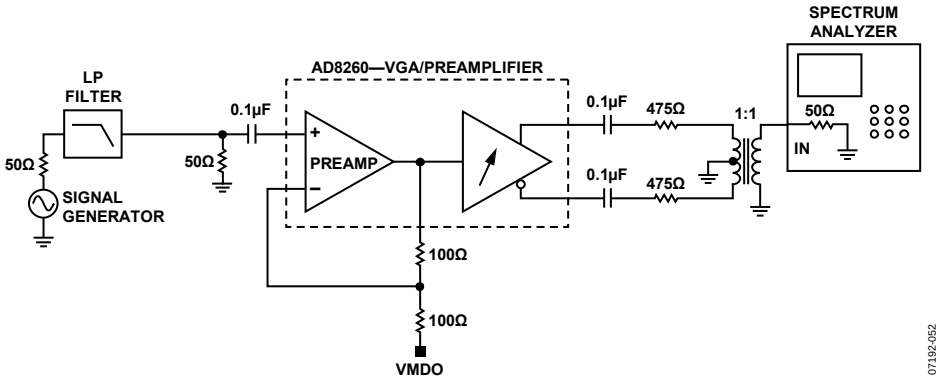


Figure 62. Test Circuit for Harmonic Distortion Measurements of the VGA/Preamplifier

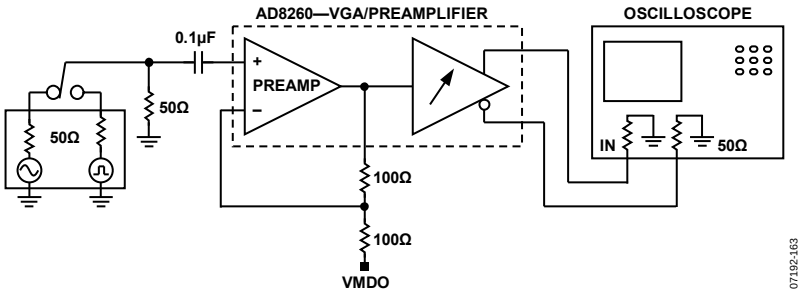


Figure 63. Test Circuit for IP1dB, Pulse Response, Overdrive Recovery, and Gain Response of the VGA/Preamplifier

THEORY OF OPERATION

OVERVIEW

The AD8260 is a self-contained transceiver intended for analog communications using a power line as the media. Operating on supplies as low as 3.3 V, it includes a high current driver usable as a transmitter and a low noise digitally programmable variable gain amplifier (DGA), usable as a receiver (see Figure 64). An uncommitted current-feedback high frequency op amp acts as a preamplifier and interface to the DGA and is user configured for gains greater than 6 dB. Combined, the VGA and preamplifier are usable at high signal levels from dc to 100 MHz, with a small-signal −3 dB bandwidth of 230 MHz. To implement a high current-output VGA, the VGA output can be connected to the driver-amplifier differential input.

The small-signal −3 dB bandwidth of the driver amplifier is 195 MHz and the large-signal bandwidth is >115 MHz, even when driving a 50 Ω load.

The device is fabricated on the Analog Devices, Inc., high speed (eXtra Fast Complementary Bipolar) XFCB process. The preamplifier and DGA feature low dc offset voltage, and a nominal gain range of −6 dB to +24 dB, a 30 dB gain span, and a differential output for ADC driving. The power consumption is 93 mW with a single 3.3 V supply. The supply current is typically about 28 mA when all circuits in the device are active. During normal usage, either the driver amplifier is on or the preamplifier and DGA are on and, therefore, the supply current in general is less than 28 mA. The gain of the AD8260 VGA is programmed via a 4-bit parallel interface. Figure 64 shows the circuit block diagram and basic application connections, and illustrates the envisioned external DAC, ADC, and power-line bus interface connections. The diagram shows the connections for single 3.3 V supply operation; if a dual supply is available, the VMID generator can be shut down and Pin VMDI, Pin VMDO, and Pin VOCM need to be grounded. Note that Pin VNCM functions as the negative supply for the bias and VMID cells, plus the logic interfaces, and should always be tied to ground.

For optimal dynamic range, it is important that the inputs and outputs to both the driver amplifier and the preamplifier and the DGA output amplifier be ac-coupled in a single-supply application. In Figure 64, the DAC and ADC are presumed to operate on a 1.8 V or 3.3 V supply with a corresponding limited output and input swing. The DAC outputs are currents that point down and generate a voltage in the 50 Ω resistors that are connected to ground. The maximum voltage with a peak DAC output current of 15 mA is 0.75 V; if a DAC with a 20 mA peak current is used, then the maximum voltage is 1 V per side for a differential input signal of 2 V p-p.

The driver amplifier supports a 3 V p-p output swing on a 3.3 V supply. Because of its gain of 1.5, the maximum input swing is 2 V p-p. The corresponding maximum output swing for the DGA is 2.4 V p-p differential; the input to the preamplifier can be a maximum of 0.6 V p-p.

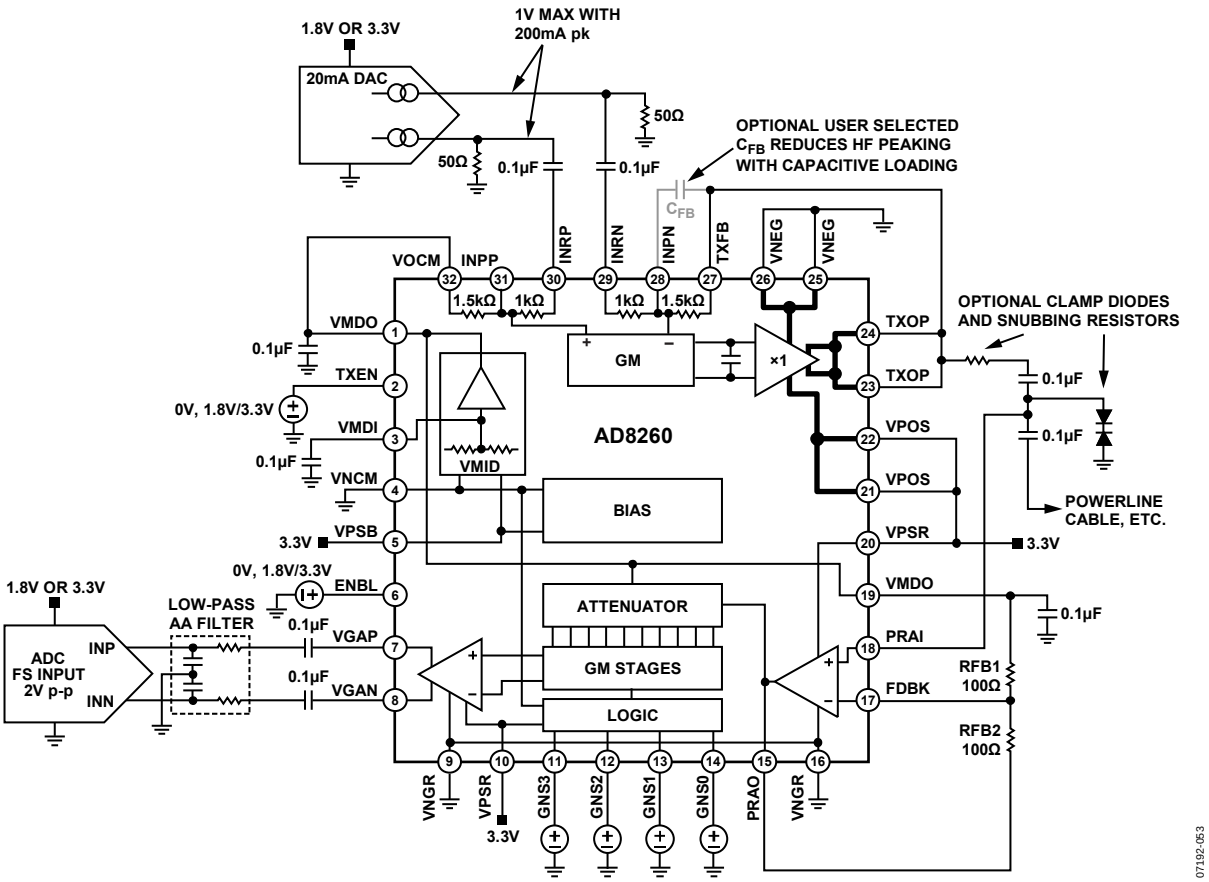


Figure 64. Block Diagram and Basic Application Connections

HIGH CURRENT DRIVER AMPLIFIER

The high current driver amplifier can deliver very large output currents suitable for driving complex impedances, such as a power line, a 50 Ω line, or a coaxial cable. The input of the amplifier is fully differential and intended to be driven by a differential current-output DAC, as shown in Figure 64. The differential input signal is amplified by 1.5× and produces a 2.25 V p-p single-ended output signal from a 1.5 V p-p input signal. A DAC with 15 mA maximum output current into a 50 Ω load provides 1.5 V p-p of input voltage and results in 2.25 V p-p at the output. A DAC whose output is 20 mA produces an output swing of 3 V p-p (neglecting a small gain error when driving the parallel combination of the 50 Ω load-resistor and the internal 1 kΩ gain resistor of the AD8260).

For a 3.3 V supply rail, the maximum limit of the output voltage is 3 V p-p and distorts severely if exceeded. The recommended output for optimum distortion is 2 V p-p for a 3.3 V supply. Correspondingly, larger output swings are accommodated for higher supply voltages such as +5 V or ±5 V.

For optimum distortion, the input drive must be controlled such that the output swing is well within saturation levels established by the supply rail. The output swing can be reduced by using load resistors with values less than 50 Ω or by reducing the amplifier gain by connecting external resistors in parallel with the internal 1 kΩ and 1.5 kΩ resistors between Pin 27, Pin 28, and Pin 29, and between Pin 30, Pin 31, and Pin 32. Coincidently, noise is reduced because the gain setting resistors are the primary noise sources of the high current driver amplifier.

The output-referred noise is 14 nV/√Hz, of which 11 nV/√Hz is due to the gain setting resistors. Matching of the gain setting resistors is important for good common-mode rejection and the accuracy of the differential gain. If external resistors are used, their accuracy should be at least ±1%. How low the resistor values can be is primarily determined by the quality of the ac ground at Pin VOCM; as the gain setting resistors decrease in value, the dynamic current increases, and the quality of the decoupling capacitors needs to increase correspondingly.

PRECAUTIONS TO BE OBSERVED DURING HALF-DUPLEX OPERATION

During receive, when the high current driver-amplifier is disabled, its gain setting resistors provide a signal path from input to output. To prevent inadvertent DAC signals from being transmitted while receiving via the preamplifier and DGA, the DAC in Figure 64 must have no output signal.

During transmit, the preamplifier and VGA should be disabled through any of the nongain-setting codes (see Table 4).

VMID BUFFER

The VMID buffer is a dc bias source that generates the voltage on Pin 1 and Pin 19, VMDO. Node VMDO cannot accommodate large dynamic currents and requires excellent ac decoupling to ground. A high quality 0.1µF capacitor located as close as possible to Pin 1 and Pin 19 (see Figure 64) is normally sufficient to decouple the high values of current from Node VMDO.

When operating with dual power supplies, the buffer is disabled by connecting Pin VMDI, Pin VOCM, and Pin VMDO to ground. Because the logic decoder in the DGA (GNSx inputs) requires 3.3 V of headroom, the positive supply rails must be 3.3 V or greater whether single-ended or dual. If a dual supply is used, the negative rails are the same magnitude (opposite polarity) as the positive, that is, −3.3 V when VPOS, VPSB, and VPSR are +3.3 V.

PREAMPLIFIER

The AD8260 includes an uncommitted current feedback op amp to buffer the resistive attenuator of the DGA. External resistors are used to adjust the gain. The preamplifier is characterized with a noninverting gain of 6 dB (2×) and both gain resistor values of 100 Ω. The preamplifier gain can be increased using different gain ratios of R_{FB1} and R_{FB2}, trading off bandwidth and offset voltage. The sum of the values of R_{FB1} and R_{FB2} should be ≥200 Ω to maintain low distortion. R_{FB2} should be ≥100 Ω because it and an internal compensation capacitor determine the −3 dB bandwidth of the amplifier. Smaller resistor values may compromise preamplifier stability.

Because the AD8260 is internally dc-coupled, larger preamplifier gains increase its offset voltage. The circuit contains an internal bias resistor and some offset compensation; however, if a lower value of offset voltage is required, it can be compensated by connecting a resistor between the FDBK pin and the supply voltage. If the offset is negative, the resistor value connects to the negative supply; otherwise, it connects to the positive supply.

For larger gains, the overall noise is reduced if a low value of R_{FB1} is selected. For values of R_{FB1} = 20 Ω and R_{FB2} = 301 Ω, the preamplifier gain is 16× (24.1 dB) and the input-referred noise is about 1.5 nV/√Hz. For this value of gain, the overall gain range increases by 18 dB so that the absolute gain range is 12 dB to 42 dB.

PREAMPLIFIER NOISE

The total input-referred voltage and current noise of the positive input of the preamplifier is about 2.4 nV/√Hz and 5 pA/√Hz, respectively. The DGA output referred noise is about 25 nV/√Hz at low gains and 39 nV/√Hz at the highest gain. The 25 nV/√Hz divided by the DGA fixed gain of 8× results in 3.12 nV/√Hz referred to the DGA input. Note that this value includes the noise of the DGA gain setting resistors as well. If this voltage is divided by the preamplifier gain of 2×, the DGA noise referred all the way to the preamplifier input is about 1.56 nV/√Hz. From this, it can be determined that the preamplifier, including the 100 Ω gain setting resistors, contributes about 1.8 nV/√Hz. The two 100 Ω resistors each contribute 1.29 nV/√Hz at the output of the preamplifier and 0.9 nV/√Hz referred to the input. With the gain resistor noise subtracted, the preamplifier noise alone is about 1.6 nV/√Hz.

Equation 1 shows the calculation that determines the output-referred noise at maximum gain (24 dB or 16×).

$$e_{n-out} = \sqrt{\left(e_{n,RS} \times A_t\right)^2 + (e_{n,PrA} \times A_t)^2 + (i_{n,PrA} \times R_S)^2 + (e_{n,RFB1} \times \frac{R_{FB2}}{R_{FB1}} \times A_{VGA})^2 + (e_{n,RFB2} \times A_{VGA})^2 + (e_{n,VGA} \times A_{VGA})^2} \quad (1)$$

where:
A_t is the total gain from preamplifier input to the VGA output.
$e_{n,RS}$ is the noise of the source resistance.
$e_{n,PrA}$ is the input-referred voltage noise of the preamplifier.
$i_{n,PrA}$ is the current noise of the preamplifier at the PRAI pin.
R_S is the source resistance.
A_{VGA} is the VGA gain.
$e_{n,RFB1}$ is the voltage noise of R_{FB1}.
$e_{n,RFB2}$ is the voltage noise of R_{FB2}.
$e_{n,VGA}$ is the input-referred voltage noise of DGA (low gain output-referred noise divided by a fixed gain of 8×).

Assuming $R_S = 0$, $R_{FB1} = R_{FB2} = 100\ \Omega$, $A_t = 16$, and $A_{VGA} = 8$, the noise simplifies to

$$e_{n-out} = \sqrt{(1.6\times16)^2 + 2\,(1.29\times8)^2 + (3.12\times8)^2} = 39\ \text{nV}/\sqrt{\text{Hz}} \quad (2)$$

Taking this result and dividing by 16 gives the total input-referred noise with a short-circuited input as 2.4 nV/√Hz. When the preamplifier is used in the inverting configuration with the same $R_{FB1} = R_{FB2} = 100\ \Omega$ as in the previous example, then $e_{n\text{-}out}$ does not change; however, because the gain decreases by 6 dB, the input-referred noise increases by a factor of 2 to about 4.8 nV/√Hz. The reason for this is that the noise gain to the DGA output of all the noise generators stays the same, but the preamp inverting gain is (−1×) compared to the (+2×) in the noninverting configuration. This doubles the input-referred noise.

DGA

Referring to Figure 64, the signal path consists of a 30 dB programmable attenuator followed by a fixed gain amplifier of 18 dB for a total DGA gain range of −12 dB to +18 dB. With the preamplifier configured for a gain of 6 dB, the composite gain range is −6 dB to +24 dB from single-ended preamplifier input to differential DGA output.

The DGA plus preamplifier with 6 dB of gain implements the following gain law:

$$Gain(\text{dB}) = \left[3.01\frac{dB}{Code}\times Code\right] + ICPT(\text{dB})$$

where:
ICPT is the nominal intercept, −9 dB.
Code values are decimal from 1 to 11.

The ICPT increases as the gain of the preamplifier is increased. For example, if the gain of the preamplifier is increased by 6 dB, then ICPT increases to −3 dB.

GAIN CONTROL

To change the gain, the desired four bits are programmed on Pin GNS0 to Pin GNS3, where GNS0 is the LSB (D0) and GNS3 is the MSB (D3). The states of Decimal 0 and Decimal 12 through Decimal 15 disable the preamplifier (PrA) and DGA (see Table 4).

Table 4. Gain Control Logic Table

D3	D2	D1	D0	Function	Comments
0	0	0	0	Disable	PrA and DGA powered down
0	0	0	1	−6	The numbers in the function column are composite gain values in dB for the corresponding code, when the preamplifier gain is 6 dB. For other values of preamplifier gain, the gain is amended accordingly; for example, if the preamplifier gain is 12 dB, the gain values increase by 6 dB. When using the DGA single ended, the composite gain decreases by 6 dB.
0	0	1	0	−3	
0	0	1	1	0	
0	1	0	0	3	
0	1	0	1	6	
0	1	1	0	9	
0	1	1	1	12	
1	0	0	0	15	
1	0	0	1	18	
1	0	1	0	21	
1	0	1	1	24	
1	1	0	0	Disable	PrA and DGA powered down
1	1	0	1	Disable	PrA and DGA powered down
1	1	1	0	Disable	PrA and DGA powered down
1	1	1	1	Disable	PrA and DGA powered down

OUTPUT STAGE

The gain of the voltage feedback output stage is fixed at 18 dB and inaccessible to the user. Otherwise, it is similar to the preamplifier in speed and bandwidth. The overall −3 dB bandwidth of the preamplifier and DGA combination is 230 MHz.

ATTENUATOR

The input resistance of the VGA attenuator is nominally 265 Ω. Assuming that the default preamplifier feedback network of R_{FB1} and R_{FB2} is 200 Ω, the effective preamplifier load is about 114 Ω. The attenuator is composed of ten 3.01 dB sections for a total attenuation span of −30.10 dB. Following the attenuator is a fixed gain amplifier with 18 dB (8×) gain. Because of this relatively low gain, the output offset is less than 20 mV over the operating temperature range; the offset is largest at maximum gain because the preamplifier offset is amplified. The VMDO pin defines the common-mode reference for the input and output. The voltage at VMID is half the supply voltage for single-supply operation and 0 V when dual supplies are used.

SINGLE-SUPPLY OPERATION AND AC COUPLING

When operating the AD8260 from a single supply, there are two bias options for VMDO.

- Use an external low impedance midpoint reference at Pin VMDO and pull VMDI to VNCM to shut down the VMID buffer.
- Use the internal VMID buffer as shown in Figure 64.

In both cases, decoupling capacitors are needed on Pin VMDO to absorb the dynamic currents.

During single-supply operation, the preamplifier input is normally ac-coupled. An internal bias resistor (nominally 1 k Ω) connected between PRAI and VMDO provides bias to the preamplifier input pin. A 50 Ω resistor connected between Pin PRAI and Pin VMDO, in parallel with the internal 1 kΩ, serves as a termination resistor and at the same time reduces the offset; the result is a composite value of about 48 Ω. The VGA input is biased through the attenuator network and the voltage at Pin VMDO. When active, the VMID buffer provides the needed bias currents. When the buffer is disabled, an external voltage is required at Pin VMDO to provide the bias currents. For example, for a single 5 V application, a reference such as the ADR43 and a stable op amp provide an adequate 2.5 V VMDO source.

POWER-UP/POWER-DOWN SEQUENCE

For glitch-free power-up operation, the following power-up and power-down sequence is recommended:

1. Enable the bias by pulling the ENBL pin high. Maintain GNS0 to GNS3 and TXEN at ground.
2. It is assumed that after the part wakes up from sleep mode, the receive section (preamplifier and DGA) needs to be active first to listen to any signals, and the driver needs to be off. Therefore, the gain code should be set to 0001 (−6 dB of gain) first and then the gain adjusted as needed. Note that any code besides 1 to 11 (binary) disables the receive section (see Table 4). During receive, it is also important that the DAC that provides the signal for the high current driver be disabled to avoid interfering with the received signal.
3. After receive, presumably data needs to be transmitted via the high current driver amplifier. At this point, the DAC should still be off. Pull Pin TXEN high and allow the high current driver to settle. Enable the DAC. Although the preamplifier and DGA can remain enabled during the previous sequence, there may be significant preamplifier overdrive, and it is best that the receiver be disabled while transmitting.
4. Pull Pin ENBL low to disable the chip. To achieve the specified sleep current of 35 μA, all logic pins must be pulled low as well.

LOGIC INTERFACES

All logic pins use the same interfaces and, therefore, have the same behavior and thresholds. The interface contains a Schmitt trigger type input with a threshold at about 1.1 V and a hysteresis of ±0.2 V.

Therefore, the logic low is between ground and 0.8 V, and logic high is from 1.4 V to VPOS. Because the threshold is so low, the logic interfaces can be driven directly from 1.8 V or 3.3 V CMOS.

The input bias current is nominally 0.2 μA when the applied voltage is 3.3 V and 18 nA when grounded.

APPLICATIONS INFORMATION

The AD8260 is ideally suited for compact applications requiring high frequency and large current drive of complex modulation products. Because the driver is capable of providing up to 300 mA (using a 3.3 V supply rail) to very low impedance loads, undefined network impedances are of little consequence. Such applications can include, but are not limited to, local power line wiring found in homes or in automobiles, or low impedance complex filters used in communications. Pulse response performance with loading effects are illustrated by various curves in the Typical Performance Characteristics section.

Figure 65 is an application block diagram showing AD8260 devices configured as transceivers in a small local network. In this figure, consider a small security system consisting of a master controller and four satellite cameras. For example, the master can be a processor-controlled switch that routes data to and from local satellite cameras. The cameras video signals are modulated for transmission over an existing power system such as the wiring found in homes or small businesses. Using the existing power network in this way eliminates the need to install additional cabling, thereby saving cost. Portability is also achieved because the system can be moved to other locations should the need arise, simply by unplugging a satellite and moving it elsewhere. The AD8260 transceivers perform the same function at the master and slave locations; a high frequency current-output DAC converts digital-to-analog data for the high current driver for transmission over a low impedance load. The input of the VGA/preamplifier connects to the same load, functioning as the receiver. In such a system, multiple AD8260 devices are connected to form a network, much like a LAN, except using the power-line wiring in a home or automobile in lieu of a Cat-5 cable, for example.

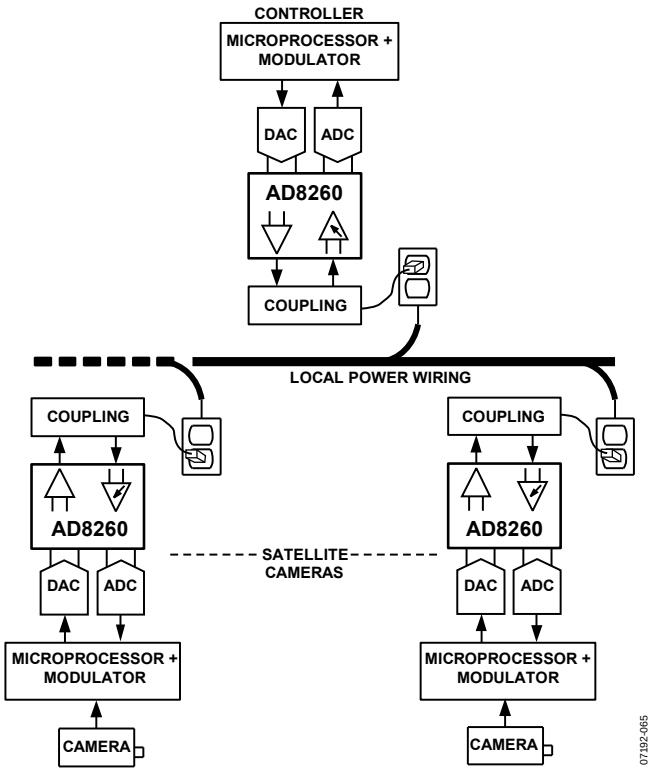


Figure 65. AD8260 Transceiver Application

Figure 66 shows the AD8260 as a low distortion, high power driver. The VGA and high current driver are combined by simply connecting the differential output of the VGA directly to the input of the driver.

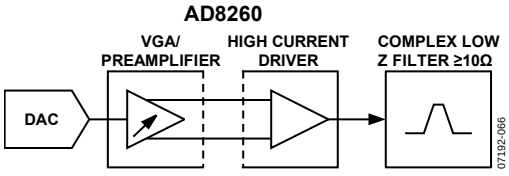


Figure 66. AD8260 Used as a VGA Driving a Low Impedance Load

EVALUATION BOARD

Analog Devices provides evaluation boards to customers as a support service so that the circuit designer can become familiar with the device in the most efficient way possible. The AD8260 evaluation board provides a fast, easy, and convenient means to assess the performance of the AD8260 before going through the inconvenience and expense of design and layout of a custom board. The board is shipped fully assembled and tested and provides basic functionality as shipped. Connectors enable the user to connect standard types of lab test equipment without having to wait for the rest of the design to be completed. Figure 67 shows a digital image of the top view and Figure 70 shows the schematic.

PCB artwork for all conductor and silkscreen layers is shown in Figure 71 through Figure 76. A description of a typical test setup is explained in the Connecting the Evaluation Board section. The artwork can be used as a guide in circuit layout and parts placement. This is particularly useful for multiple function circuits with many pins, requiring multiple passive components.

The board is shipped with the device fully enabled. Moving the ENABLE jumper to its upper position on the board disables the device. When the TX_EN jumper is in its upper position, the high current driver is disabled.

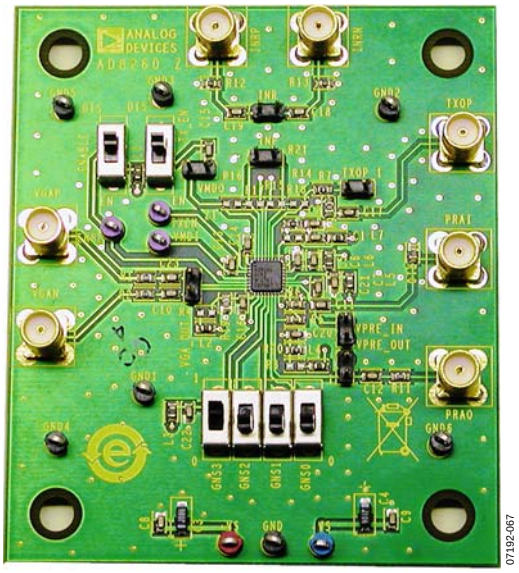


Figure 67. Top View of the AD8260-EVALZ

CONNECTING THE EVALUATION BOARD

Figure 69 shows an evaluation board with typical test connections. The various pieces of test equipment are representative, and equivalent equipment may be substituted.

The AD8260 includes two amplifier channels: a high current driver and a digitally controlled VGA that is independently enabled. The slide switch labeled ENABLE functions as the chip enable, the GNSx switches permit the preamplifier/VGA to operate, and the TX_EN switch enables the high current driver. These independent enable functions permit the device to operate in a send or listen mode when used as a transceiver.

The high current driver features differential inputs and is optimally driven by a differential signal source. The input signal is monitored at the 2-pin header labeled INP, using a differential probe such as the Tektronix P6247 (not shown). Two 49.9 Ω resistors are provided (R12 and R13), either for terminating coaxial cables from a signal generator or to be used as load resistors for a DAC with a current source output. An optional external load resistor is connected at the SMA connector TXOP and the output signal monitored at the 2-pin header labeled TXOP_1.

As shipped, the gain of the high current driver is 1.5×, its default value. The internal differential network with resistor values of 1 kΩ and 1.5 kΩ establishes this value. Other values of gain are realized by connecting external resistors to the device at Pin 23, Pin 24, Pin 27, Pin 28, and Pin 31, as shown in Figure 68, which shows the internal structure for the default gain and how the gain can be modified.

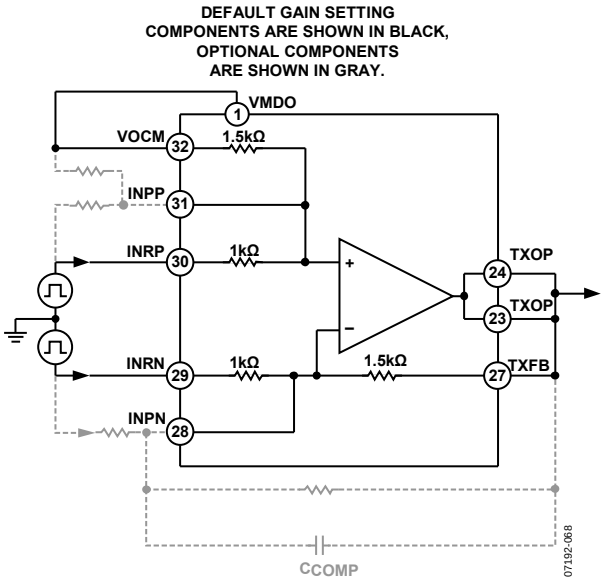


Figure 68. Gain-Setting Resistors of the High Current Driver

The VGA/preamplifier is completely independent of the high current driver and features a single-ended input at the SMA connector PRAI. The input signal is monitored at the header VPRE_IN. The output is monitored at the 2-pin header VGA_OUT.

The gain bits, GNS0 through GNS3, must be set before the VGA/preamplifier can operate. Table 4 lists the binary gain codes. The board is shipped with both enables (ENBL and TXEN) engaged and the gain-code switches adjusted for maximum DGA gain (1011). Resistor R5 and Resistor R6 establish the preamplifier gain and are 100 Ω as shipped for a noninverting preamplifier gain of 2×.

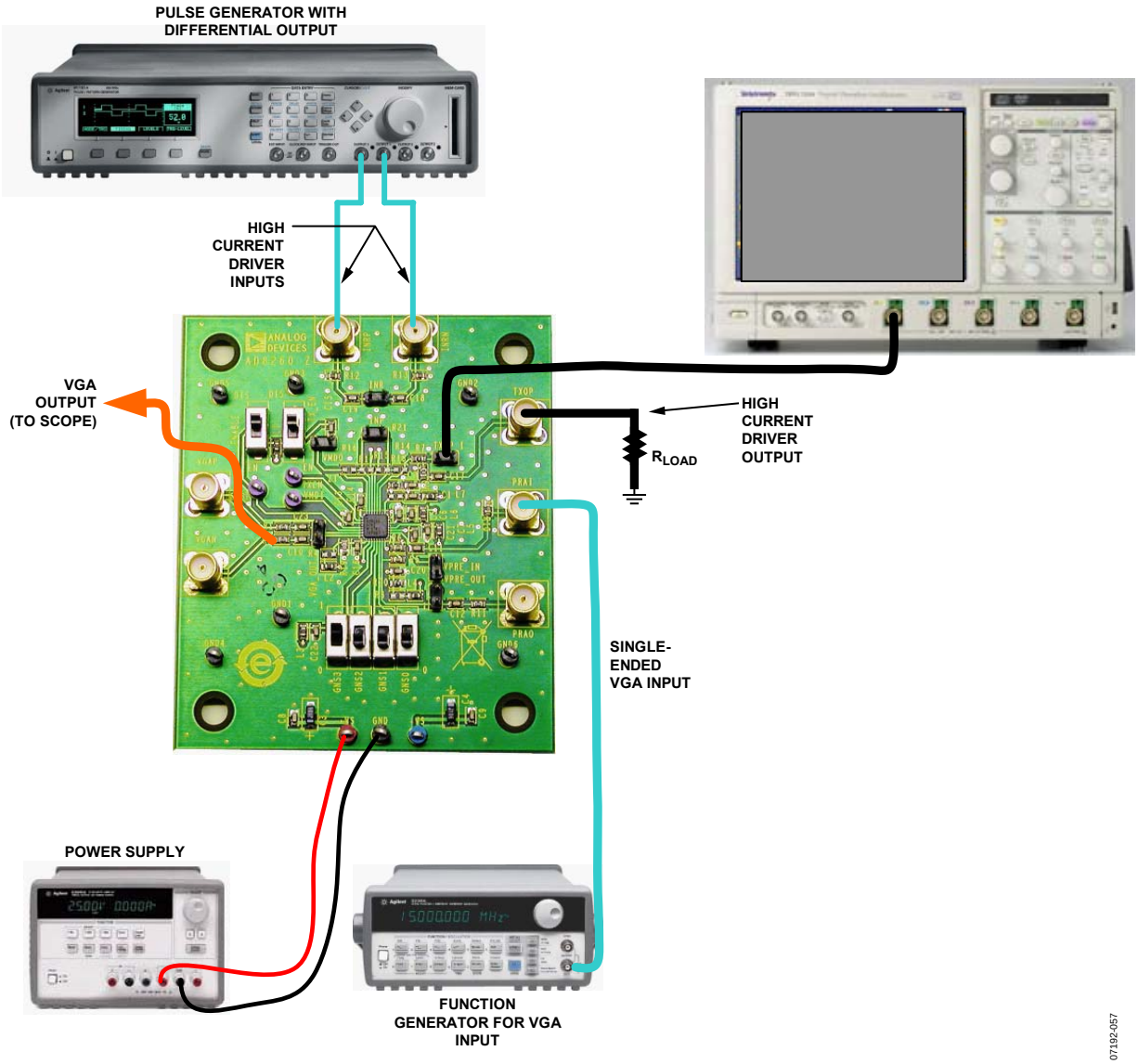


Figure 69. Typical Evaluation Board Connections

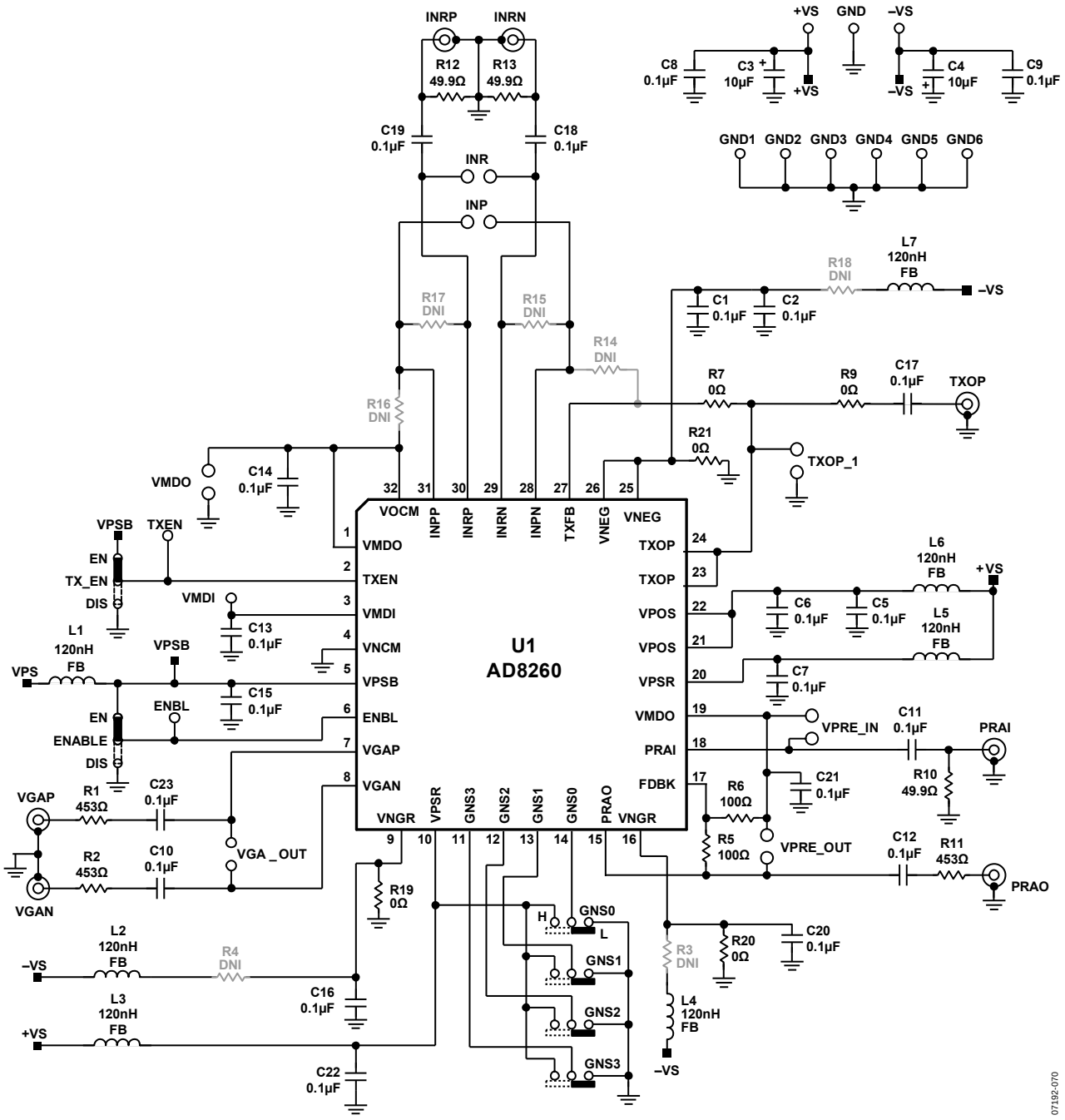


Figure 70. AD8260 Evaluation Board—Schematic Diagram

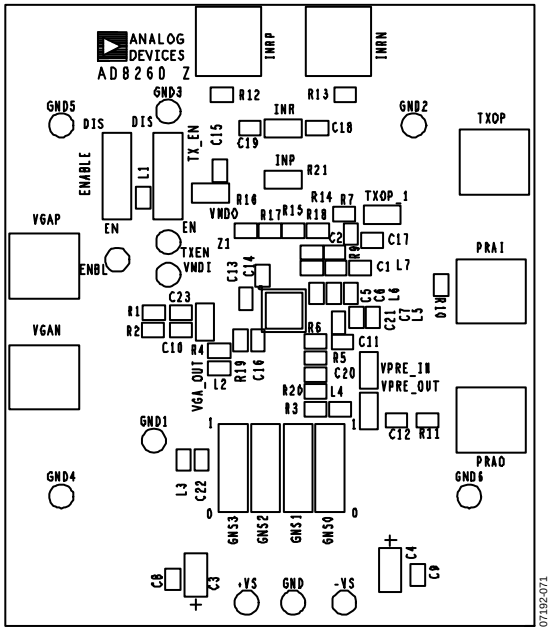


Figure 71. AD8260-EVALZ Component Side Assembly

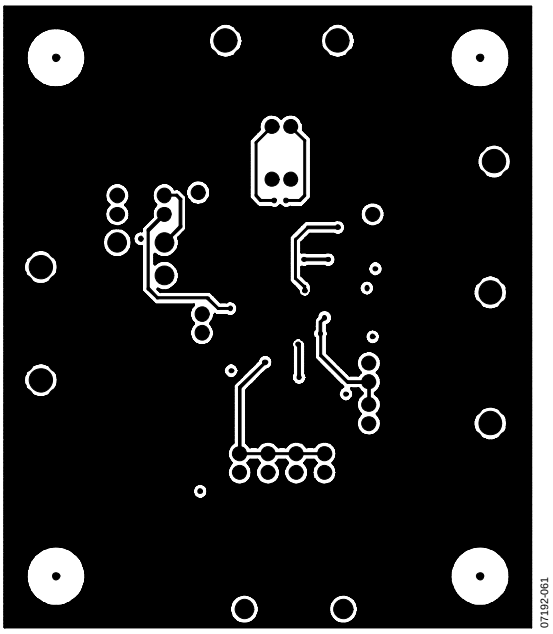


Figure 73. AD8260-EVALZ Secondary Side Copper

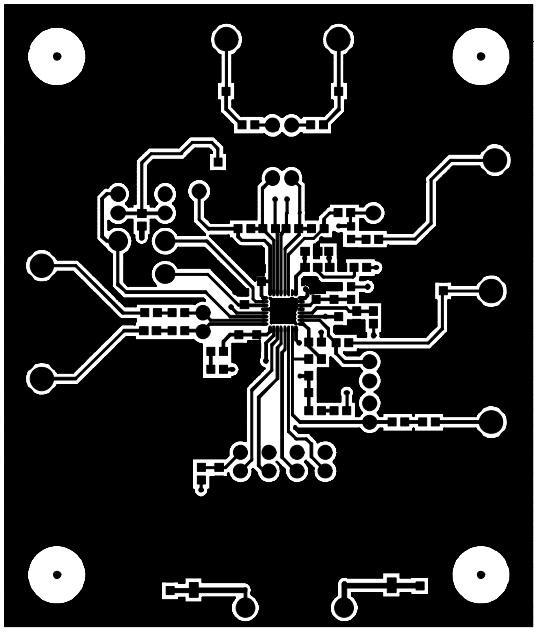


Figure 72. AD8260-EVALZ Component Side Copper

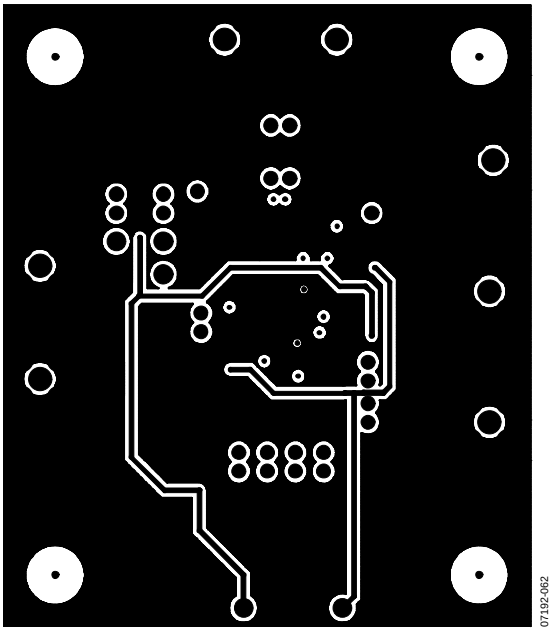


Figure 74. AD8260-EVALZ Power Plane

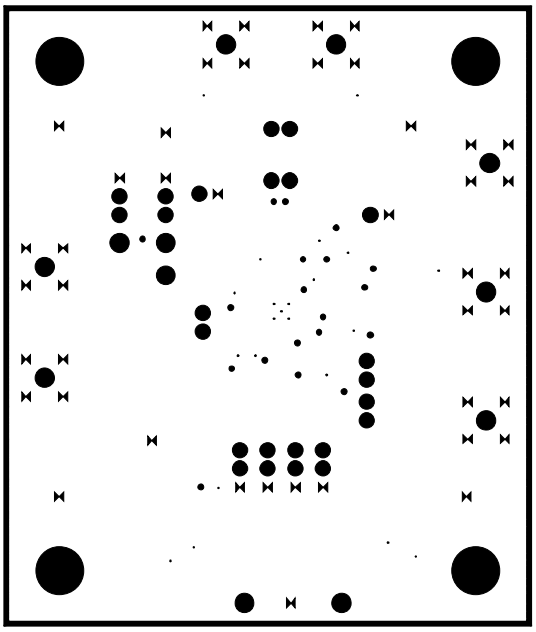


Figure 75. AD8260-EVALZ Ground Plane

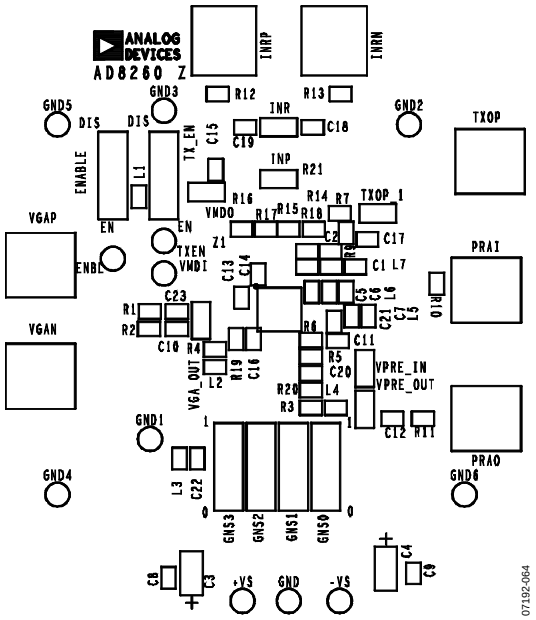


Figure 76. AD8260-EVALZ Component Side Silkscreen

OUTLINE DIMENSIONS

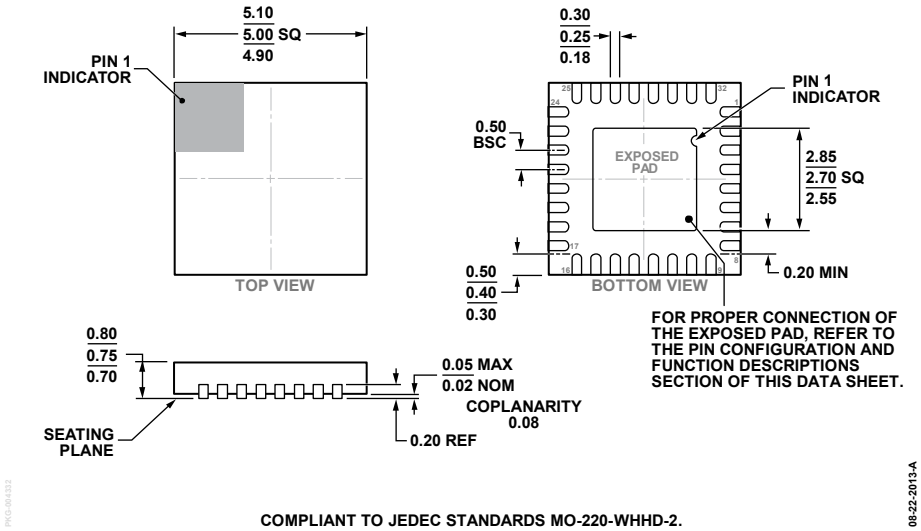


Figure 77. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	Package Description	Package Option
AD8260ACPZ-R7	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-21
AD8260ACPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-21
AD8260ACPZ-WP	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-21
AD8260-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D07192-0-5/16(B)

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