THE DATASHEET OF

AD7302BNZ

www.win-source.net 0086-755-83957316

2.7 V to 5.5 V, Parallel Input Dual Voltage Output 8-Bit DAC

AD7302

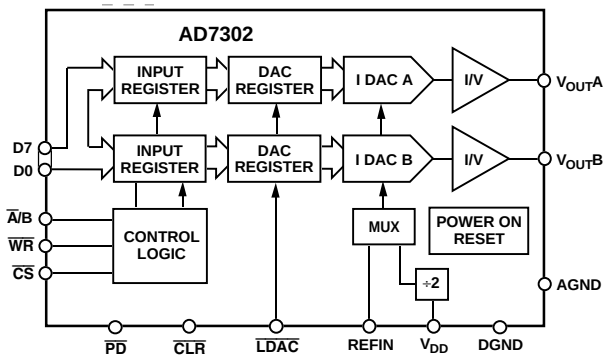
FEATURES

Two 8-Bit DACs In One Package
20-Lead DIP/SOIC/TSSOP Package
+2.7 V to +5.5 V Operation
Internal and External Reference Capability
DAC Power-Down Function
Parallel Interface
On-Chip Output Buffer
Rail-to-Rail Operation
Low Power Operation 3 mA max @ 3.3 V
Power-Down to 1 μA max @ 25°C

APPLICATIONS

Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7302 is a dual, 8-bit voltage out DAC that operates from a single +2.7 V to +5.5 V supply. Its on-chip precision output buffers allow the DAC outputs to swing rail to rail. The AD7302 has a parallel microprocessor and DSP-compatible interface with high speed registers and double buffered interface logic. Data is loaded to the registers on the rising edge of $\overline{CS}$ or $\overline{WR}$ and the $\overline{A}$/B pin selects either DAC A or DAC B.

Reference selection for AD7302 can be either an internal reference derived from the V_{DD} or an external reference applied at the REFIN pin. Both DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and can be cleared by using the asynchronous $\overline{CLR}$ input.

The low power consumption of this part makes it ideally suited to portable battery operated equipment. The power consumption is less than 10 mW at 3.3 V, reducing to 3 μW in power-down mode.

The AD7302 is available in a 20-pin plastic dual-in-line package, 20-lead SOIC and a 20-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Low Power, Single Supply Operation. This part operates from a single +2.7 V to +5.5 V supply and typically consumes 15 mW at 5 V, making it ideal for battery powered applications.
2. The on-chip output buffer amplifiers allow the outputs of the DACs to swing rail to rail with a settling time of typically 1.2 μs.
3. Internal or external reference capability.
4. High speed parallel interface.
5. Power-Down Capability. When powered down the DAC consumes less than 1 μA at 25°C.
6. Packaged in 20-lead DIP, SOIC and TSSOP packages.

REV. 0

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AD7302–SPECIFICATIONS (V_{DD} = +2.7 V to +5.5 V, Internal Reference; C_L = 100 pF, R_L = 10 kΩ to V_{DD} and GND; to T_{MAX} unless otherwise noted)

Parameter	B Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Relative Accuracy	±1	LSB max	Note 2
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	–0.75	LSB typ	
Zero Code Error @ 25°C	3	LSB typ	All Zeroes Loaded to DAC Register
Gain Error[3]	±1	% FSR typ	
Zero Code Temperature Coefficient	100	µV/°C typ	
DAC REFERENCE INPUT			
REFIN Input Range	1.0 to V_{DD}/2	V min to max	
REFIN Input Impedance	10	MΩ typ	
OUTPUT CHARACTERISTICS			
Output Voltage Range	0 to V_{DD}	V min to max	
Output Voltage Settling Time	2	µs max	Typically 1.2 µs
Slew Rate	7.5	V/µs typ	
Digital to Analog Glitch Impulse	1	nV-s typ	1 LSB Change Around Major Carry
Digital Feedthrough	0.2	nV-s typ	
Digital Crosstalk	0.2	nV-s typ	
Analog Crosstalk	±0.2	LSB typ	
DC Output Impedance	40	Ω typ	
Short Circuit Current	14	mA typ	
Power Supply Rejection Ratio[4]	0.0003	%/% max	ΔV_{DD} = ±10%
LOGIC INPUTS			
Input Current	±10	µA max	
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = +5 V
V_{INL}, Input Low Voltage	0.6	V max	V_{DD} = +3 V
V_{INH}, Input High Voltage	2.4	V min	V_{DD} = +5 V
V_{INH}, Input High Voltage	2.1	V min	V_{DD} = +3 V
Pin Capacitance	7	pF max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.5	V min/max	
I_{DD}			Both DACs Active and Excluding Load Currents
V_{DD} = 3.3 V			V_{IH} = V_{DD} and V_{IL} = GND
@ 25°C	2.8	mA max	Typically 2.3 mA
@ T_{MIN} to T_{MAX}	3	mA max	See Figures 6 and 7
V_{DD} = 5.5 V			V_{IH} = V_{DD} and V_{IL} = GND
@ 25°C	4.5	mA max	Typically 2.8 mA
@ T_{MIN} to T_{MAX}	5	mA max	See Figures 6 and 7
I_{DD} (Full Power-Down)			
@ 25°C	1	µA max	V_{IH} = V_{DD} and V_{IL} = GND
T_{MIN} to T_{MAX}	2	µA max	See Figure 18

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +105°C.

[2]Relative Accuracy is calculated using a reduced code range of 15 to 245.

[3]Gain error is specified between Codes 15 and 245. The actual error at Code 15 is typically 3 LSB.

[4]Guaranteed by characterization at product release, not production tested.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +2.7 V to +5.5 V; GND = 0 V; Reference = Internal V_{DD}/2 Reference; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	0	ns min	Address to Write Setup Time
t_2	0	ns min	Address Valid to Write Hold Time
t_3	0	ns min	Chip Select to Write Setup Time
t_4	0	ns min	Chip Select to Write Hold Time
t_5	20	ns min	Write Pulse Width
t_6	15	ns min	Data Setup Time
t_7	4.5	ns min	Data Hold Time
t_8	20	ns min	Write to $\overline{\text{LDAC}}$ Setup Time
t_9	20	ns min	$\overline{\text{LDAC}}$ Pulse Width
t_{10}	20	ns min	$\overline{\text{CLR}}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. tr and tf should not exceed 1 µs on any digital input.
[2]See Figure 1.

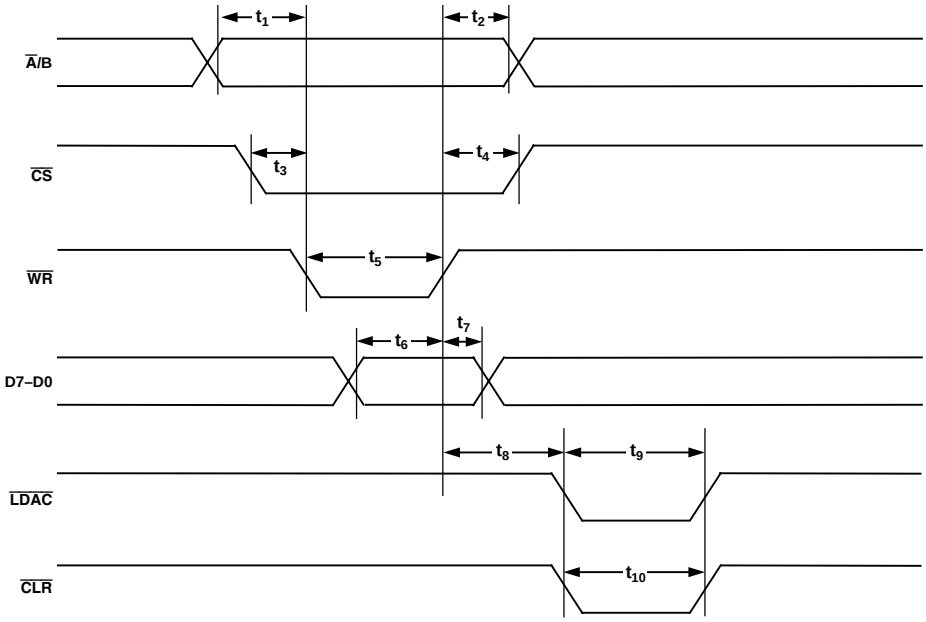


Figure 1. Timing Diagram for Parallel Data Write

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Reference Input Voltage to AGND . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V, 0.3 V
V_{OUT}A, V_{OUT}B to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 900 mW
  θ_{JA} Thermal Impedance . . . . . 102°C/W
  Lead Temperature (Soldering, 10 sec) . . . . . +260°C
TSSOP Package, Power Dissipation . . . . . 700 mW
  θ_{JA} Thermal Impedance . . . . . 143°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
SOIC Package, Power Dissipation . . . . . 870 mW
  θ_{JA} Thermal Impedance . . . . . 74°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7302 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

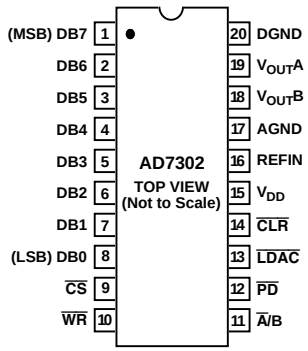
Model	Temperature Range	Package Options*
AD7302BN	–40°C to +105°C	N-20
AD7302BR	–40°C to +105°C	R-20
AD7302BRU	–40°C to +105°C	RU-20

*N = Plastic DIP; R = Small Outline; RU =Thin Shrink Small Outline.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1-8	D7–D0	Parallel Data Inputs. Eight-bit data is loaded to the input register of the AD7302 under the control of $\overline{CS}$ and $\overline{WR}$.
9	$\overline{CS}$	Chip Select. Active low logic input.
10	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input used in conjunction with $\overline{CS}$ and $\overline{A}$/B to write data to the selected DAC register.
11	$\overline{A}$/B	DAC Select. Address pin used to select writing to either DAC A or DAC B.
12	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to less than 1 μA.
13	$\overline{LDAC}$	Load DAC Logic Input. When this logic input is taken low both DAC outputs are simultaneously updated with the contents of their DAC registers. If $\overline{LDAC}$ is permanently tied low, the DACs are updated on the rising edge of $\overline{WR}$.
14	$\overline{CLR}$	Asynchronous Clear Input (Active Low). When this input is taken low the DAC registers are loaded with all zeroes and the DAC outputs are cleared to zero volts.
15	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V and should be decoupled to AGND.
16	REFIN	External Reference Input. This can used as the reference for both DACs. The range on this reference input is 1 V to V_{DD}/2. If REFIN is directly tied to V_{DD} the internal V_{DD}/2 reference is selected.
17	AGND	Analog Ground reference point and return point for all analog current on the part.
18	V_{OUT}B	Analog output voltage from DAC B. The output amplifier can swing rail to rail on its output.
19	V_{OUT}A	Analog output voltage from DAC A. The output amplifier can swing rail to rail on its output.
20	DGND	Digital Ground reference point and return point for all digital current on the part.

PIN CONFIGURATION



TERMINOLOGY

INTEGRAL NONLINEARITY

For the DACs, relative accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A graphical representation of the transfer curve is shown in Figure 14.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

ZERO CODE ERROR

Zero Code Error is the measured output voltage from V_{OUT} of either DAC when zero code (all zeros) is loaded to the DAC latch. It is due to a combination of the offset errors in the DAC and output amplifier. Zero scale error is expressed in LSBs.

GAIN ERROR

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale value. It includes full-scale errors but not offset errors.

DIGITAL-TO-ANALOG GLITCH IMPULSE

Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected and the $\overline{\text{LDAC}}$ used to update the DAC. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

DIGITAL FEEDTHROUGH

Digital Feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital inputs of the same DAC, but is measured when the DAC is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch impulse transferred to the output of one converter due to a digital code change to another DAC. It is specified in nV-s.

ANALOG CROSSTALK

Analog Crosstalk is a change in output of any DAC in response to a change in the output of the other DAC. It is measured in LSBs.

POWER SUPPLY REJECTION RATIO (PSRR)

This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied ±10%.

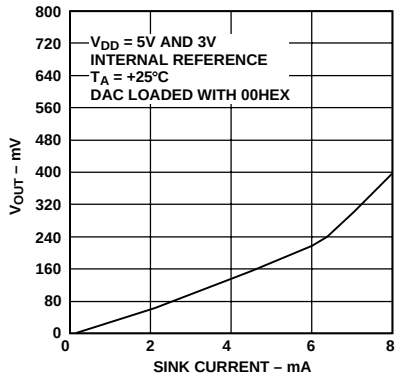


Figure 2. Output Sink Current Capability with V_{DD} = 3 V and V_{DD} = 5 V

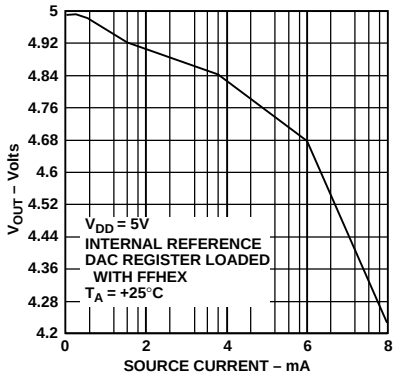


Figure 3. Output Source Current Capability with V_{DD} = 5 V

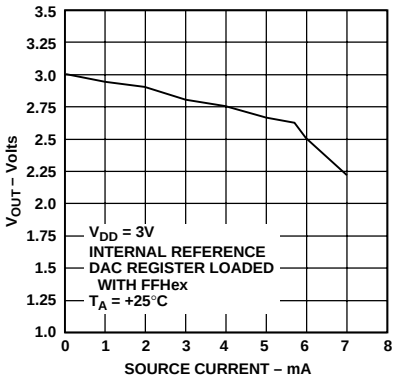


Figure 4. Output Source Current Capability with V_{DD} = 3 V

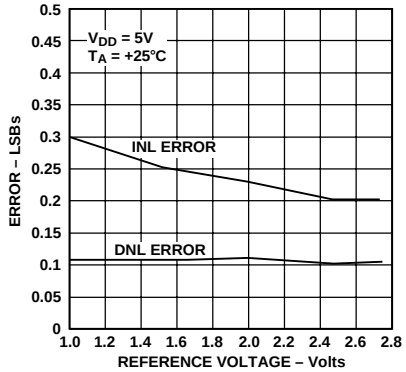


Figure 5. Relative Accuracy vs. External Reference

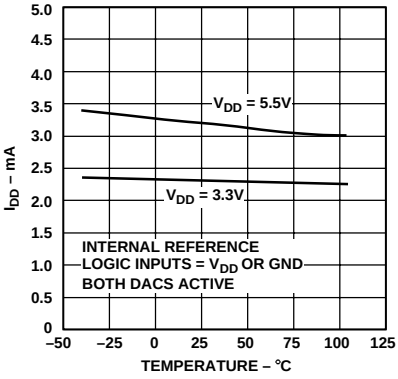


Figure 6. Typical Supply Current vs. Temperature

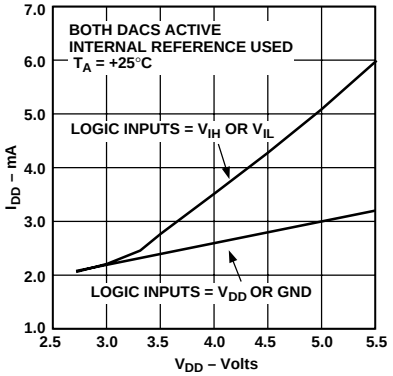


Figure 7. Typical Supply Current vs. Supply Voltage

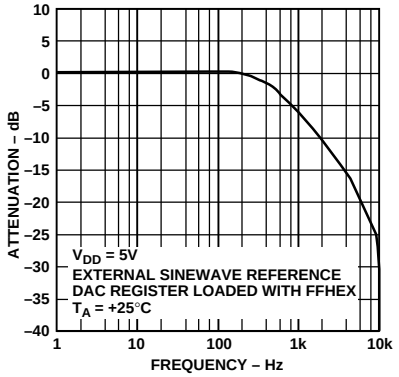


Figure 8. Large Scale Signal Frequency Response

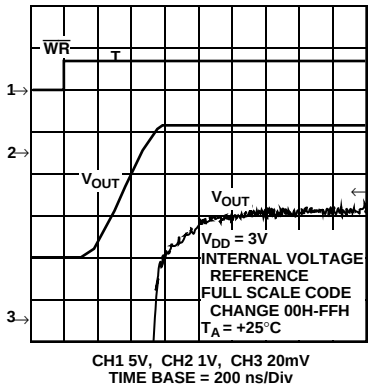


Figure 9. Full-Scale Settling Time

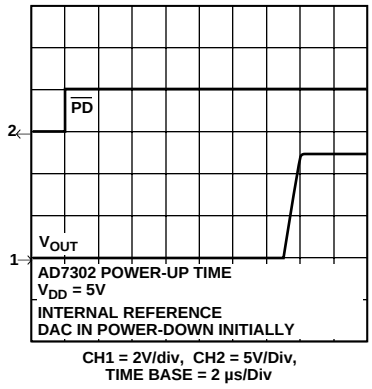


Figure 10. Exiting Power-Down (Full Power-Down)

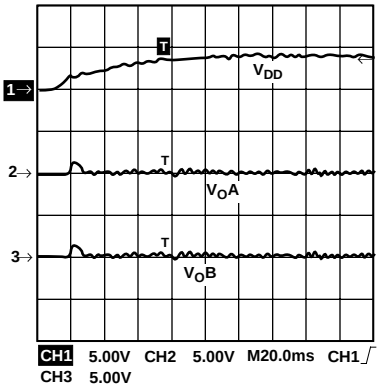


Figure 11. Power-On—RESET

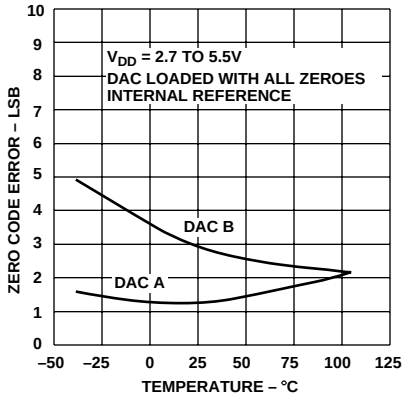


Figure 12. Zero Code Error vs. Temperature

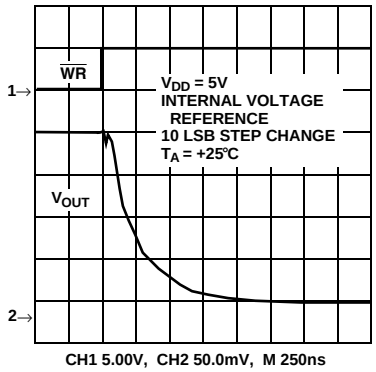


Figure 13. Small-Scale Settling Time

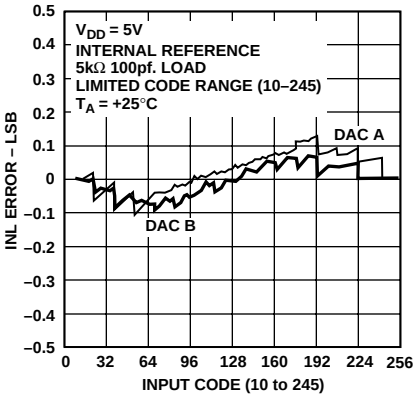


Figure 14. Integral Linearity Plot

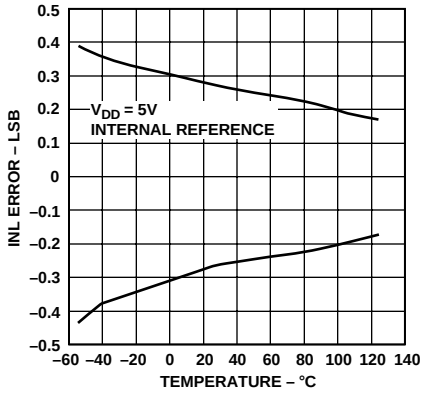


Figure 15. Typical INL vs. Temperature

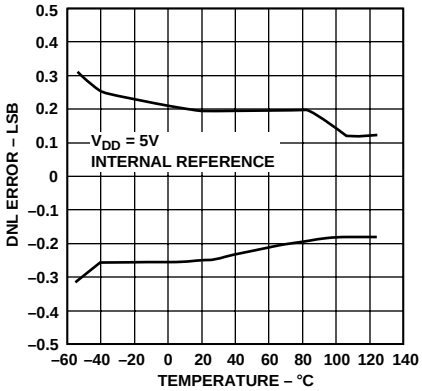


Figure 16. Typical DNL vs. Temperature

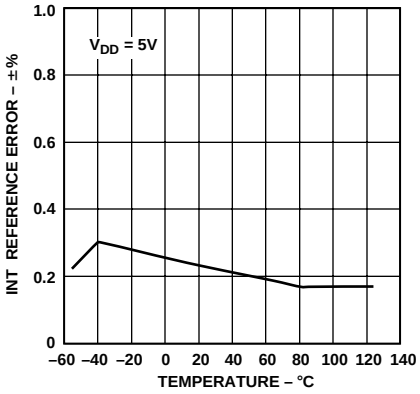


Figure 17. Typical Internal Reference Error vs. Temperature

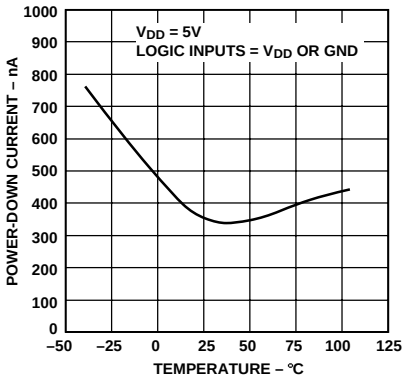


Figure 18. Power-Down Current vs. Temperature

GENERAL DESCRIPTION

D/A Section

The AD7302 is a dual 8-bit voltage output digital-to-analog converter. The architecture consists of a reference amplifier, a current source DAC followed by a current-to-voltage converter capable of generating rail-to-rail voltages on the output of the DAC. Figure 19 shows a block diagram of the basic DAC architecture.

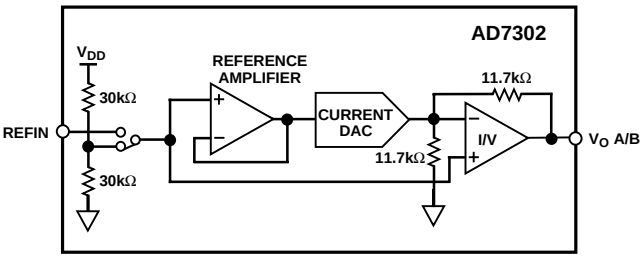


Figure 19. DAC Architecture

Both DAC A and DAC B outputs are internally buffered and these output buffer amplifiers have rail-to-rail output characteristics. The output amplifier is capable driving a load of 10 kΩ to both V_{DD} and ground in parallel with a 100 pF to ground. The reference selection for the DAC can either be internally generated from V_{DD} or externally applied through the REFIN pin. A comparator on the REFIN pin detects whether the required reference is the internally generated reference or the externally applied voltage to the REFIN pin. If REFIN is connected to V_{DD}, the reference selected is the internally generated $V_{DD}/2$ reference. When an externally applied voltage is more than one volt below V_{DD}, the comparator selection switches to the externally applied voltage to the REFIN pin. The range on the external reference input is from 1.0 V to $V_{DD}/2$. The output voltage from either DAC is given by:

$$V_O\,A/B = 2 \times V_{REF} \times (N/256)$$

where:

V_{REF} is the voltage applied to the external REFIN pin or $V_{DD}/2$ when the internal reference is selected.

N is the decimal equivalent of the code loaded to the DAC register and ranges from 0 to 255.

Reference

The AD7302 has the facility to use either an external reference applied through the REFIN pin or an internal reference generated from V_{DD}. Figure 20 shows the reference input arrangement where either the internal $V_{DD}/2$ reference or the externally applied reference can be selected.

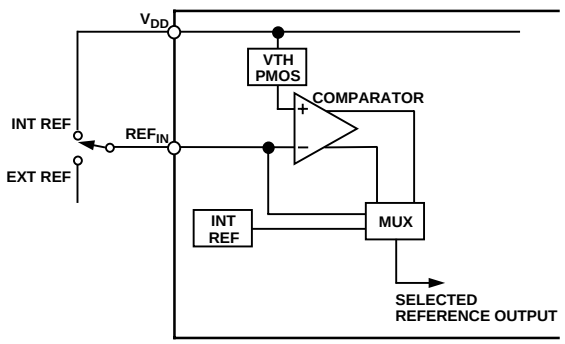


Figure 20. Reference Selection Circuitry

The internal reference is selected by tying the REFIN pin to V_{DD}. If an external reference is to be used, this can be directly applied to the REFIN pin; if this is 1 V below V_{DD}, the internal circuitry will select this externally applied reference as the reference source for the DAC.

Digital Interface

The AD7302 contains a fast parallel interface allowing this dual DAC to interface to industry standard microprocessors, microcontrollers and DSP machines. There are two modes in which this parallel interface can be configured to update the DAC outputs. The simultaneous update mode allows simultaneous updating of both DAC outputs. The automatic update mode allows each DAC to be individually updated following a write cycle. Figure 21 shows the internal logic associated with the digital interface. The PON STRB signal is internally generated from the power on reset circuitry and is low during the power-on reset phase of the power-up procedure.

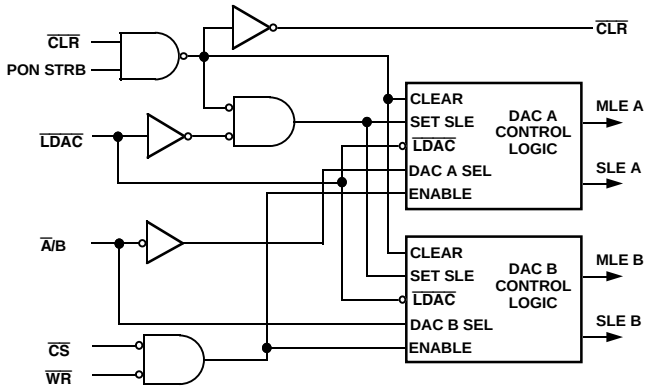


Figure 21. Logic Interface

The AD7302 has a double buffered interface, which allows for simultaneous updating of the DAC outputs. Figure 22 shows a block diagram of the register arrangement within the AD7302.

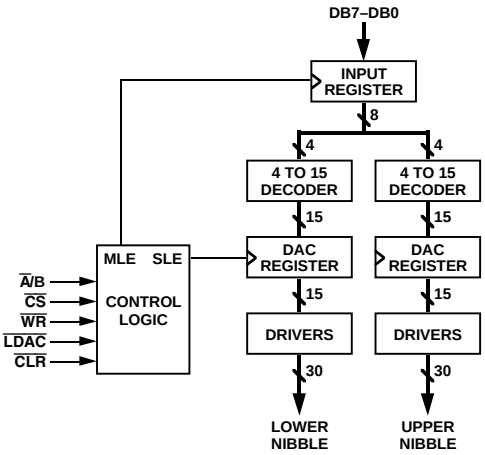


Figure 22. Register Arrangement

Automatic Update Mode

In this mode of operation the $\overline{\text{LDAC}}$ signal is permanently tied low. The state of the $\overline{\text{LDAC}}$ is sampled on the rising edge of $\overline{\text{WR}}$. $\overline{\text{LDAC}}$ being low allows the selected DAC register to be automatically updated on the rising edge of $\overline{\text{WR}}$. The output update occurs on the rising edge of $\overline{\text{WR}}$. Figure 23 shows the timing associated with the automatic update mode of operation and also the status of the various registers during this frame.

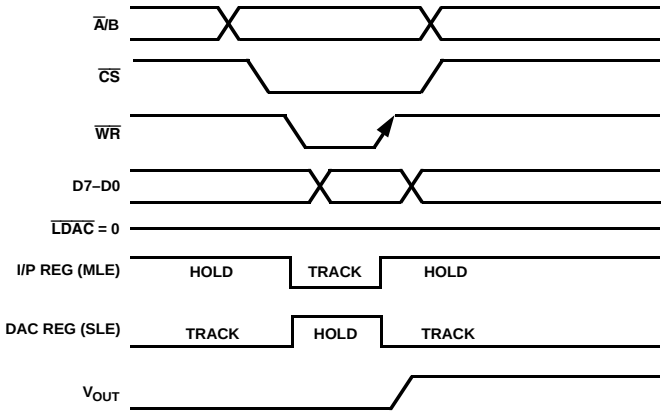


Figure 23. Timing and Register Arrangement for Automatic Update Mode

Simultaneous Update Mode

In this mode of operation the $\overline{\text{LDAC}}$ signal is used to update both DAC outputs simultaneously. The state of the $\overline{\text{LDAC}}$ is sampled on the rising edge of $\overline{\text{WR}}$. If $\overline{\text{LDAC}}$ is high, the automatic update mode is disabled and both DAC latches are updated at any time after the write by taking $\overline{\text{LDAC}}$ low. The output update occurs on the falling edge of $\overline{\text{LDAC}}$. $\overline{\text{LDAC}}$ must be taken back high again before the next data transfer takes place. Figure 24 shows the timing associated with the simultaneous update mode of operation and also the status of the various registers during this frame.

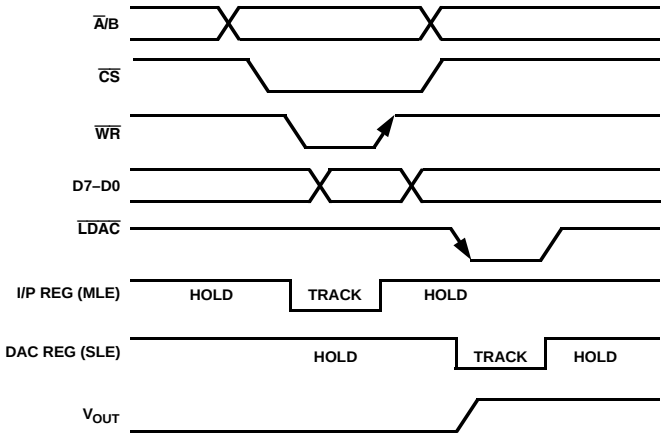


Figure 24. Timing and Register Arrangement for Simultaneous Update Mode

POWER-ON RESET

The AD7302 has a power-on reset circuit designed to allow output stability during power-up. This circuit holds the DACs in a reset state until a write takes place to the DAC. In the reset state all zeros are latched into the input registers of each DAC and the DAC registers are in transparent mode, thus the output of both DACs is held at ground potential until a write takes place to the DAC. The power-on reset circuitry generates a PON STRB signal, which is a gating signal used within the logic to identify a power-on condition.

POWER-DOWN FEATURES

The AD7302 has a power-down feature. This is implemented by exercising the external $\overline{\text{PD}}$ pin; an active low signal puts the complete DAC into power-down mode. When in power-down the current consumption of the device is reduced to 1 μA max at 25°C and 2 μA max over temperature, making the device suitable for use in portable battery powered equipment. When power-down is activated, the reference bias servo loop and the output amplifiers with their associated linear circuitry are powered down, the reference resistors are open circuited to further reduce the power consumption. The output sees a load of approximately 23 kΩ to GND when in power-down mode as shown in Figure 25. The contents of the data registers are unaffected when in power-down mode. The device comes out of power-down in typically 13 μs (see Figure 10).

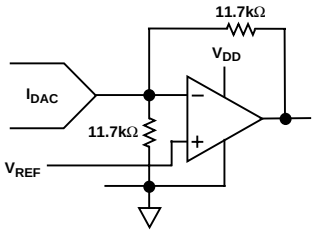


Figure 25. Output Stage During Power-Down

Analog Outputs

The AD7302 contains two independent voltage output DACs with 8-bit resolution and rail-to-rail operation. The output buffer provides a gain of two at the output. Figures 2 to 4 show the source and sink capabilities of the output amplifier. The slew rate of the output amplifier is typically 7.5 V/μs and has a full-scale settling to 8 bits with a 100 pF capacitive load in typically 1.2 μs.

The input coding to the DAC is straight binary. Table I shows the binary transfer function for the AD7302. Figure 26 shows the DAC transfer function for binary coding. Any DAC output voltage can be expressed as:

$$V_{OUT} = 2 \times V_{REF} (N/256)$$

where:

N is the decimal equivalent of the binary input code. N ranges from 0 to 255.

V_{REF} is the voltage applied to the external REFIN pin when the external reference is selected and is $V_{DD}/2$ if the internal reference is used.

Table I. Output Voltage for Selected Input Codes

Digital Input MSB . . . LSB	Analog Output
1111 1111	$2 \times 255/256 \times V_{REF}$ V
1111 1110	$2 \times 254/256 \times V_{REF}$ V
1000 0001	$2 \times 129/256 \times V_{REF}$ V
1000 0000	V_{REF} V
0111 1111	$2 \times 127/256 \times V_{REF}$ V
0000 0001	$2 \times V_{REF}/256$ V
0000 0000	0 V

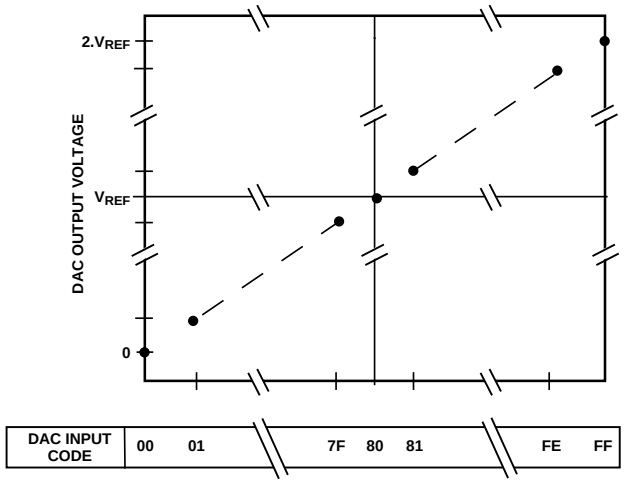


Figure 26. DAC Transfer Function

Figure 27 shows a typical setup for the AD7302 when using its internal reference. The internal reference is selected by tying the REFIN pin to V_{DD}. Internally in the reference section there is a reference detect circuit that will select the internal $V_{DD}/2$ based on the voltage connected to the REFIN pin. If REFIN is within a threshold voltage of a PMOS device (approximately 1 V) of V_{DD} the internal reference is selected. When the REFIN voltage is more than 1 V below V_{DD}, the externally applied voltage at this pin is used as the reference for the DAC. The internal reference on the AD7302 is $V_{DD}/2$, the output current to voltage converter within the AD7302 provides a gain of two. Thus the output range of the DAC is from 0 V to V_{DD}, based on Table I.

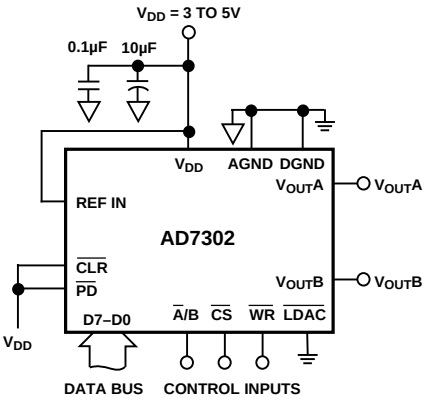


Figure 27. Typical Configuration Selecting the Internal Reference

Figure 28 shows a typical setup for the AD7302 when using an external reference. The reference range for the AD7302 is from 1 V to $V_{DD}/2$ V. Higher values of reference can be incorporated, but will saturate the output at both the top and bottom end of the transfer function. There is a gain of two from input to output on the AD7302. Suitable references for 5 V operation are the AD780 and REF192. For 3 V operation a suitable external reference would be the AD589 a 1.23 V bandgap reference.

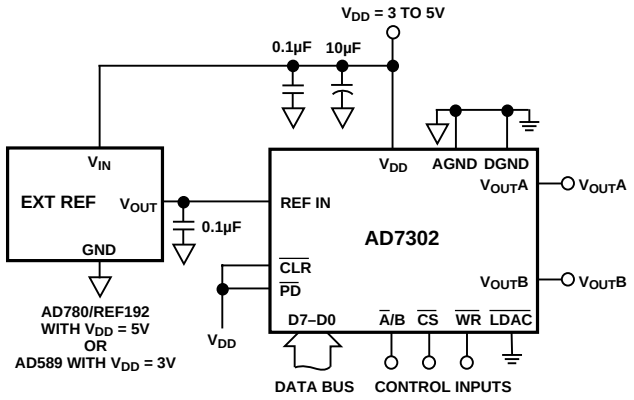


Figure 28. Typical Configuration Using An External Reference

MICROPROCESSOR INTERFACING

AD7302–ADSP-2101/ADSP-2103 Interface

Figure 29 shows an interface between the AD7302 and the ADSP-2101/ADSP-2103. The fast interface timing associated with the AD7302 allows easy interface to the ADSP-2101/ ADSP-2103.

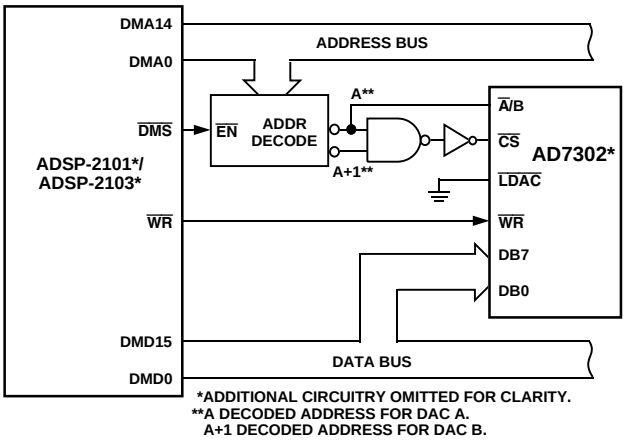


Figure 29. AD7302–ADSP-2101/ADSP-2103 Interface

Two addresses are decoded to select loading data to either DAC A or DAC B. $\overline{\text{LDAC}}$ is permanently tied low in this circuit, so the selected DAC output is updated on the rising edge of the $\overline{\text{WR}}$ signal.

Data is loaded to the AD7302 input register using the following ADSP-21xx instruction:

DM (*DAC*) = *MR0*

MR0 = ADSP-21xx MR0 Register.

DAC = Decoded DAC Address.

AD7302–TMS32020 Interface

Figure 30 shows an interface between the AD7302 and the TMS32020. The address decoder is used to decode the addresses for DAC A and DAC B. Data is loaded to the AD7302 using the following instruction:

OUT DAC, D

DAC = Decoded DAC Address.

D = Data Memory Address.

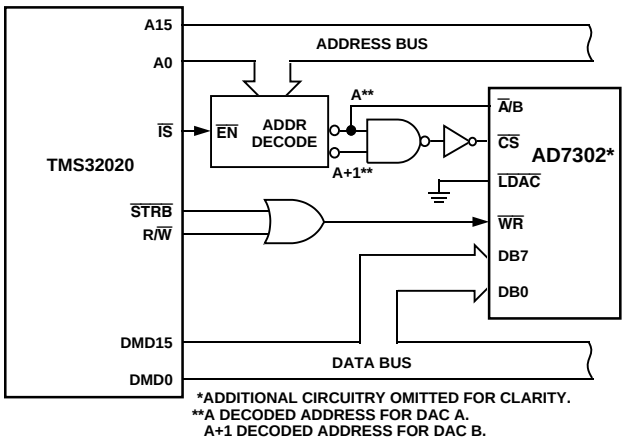


Figure 30. AD7302–TMS32020 Interface

In the circuit shown the $\overline{\text{LDAC}}$ is hardwired low, thus the selected DAC output is updated on the rising edge of $\overline{\text{WR}}$. Some applications may require simultaneous updating of both DACs in the AD7302. In this case the $\overline{\text{LDAC}}$ signal can be driven from an external timer or can be controlled by the microprocessor. One option for simultaneous updating is to decode the $\overline{\text{LDAC}}$ from the address bus so that a write operation at this address will simultaneously update both DAC outputs. A simple OR gate with one input driven from the decoded address and the second input from the $\overline{\text{WR}}$ signal will implement this function.

AD7302–8051/8088 Interface

Figure 31 shows a serial interface between the AD7302 and the 8051/8088 processors. The address decoder is used to decode the addresses for DAC A and DAC B.

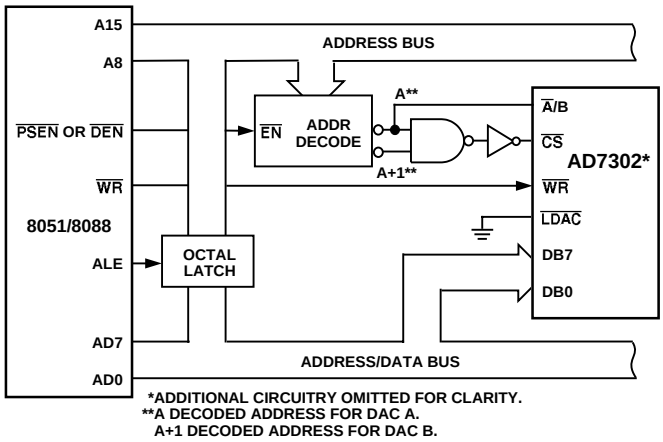


Figure 31. AD7302–8051//8088 Interface

APPLICATIONS

Bipolar Operation Using the AD7302

The AD7302 has been designed for single supply operation, but bipolar operation is achievable using the circuit shown in Figure 32. The circuit shown has been configured to achieve an output voltage range of –5 V < V_O < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = [(1+R4/R3) \times (R2/(R1+R2) \times (2 \times V_{REF} \times D/256)] - R4 \times V_{REF}/R3$$

where

D is the decimal equivalent of the code loaded to the DAC and

V_{REF} is the reference voltage input.

With V_{REF} = 2.5 V, R1 = R3 = 10 kΩ and R2 = R4 = 20 kΩ and V_{DD} = 5 V.

$$V_{OUT} = (10 \times D/256) - 5 \text{ V}$$

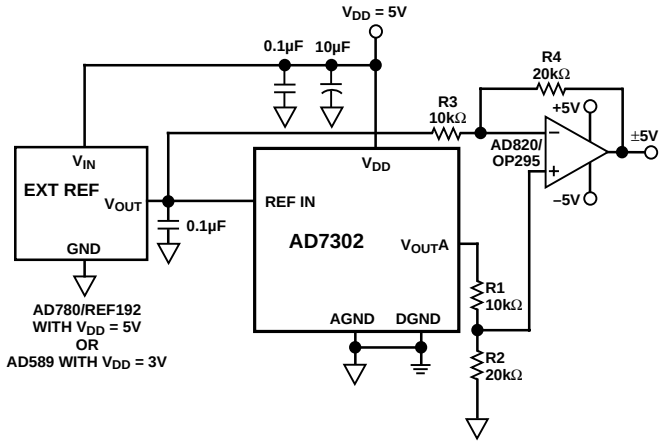


Figure 32. Bipolar Operation Using the AD7302

Decoding Multiple AD7302 in a System

The $\overline{CS}$ pin on the AD7302 can be used in applications to decode a number of DACs. In this application all DACs in the system receive the same input data, but only the $\overline{CS}$ to one of the DACs will be active at any one time allowing access to two channels in the system. The 74HC139 is used as a two-to-four line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 33 shows a diagram of a typical setup for decoding multiple AD7302 devices in a system. The built-in power-on reset circuit on the AD7302 ensures that the outputs of all DACs in the system power up with zero volts on their outputs.

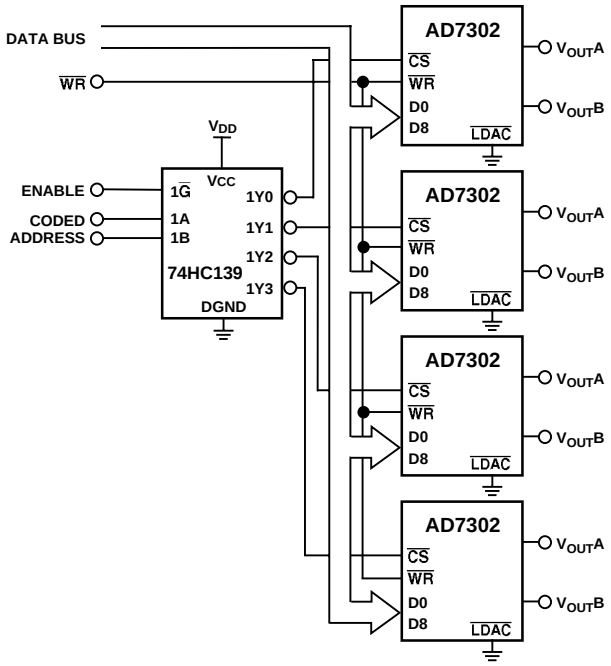


Figure 33. Decoding Multiple AD7302 DACs in a System

AD7302 As a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using the two DACs in the AD7302 is shown in Figure 34. The upper and lower limits for the test are loaded to DACs A and B, which in turn set the limits on the CMP04. If a signal at the V_{IN} input is not within the programmed window an LED will indicate the fail condition.

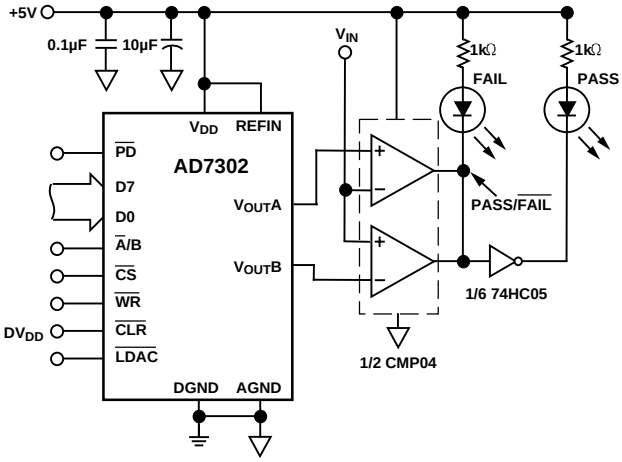


Figure 34. Programmable Window Detector

Programmable Current Source

Figure 35 shows the AD7302 used as the control element of a programmable current source. In this circuit the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the full-scale setting resistor of 470 Ω. Transistors suitable to place in the feedback loop of the amplifier include the BC107 or the 2N3904, which enable the current source to operate from a min V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the of the transistor. Suitable amplifiers include the AD820 and the OP295 both having rail-to-rail operation on their outputs. The current for any digital input code can be calculated as follows:

$$I = 2 \times V_{REF} \times D/(5E +3 \times 256)\ mA$$

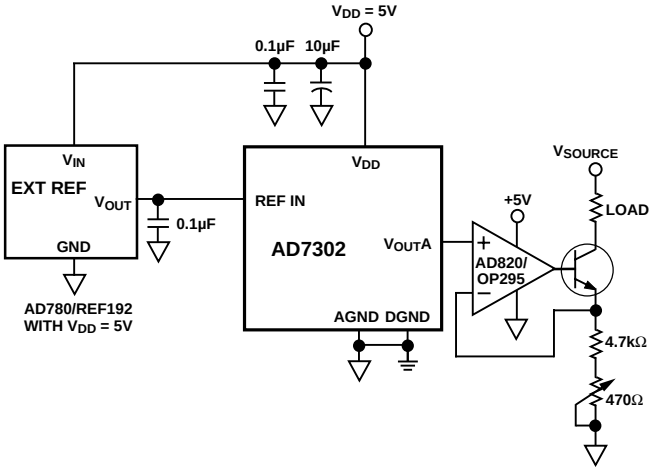


Figure 35. Programmable Current Source

Coarse and Fine Adjustment Using the AD7302

The DACs on the AD7302 can be paired together to form a coarse and fine adjustment function as shown in Figure 36. In this circuit DAC A is used to provide the coarse function while DAC B is used to provide the fine adjustment. Varying the ratio of R1 and R2 will vary the relative effect of the coarse and fine tune elements in the circuit. For the resistor values shown DAC B has a resolution of 148 µV giving a fine tune range of approximately 2 LSBs for operation with a V_{DD} of 5 V and a reference of 2.5 V. The amplifiers shown allow a rail-to-rail output voltage to be achieved on the output. A typical application for such a circuit would be in a setpoint controller.

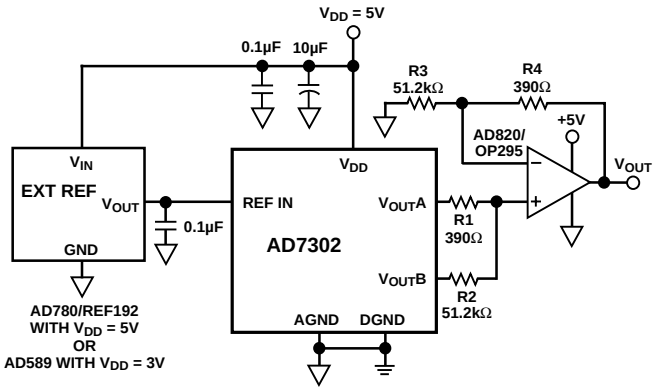


Figure 36. Coarse/Fine Adjust Circuit

Power Supply Bypassing and Grounding

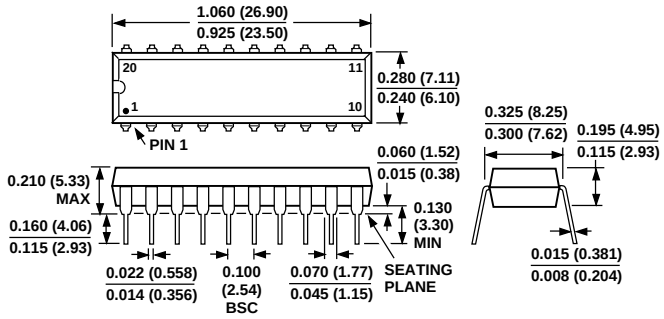
In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7302 is mounted should be designed so the analog and digital sections are separated and confined to certain areas of the board. If the AD7302 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only, a star ground point that should be established as closely as possible to the AD7302. The AD7302 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD7302 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

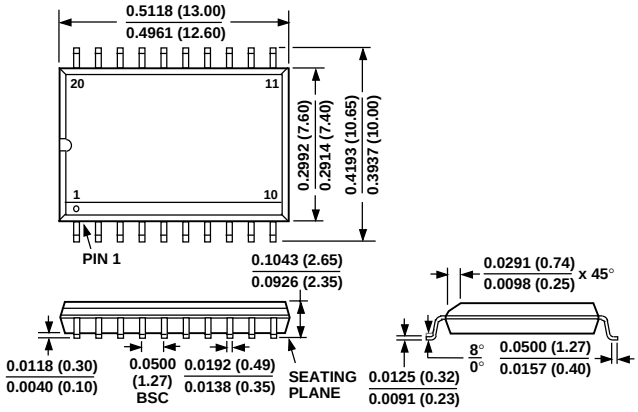
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

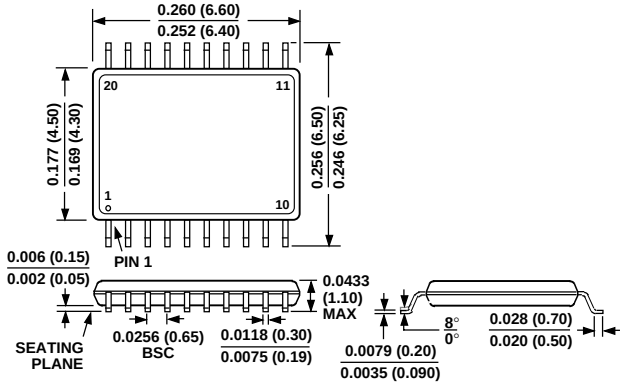
20-Lead Plastic DIP
(N-20)



20-Lead SO
(R-20)



20-Lead TSSOP
(RU-20)



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