



**THE DATASHEET OF  
AD7542GKNZ**



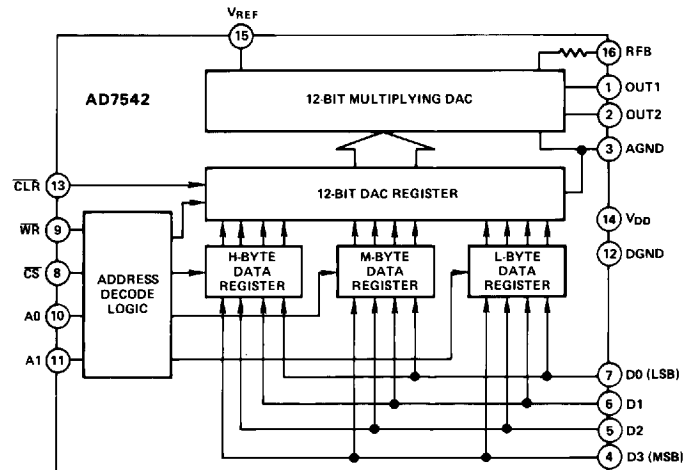
**FEATURES**

- Resolution: 12 Bits**
- Nonlinearity:  $\pm 1/2\text{LSB } T_{\min}$  to  $T_{\max}$**
- Low Gain Drift: 2ppm/°C typ, 5ppm/°C max**
- Microprocessor Compatible**
- Full 4-Quadrant Multiplication**
- Fast Interface Timing**
- Low Power Dissipation: 40mW max**
- Low Cost**
- Small Size: 16-pin DIP and 20-Terminal Surface Mount Package**
- Latch Free (Protection Schottky Not Required)**

**GENERAL DESCRIPTION**

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

**FUNCTIONAL BLOCK DIAGRAM**


The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP and 20 terminal surface mount packages) and easy μP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

**REV. A**

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# AD7542—SPECIFICATIONS ( $V_{DD} = +5V$ , $V_{REF} = +10V$ , $V_{OUT1} = V_{OUT2} = 0V$ unless otherwise noted)

Parameter	Limit At $T_A = +25^\circ C$	Limit At <sup>1</sup> $T_A = -40^\circ C$ to $+85^\circ C$	Limit At <sup>1</sup> $T_A = -55^\circ C$ & $+125^\circ C$	Units	Conditions/Comments
<b>ACCURACY</b>					
Resolution	12	12	12	Bits	
Relative Accuracy <sup>2</sup>					
J, A, S Versions	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	
K, B, T Versions	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max	
GK, GB, GT Versions	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max	
Differential Nonlinearity <sup>2</sup>					
J, A, S Versions	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	All grades are guaranteed monotonic $T_{min}$ to $T_{max}$
K, B, T Versions	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	
GK, GB, GT Versions	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	
Gain Error <sup>2</sup>					
J, K, A, B, S, T	$\pm 3$	$\pm 4$	$\pm 4$	LSB max	Using internal $R_{FB}$ only (gain error can be trimmed to zero using circuits of Figure 4 & 5)
GK, GB, GT	$\pm 1$	$\pm 1$	$\pm 2$	LSB max	
Gain Temperature Coefficient $\Delta$ Gain/ $\Delta$ Temperature	5	5	5	ppm/ $^\circ C$ max	Typical value is 2ppm/ $^\circ C$
Power Supply Rejection $\Delta$ Gain/ $\Delta V_{DD}$	0.005	0.01	0.01	% per % max	$V_{DD} = +4.75V$ to $+5.25V$
Output Leakage Current					
$I_{OUT1}$	10	10	200	nA max	DAC Register loaded with all 0s
$I_{OUT2}$	10	10	200	nA max	DAC Register loaded with all 1s
<b>DYNAMIC PERFORMANCE</b>					
Current Settling Time <sup>3</sup>	2.0	2.0	2.0	$\mu s$ max	To 1/2LSB, $I_{OUT1}$ load = 100 $\Omega$ . DAC output measured from falling edge of $\overline{WR}$ .
Multiplying Feedthrough Error <sup>3</sup>	2.5	2.5	2.5	mV p-p max	$V_{REF} = \pm 10V$ , 10kHz sine wave
<b>REFERENCE INPUT</b>					
Input Resistance	8/15/25	8/15/25	8/15/25	k $\Omega$ min/typ/max	
<b>ANALOG OUTPUTS</b>					
Output Capacitance					
$C_{OUT1}^3$	75	75	75	pF max	DAC register loaded to 0000 0000 0000
$C_{OUT1}^3$	260	260	260	pF max	DAC register loaded to 1111 1111 1111
$C_{OUT2}^3$	75	75	75	pF max	DAC register loaded to 1111 1111 1111
$C_{OUT2}^3$	260	260	260	pf max	DAC register loaded to 0000 0000 0000
<b>LOGIC INPUTS</b>					
$V_{INH}$ (Logic HIGH Voltage)	+2.4	+2.4	+2.4	V min	$V_{IN} = 0V$ or $V_{DD}$
$V_{INL}$ (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
$I_{IN}^4$	1	1	1	$\mu A$ max	
$C_{IN}$ (Input Capacitance) <sup>3</sup>	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (See Figures 4 and 5). Data is Loaded into Data Registers in 4-Bit Bytes.				
<b>SWITCHING CHARACTERISTICS<sup>5</sup></b>	(See Figure 1)				
$t_{WR}$	80	120	160	ns min	$t_{WR}$ : WRITE pulse width
$t_{AWH}$	0	10	10	ns min	$t_{AWH}$ : Address-to-WRITE hold time
$t_{CWH}$	0	10	10	ns min	$t_{CWH}$ : Chip select-to-WRITE hold time
$t_{CLR}$	200	200	250	ns min	$t_{CLR}$ : Minimum CLEAR pulse width
$t_{CWS}$	10	20	20	ns min	$t_{CWS}$ : Chip select-to-WRITE setup time
$t_{AWS}$	40	40	40	ns min	$t_{AWS}$ : Address valid-to-WRITE setup time
$t_{DS}$	60	100	100	ns min	$t_{DS}$ : Data setup time
$t_{DH}$	10	10	10	ns min	$t_{DH}$ : Data hold time
<b>POWER SUPPLY</b>					
$V_{DD}$ (Supply Voltage)	+5	+5	+5	V	$\pm 5\%$ for specified performance
$I_{DD}$ (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = $V_{INH}$ or $V_{INL}$

## NOTES

<sup>1</sup>Temperature Ranges as follows: J, K, GK Versions;  $-40^\circ C$  to  $+85^\circ C$   
A, B, GB Versions;  $-40^\circ C$  to  $+85^\circ C$   
S, T, GT Versions;  $-55^\circ C$  to  $+125^\circ C$

<sup>2</sup>See definitions on next page.

<sup>3</sup>Guaranteed but not tested.

<sup>4</sup>Logic inputs are MOS gates. Typical input current ( $+25^\circ C$ ) is less than  $-1nA$ .

<sup>5</sup>Sample tested at  $+25^\circ C$  to ensure compliance.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS\*

(\*T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to AGND	0V, +7V
V <sub>DD</sub> to DGND	0V, +7V
AGND to DGND	V <sub>DD</sub> + 0.3V
DGND to AGND	V <sub>DD</sub> + 0.3V
Digital Input Voltage to GND	-0.3V, V <sub>DD</sub> + 0.3V
V <sub>OUT1</sub> , V <sub>OUT2</sub> to AGND	-0.3V, V <sub>DD</sub> + 0.3V
V <sub>REF</sub> to AGND	±25V
V <sub>RFB</sub> to AGND	±25V

## Power Dissipation (Package)

Plastic	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic	
To +75°C	450mW
Derates above +75°C by	6mW/°C

## Operating Temperature Range

Commercial (J, K, GK Versions)	-40°C to +85°C
Industrial (A, B, GB Versions)	-40°C to +85°C
Extended (S, T, GT Versions)	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

\*COMMENTS: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



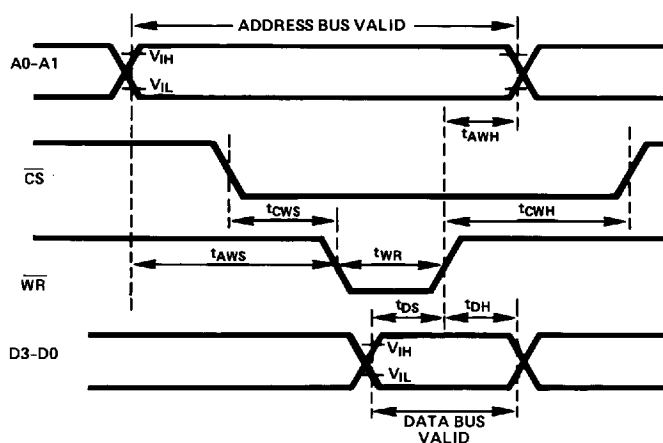
## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Relative Accuracy	Gain Error	Package Option <sup>2</sup>
AD7542JN	-40°C to +85°C	±1LSB	±3LSB	N-16
AD7542KN	-40°C to +85°C	±1/2LSB	±3LSB	N-16
AD7542GKN	-40°C to +85°C	±1/2LSB	±1LSB	N-16
AD7542JP	-40°C to +85°C	±1LSB	±3LSB	P-20A
AD7542KP	-40°C to +85°C	±1/2LSB	±3LSB	P-20A
AD7542GKP	-40°C to +85°C	±1/2LSB	±1LSB	P-20A
AD7542AQ	-40°C to +85°C	±1LSB	±3LSB	Q-16
AD7542BQ	-40°C to +85°C	±1/2LSB	±3LSB	Q-16
AD7542GBQ	-40°C to +85°C	±1/2LSB	±1LSB	Q-16
AD7542SQ	-55°C to +125°C	±1LSB	±3LSB	Q-16
AD7542TQ	-55°C to +125°C	±1/2LSB	±3LSB	Q-16
AD7542GTQ	-55°C to +125°C	±1/2LSB	±1LSB	Q-16
AD7542SE	-55°C to +125°C	±1LSB	±3LSB	E-20A
AD7542TE	-55°C to +125°C	±1/2LSB	±3LSB	E-20A
AD7542GTE	-55°C to +125°C	±1/2LSB	±1LSB	E-20A

### NOTES

<sup>1</sup>To order MIL-STD-883 Class B processed parts, add /883B to part number.

<sup>2</sup>E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

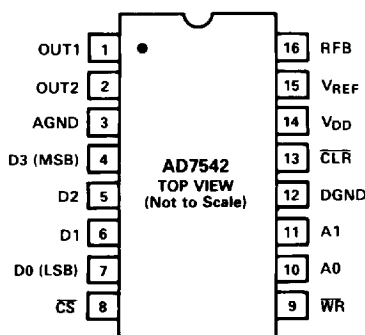


NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS  $\frac{V_{IH} + V_{IL}}{2}$

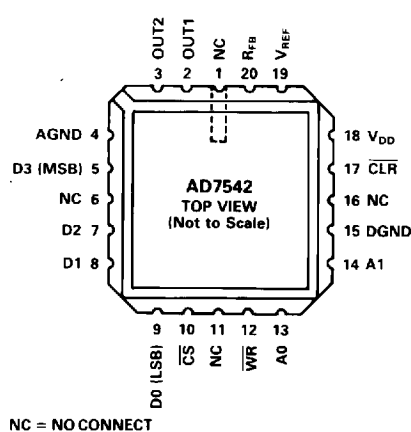
Figure 1. AD7542 Timing Diagram

## PIN CONFIGURATIONS

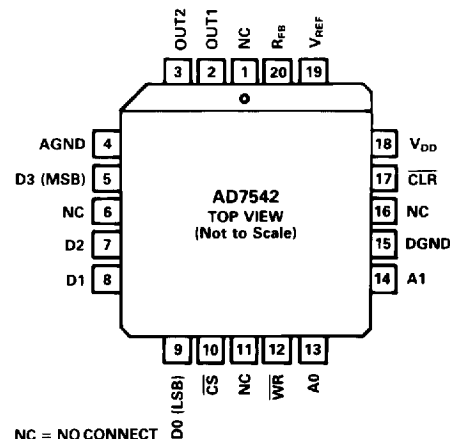
### DIP



### LCSS



### PLCC



# AD7542

## TERMINOLOGY

### RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

### DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$ LSB max over the operating temperature range insures monotonicity.

### GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of  $-4095/4096$ . Gain error is adjustable using external trims as shown in Figures 4 and 5.

### OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

### MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from  $V_{REF}$  terminal to OUT1 with DAC register loaded to all 0s.

Table 1. Pin Function Description (DIP Pin Numbers)

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at ground
3	AGND	Analog Ground
4	D3	Data Input (MSB)
5	D2	Data Input
6	D1	Data Input
7	D0	Data Input (LSB)
8	$\overline{CS}$	Chip Select Input
9	$\overline{WR}$	WRITE Input
10	A0	Address Bus Input
11	A1	Address Bus Input
12	DGND	Digital Ground
13	$\overline{CLR}$	Clear Input
14	$V_{DD}$	+5V Supply Input
15	$V_{REF}$	Reference Input
16	$R_{FB}$	DAC Feedback Resistor

## Analog Circuit Description

### GENERAL CIRCUIT INFORMATION

The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used—that is, the binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

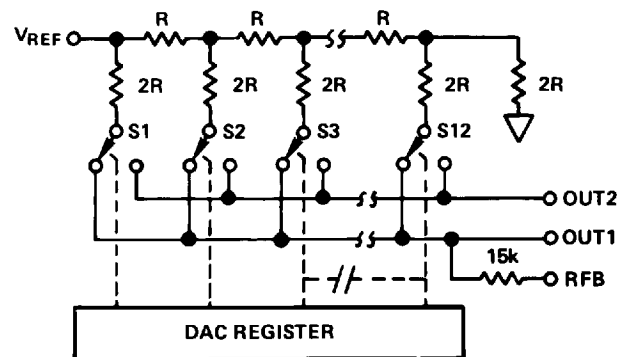


Figure 2. D/A Simplified Circuit Diagram

One of the current switches is shown in Figure 3. The input resistance at  $V_{REF}$  (Figure 2) is always equal to  $R_{LDR}$  ( $R_{LDR}$  is the R/2R ladder characteristic resistance and is equal to value "R"). Since  $R_{IN}$  at the  $V_{REF}$  pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient  $R_{FB}$  is recommended to define scale factor.)

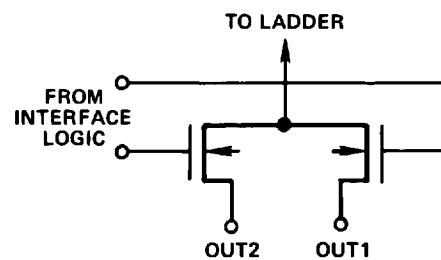


Figure 3. N-Channel Current Steering Switch

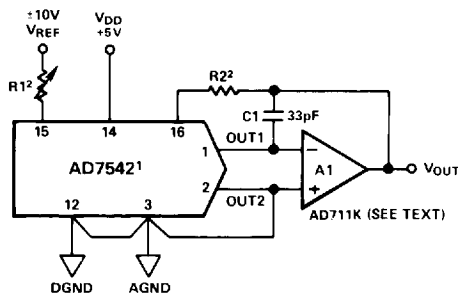
## UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at  $V_{REF}$ , the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for  $V_{OUT} = -V_{REF}$  (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 33pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide  $V_{OS} \leq 10\%$  of the voltage resolution at  $V_{OUT}$ . Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at  $V_{OUT}$  equal to  $I_B$  times the DAC feedback resistance, nominally 15k $\Omega$ ). The AD711K is a high-speed implanted FET-input op amp with low, factory-trimmed  $V_{OS}$ .



NOTES  
1. LOGIC INPUTS OMITTED FOR CLARITY, DIP PIN NUMBERS SHOWN.  
2. SEE APPLICATION HINT NO. 4.

Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Table II. Unipolar Binary Code Table for Circuit of Figure 4

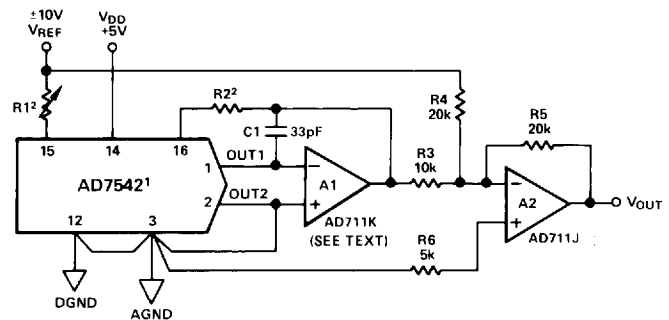
BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, $V_{OUT}$
MSB	LSB	
1111	1111 1111	$-V_{REF} \left( \frac{4095}{4096} \right)$
1000	0000 0000	$-V_{REF} \left( \frac{2048}{4096} \right) = -1/2 V_{REF}$
0000	0000 0001	$-V_{REF} \left( \frac{1}{4096} \right)$
0000	0000 0000	0V

## BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the circuit provides full 4-quadrant multiplication.

With the DAC register loaded to 1000 0000 0000, adjust R1 for  $V_{OUT} = 0V$  (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for  $V_{OUT} = 0V$ ). Full scale trimming can be accomplished by adjusting the amplitude of  $V_{REF}$  or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low  $V_{OS}$  and low  $I_B$ . R3, R4 and R5 must be selected for matching and tracking. Mismatch of R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.



NOTES  
1. LOGIC INPUTS OMITTED FOR CLARITY, DIP PIN NUMBERS SHOWN.  
2. SEE APPLICATION HINT NO. 4.

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, $V_{OUT}$
MSB	LSB	
1111	1111 1111	$+V_{REF} \left( \frac{2047}{2048} \right)$
1000	0000 0001	$+V_{REF} \left( \frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{REF} \left( \frac{1}{2048} \right)$
0000	0000 0000	$-V_{REF} \left( \frac{2048}{2048} \right)$

# AD7542

## INTERFACE LOGIC

### INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 6.  $\overline{CS}$  is the decoded *device* address, and is derived by decoding the three higher order address bits. A0 and A1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e., load high byte, middle byte, low byte or DAC register). Table IV shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 1.

Additionally, the  $\overline{CLR}$  input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 4), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 5), a CLEAR causes the DAC output to go to  $-V_{REF}$ .

In summary:

1. The AD7542 DAC register can be asynchronously cleared with the  $\overline{CLR}$  input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

Table IV. AD7542 Truth Table

AD7542 Control Inputs					AD7542 Operation
A <sub>1</sub>	A <sub>0</sub>	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$	
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000
X	X	1	X	1	No Operation Device Not Selected
0	0	0	$\overline{\uparrow}$	1	Load LOW Byte <sup>5</sup> Data Register On Edge As Shown
0	1	0	$\overline{\uparrow}$	1	Load MIDDLE Byte <sup>5</sup> Data Register On Edge As Shown
1	0	0	$\overline{\uparrow}$	1	Load HIGH Byte <sup>5</sup> Data Register On Edge As Shown
1	1	0	$\overline{\square}$	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers <sup>6</sup>

NOTES:

<sup>1</sup> 1 indicates logic HIGH

<sup>2</sup> 0 indicates logic LOW

<sup>3</sup> X indicates don't care

<sup>4</sup>  $\overline{\uparrow}$  indicates LOW to HIGH transition <sup>5</sup> MSB  $\rightarrow$  XXXX XXXX XXXX  $\leftarrow$  LSB

high middle low  
byte byte byte

<sup>6</sup> These control signals are level triggered.

### AD7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 6. Since the AD7542 contains four registers each AD7542 is assigned four locations in memory. A0 and A1 provides the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the four addresses. Table V gives a sample loading subroutine written in re-entrant form.

Choosing an arbitrary start address of PPQQ, locations PPQQ, PPQQ+1 and PPQQ+2 select the low, middle and high byte registers respectively while address PPQQ+3 selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1.

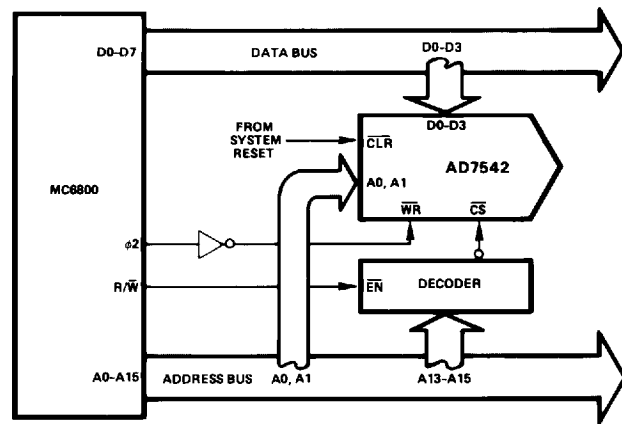


Figure 6. Interfacing the AD7542 to an MC6800 Microprocessor

Table V. Sample Routine for AD7542-6800 Interface

WWZZ	JSR	WWZZ	
	PSH A		PUSH ACC. A ONTO STACK
	TPA		
	PSH A		PUSH CCR ONTO STACK
	LDA A	XXYY	
	STA A	PPQQ	LOAD LOW BYTE
	ROR A		
	ROR A		
	ROR A		
	ROR A		
	STA A	PPQQ+1	LOAD MIDDLE BYTE
	LDA A	XXYY+1	
	STA A	PPQQ+2	LOAD HIGH BYTE
	STA A	PPQQ+3	LOAD DAC REGISTER
	PUL A		
	TAP		POP CCR FROM STACK
	PUL A		POP ACC. A FROM STACK
	RTS		RETURN TO MAIN PROGRAM

## AD7542 INTERFACE TO 8085

A typical 8085 system configuration is shown in Figure 7. The AD7542 CS input is decoded from the three high order address lines A13-A15. The 8085 WR output is directly connected to the WR input of the AD7542. Table VI gives a sample loading subroutine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYX and XXYX+1. The four most significant data bits are assumed to occupy the lower half of XXYX+1. As before, arbitrary addresses PPQQ to PPQQ+3 select the low byte, middle byte, high byte and DAC registers respectively.

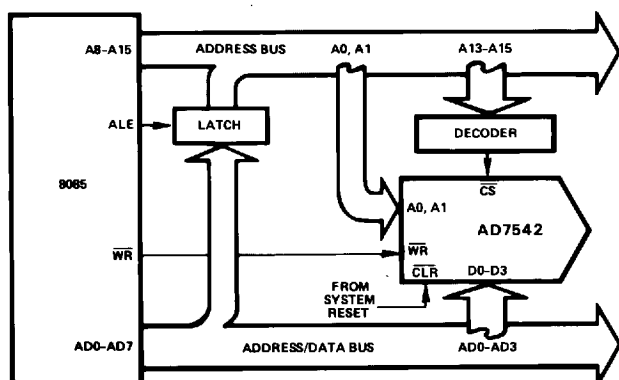


Figure 7. Interfacing the AD7542 to an 8085 Microprocessor

Table VI. Sample Routine for AD7542-8085 Interface

	CALL	7542	
7542	PUSH	PSW	PUSH REGISTER CONTENTS
	PUSH	B	ONTO STACK
	PUSH	H	
	LXI	H, XXYX	
	MOV	A, M	
	STA	PPQQ	LOAD LOW BYTE
	MVI	B, 04	
LOOP	RAR		
	DCR	B	
	JNZ	LOOP	
	STA	PPQQ+1	LOAD MIDDLE BYTE
	INX	H	
	MOV	A, M	
	STA	PPQQ+2	LOAD HIGH BYTE
	STA	PPQQ+3	LOAD DAC REGISTER
	POP	H	POP REGISTER CONTENTS
	POP	B	FROM STACK
	POP	PSW	
	RET		RETURN TO MAIN PROGRAM

## APPLICATION HINTS

The AD7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. **GENERAL GROUND MANAGEMENT:** Voltage differences between the AD7542 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7542. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7542 AGND and DGND pins (1N914 or equivalent).

2. **OUTPUT AMPLIFIER OFFSET:** CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a non-linearity term at the amplifier output which depends on  $V_{OS}$  ( $V_{OS}$  is amplifier input offset voltage). This non-linearity term adds to the R/2R nonlinearity. To maintain specified operation, it is recommended that amplifier  $V_{OS}$  be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution =  $V_{REF} (2^{-n})$  where n is the number of bits exercised].
3. **HIGH FREQUENCY CONSIDERATIONS:** AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. **GAIN TEMPERATURE COEFFICIENTS:** The gain temperature coefficient of the AD7542 has a maximum value of  $5 \text{ ppm}/^\circ\text{C}$  and a typical value of  $2 \text{ ppm}/^\circ\text{C}$ . This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a  $100^\circ\text{C}$  temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 4 and 5 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows: -

$$\text{Temperature Coefficient contribution due to R1} = - \frac{R_1}{R_{IN}} (\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = + \frac{R_2}{R_{IN}} (\gamma_2 + 300)$$

Where  $\gamma_1$  and  $\gamma_2$  are the temperature coefficients in  $\text{ppm}/^\circ\text{C}$  of R1 and R2 respectively and  $R_{IN}$  is the DAC input resistance at the  $V_{REF}$  terminal (pin 2). For high quality wire-wound resistors and trimming potentiometers  $\gamma$  is of the order of  $50 \text{ ppm}/^\circ\text{C}$ . It will be seen that if R1 and R2 are small compared with  $R_{IN}$ , their contribution to gain temperature coefficient will also be small. For the standard AD7542 gain error specification of  $\pm 3 \text{ LSBs}$  it is recommended that  $R_1 = 50 \Omega$  and  $R_2 = 25 \Omega$ . With  $\gamma = 50$  these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.025}{8} (50 + 300) = 6 \text{ ppm}/^\circ\text{C}$$

However, if the AD7542GTD is used which has a specified gain error of  $\pm 1 \text{ LSB}$ , then with  $R_1 = 10 \Omega$  and  $R_2 = 5 \Omega$  the overall maximum gain temperature coefficient is increased by only  $0.25 \text{ ppm}/^\circ\text{C}$ . Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630-10-6/81 available from Analog Devices.

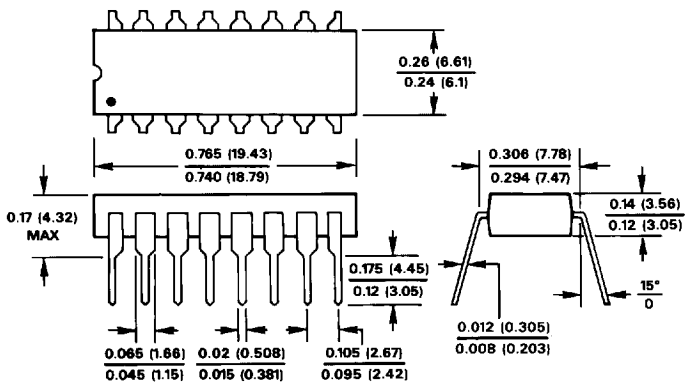
5. For additional information on multiplying DACs refer to "CMOS DAC Application Guide," Publication Number G872a-15-4/86, available from Analog Devices.

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

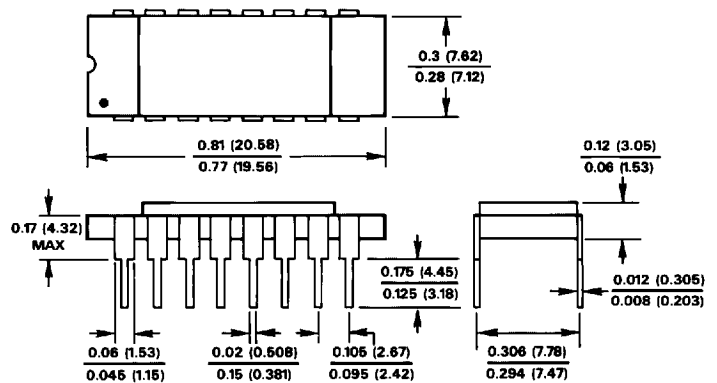
Dimensions shown in inches and (mm).

16-Pin Plastic DIP (Suffix N)



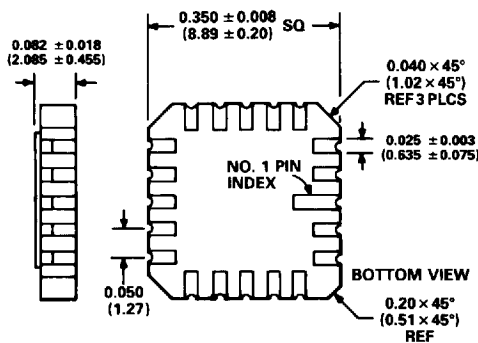
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

16-Pin Ceramic DIP (Suffix D)

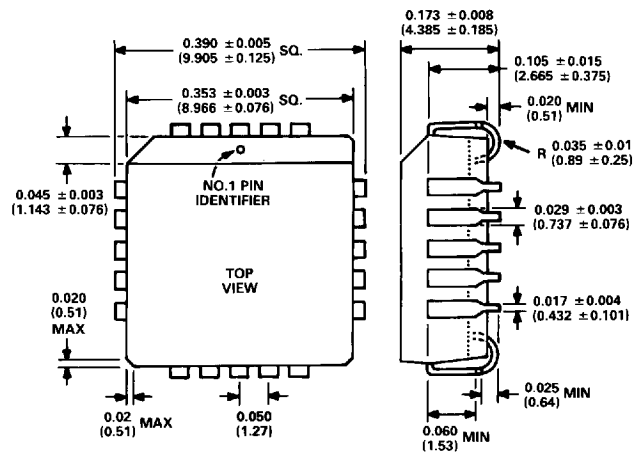


1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
2. LEADS WILL BE EITHER GOLD OR TIN PLATED

20-Terminal  
Leadless Ceramic Chip  
Carrier (Suffix E)



20-Terminal  
Plastic Leaded  
Chip Carrier (Suffix P)



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