



**THE DATASHEET OF
NCP3334DADJG**



NCP3334

Voltage Regulator - High Accuracy, Ultra Low Iq, Adjustable, Low Dropout

500 mA

The NCP3334 is a high performance, low dropout regulator. With accuracy of $\pm 0.9\%$ over line and load and ultra-low quiescent current and noise it encompasses all of the necessary features required by today's consumer electronics. This unique device is guaranteed to be stable without a minimum load current requirement and stable with any type of capacitor as small as 1.0 μF . The NCP3334 offers reverse bias protection.

Features

- High Accuracy Over Line and Load ($\pm 0.9\%$ at 25°C)
- Ultra-Low Dropout Voltage
- Low Noise
- Low Shutdown Current (0.07 μA)
- Reverse Bias Protected
- 2.6 V to 12 V Supply Range
- Thermal Shutdown Protection
- Current Limitation
- Requires Only 1.0 μF Output Capacitance for Stability
- Stable with Any Type of Capacitor (including MLCC)
- No Minimum Output Current Required for Stability
- This is a Pb-Free Device

Applications

- PCMCIA Card
- Cellular Phones
- Camcoders and Cameras
- Networking Systems, DSL/Cable Modems
- Cable Set-Top Box
- MP3/CD Players
- DSP Supply
- Displays and Monitors



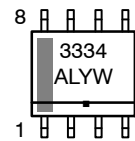
ON Semiconductor®

<http://onsemi.com>



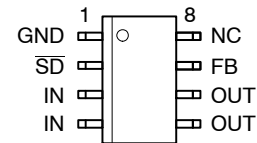
SOIC-8
CASE 751

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NCP3334

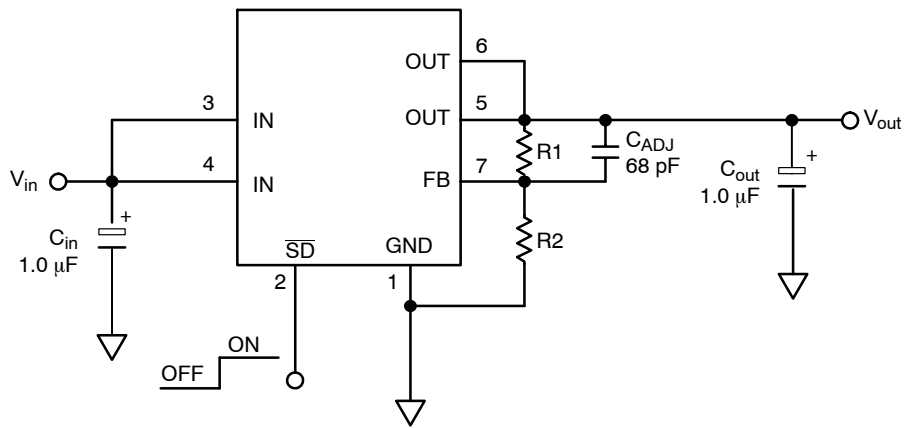


Figure 1. Typical Adjustable Version Application Schematic

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	GND	Power Supply Ground
2	\overline{SD}	Shutdown pin. When not in use, this pin should be connected to the input pin.
3, 4	IN	Power Supply Input Voltage
5, 6	OUT	Regulated output voltage. Bypass to ground with $C_{out} \geq 1.0 \mu F$.
7	FB	Feedback pin; reference voltage = 1.25 V.
8	NC	Not Connected

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	-0.3 to +16	V
Output Voltage	V_{out}	-0.3 to $V_{in} + 0.3$ or 10 V*	V
Shutdown Pin Voltage	V_{sh}	-0.3 to +16	V
Thermal Characteristics Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	238	$^{\circ}C/W$
Operating Junction Temperature Range	T_J	-40 to +150	$^{\circ}C$
Storage Temperature Range	T_{stg}	-50 to +150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) JESD 22-A114-B

Machine Model (MM) JESD 22-A115-A

*Whichever is less. Reverse bias protection feature valid only if $V_{out} - V_{in} \leq 7.0 V$.

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ELECTRICAL CHARACTERISTICS ($V_{out} = 1.25\text{ V}$ (V_{ref}) typical, $V_{in} = 2.9\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage Accuracy $V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$, $I_L = 0.1\text{ mA}$ to 500 mA , $T_A = 25^\circ\text{C}$	V_{REF}	-0.9% 1.239	1.25	+0.9% 1.261	V
Reference Voltage Accuracy $V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$, $I_L = 0.1\text{ mA}$ to 500 mA , $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$	V_{REF}	-1.4% 1.233	1.25	+1.4% 1.268	V
Reference Voltage Accuracy (Note 1) $V_{in} = 2.9\text{ V}$ to $V_{out} + 4.0\text{ V}$, $I_L = 0.1\text{ mA}$ to 500 mA , $T_A = -40^\circ\text{C}$ to $+150^\circ\text{C}$	V_{REF}	-1.5% 1.231	1.25	+1.5% 1.269	V
Line Regulation $V_{in} = 2.9\text{ V}$ to 12 V , $I_L = 0.1\text{ mA}$	$Line_{Reg}$		0.04		mV/V
Load Regulation $V_{in} = 2.9\text{ V}$, $I_L = 0.1\text{ mA}$ to 500 mA	$Load_{Reg}$		0.04		mV/mA
Dropout Voltage, $V_{out} = 2.5\text{ V}$ to 10 V $I_L = 500\text{ mA}$ (Note 2) $I_L = 300\text{ mA}$ $I_L = 50\text{ mA}$ $I_L = 0.1\text{ mA}$	V_{Drop}			340 230 110 10	mV
Peak Output Current (Notes 1 and 2) (See Figure 6)	I_{pk}	500	700	860	mA
Short Output Current (See Figure 6)	I_{sc}	$V_{out} \leq 3.3\text{ V}$ $V_{out} > 3.3\text{ V}$		900 1300	mA
Thermal Shutdown	T_{JSD}		160		$^\circ\text{C}$
Ground Current In Regulation $I_L = 500\text{ mA}$ (Note 2) $I_L = 300\text{ mA}$ (Note 2) $I_L = 50\text{ mA}$ $I_L = 0.1\text{ mA}$ In Dropout $V_{in} = V_{out} - 0.1\text{ V}$, $I_L = 0.1\text{ mA}$ In Shutdown $V_{SD} = 0\text{ V}$	I_{GND} I_{GNDsh}		9.0 4.6 0.8 - - 0.07	14 7.5 2.5 190 500 1.0	mA μA
Output Noise $I_L = 500\text{ mA}$, $f = 10\text{ Hz}$ to 100 kHz , $C_{out} = 10\text{ }\mu\text{F}$	V_{noise}		38		μV_{rms}
Shutdown Threshold Voltage ON Threshold Voltage OFF	V_{THSD}	2.0		0.4	V V
SD Input Current, $V_{SD} = 0\text{ V}$ to 0.4 V or $V_{SD} = 2.0\text{ V}$ to V_{in}	I_{SD}	$V_{in} \leq 5.4\text{ V}$ $V_{in} > 5.4\text{ V}$	0.07	1.0 5.0	μA
Output Current In Shutdown Mode, $V_{out} = 0\text{ V}$	I_{OSD}		0.07	1.0	μA
Reverse Bias Protection, Current Flowing from the Output Pin to GND ($V_{in} = 0\text{ V}$, $V_{out_forced} = V_{out}(\text{nom}) \leq 7\text{ V}$) (Note 3)	I_{OUTR}		1.0		μA

RECOMMENDED OPERATING CONDITIONS

Input Voltage	V_{IN}	2.6		12	V
---------------	----------	-----	--	----	---

- For output current capability for $T_J < 0^\circ\text{C}$, please refer to Figure 8.
- T_A must be greater than 0°C .
- Reverse bias protection feature valid only if $V_{out} - V_{in} \leq 7.0\text{ V}$.

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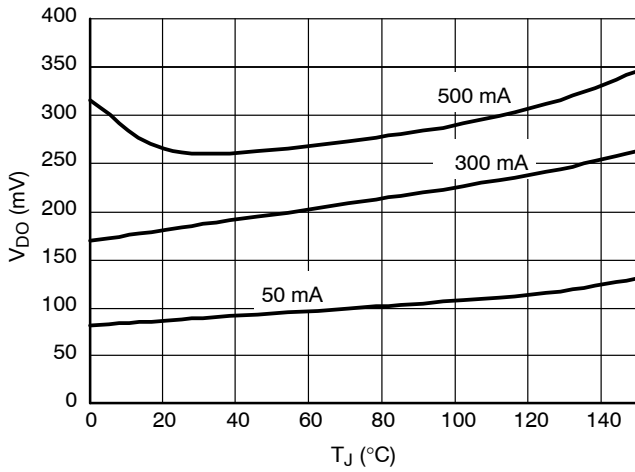


Figure 2. Dropout Voltage vs. Temperature

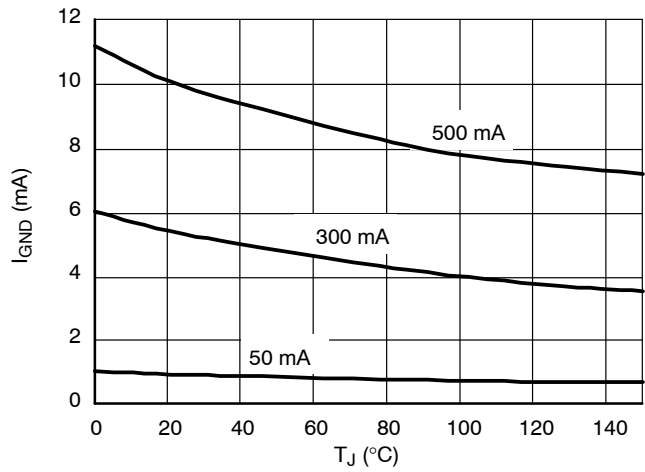


Figure 3. Ground Current vs. Temperature

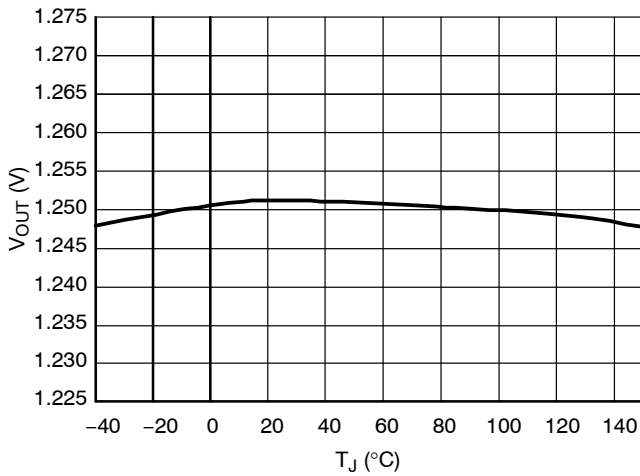


Figure 4. Output Voltage vs. Temperature

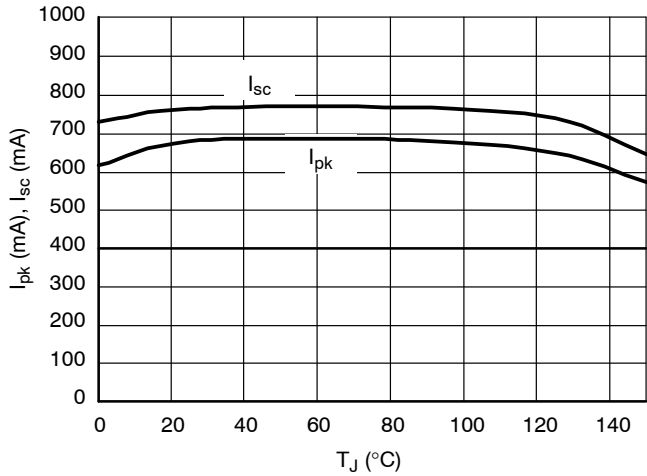


Figure 5. Peak and Short Current vs. Temperature

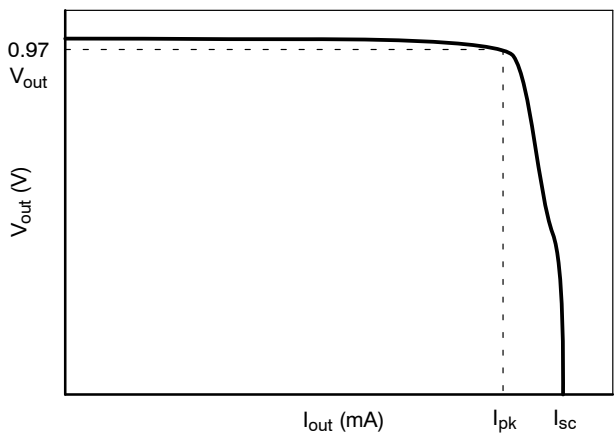


Figure 6. Output Voltage vs. Output Current

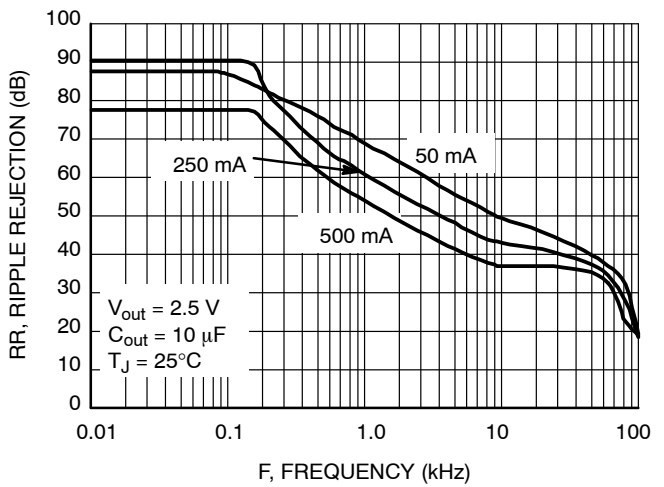


Figure 7. Ripple Rejection vs. Frequency

NCP3334

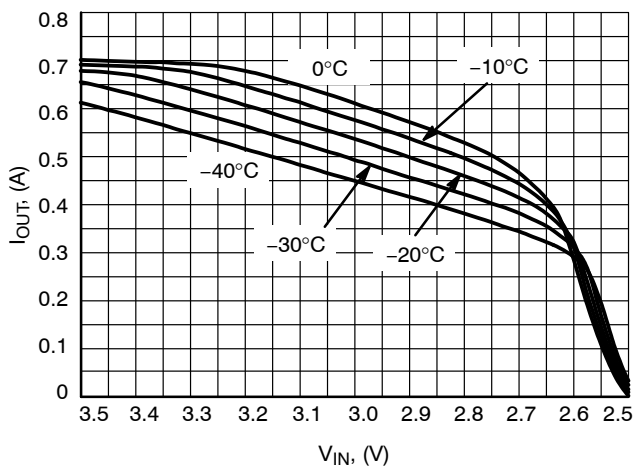


Figure 8. Output Current Capability when set at 2.5 V V_{out}

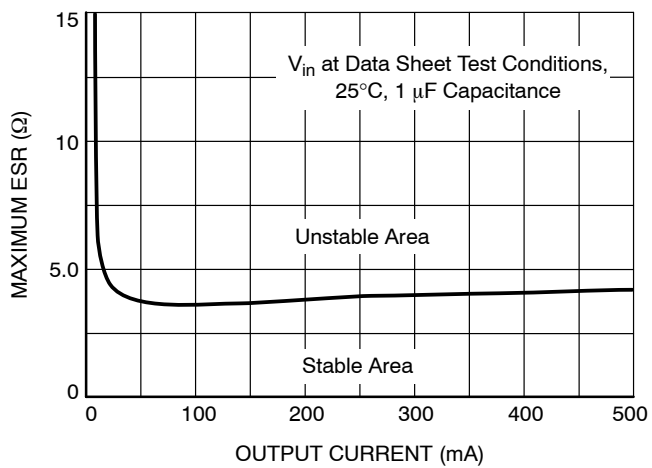


Figure 9. Stability with ESR vs. I_{out}

NCP3334

APPLICATIONS INFORMATION

Reverse Bias Protection

Reverse bias is a condition caused when the input voltage goes to zero, but the output voltage is kept high either by a large output capacitor or another source in the application which feeds the output pin.

Normally in a bipolar LDO all the current will flow from the output pin to input pin through the PN junction with limited current capability and with the potential to destroy the IC.

Due to an improved architecture, the NCP3334 can withstand up to 7.0 V on the output pin with virtually no current flowing from output pin to input pin, and only negligible amount of current (tens of μA) flowing from the output pin to ground for infinite duration.

Operation with output voltages in the range of 7 to 10 volts requires that the output to input voltage differential be less than 7 volts.

Input Capacitor

An input capacitor of at least 1.0 μF , any type, is recommended to improve the transient response of the regulator and/or if the regulator is located more than a few inches from the power source. It will also reduce the circuit's sensitivity to the input line impedance at high frequencies. The capacitor should be mounted with the shortest possible track length directly across the regulator's input terminals.

Output Capacitor

The NCP3334 remains stable with any type of capacitor as long as it fulfills its 1.0 μF requirement. There are no constraints on the minimum ESR and it will remain stable up to an ESR of 5.0 Ω . Larger capacitor values will improve the noise rejection and load transient response.

Noise Reduction

A 68 pF capacitor connected in parallel with R1 (see Figure 1) is recommended to reduce output noise and improve stability.

Adjustable Operation

The output voltage can be set by using a resistor divider as shown in Figure 1 with a range of 1.25 to 10 V. The appropriate resistor divider can be found by solving the equation below. The recommended current through the resistor divider is from 10 μA to 100 μA . This can be accomplished by selecting resistors in the $\text{k}\Omega$ range. As result, the $I_{\text{adj}} * R2$ becomes negligible in the equation and can be ignored.

$$V_{\text{out}} = 1.25 * \left(1 + \frac{R1}{R2}\right) + I_{\text{adj}} * R2 \quad (\text{eq. 1})$$

Example:

For $V_{\text{out}} = 2.9 \text{ V}$, can use $R1 = 36 \text{ k}\Omega$ and $R2 = 27 \text{ k}\Omega$.

$$1.25 * \left(1 + \frac{36 \text{ k}\Omega}{27 \text{ k}\Omega}\right) = 2.91 \text{ V} \quad (\text{eq. 2})$$

Dropout Voltage

The voltage dropout is measured at 97% of the nominal output voltage.

Thermal Considerations

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. This feature provides protection from a catastrophic device failure due to accidental overheating. This protection feature is not intended to be used as a substitute to heat sinking. The maximum power that can be dissipated, can be calculated with the equation below:

$$P_D = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}} \quad (\text{eq. 3})$$

For improved thermal performance, contact the factory for the DFN package option. The DFN package includes an exposed metal pad that is specifically designed to reduce the junction to air thermal resistance, $R_{\theta JA}$.

ORDERING INFORMATION

Device	Package	Shipping†
NCP3334DADJG	SO-8 (Pb-Free)	98 Units / Rail
NCP3334DADJR2G	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The products described herein NCP3334, may be covered by one or more of the following U.S. patents; 5,920,184, 5,966,004, and 5,834,926. There may be other patents pending.

Micro8 is a trademark of International Rectifier.

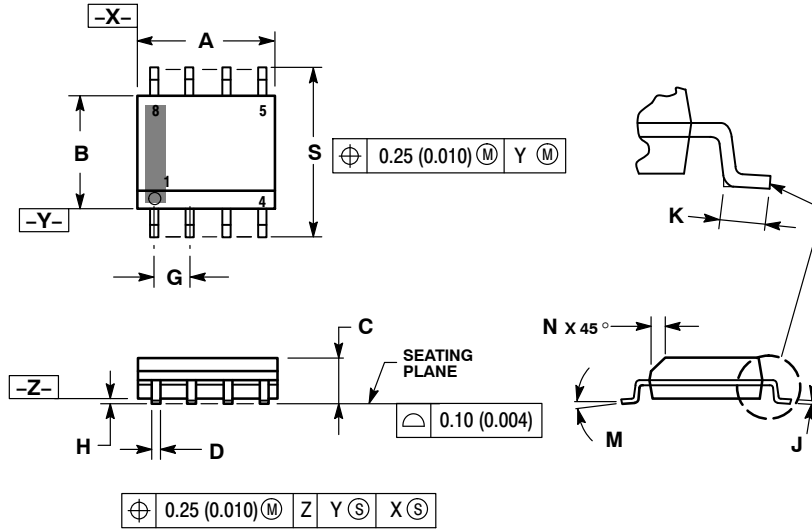
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

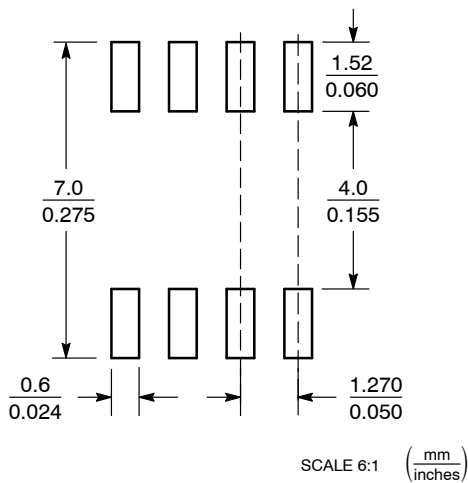
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

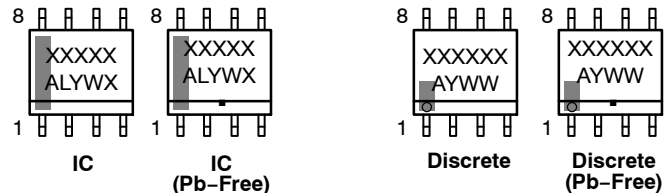
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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