



**THE DATASHEET OF
NTHL082N65S3F**



MOSFET – Power, N-Channel, SUPERFET III, FRFET

650 V, 40 A, 82 mΩ

NTHL082N65S3F

Description

SUPERFET III MOSFET is onsemi’s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET’s optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

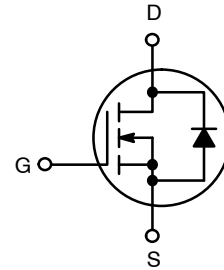
Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 70\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 81\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 722\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

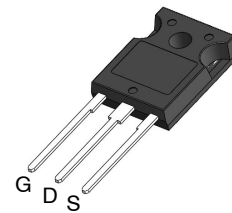
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

| V_{DSS} | $R_{DS(ON)}\text{ MAX}$ | $I_D\text{ MAX}$ |
|-----------|-------------------------|------------------|
| 650 V | 82 mΩ @ 10 V | 40 A |

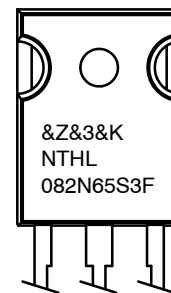


POWER MOSFET



**TO-247 LONG LEADS
 CASE 340CH**

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- NTHL082N65S3F = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTHL082N65S3F

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

| Symbol | Parameter | NTHL082N65S3F | Unit |
|-----------------------------------|--|---------------------------------------|------|
| V _{DSS} | Drain to Source Voltage | 650 | V |
| V _{GSS} | Gate to Source Voltage | - DC | ±30 |
| | | - AC (f > 1 Hz) | ±30 |
| I _D | Drain Current | - Continuous (T _C = 25°C) | 40 |
| | | - Continuous (T _C = 100°C) | 25.5 |
| I _{DM} | Drain Current | - Pulsed (Note 1) | 100 |
| E _{AS} | Single Pulsed Avalanche Energy (Note 2) | 510 | mJ |
| I _{AS} | Avalanche Current (Note 2) | 4.8 | A |
| E _{AR} | Repetitive Avalanche Energy (Note 1) | 3.13 | mJ |
| dv/dt | MOSFET dv/dt | 100 | V/ns |
| | Peak Diode Recovery dv/dt (Note 3) | 50 | |
| P _D | Power Dissipation | (T _C = 25°C) | 313 |
| | | - Derate Above 25°C | 2.5 |
| T _J , T _{STG} | Operating and Storage Temperature Range | -55 to +150 | °C |
| T _L | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds | 300 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

| Symbol | Parameter | NTHL082N65S3F | Unit |
|------------------|---|---------------|------|
| R _{θJC} | Thermal Resistance, Junction to Case, Max. | 0.4 | °C/W |
| R _{θJA} | Thermal Resistance, Junction to Ambient, Max. | 40 | |

PACKAGE MARKING AND ORDERING INFORMATION

| Part Number | Top Marking | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---------------|---------------|---------|----------------|-----------|------------|----------|
| NTHL082N65S3F | NTHL082N65S3F | TO-247 | Tube | N/A | N/A | 30 Units |

NTHL082N65S3F

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

OFF CHARACTERISTICS

| | | | | | | |
|--------------------------------------|---|--|-----|-----|------|------|
| BV _{DSS} | Drain to Source Breakdown Voltage | V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C | 650 | – | – | V |
| | | V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C | 700 | – | – | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 10 mA, Referenced to 25°C | – | 0.7 | – | V/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 650 V, V _{GS} = 0 V | – | – | 10 | μA |
| | | V _{DS} = 520 V, T _C = 125°C | – | 124 | – | |
| I _{GSS} | Gate to Body Leakage Current | V _{GS} = ±30 V, V _{DS} = 0 V | – | – | ±100 | nA |

ON CHARACTERISTICS

| | | | | | | |
|---------------------|--------------------------------------|---|-----|----|-----|----|
| V _{GS(th)} | Gate Threshold Voltage | V _{GS} = V _{DS} , I _D = 1.0 mA | 3.0 | – | 5.0 | V |
| R _{DS(on)} | Static Drain to Source On Resistance | V _{GS} = 10 V, I _D = 20 A | – | 70 | 82 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} = 20 V, I _D = 20 A | – | 24 | – | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|------------------------|-----------------------------------|--|---|------|---|----|
| C _{iss} | Input Capacitance | V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz | – | 3410 | – | pF |
| C _{oss} | Output Capacitance | | – | 70 | – | pF |
| C _{oss(eff.)} | Effective Output Capacitance | V _{DS} = 0 V to 400 V, V _{GS} = 0 V | – | 722 | – | pF |
| C _{oss(er.)} | Energy Related Output Capacitance | V _{DS} = 0 V to 400 V, V _{GS} = 0 V | – | 126 | – | pF |
| Q _{g(tot)} | Total Gate Charge at 10 V | V _{DS} = 400 V, I _D = 20 A, V _{GS} = 10 V (Note 4) | – | 81 | – | nC |
| Q _{gs} | Gate to Source Gate Charge | | – | 24 | – | nC |
| Q _{gd} | Gate to Drain "Miller" Charge | | – | 32 | – | nC |
| ESR | Equivalent Series Resistance | f = 1 MHz | – | 1.9 | – | Ω |

SWITCHING CHARACTERISTICS

| | | | | | | |
|---------------------|---------------------|--|---|----|---|----|
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 400 V, I _D = 20 A, V _{GS} = 10 V R _g = 3 Ω (Note 4) | – | 27 | – | ns |
| t _r | Turn-On Rise Time | | – | 27 | – | ns |
| t _{d(off)} | Turn-Off Delay Time | | – | 79 | – | ns |
| t _f | Turn-Off Fall Time | | – | 5 | – | ns |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|-----------------|--|--|---|-----|-----|----|
| I _S | Maximum Continuous Source to Drain Diode Forward Current | – | – | 40 | A | |
| I _{SM} | Maximum Pulsed Source to Drain Diode Forward Current | – | – | 100 | A | |
| V _{SD} | Source to Drain Diode Forward Voltage | V _{GS} = 0 V, I _{SD} = 20 A | – | – | 1.3 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _{SD} = 20 A, dI _F /dt = 100 A/μs | – | 108 | – | ns |
| Q _{rr} | Reverse Recovery Charge | | – | 410 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

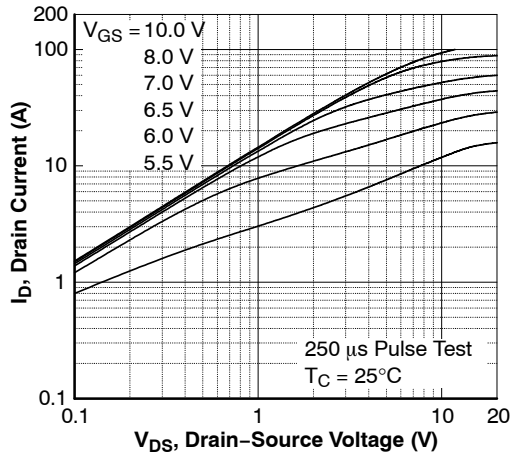


Figure 1. On-Region Characteristics

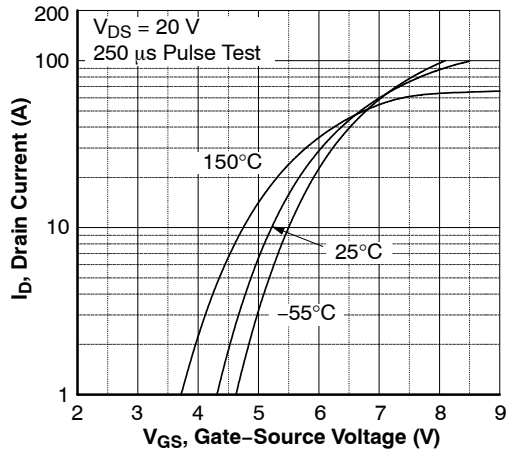


Figure 2. Transfer Characteristics

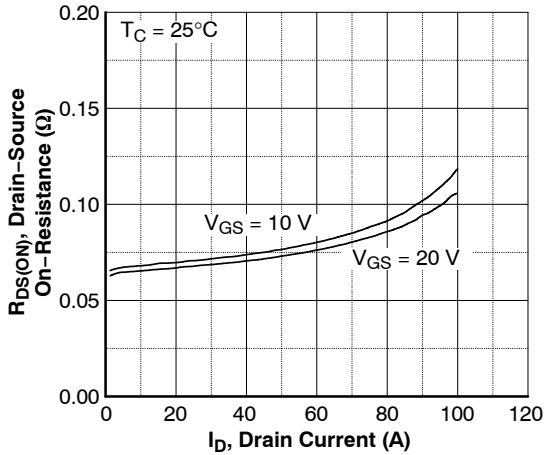


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

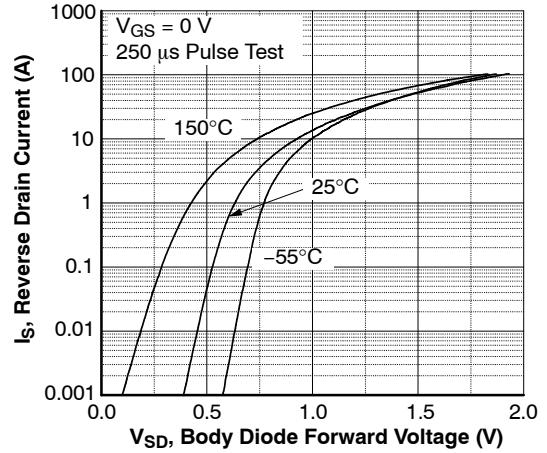


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

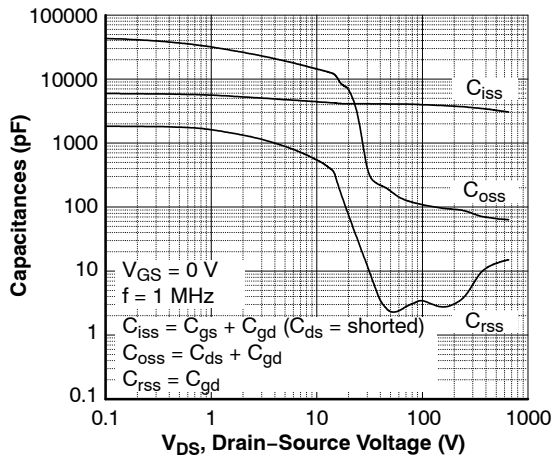


Figure 5. Capacitance Characteristics

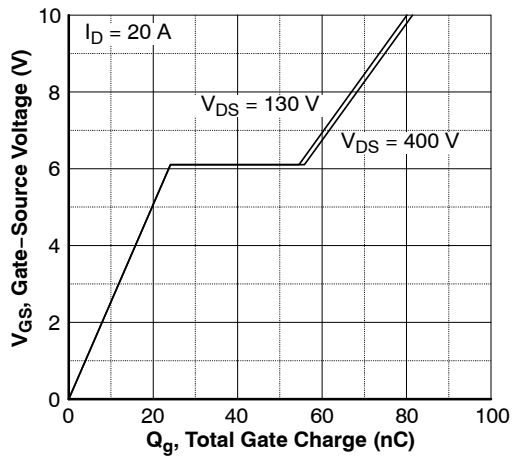


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

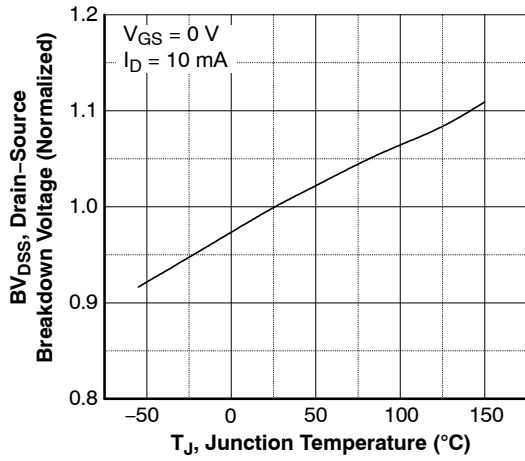


Figure 7. Breakdown Voltage Variation vs. Temperature

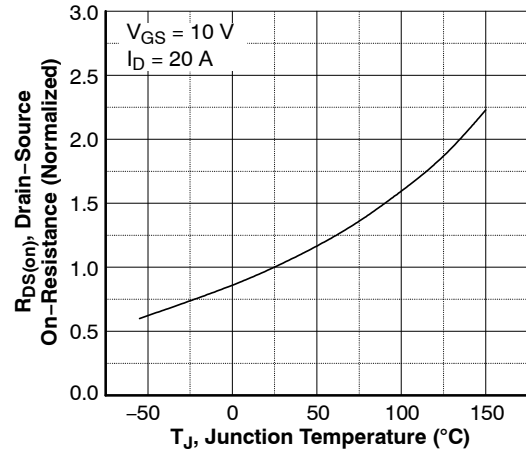


Figure 8. On-Resistance Variation vs. Temperature

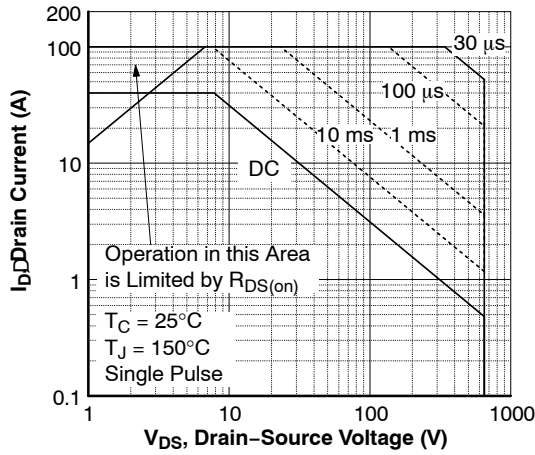


Figure 9. Maximum Safe Operating Area

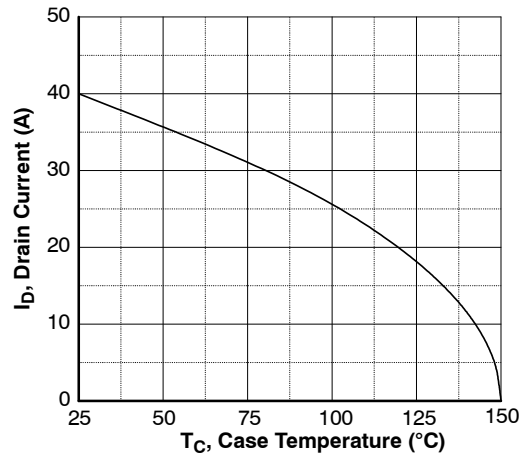


Figure 10. Maximum Drain Current vs. Case Temperature

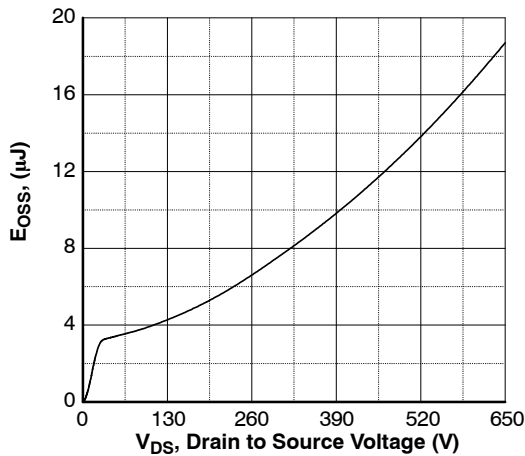


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

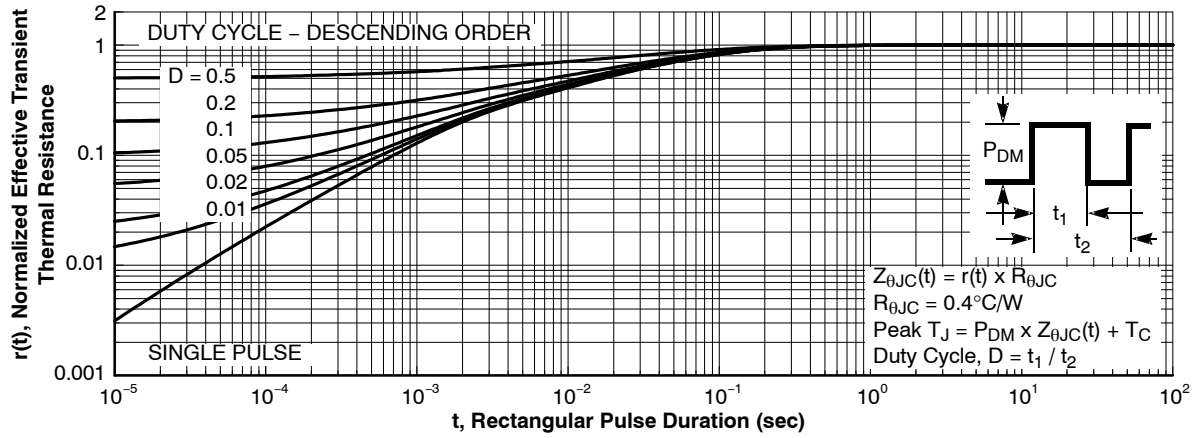


Figure 12. Transient Thermal Response Curve

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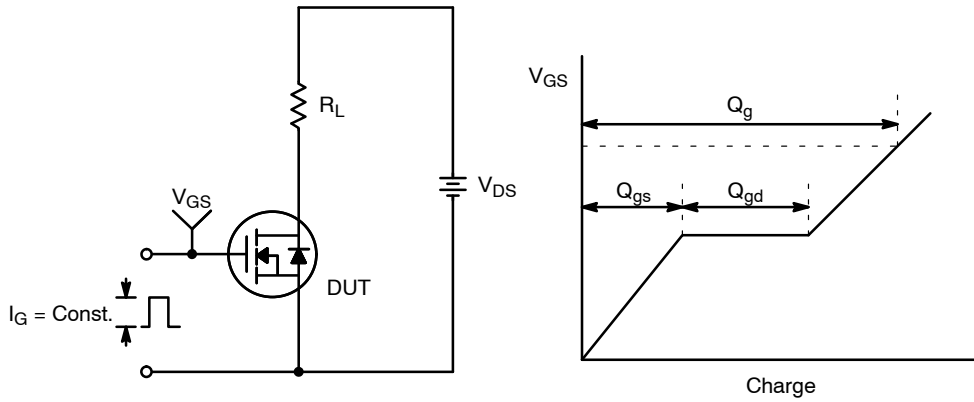


Figure 13. Gate Charge Test Circuit & Waveform

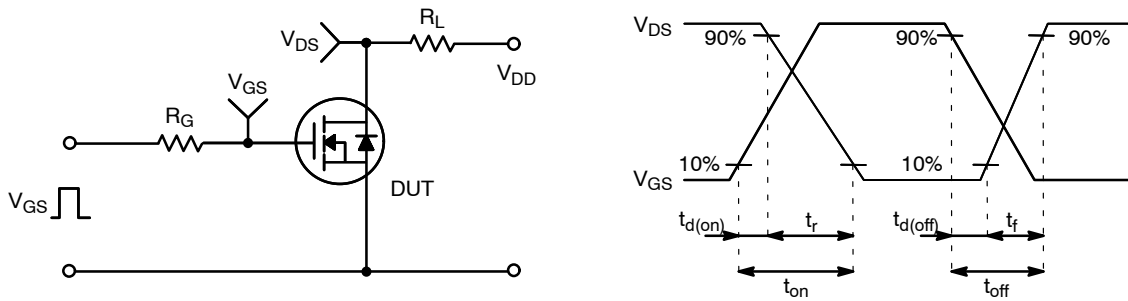


Figure 14. Resistive Switching Test Circuit & Waveforms

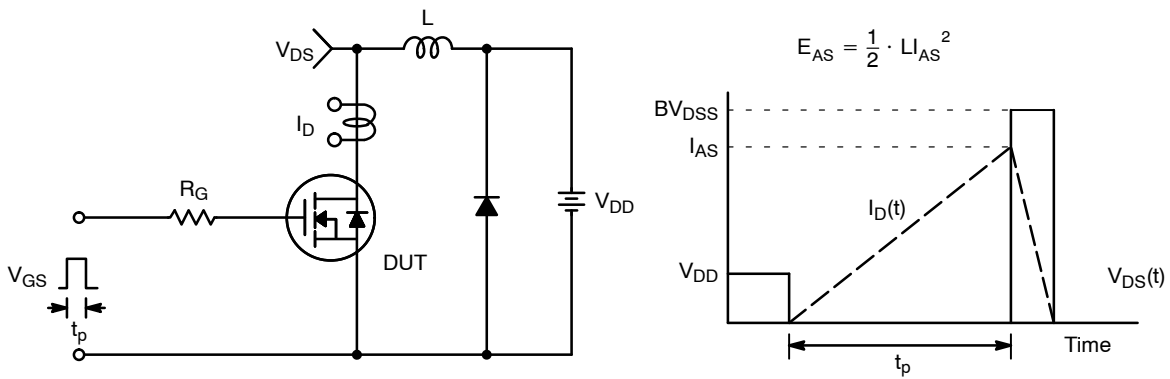


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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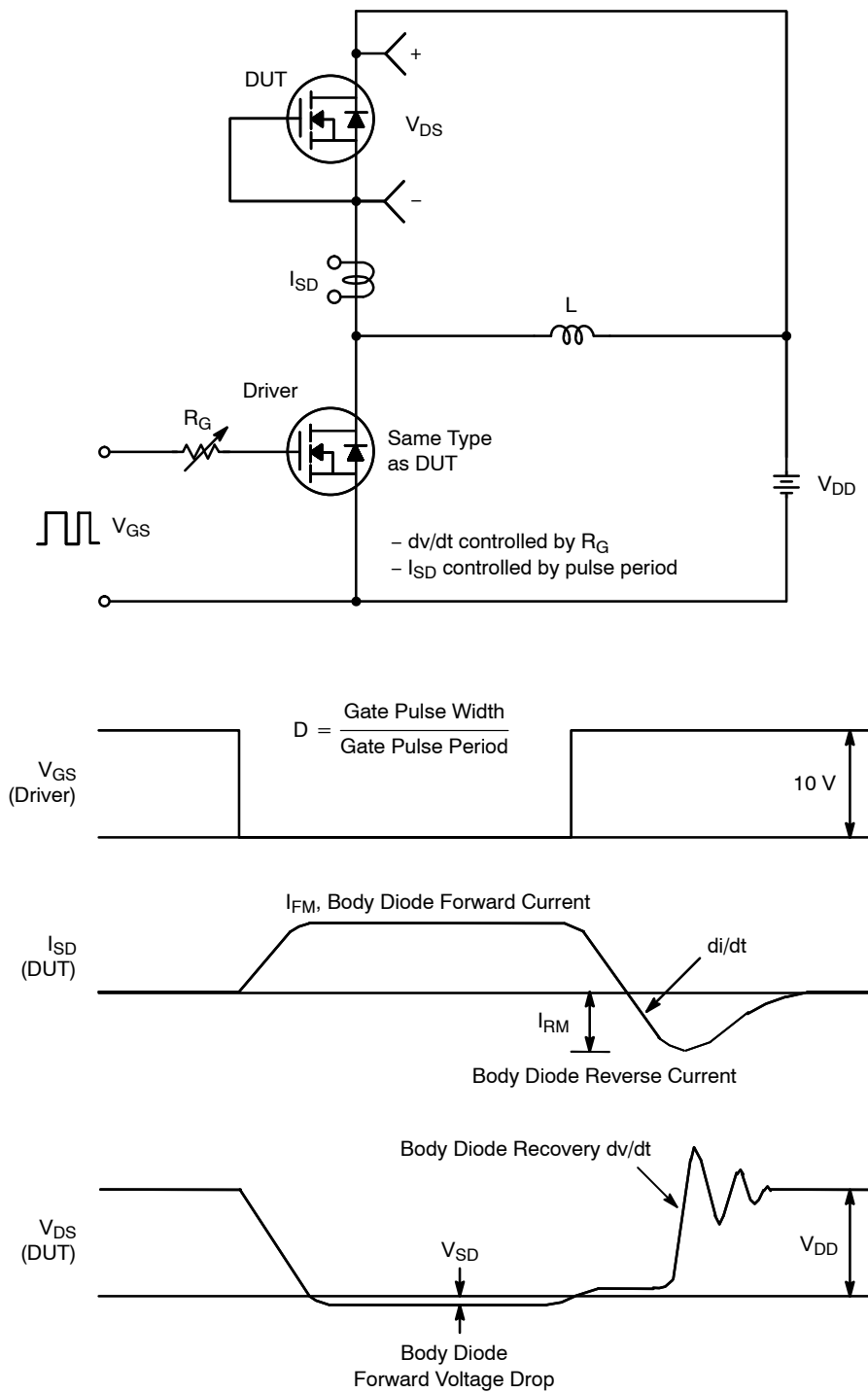


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE

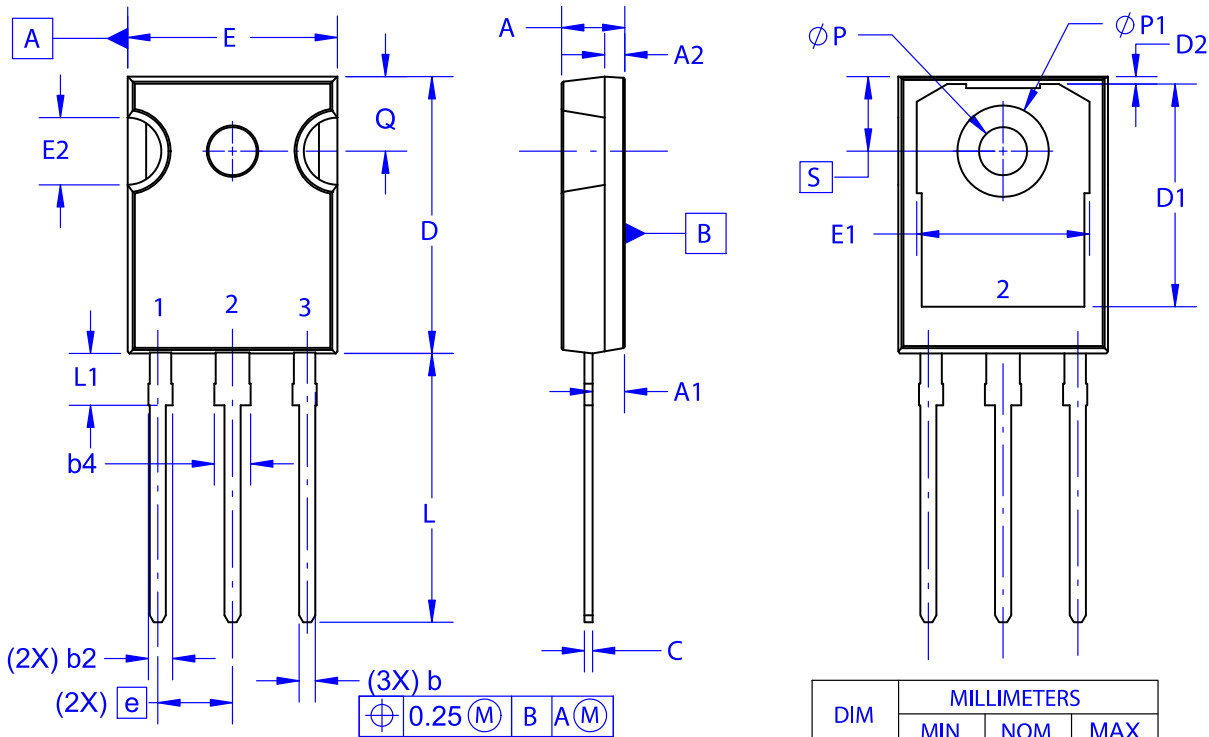
PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CH
ISSUE A

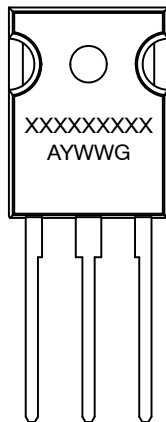
DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN | NOM | MAX |
| A | 4.58 | 4.70 | 4.82 |
| A1 | 2.29 | 2.475 | 2.66 |
| A2 | 1.40 | 1.50 | 1.60 |
| D | 20.32 | 20.57 | 20.82 |
| E | 15.37 | 15.62 | 15.87 |
| E2 | 4.96 | 5.08 | 5.20 |
| e | ~ | 5.56 | ~ |
| L | 19.75 | 20.00 | 20.25 |
| L1 | 3.69 | 3.81 | 3.93 |
| ∅P | 3.51 | 3.58 | 3.65 |
| Q | 5.34 | 5.46 | 5.58 |
| S | 5.34 | 5.46 | 5.58 |
| b | 1.17 | 1.26 | 1.35 |
| b2 | 1.53 | 1.65 | 1.77 |
| b4 | 2.42 | 2.54 | 2.66 |
| c | 0.51 | 0.61 | 0.71 |
| D1 | 13.08 | ~ | ~ |
| D2 | 0.51 | 0.93 | 1.35 |
| E1 | 12.81 | ~ | ~ |
| ∅P1 | 6.61 | 6.73 | 6.85 |

| | | |
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