THE DATASHEET OF

DCP021212DU

DCP02 Series, 2-W, 1000-V_{RMS} Isolated, Unregulated DC/DC Converter Modules

1 Features

- 1-kV Isolation (operational): 1-second test
- Continuous voltage applied across isolation barrier: 60 VDC / 42.5 VAC
- UL1950 recognized component
- EN55022 class B EMC performance
- 7-Pin PDIP and 12-pin SOP packages
- Input voltage: 5 V, 12 V, 15 V, or 24 V
- Output voltage: 3.3 V, ±5 V, 7 V, 9 V, ±12 V, or ±15 V
- Device-to-device synchronization
- Thermal protection
- Short-circuit protection
- High efficiency

2 Applications

- Signal path isolation
- Ground loop elimination
- Data acquisition
- Industrial control and instrumentation
- Test equipment

3 Description

The DCP02 series is a family of 2-W, isolated, unregulated DC/DC converter modules. Requiring a minimum of external components and including on-chip device protection, the DCP02 series of devices provide extra features such as output disable and synchronization of switching frequencies.

This combination of features and small size makes the DCP02 series of devices suitable for a wide range of applications, and is an easy-to-use solution in applications requiring signal path isolation.

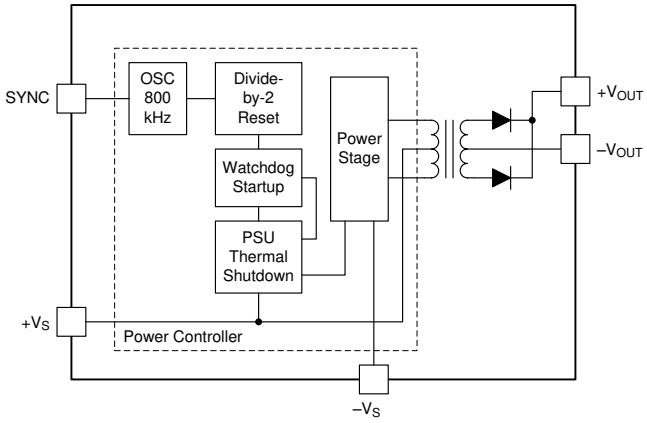
WARNING

This product has operational isolation and is intended for signal isolation only. It should not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in *Feature Description*

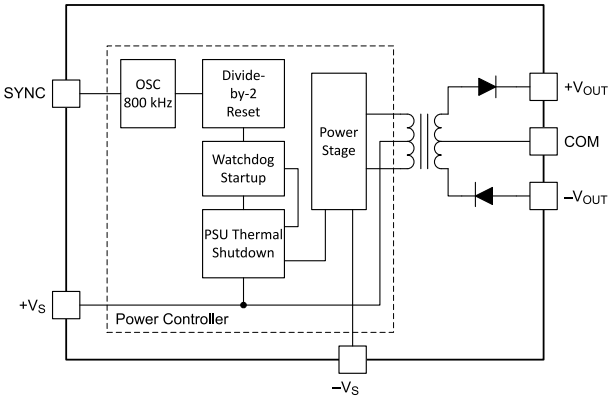
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DCP02xxxx	PDIP (7)	19.18 mm × 10.60 mm
	SOP (12)	17.90 mm × 10.33 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Single Output Block Diagram



Dual Output Block Diagram

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....4
Pin Functions....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....5
6.5 Electrical Characteristics....6
6.6 Switching Characteristics....6
6.7 Typical Characteristics....7
7 Detailed Description....12
7.1 Overview....12
7.2 Functional Block Diagrams....12
7.3 Feature Description....13
7.4 Device Functional Modes....16
8 Layout....22
8.1 Layout Guidelines....22
8.2 Layout Example....22
9 Device and Documentation Support....24
9.1 Device Support....24
9.2 Documentation Support....24
9.3 Support Resources....24
9.4 Related Links....25
9.5 Trademarks....25
9.6 Receiving Notification of Documentation Updates....25
9.7 Electrostatic Discharge Caution....25
9.8 Glossary....25

4 Revision History

Changes from Revision M (April 2020) to Revision N (July 2020)	Page
• Updated Figure 3-1	1

Changes from Revision L (May 2015) to Revision M (April 2020)	Page
• Added links to *Section 2*	1
• Added Efficiency and Load Regulation plots to *Section 6.7*	7
• Added *Section 7.3.6* section	14
• Added *Section 7.3.7* section	14
• Added *Section 7.3.10* section	15

Changes from Revision K (February 2008) to Revision L (January 2015)	Page
• Updated Section 1	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added Table 3-1 table	1
• Added Figure 3-1	1
• Renamed pin "**0V**" to "**COM**" (output side common pin) in Section Pin Functions table	4
• Renamed pin "**V_S**" to "**+V_S**" (input voltage pin) in Section Pin Functions table	4
• Renamed pin "**0V**" to "**–V_S**" (input side common pin) in Section Pin Functions table	4
• Added Section 6.2 table	5
• Added Section 6.3 table	5
• Added Section 6.4 table	5
• Added information to the ISOLATION section of the Section 6.5 table	6
• Added *Section 7.3.1*section to the *Section 7.3* section	13
• Added a typical application design to the *Section 8.1* section	18
• Added Section Power Supply Recommendations section	21

Device Comparison Table

DEVICE NUMBER	INPUT VOLTAGE V_S (V)			OUTPUT VOLTAGE V_{NOM} @ V_S (TYP)(V) 75% LOAD			DEVICE OUTPUT CURRENT (mA) (3)	LOAD REGULATION 10% TO 100% LOAD(1)		NO LOAD CURRENT I_Q (mA) 0% LOAD	EFFICIENCY (%) 100% LOAD	BARRIER CAPACITANCE C_{ISO} (pF) V_{ISO} = 750Vrms
	MIN	TYP	MAX	MIN	TYP	MAX	MAX	TYP	MAX	TYP	TYP	TYP
DCP020503P DCP020503U	4.5	5	5.5	3.13	3.3	3.46	600	19	30	18	74	26
DCP020505P DCP020505U				4.75	5	5.25	400	14	20	18	80	22
DCP020507P DCP020507U				6.65	7	7.35	285	14	25	20	81	30
DCP020509P DCP020509U				8.55	9	9.45	222	12	20	23	82	31
DCP020515DP DCP020515DU				±14.25	±15	±15.75	133(2)	11	20	27	85	24
DCP021205P DCP021205U	10.8	12	13.2	4.75	5	5.25	400	7	15	14	83	33
DCP021212P DCP021212U				11.4	12	12.6	166	7	20	15	87	47
DCP021212DP DCP021212DU				±11.4	±12	±12.6	166(2)	6	20	16	88	35
DCP021515P DCP021515U	13.5	15	16.5	14.25	15	15.75	133	6	20	15	88	42
DCP022405P DCP022405U	21.6	24	26.4	4.75	5	5.25	400	6	15	13	81	33
DCP022405DP DCP022405DU				±4.75	±5	±5.25	400(2)	6	15	12	80	22
DCP022415DP DCP022415DU				±14.25	±15	±15.75	133(2)	6	25	16	79	44

(1) Load regulation = (V_{OUT} at 10% load – V_{OUT} at 100%)/V_{OUT} at 75% load
(2) I_{OUT1} + I_{OUT2}
(3) $P_{OUT(max)}$ = 2 W

5 Pin Configuration and Functions

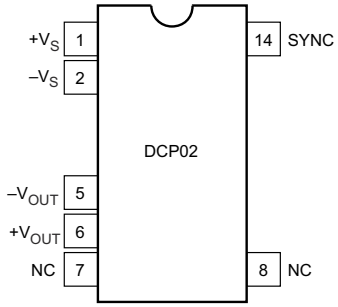


Figure 5-1. NVA Package 7-Pin PDIP (Single Output) (Top View)

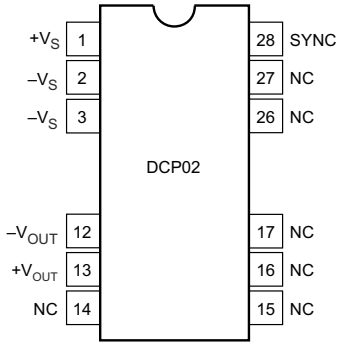


Figure 5-2. DVB PACKAGE 12-Pin SOP (Single Output) (Top View)

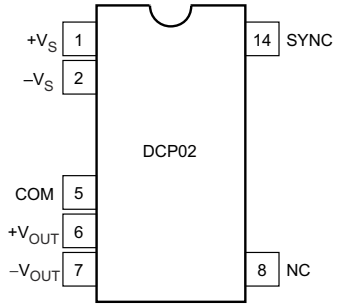


Figure 5-3. NVA Package 7-Pin PDIP (Dual Output) (Top View)

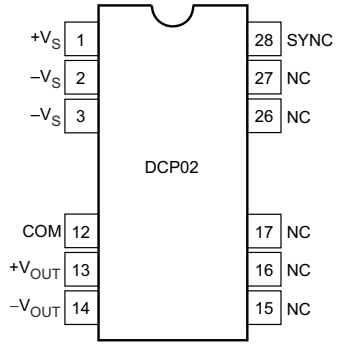


Figure 5-4. DVB Package 12-Pin SOP (Dual Output) (Top View)

Pin Functions

PIN NAME	NUMBER				I/O[1]	DESCRIPTION
	DVB (DUAL)	DVB (SINGLE)	NVA (DUAL)	NVA (SINGLE)		
COM	12	—	5	—	O	Output side common
NC	15	14	8	7	—	No connection
		15				
	16	16				
	17	17		8		
	26	26				
	27	27				
SYNC	28	28	14	14	I	Synchronization Pin - Synchronize multiple devices by connecting their SYNC pins together. Pulling this pin low disables the internal oscillator.
$+V_{OUT}$	13	13	6	6	O	Positive output voltage
$–V_{OUT}$	14	12	7	5	O	Negative output voltage
$+V_S$	1	1	1	1	I	Input voltage
$–V_S$	2	2	2	2	I	Input side common
	3	3				

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	5-V input devices		7	V
	12-V input devices		15	
	15-V input devices		18	
	24-V input devices		29	
Storage temperature, T_{stg}		–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	5-V input devices	4.5	5	5.5	V
	12-V input devices	10.8	12	13.2	
	15-V input devices	13.5	15	16.5	
	24-V input devices	21.6	24	26.4	
Operating temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		DCP020x NVA (PDIP) 7 PINS	DCP020x DVB (SOP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61	61	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19	19	
$R_{\theta JB}$	Junction-to-board thermal resistance	24	24	
ψ_{JT}	Junction-to-top characterization parameter	7	7	
ψ_{JB}	Junction-to-board characterization parameter	24	24	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
P_{OUT}	Output power	I_{LOAD} = 100% (full load)				2	W
V_{RIPPLE}	Output voltage ripple	C_{OUT} = 1 µF, I_{LOAD} = 50%			20		mV_{PP}
	Voltage vs. Temperature	–40°C ≤ T_A ≤ 25°C			0.046		%/°C
		25°C ≤ T_A ≤ 85°C			0.016		%/°C
INPUT							
V_S	Input voltage range			–10%		10%	
ISOLATION							
V_{ISO}	Isolation	1-second flash test	Voltage	1			kVrms
			dV/dt			500	V/s
			Leakage Current			30	nA
		Continuous working voltage across isolation barrier	DC			60	VDC
			AC			42.5	VAC
LINE REGULATION							
	Output voltage	I_{OUT} ≥ 10% load current and constant, V_S (min) to V_S (typ)			1%	15%	
		I_{OUT} ≥ 10% load current and constant, V_S (typ) to V_S (max)			1%	15%	
RELIABILITY							
	Demonstrated	T_A = 55°C		75			FITS
THERMAL SHUTDOWN							
T_{SD}	Die temperature at shutdown				150		°C
I_{SD}	Shutdown current				3		mA

6.6 Switching Characteristics

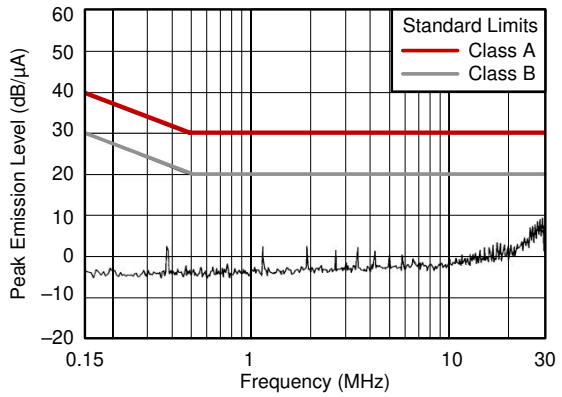
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	$f_{SW} = f_{OSC}/2$		800		kHz
V_{IL}	Low-level input voltage, SYNC		0		0.4	V
I_{SYNC}	Input current, SYNC	V_{SYNC} = 2 V		75		µA
$t_{DISABLE}$	Disable time			2		µs
C_{SYNC}	Capacitance loading on SYNC pin(1)	External			3	pF

(1) The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* (SBAA035) describes this configuration.

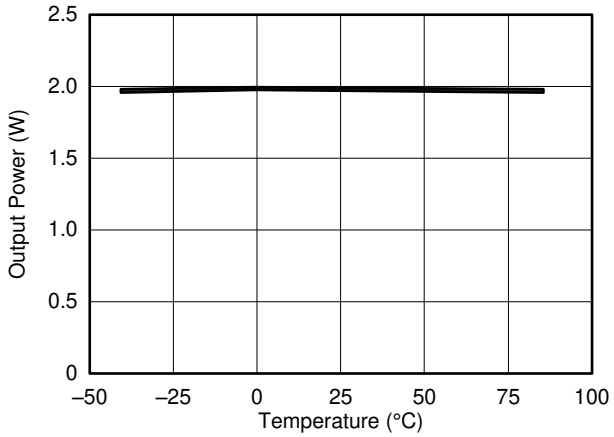
6.7 Typical Characteristics

T_A = 25°C, unless otherwise noted.



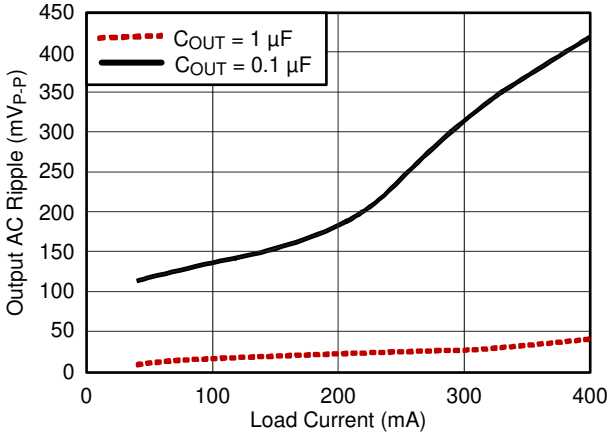
DCP020505P I_{LOAD} = 400 mA

Figure 6-1. Conducted Emissions versus Frequency



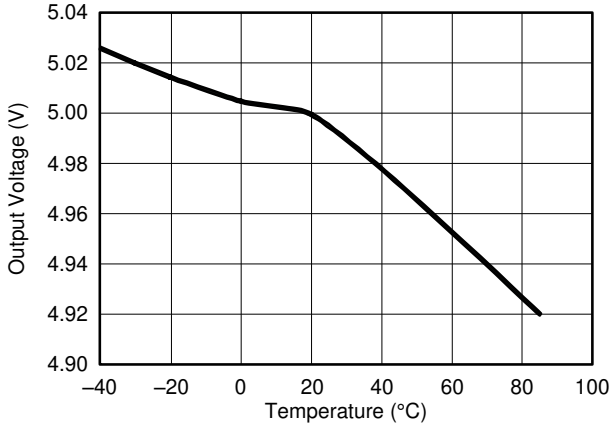
100% Load

Figure 6-2. Output Power versus Temperature



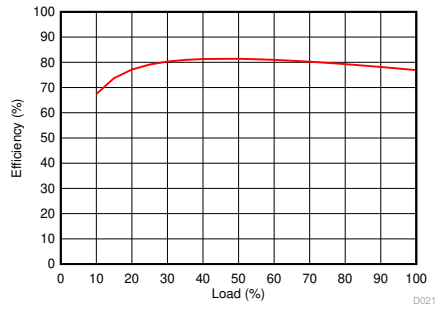
DCP020505P (20 MHz Bandwidth)

Figure 6-3. Output AC Ripple versus Load Current



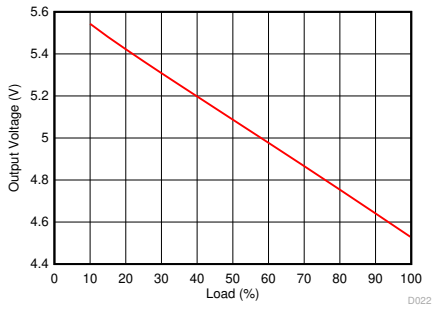
DCP020505P 75% Load Current

Figure 6-4. Output Voltage versus Temperature



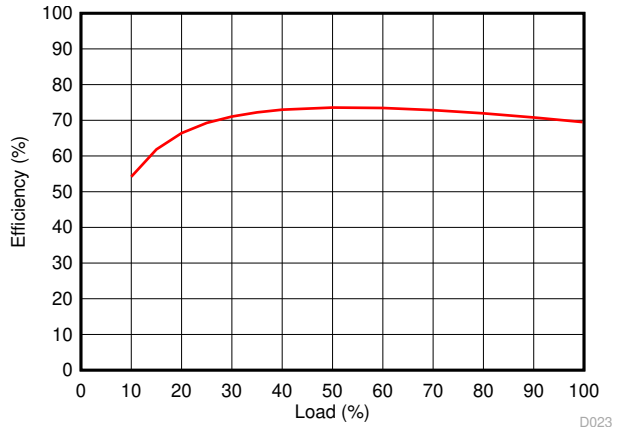
A. DCP020505P

Figure 6-5. Efficiency versus Load



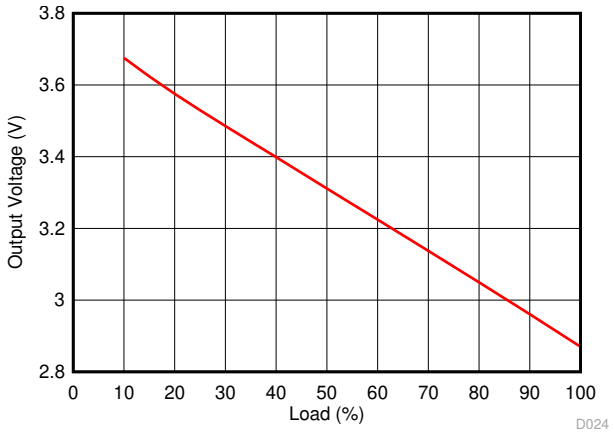
A. DCP020505P **Note:** Operations under 10% Load

Figure 6-6. Load Regulation



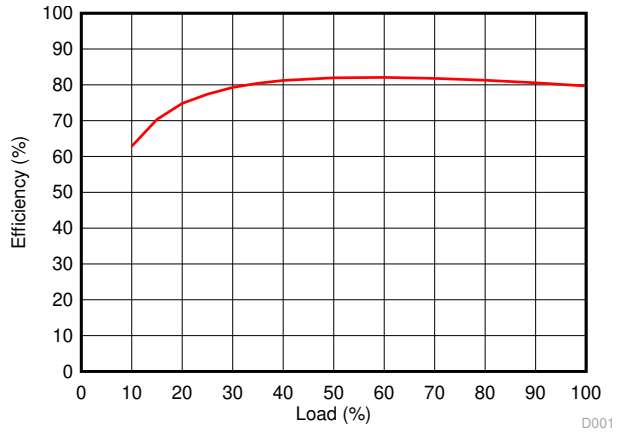
A. DCP020503P

Figure 6-7. Efficiency versus Load



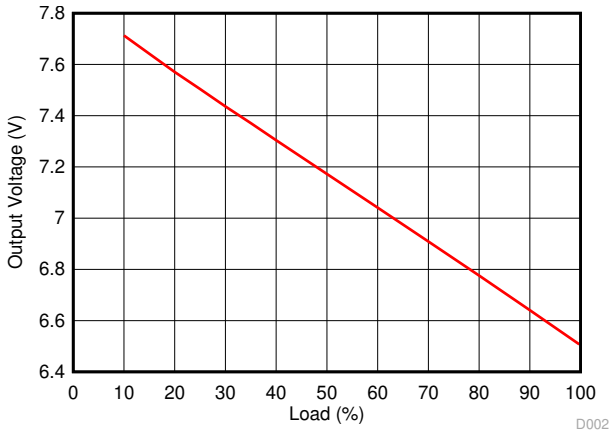
A. DCP020503P **Note:** Operations under 10% Load

Figure 6-8. Load Regulation



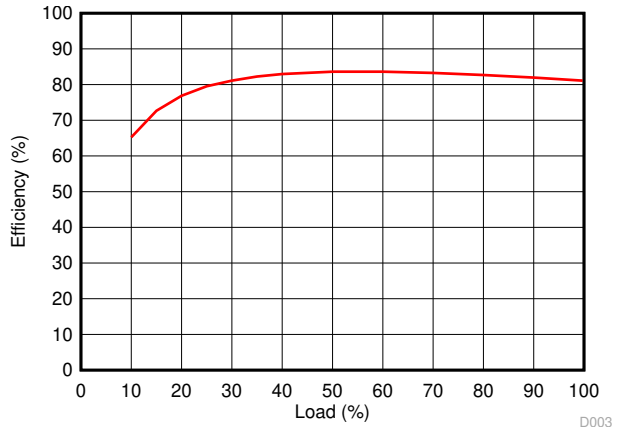
A. DCP020507P

Figure 6-9. Efficiency versus Load



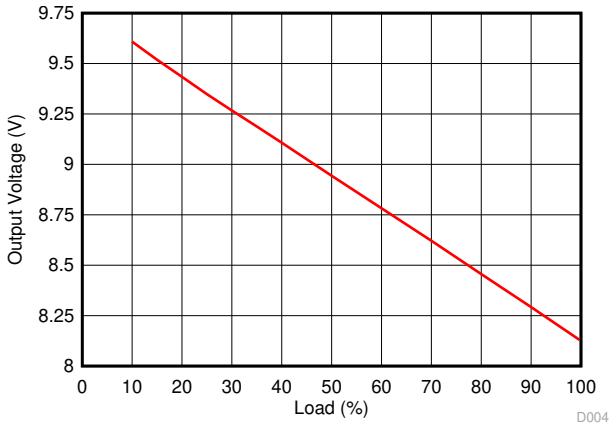
A. DCP020507P **Note:** Operations under 10% Load

Figure 6-10. Load Regulation



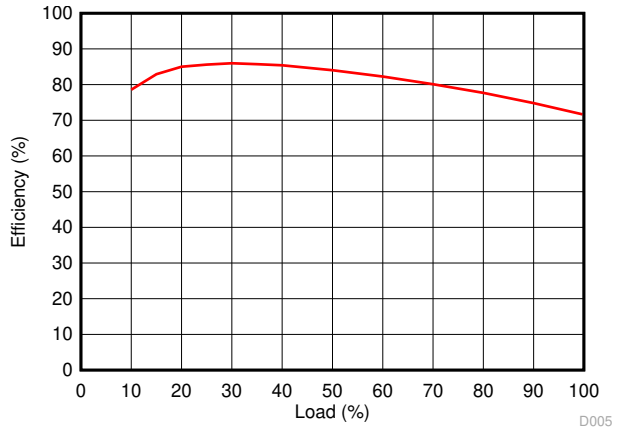
A. DCP020509P

Figure 6-11. Efficiency versus Load



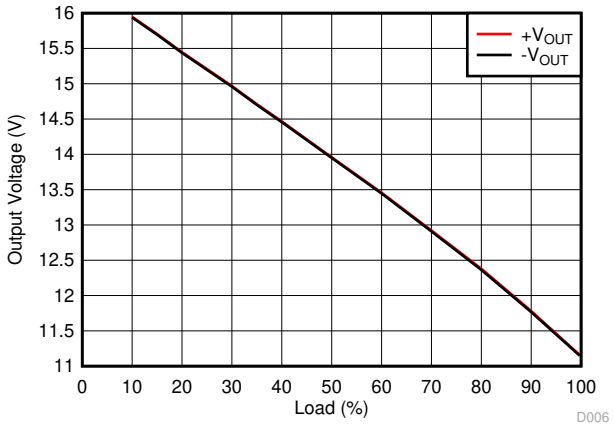
A. DCP020509P **Note:** Operations under 10% Load

Figure 6-12. Load Regulation



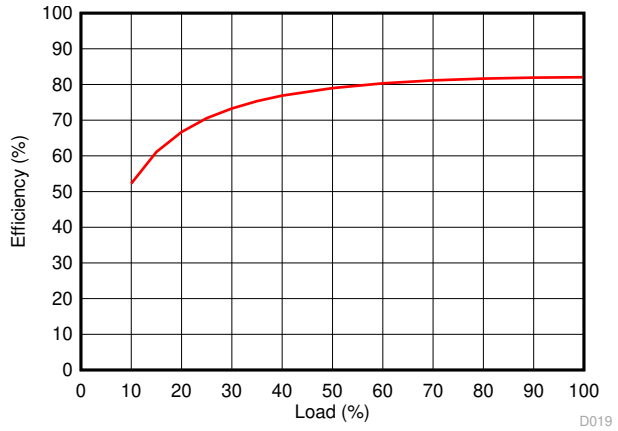
A. DCP020515DP

Figure 6-13. Efficiency versus Load



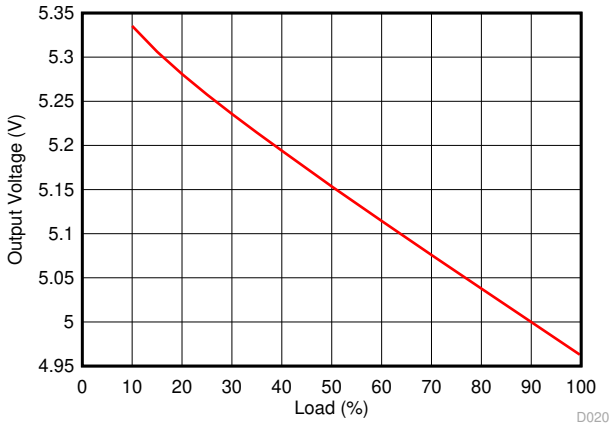
A. DCP020515P **Note:** Operations under 10% Load

Figure 6-14. Load Regulation



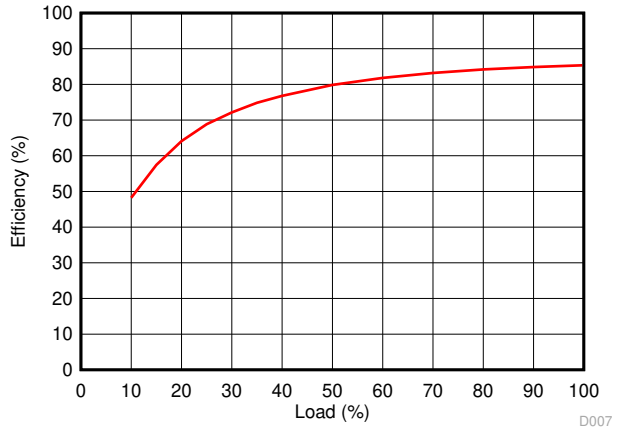
A. DCP021205P

Figure 6-15. Efficiency versus Load



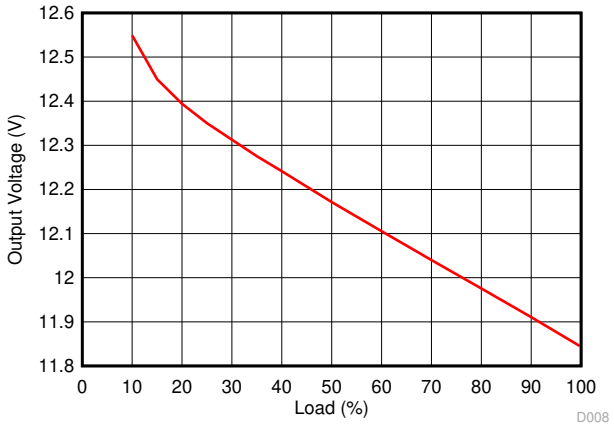
DCP021205P **Note:** Operations under 10% Load

Figure 6-16. Load Regulation



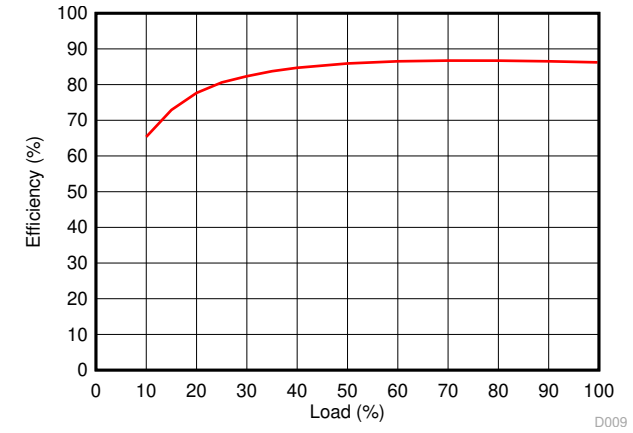
A. DCP021212P

Figure 6-17. Efficiency versus Load



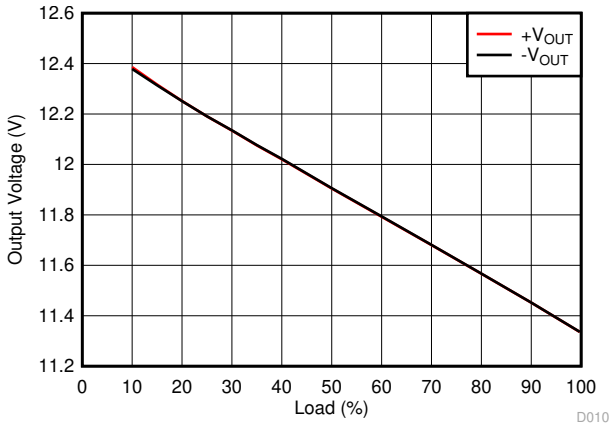
A. DCP021212P **Note:** Operations under 10% Load

Figure 6-18. Load Regulation



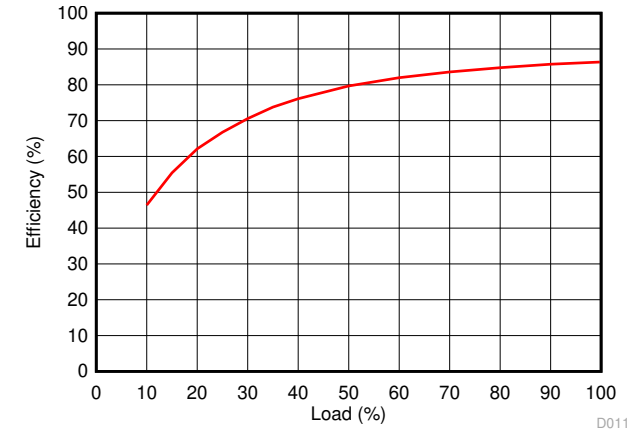
A. DCP021212DP

Figure 6-19. Efficiency versus Load



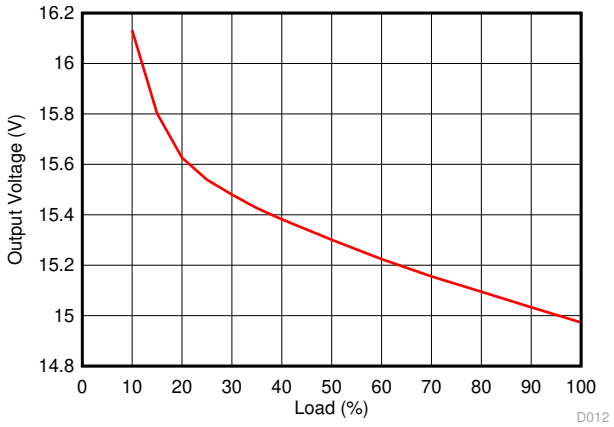
A. DCP021212DP **Note:** Operations under 10% Load

Figure 6-20. Load Regulation



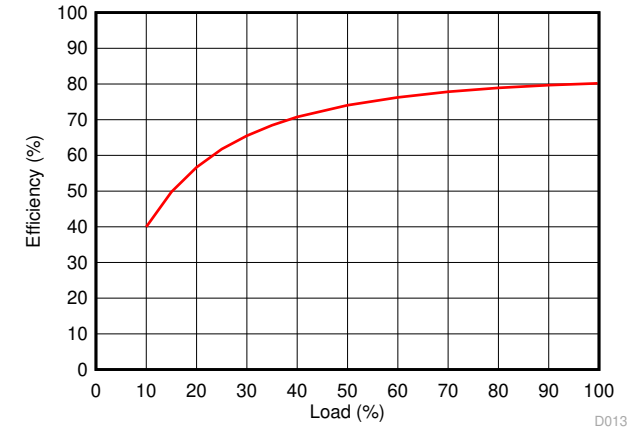
A. DCP021515P

Figure 6-21. Efficiency versus Load



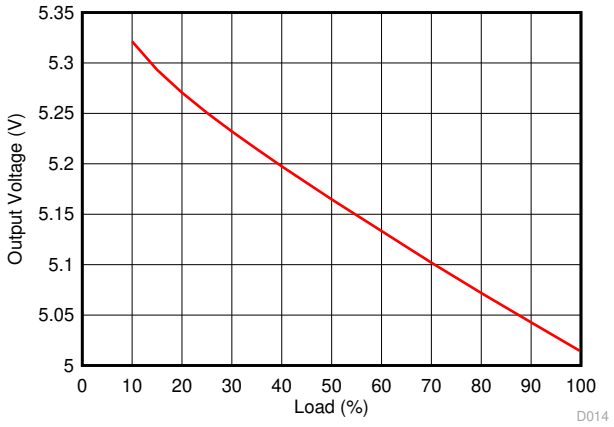
A. DCP021515P **Note:** Operations under 10% Load

Figure 6-22. Load Regulation



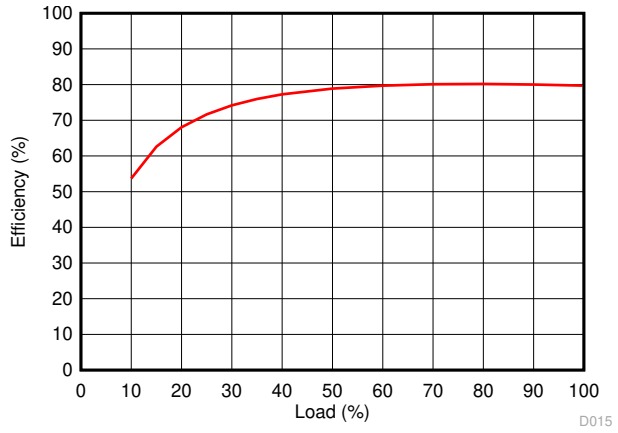
A. DCP022405P

Figure 6-23. Efficiency versus Load



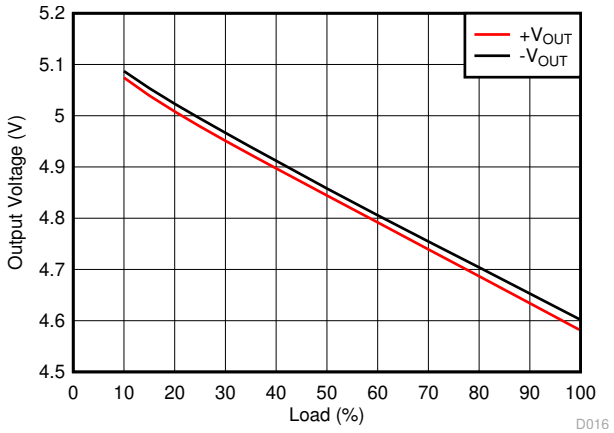
A. DCP022405P **Note:** Operations under 10% Load

Figure 6-24. Load Regulation



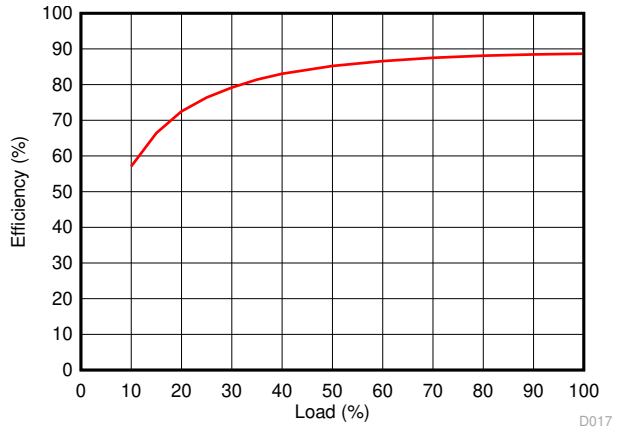
A. DCP022405DP

Figure 6-25. Efficiency versus Load



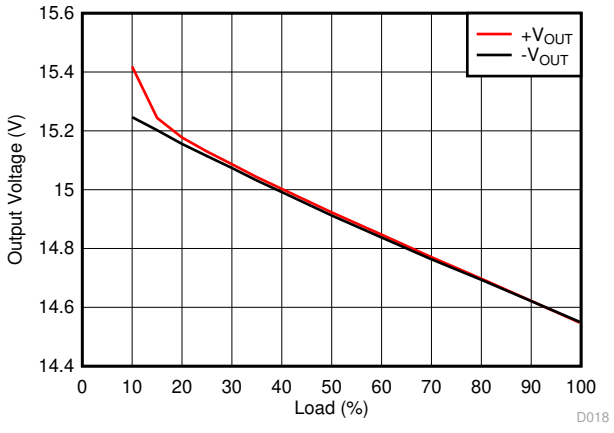
A. DCP022405DP **Note:** Operations under 10% Load

Figure 6-26. Load Regulation



A. DCP022415DP

Figure 6-27. Efficiency versus Load



A. DCP022415DP **Note:** Operations under 10% Load

Figure 6-28. Load Regulation

7 Detailed Description

7.1 Overview

The DCP02 offers up to 2 W of isolated, unregulated output power from a 5-V, 12-V, 15-V, or 24-V input source with a typical efficiency of up to 89%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCP02 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

7.2 Functional Block Diagrams

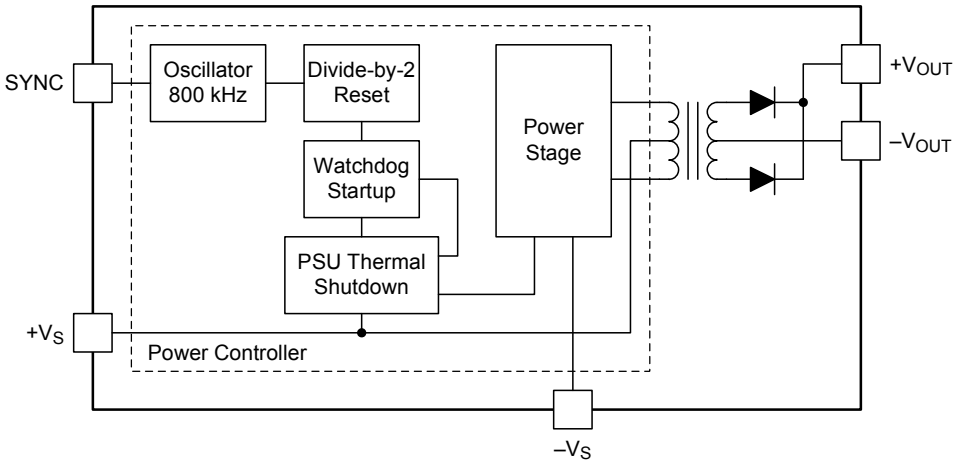


Figure 7-1. Single Output Device

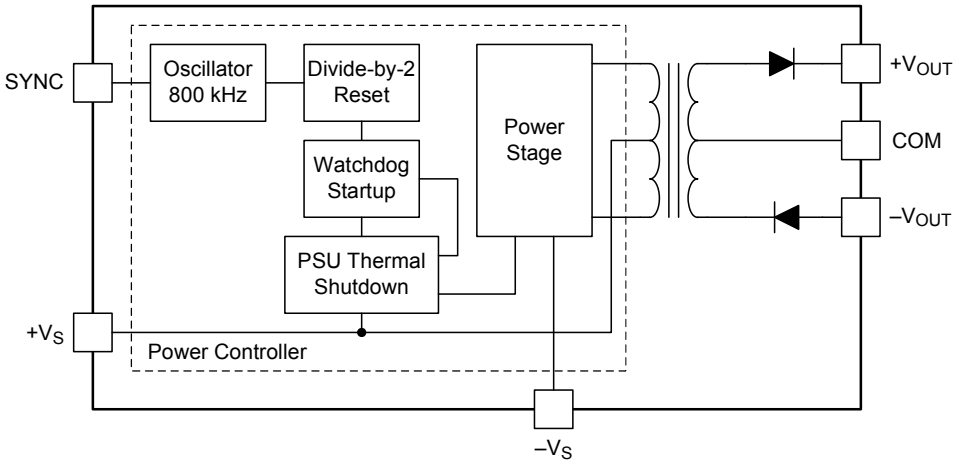


Figure 7-2. Dual Output Device

7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.5 V peak or 60 V_{DC} for more than 1 second.

7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation should never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.5 V_{RMS} or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.5 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage

Hipot test, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCP02 series of dc-dc converters are all 100% production tested at 1.0 kV_{AC} for one second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCP02 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

7.3.2 Power Stage

The DCP02 series of devices use a push-pull, center-tapped topology. The DCP02 devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator).

7.3.3 Oscillator And Watchdog Circuit

The onboard, 800-kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP02-series device circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be disabled by pulling the SYNC pin low. When the SYNC pin goes low, the output pins transition into tri-state mode, which occurs within 2 µs.

7.3.4 Thermal Shutdown

The DCP02 series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C, the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C.

7.3.5 Synchronization

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCP02 series of devices overcome this interference by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) has the effect of reducing the switching frequency, or even stopping the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3.0 V.

For an application that uses more than eight synchronized devices use an external device to drive the SYNC pins. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes this configuration.

Note

During the start-up period, all synchronized devices draw maximum current from the input simultaneously. If the input voltage falls below approximately 4 V, the devices may not start up. A 2.2-µF capacitor should be connected close to each device's input pin.

7.3.6 Light Load Operation (< 10%)

Operation below 10% load can cause the output voltage to increase up to double the typical output voltage. For applications that operate less than 10% of rated output current, it is recommended to add a minimum load to ensure the output voltage of the device is within the load regulation range. For example, connect a 125-Ω pre-load resistor to meet the 10% minimum load condition for the DCP020505P.

7.3.7 Load Regulation (10% to 100%)

The load regulation of the DCP02 series of devices is specified at 10% to 100% load placing a minimum 10% load will ensure the output voltage is within the range specified in the *Section 6.5* table. For more information regarding operation below 10% load, see the *Section 7.3.6* section.

7.3.8 Construction

The basic construction of the DCP02 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCP02 series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

7.3.9 Thermal Management

Due to the high power density of this device, it is advisable to provide ground planes on the input and output.

7.3.10 Power-Up Characteristics

The DCP02 series of devices do not include a soft-start feature. Therefore, a high in-rush current during power up is expected. To ensure a more stable start-up, allow the input voltage to be in regulation before enabling the device. Refer to the *Section 7.4.1* section on how to disable/enable the device. Figure 7-6 shows the typical start-up waveform for a DCP020505P when enabled after the input voltage is in regulation. Figure 7-3 shows the typical start-up waveform for a DCP020505P, operating from a 5-V input with no load on the output. Figure 7-4 shows the start-up waveform for a DCP020505P starting up into a 10% load. Figure 7-5 shows the start-up waveform into a full (100%) load.

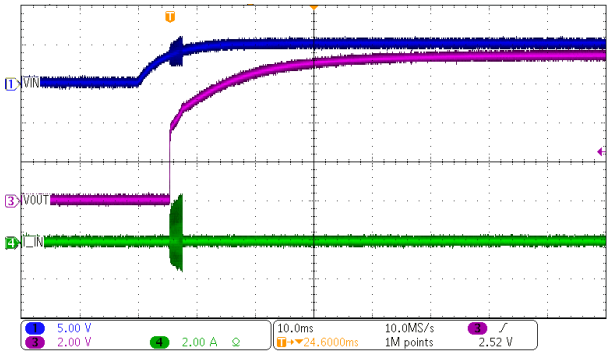


Figure 7-3. DCP020505P Start-Up at No Load

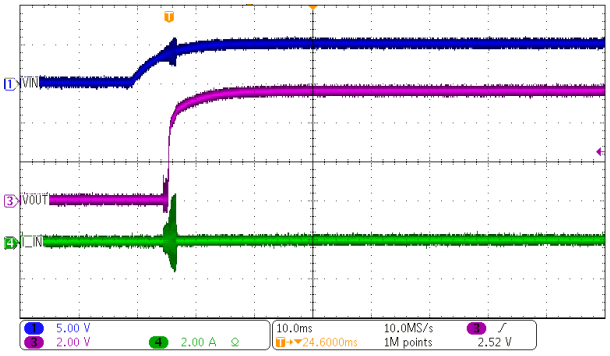


Figure 7-4. DCP020505P Start-Up at 10% Load

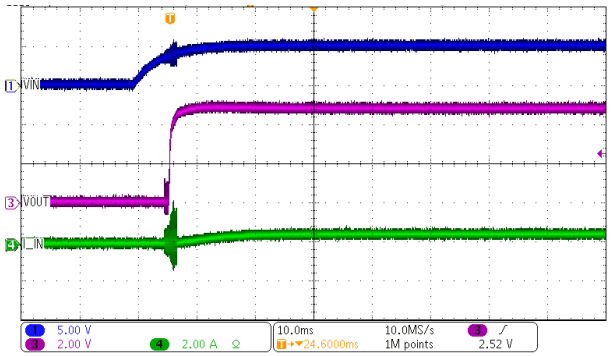


Figure 7-5. DCP020505P Start-Up at 100% Load

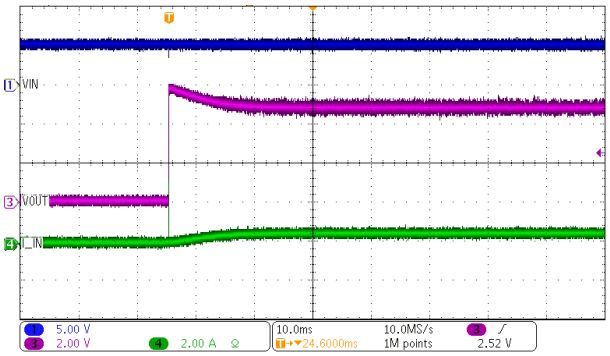


Figure 7-6. DCP020505P Enable Start-Up at 100% Load

7.4 Device Functional Modes

7.4.1 Disable/Enable (SYNC pin)

Any of the DCP02 series devices can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 becomes disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2 µs. Removal of the pull down causes the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized (≤ 3 pF) in order to prevent a reduction in the oscillator frequency. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes disable/enable control circuitry.

7.4.2 Decoupling

7.4.2.1 Ripple Reduction

The high switching frequency of 400 kHz allows simple filtering. To reduce ripple, it is recommended that a minimum of 1-µF capacitor be used on the V_{OUT} pin. For dual output devices, decouple both of the outputs to the COM pin. A 2.2-µF capacitor on the input is also recommended.

7.4.2.2 Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCP02.

Connect the $+V_{OUT}$ from one DCP02 to the $–V_{OUT}$ of another (see Figure 7-7). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 prevents beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, thus minimizing cost.

The outputs of a dual-output DCP02 can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 7-8. For example, connect a dual-output, 15-V, DCP022415D device to provide a 30-V rail.

All 5-V, 12-V, and 15-V input voltage designs require a 2.2-µF, low-ESR ceramic input capacitor, while 24-V input applications require only 0.47 µF of input capacitance.

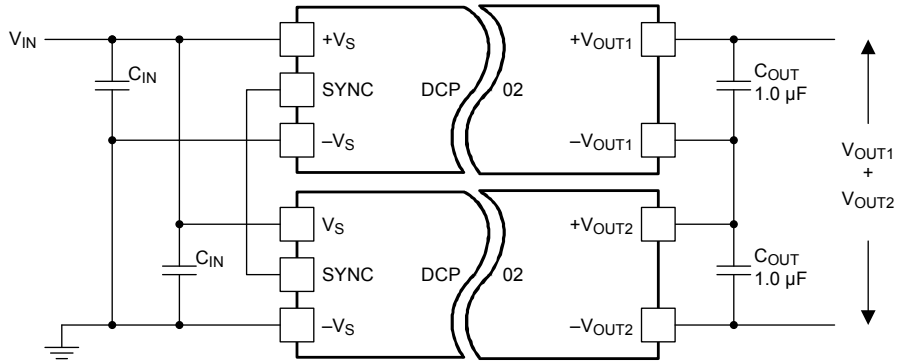


Figure 7-7. Multiple DCP02 Devices Connected in Series

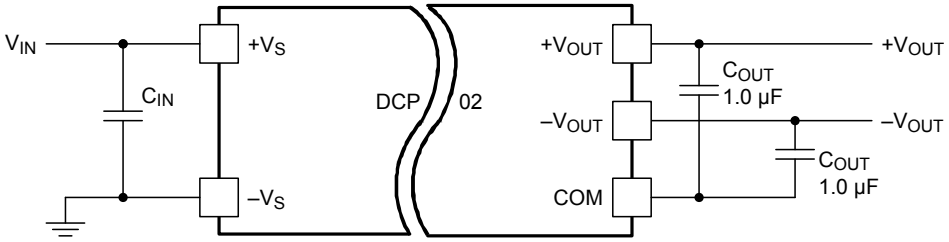


Figure 7-8. Dual Output Devices Connected in Series

7.4.2.3 Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in Figure 7-9, (applies to single output devices only). The SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

All 5-V, 12-V, and 15-V input voltage designs require a 2.2-µF, low-ESR, ceramic input capacitor, while 24-V input applications require only 0.47 µF of input capacitance.

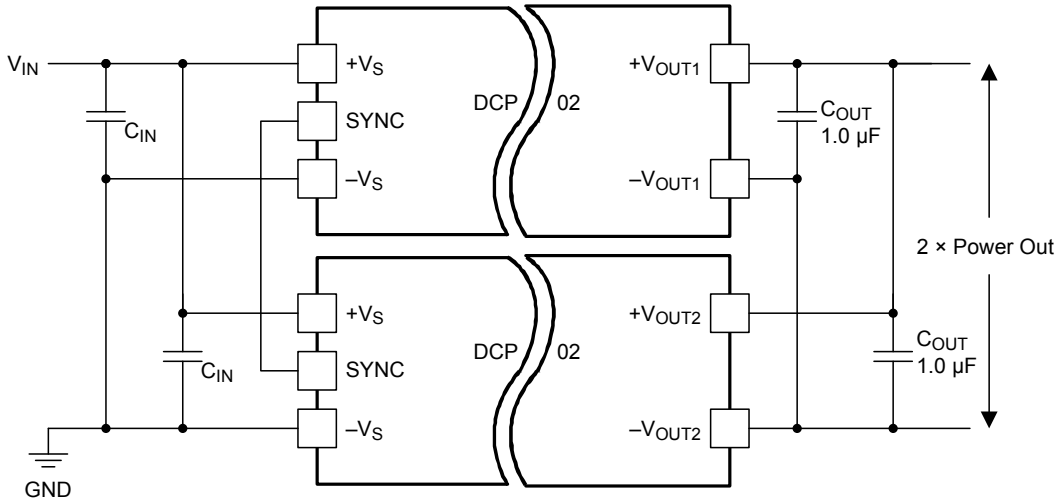


Figure 7-9. Multiple DCP02 Devices Connected in Parallel

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

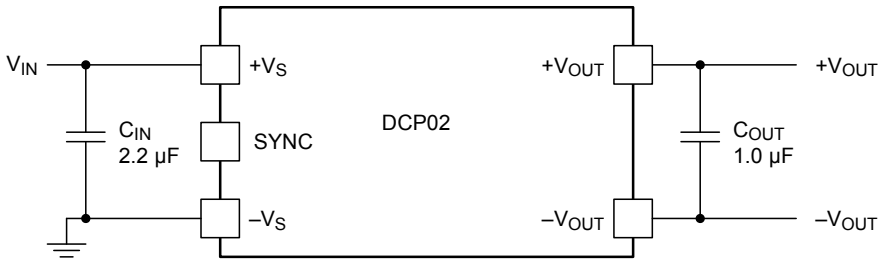


Figure 8-1. Typical DCP020505 Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 and follow the design procedures shown in the *Section 8.2.2*.

Table 8-1. Design Example Parameters

PARAMETER		VALUE	UNIT
$V_{(+VS)}$	Input voltage	5	V
$V_{(+VOUT)}$	Output voltage	5	V
I_{OUT}	Output current rating	400	mA
f_{SW}	Operating frequency	400	kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

For all 5-V, 12-V, and 15-V input voltage designs, select a 2.2-µF low-ESR ceramic input capacitor to ensure a good startup performance. 24-V input applications require only 0.47-µF of input capacitance.

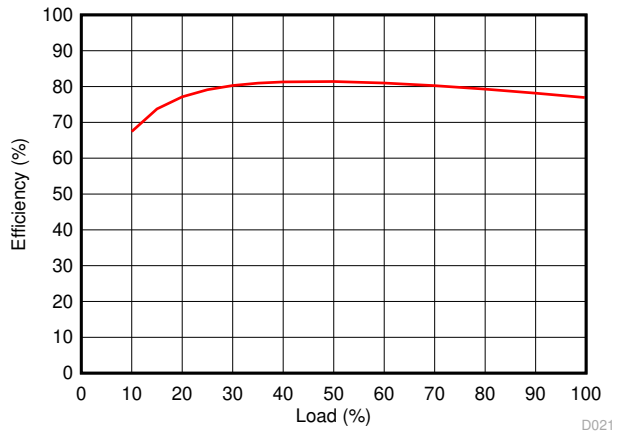
8.2.2.2 Output Capacitor

For any DCP02 design, select a 1.0-µF low-ESR ceramic output capacitor to reduce output ripple.

8.2.2.3 SYNC Pin

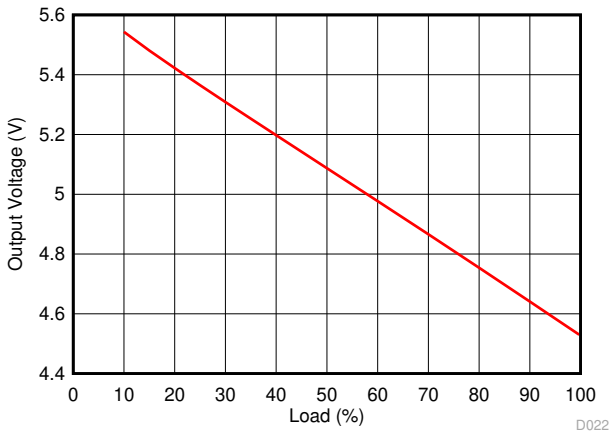
In a stand-alone application, leave the SYNC pin floating.

8.2.3 DCP020505 Application Curves



A. DCP020505P

Figure 8-2. Efficiency versus Load



A. DCP020505P **Note:** Operations under 10% Load

Figure 8-3. Load Regulation

8.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes (tracks) where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the track must be deployed; devices must not be connected in series, as this will cascade the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See the *PCB Layout* section for more details.

8.2.5 Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in Figure 8-4). In Figure 8-4, X_C is the reactance due to the capacitance, X_L is the reactance due to the ESL, and f_0 is the resonant frequency. As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

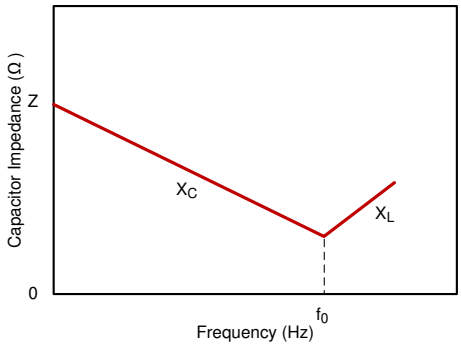


Figure 8-4. Capacitor Impedance versus Frequency

At f_0, $X_C = X_L$; however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance; namely, the value of the ESR. The resonant frequency must be well above the 800-kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in Equation 1.

$$V_{IN} = V_{PK} – (ESR \times I_{TR}) \quad (1)$$

where

- V_{IN} is the voltage at the device input
- V_{PK} is the maximum value of the voltage on the capacitor during charge
- I_{TR} is the transient load current

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), ESR is the dominant factor.

8.2.6 Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic (and has an ESR greater than 20 mΩ), then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. If the voltage falls below approximately 4 V, the DCP detects an undervoltage condition and switches the DCP drive circuits to the off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage results in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value, at which time the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process repeats until the input capacitor charges sufficiently to start the device correctly.

Normal start-up should occur in approximately 1 ms after power is applied to the device. If a considerably longer start-up duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5-V to 15-V input devices, a 2.2-µF, low-ESR ceramic capacitor ensures a good start-up performance. For 24-V input voltage devices, 0.47 µF ceramic capacitors are recommended. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

Note

During the start-up period, these devices may draw maximum current from the input supply. If the input voltage falls below approximately 4 V, the devices may not start up. Connect a 2.2-µF ceramic capacitor close to the input pins.

8.2.7 Ripple and Noise

A good quality, low-ESR ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensures a smooth startup.

A good quality, low-ESR ceramic capacitor placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance. See application report *DC-to-DC Converter Noise Reduction* for more information on noise rejection.

8.2.7.1 Output Ripple Calculation Example

The following example shows that increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

To calculate the output ripple for a DCP020505 device:

- V_{OUT} = 5 V
- I_{OUT} = 0.4 A
- At full output power, the load resistor is 12.5 Ω

- Output capacitor of 1 µF, ESR of 0.1 Ω
- Capacitor discharge time 1% of 800-kHz (ripple frequency)

t_{DIS} = 0.0125 µs

$\tau = C \times R_{LOAD}$

$\tau = 1 \times 10^{-6} \times 12.5 = 12.5$ µs

$V_{DIS} = V_O(1 – EXP(–t_{DIS} / \tau))$

V_{DIS} = 5 mV

By contrast, the voltage dropped because of ESR:

$V_{ESR} = I_{LOAD} \times ESR$

V_{ESR} = 40 mV

Ripple voltage = 45 mV

8.2.8 Dual DCP02 Output Voltage

The voltage output for dual DCP02 devices is half wave rectified; therefore, the discharge time is 1.25 µs. Repeating the above calculations using the 100% load resistance of 25 Ω (0.2 A per output), the results are:

τ = 25 µs

t_{DIS} = 1.25 µs

V_{DIS} = 244 mV

V_{ESR} = 20 mV

Ripple Voltage = 266 mV

This time, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to 10 µF, and repeating the calculations, the result is:

Ripple Voltage = 45 mV

This value is composed of almost equal components.

The previous calculations are offered as a guideline only. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

8.2.9 Optimizing Performance

Optimum performance can only be achieved if the device is correctly supported. The very nature of a switching converter requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected by a low-impedance path.

The optimum performance primarily depends on two factors:

- Connection of the input and output circuits for minimal loss.
- The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

Power Supply Recommendations

The DCP02 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCP02. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

8 Layout

8.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output.

Figure 8-4 and Figure 8-2 illustrate a printed circuit board (PCB) layout for the two conventional (DCP01/02, DCV01), and two SOP surface-mount packages (DCP02U). Figure 8-1 shows the schematic.

Including input power and ground planes provides a low-impedance path for the input power. For the output, the COM signal connects via a ground plane, while the connections for the positive and negative voltage outputs conduct through wide traces in order to minimize losses.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

Allow the unused SYNC pin, to remain configured as a floating pad. It is advisable to place a guard ring (connected to input ground) or annulus connected around this pin to avoid any noise pick up. When connecting a SYNC pin to one or more SYNC design the linking trace to be short and narrow to avoid stray capacitance. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

8.2 Layout Example

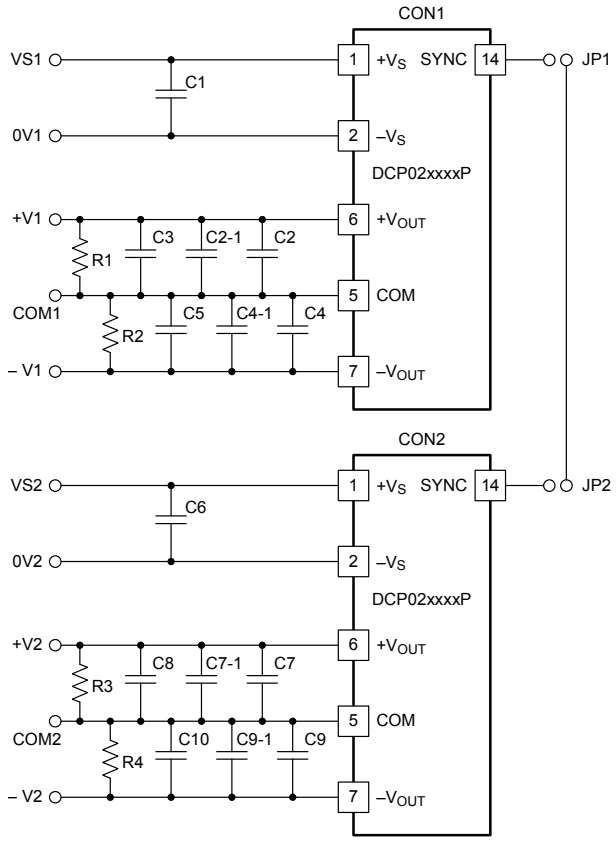


Figure 8-1. PCB Schematic, P Package

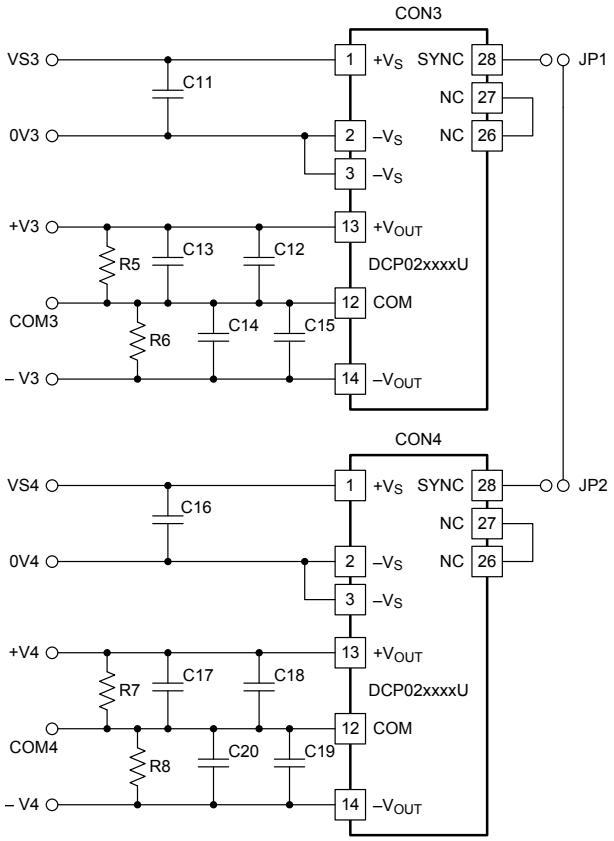


Figure 8-2. PCB Schematic, U Package

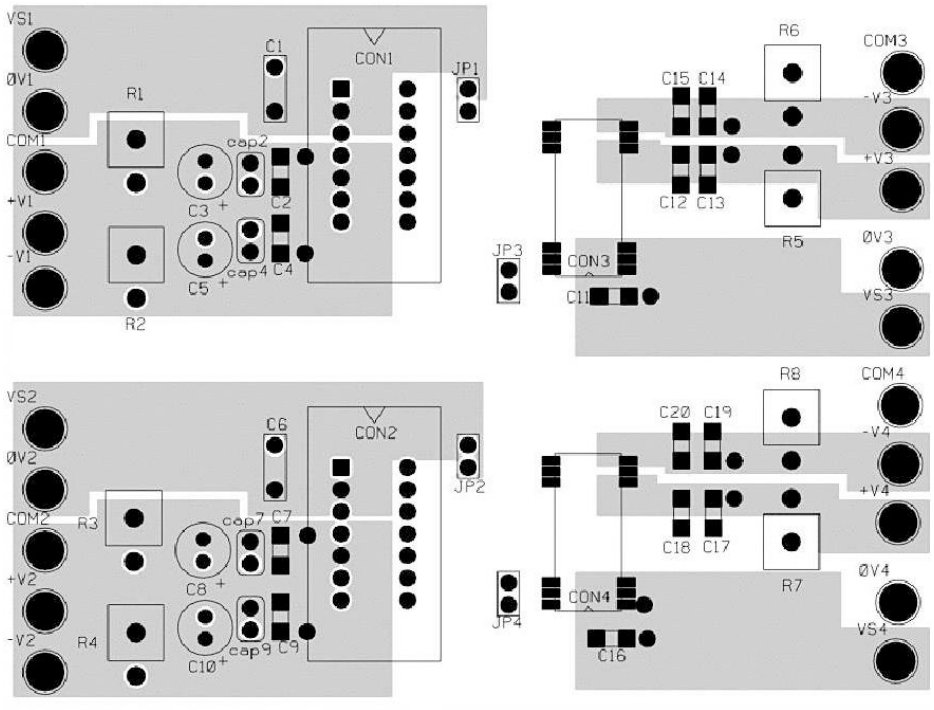


Figure 8-3. PCB Layout Example, Component-Side View

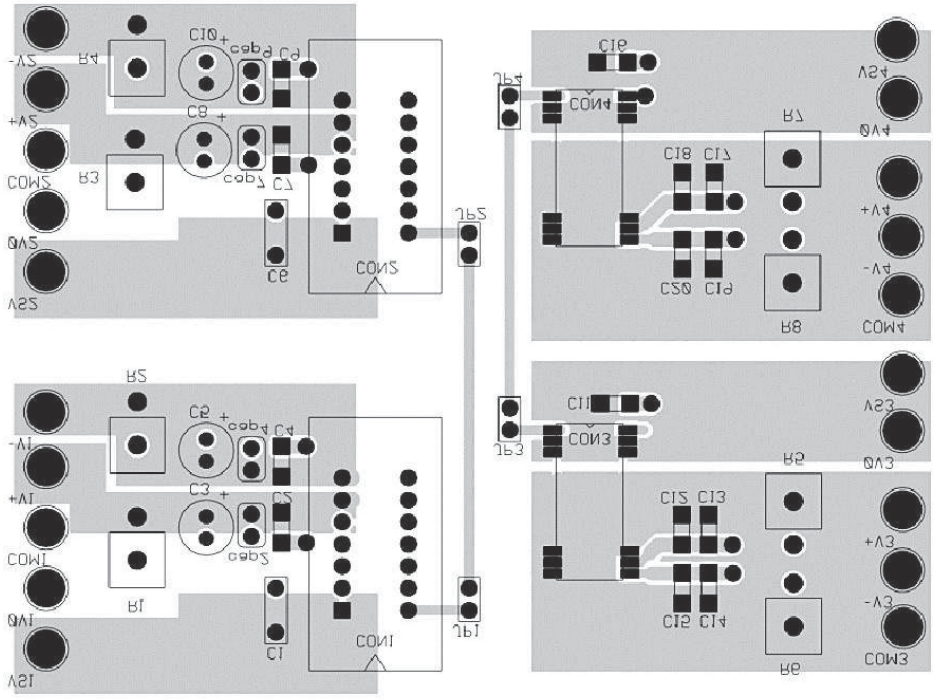


Figure 8-4. PCB Layout Example, Non-Component-Side View

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

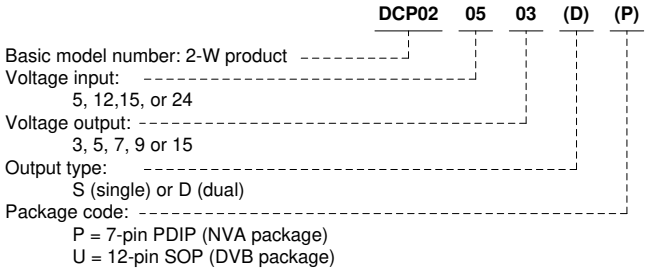


Figure 9-1. Supplemental Ordering Information

9.2 Documentation Support

9.2.1 Related Documentation

- Texas Instruments, *DC-to-DC Converter Noise Reduction*
- Texas Instruments, *External Synchronization of the DCP01/02 Series of DC/DC Converters*
- Texas Instruments, *Optimizing Performance of the DCP01/02 Series of DC/DC Converters*

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DCP020503	Click here	Click here	Click here	Click here	Click here
DCP020505	Click here	Click here	Click here	Click here	Click here
DCP020507	Click here	Click here	Click here	Click here	Click here
DCP020509	Click here	Click here	Click here	Click here	Click here
DCP020515D	Click here	Click here	Click here	Click here	Click here
DCP021205	Click here	Click here	Click here	Click here	Click here
DCP021212	Click here	Click here	Click here	Click here	Click here
DCP021212D	Click here	Click here	Click here	Click here	Click here
DCP021515	Click here	Click here	Click here	Click here	Click here
DCP022405	Click here	Click here	Click here	Click here	Click here
DCP022405D	Click here	Click here	Click here	Click here	Click here
DCP022415D	Click here	Click here	Click here	Click here	Click here

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TI E2E™ is a trademark of Texas Instruments Incorporated.
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9.6 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP020503P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP020503P	Samples
DCP020503U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020503U	Samples
DCP020505P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP020505P	Samples
DCP020505U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020505U	Samples
DCP020505U/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020505U	Samples
DCP020505UE4	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020505U	Samples
DCP020507P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP020507P	Samples
DCP020507U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020507U	Samples
DCP020507U/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020507U	Samples
DCP020509P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP020509P	Samples
DCP020509U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020509U	Samples
DCP020515DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP020515DP	Samples
DCP020515DU	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020515DU	Samples
DCP020515DU/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP020515DU	Samples
DCP021205P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP021205P	Samples
DCP021205U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021205U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP021205U/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021205U	Samples
DCP021212DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP021212DP	Samples
DCP021212DU	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021212DU	Samples
DCP021212DU/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021212DU	Samples
DCP021212P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP021212P	Samples
DCP021212U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021212U	Samples
DCP021212U/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021212U	Samples
DCP021515P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP021515P	Samples
DCP021515U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021515U	Samples
DCP021515U/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP021515U	Samples
DCP022405DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP022405DP	Samples
DCP022405DU	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP022405DU	Samples
DCP022405P	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP022405P	Samples
DCP022405U	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP022405U	Samples
DCP022415DP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	DCP022415DP	Samples
DCP022415DU	ACTIVE	SOP	DVB	12	28	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP022415DU	Samples
DCP022415DU/1K	ACTIVE	SOP	DVB	12	1000	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DCP022415DU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

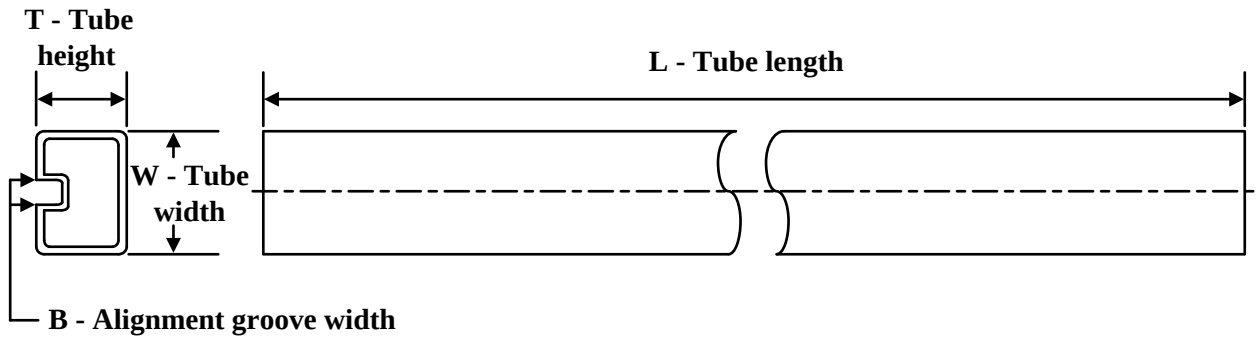
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

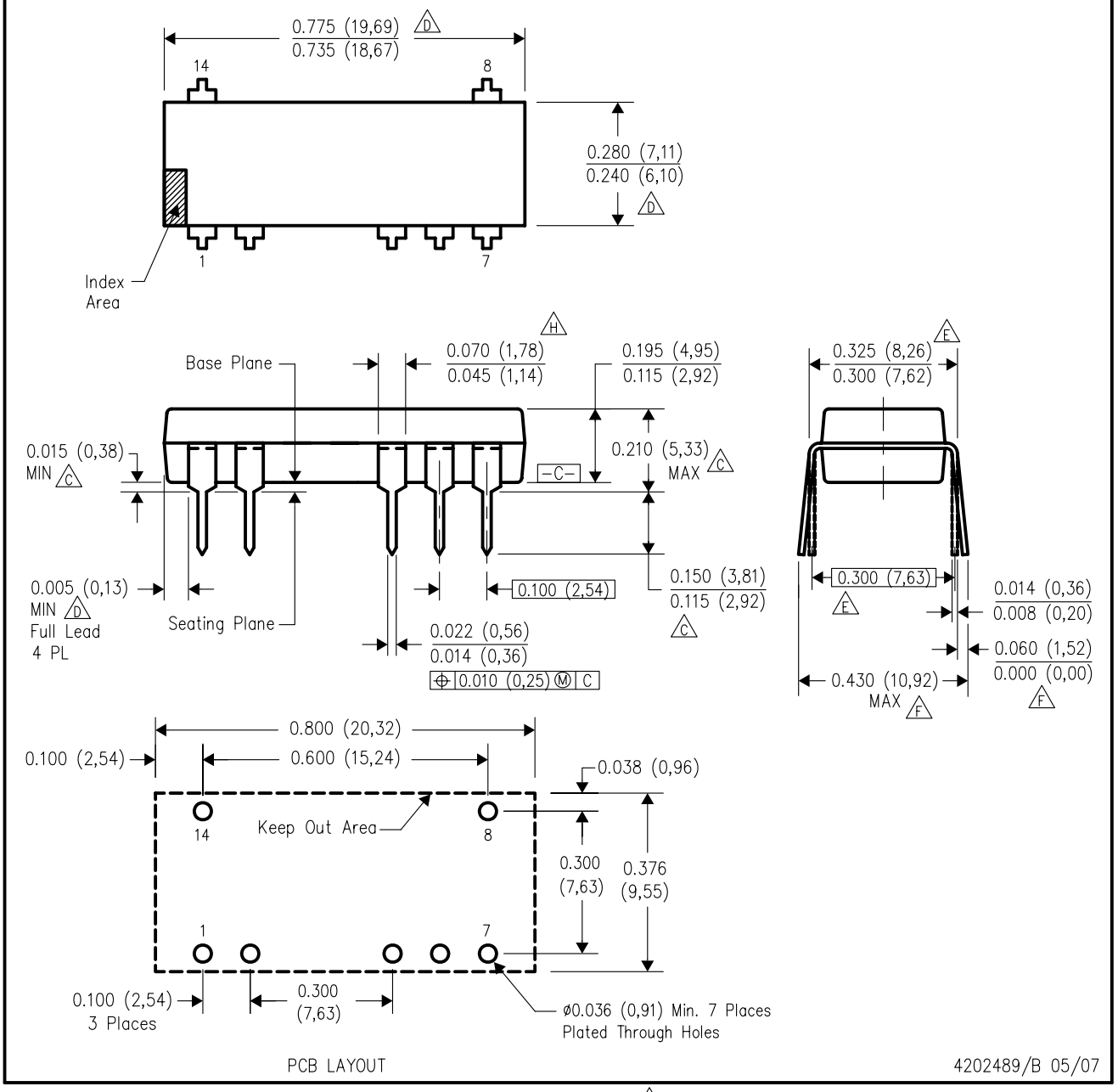
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DCP020503P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP020503U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP020505P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP020505U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP020505UE4	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP020507P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP020507U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP020509P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP020509U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP020515DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP020515DU	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP021205P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP021205U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP021212DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP021212DU	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP021212P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP021212U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP021515P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP021515U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP022405DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP022405DU	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP022405P	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP022405U	DVB	SOP	12	28	532.13	14.73	5.13	6.6
DCP022415DP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP022415DU	DVB	SOP	12	28	532.13	14.73	5.13	6.6

NVA (R–PDIP–T7/14) PLASTIC DUAL–IN–LINE



PCB LAYOUT

4202489/B 05/07

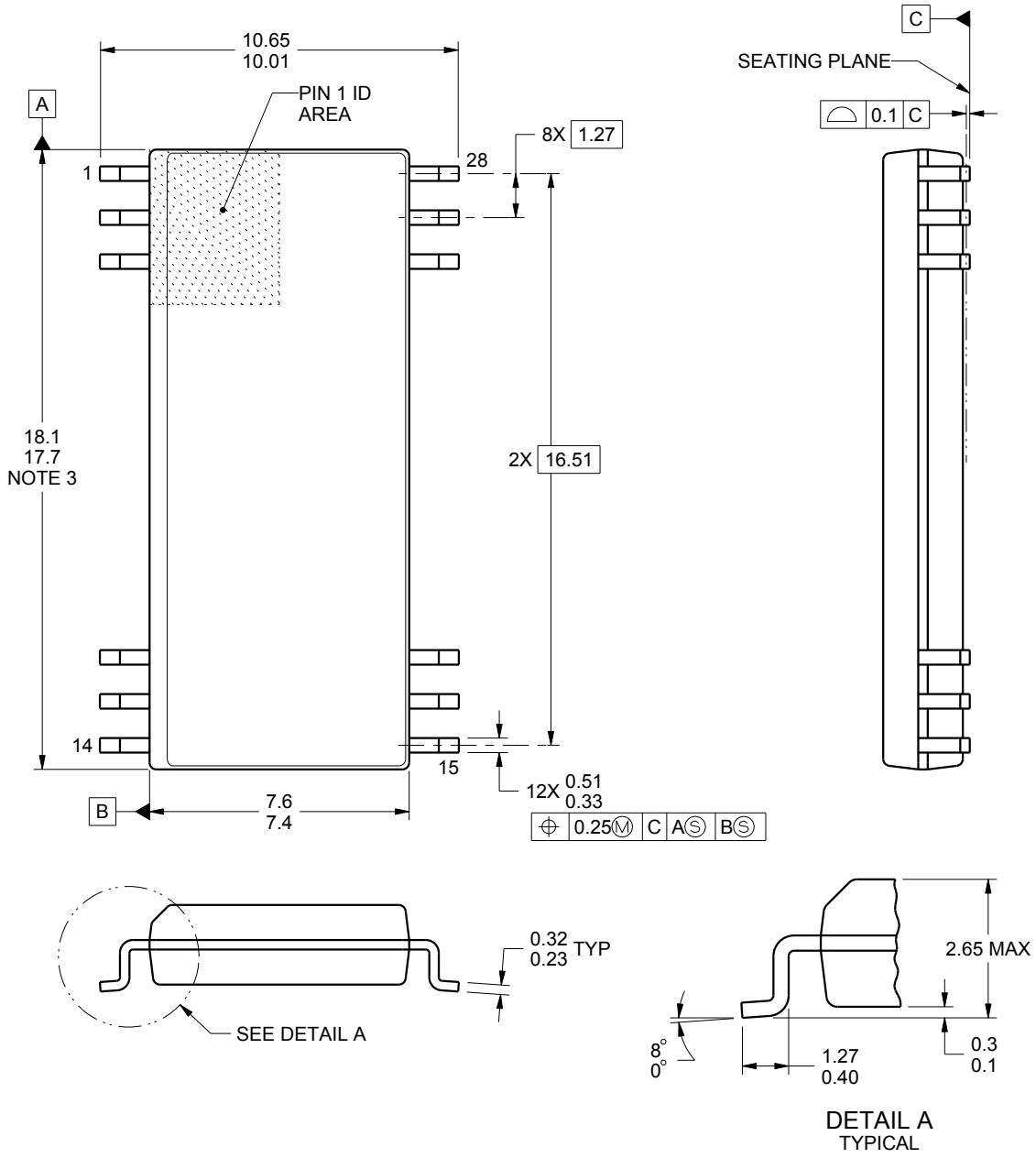
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS–3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross–hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS–001–AA.

PACKAGE OUTLINE

DVB0012A

SOP - 2.65 mm max height

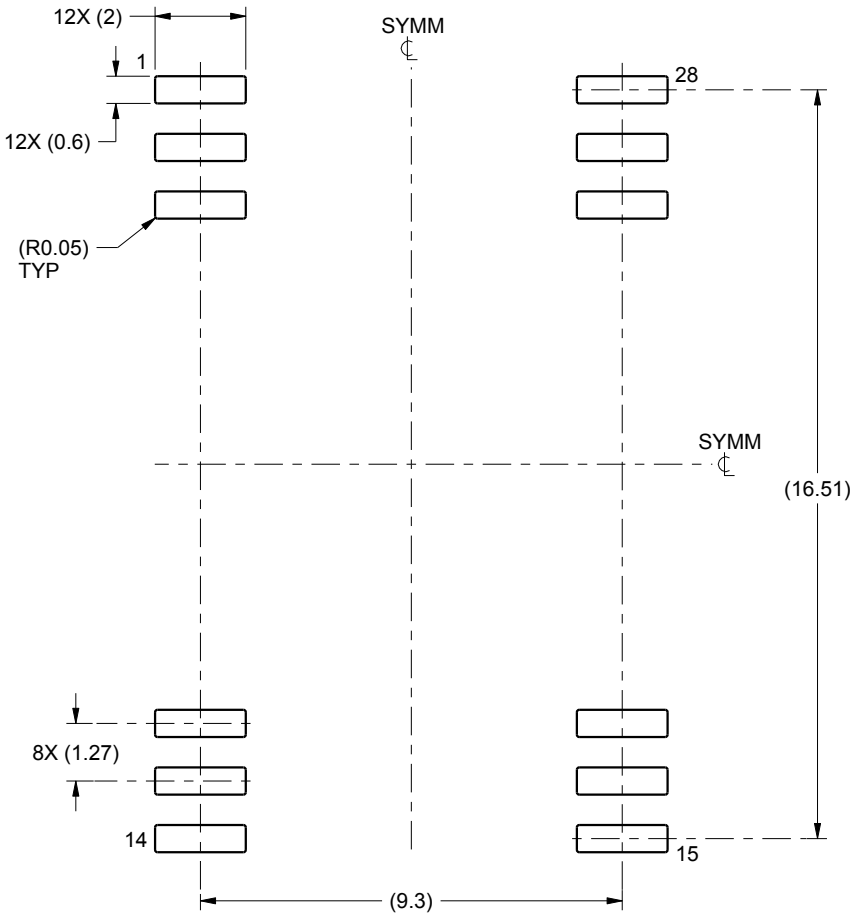
PLASTIC SMALL OUTLINE



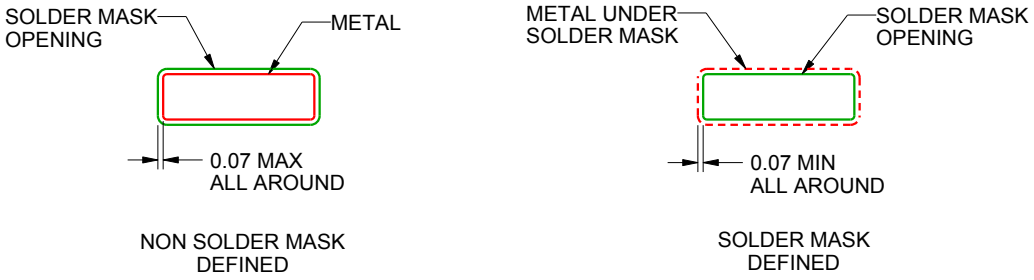
4222497/A 10/2015

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

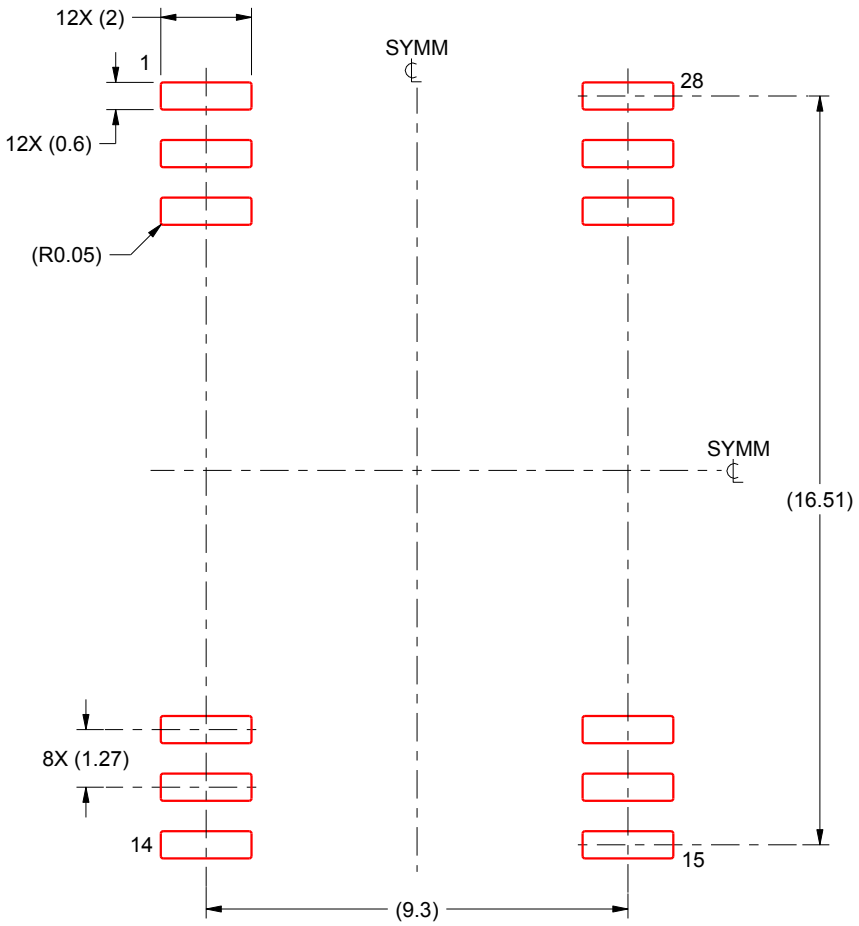


SOLDER MASK DETAILS

4222497/A 10/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222497/A 10/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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