



**THE DATASHEET OF  
C3M0075120J**



# C3M0075120J

Silicon Carbide Power MOSFET  
C3M™ MOSFET Technology  
N-Channel Enhancement Mode

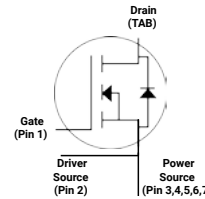


TO-263-7



## Features

- 3<sup>rd</sup> generation SiC MOSFET technology
- Low impedance package with driver source pin
- 7 mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant



Package Types: TO-263-7  
PN's: C3M0075120J

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## Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch mode power supplies

## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			1200	v	$T_C = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	$I_D$			30	A	$V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19 Note 2
				19.7		$V_{GS} = 15\text{ V}, T_C = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$			80		$t_{Pmax}$ limited by $T_{Jmax}$ $V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}$	Fig. 22
Power Dissipation	$P_D$			113.6	W	$T_C = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	$T_J, T_{stg}$			-55 to +150	°C		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with  $\pm 5\%$  regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


**Electrical Characteristics** ( $T_C = 25\text{ }^\circ\text{C}$  Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	$V_{DS} = V_{GS}, I_D = 5\text{ mA}$	Fig. 11
			2.2			$V_{DS} = V_{GS}, I_D = 5\text{ mA}, T_J = 150\text{ }^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$		1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		75	90	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 20\text{ A}$	Fig. 4, 5, 6
			100			$V_{GS} = 15\text{ V}, I_D = 20\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Transconductance	$g_{fs}$		12		S	$V_{DS} = 20\text{ V}, I_{DS} = 20\text{ A}$	Fig. 7
			13			$V_{DS} = 20\text{ V}, I_{DS} = 20\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Input Capacitance	$C_{iss}$		1390		pF	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V}$ $f = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	$C_{oss}$		58				
Reverse Transfer Capacitance	$C_{rss}$		2				
$C_{oss}$ Stored Energy	$E_{oss}$		33		$\mu\text{J}$		Fig. 16
Turn-On Switching Energy (Body Diode FWD)	$E_{ON}$		200		$\mu\text{J}$	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 20\text{ A},$ $R_{G(ext)} = 0\text{ }\Omega, L = 156\text{ }\mu\text{H}, T_J = 150\text{ }^\circ\text{C}$	Fig. 26, 29
Turn-Off Switching Energy (Body Diode FWD)	$E_{OFF}$		90				
Turn-On Delay Time	$t_{d(on)}$		7		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 20\text{ A}, R_{G(ext)} = 0\text{ }\Omega,$ Timing Relative to $V_{DS}$ Inductive Load	Fig. 27, 28, 29
Rise Time	$t_r$		15				
Turn-Off Delay Time	$t_{d(off)}$		24				
Fall Time	$t_f$		8				
Internal Gate Resistance	$R_{G(int)}$		9		$\Omega$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	$Q_{gs}$		18		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 20\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	$Q_{gd}$		12				
Total Gate Charge	$Q_g$		48				



### Reverse Diode Characteristics ( $T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	$V_{SD}$	4.5		V	$V_{GS} = -4\text{ V}, I_{SD} = 10\text{ A}$	Fig. 8, 9, 10
		4.0			$V_{GS} = -4\text{ V}, I_{SD} = 10\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Continuous Diode Forward Current	$I_S$		22.4	A	$V_{GS} = -4\text{ V}$	
Diode Pulse Current	$I_{S, pulse}$	80			$V_{GS} = -4\text{ V}$ , Pulse Width $t_p$ Limited by $T_{Jmax}$	
Reverse Recovery Time	$t_{rr}$	25		ns	$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1925\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Fig. 29
Reverse Recovery Charge	$Q_{rr}$	109		nC		
Peak Reverse Recovery Current	$I_{rrm}$	11		A		

### Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40			

Typical Performance

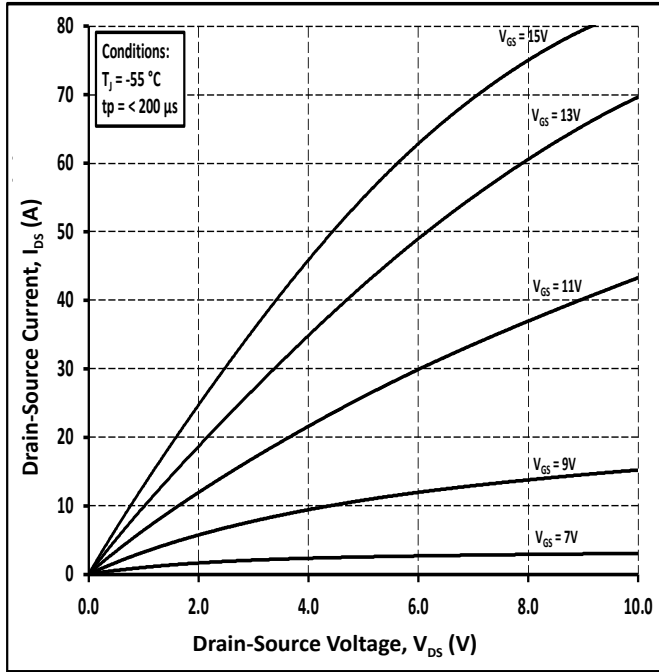


Figure 1. Output Characteristics  $T_j = -55\text{ }^\circ\text{C}$

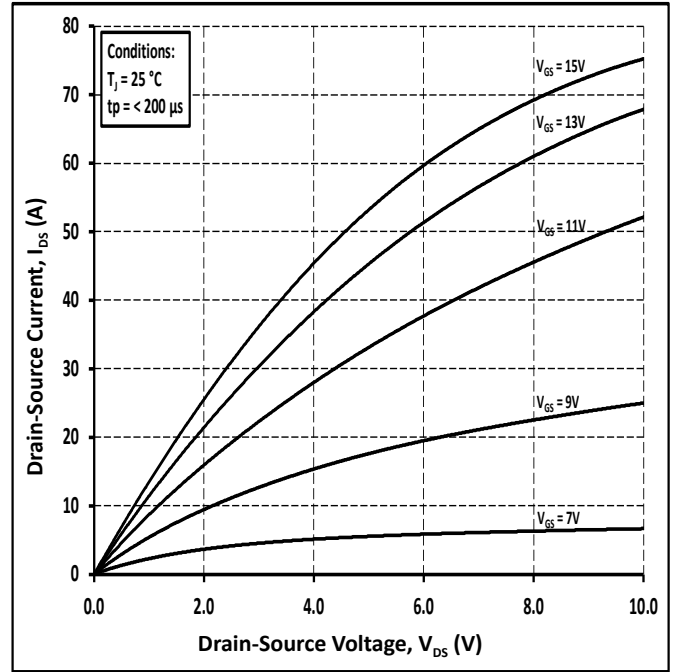


Figure 2. Output Characteristics  $T_j = 25\text{ }^\circ\text{C}$

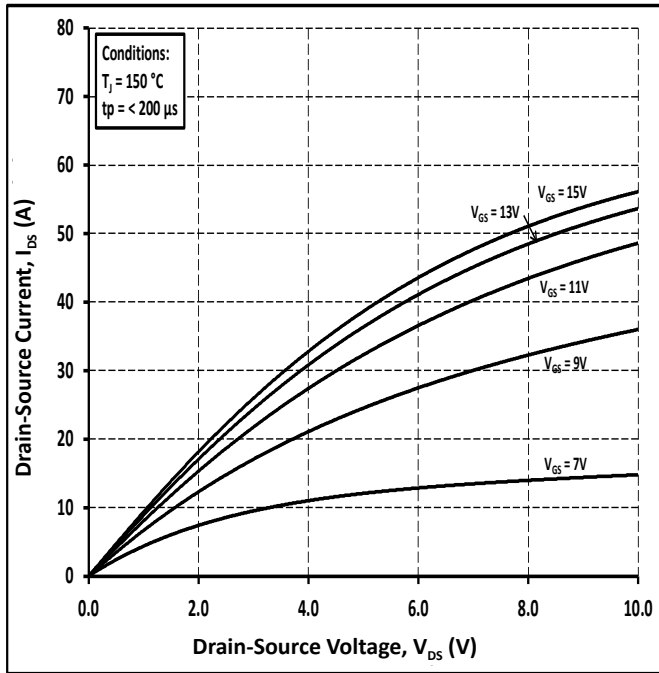


Figure 3. Output Characteristics  $T_j = 150\text{ }^\circ\text{C}$

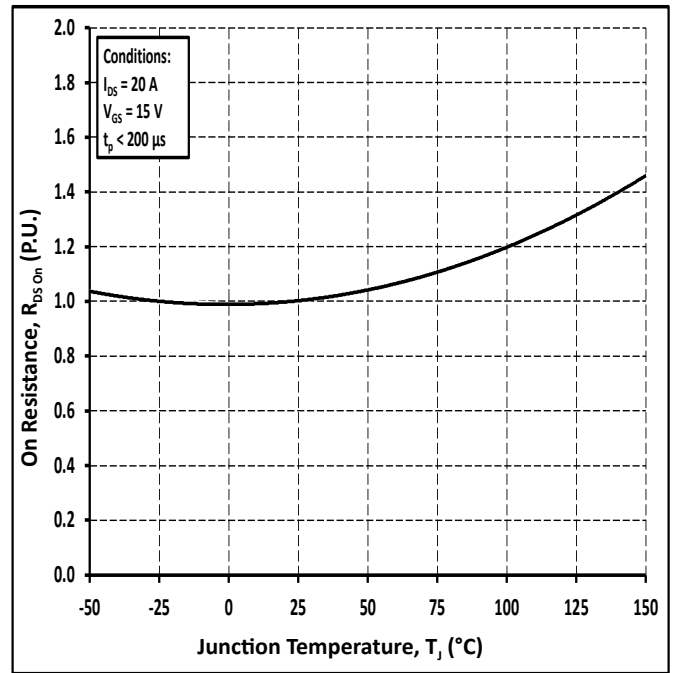


Figure 4. Normalized On-Resistance vs Temperature



Typical Performance

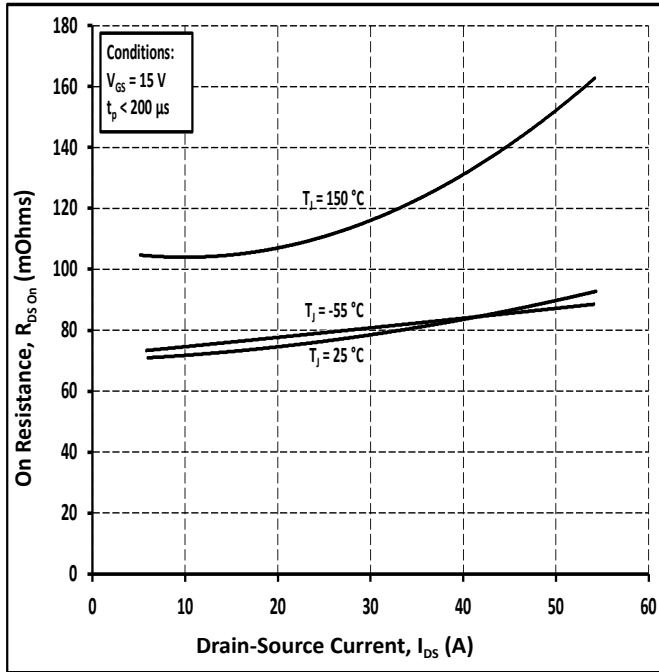


Figure 5. On-Resistance vs Drain Current for Various Temperatures

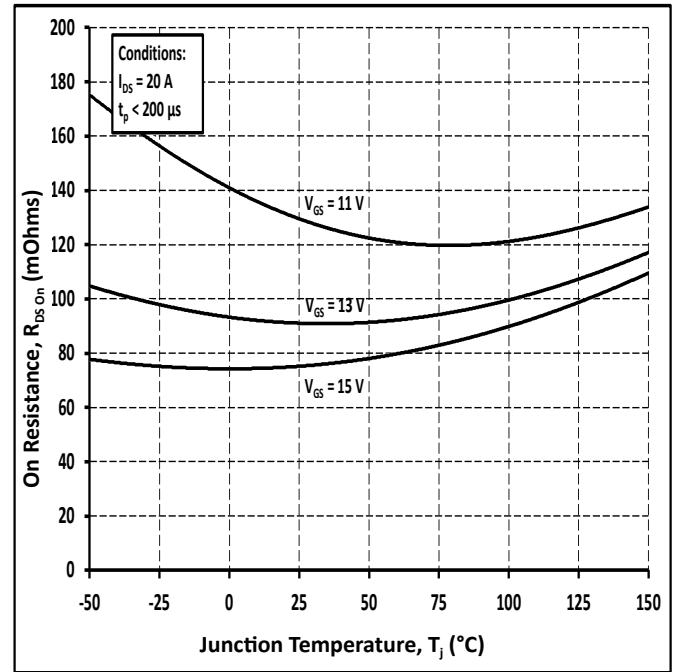


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

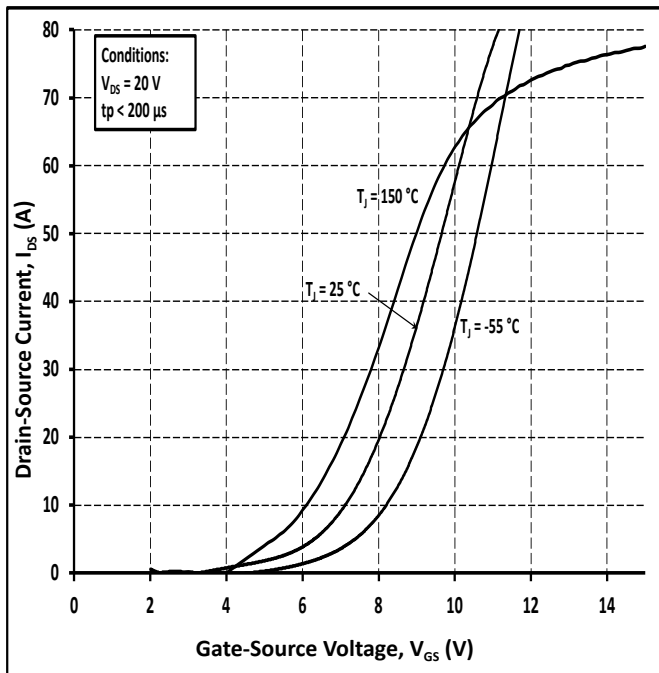


Figure 7. Transfer Characteristic for Various Junction Temperatures

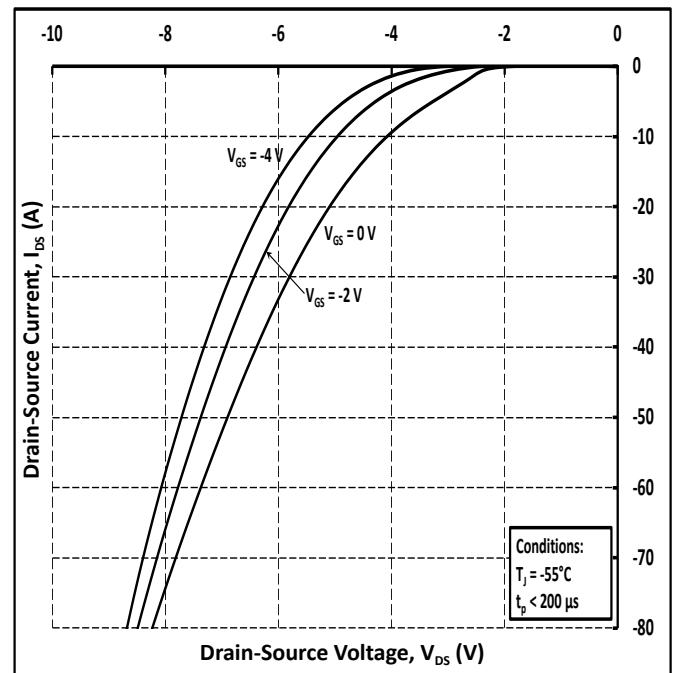


Figure 8. Body Diode Characteristic at -55°C



Typical Performance

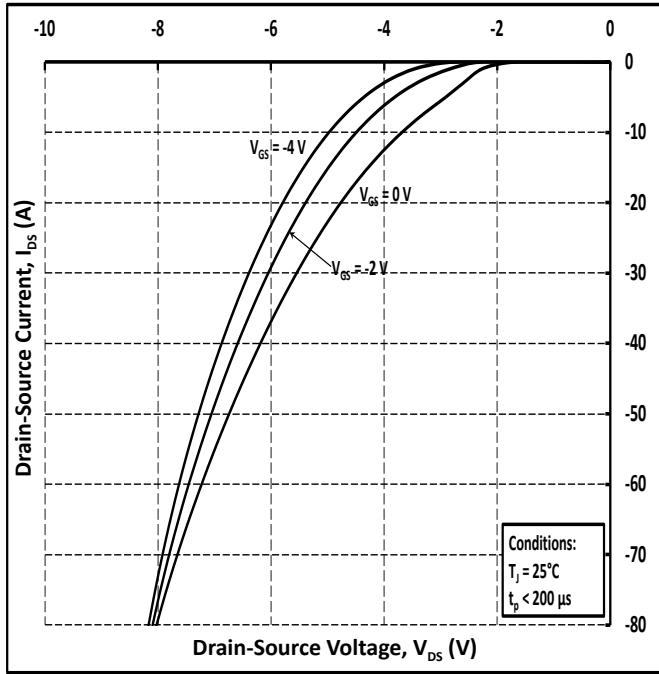


Figure 9. Body Diode Characteristic at 25 °C

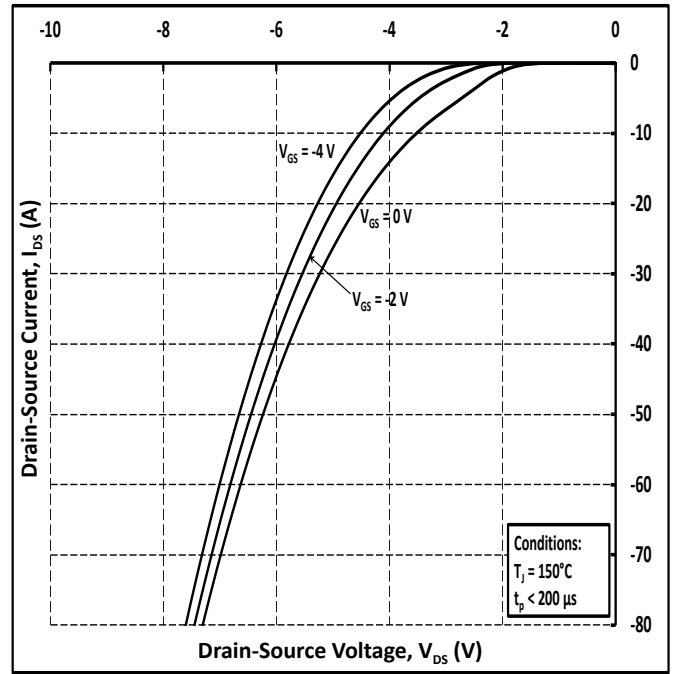


Figure 10. Body Diode Characteristic at 150 °C

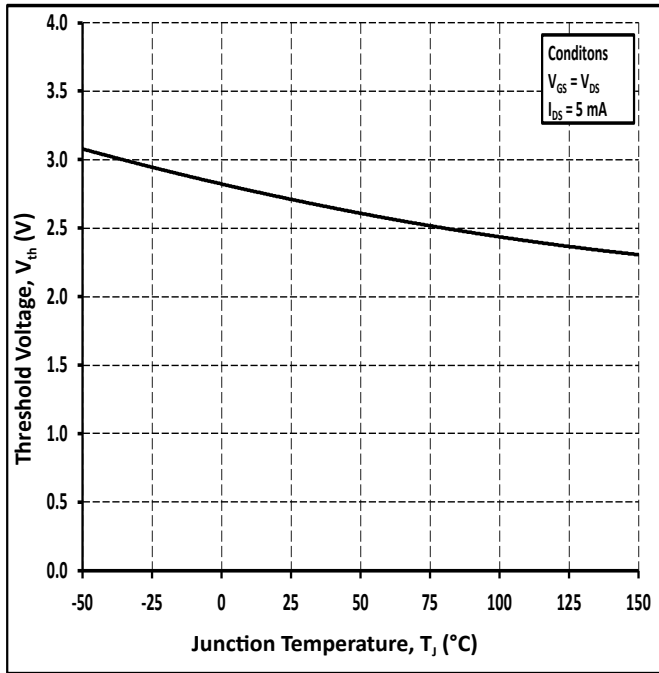


Figure 11. Threshold Voltage vs Temperature

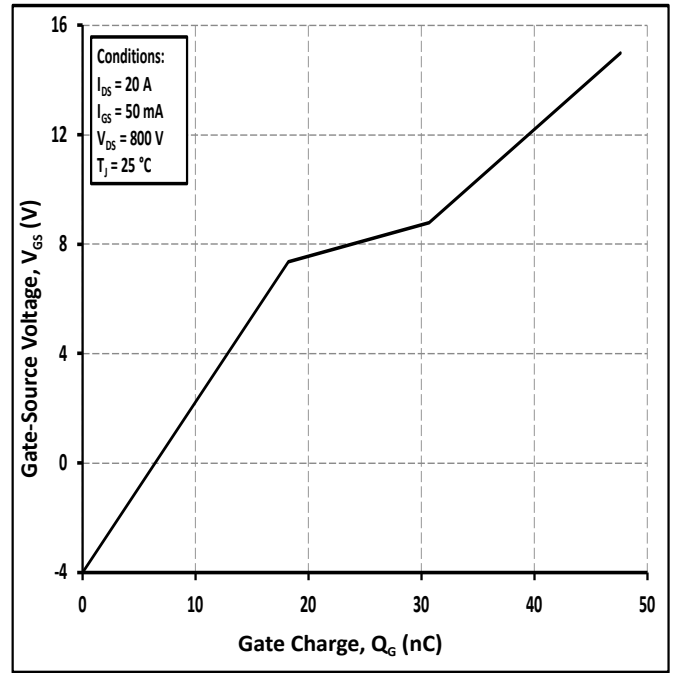


Figure 12. Gate Charge Characteristic



Typical Performance

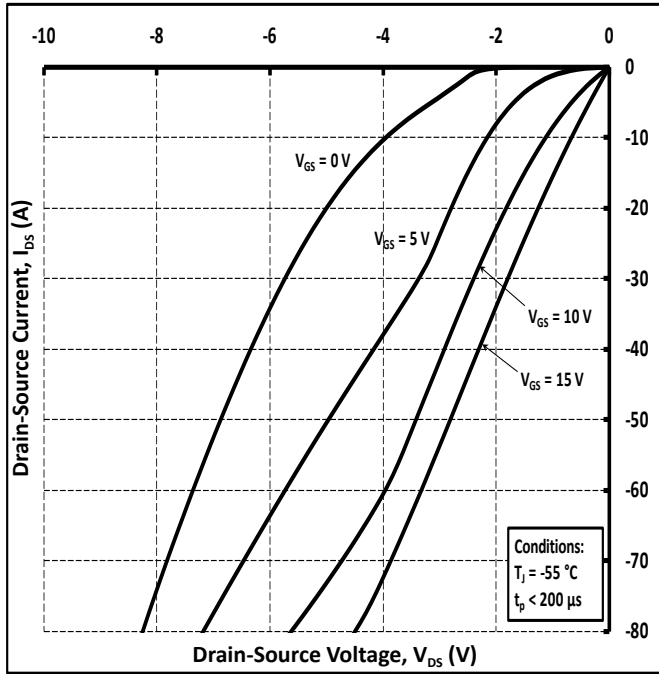


Figure 13. 3<sup>rd</sup> Quadrant Characteristic at  $-55\text{ }^\circ\text{C}$

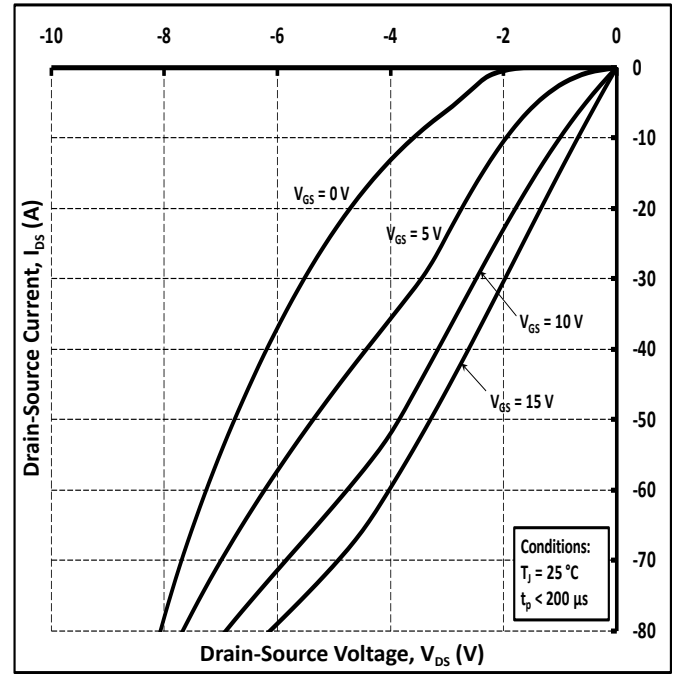


Figure 14. 3<sup>rd</sup> Quadrant Characteristic at  $25\text{ }^\circ\text{C}$

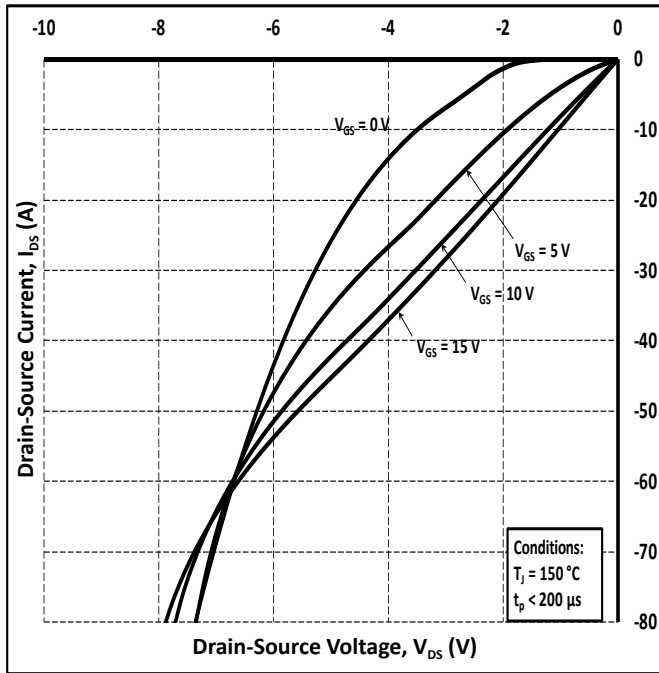


Figure 15. 3<sup>rd</sup> Quadrant Characteristic at  $150\text{ }^\circ\text{C}$

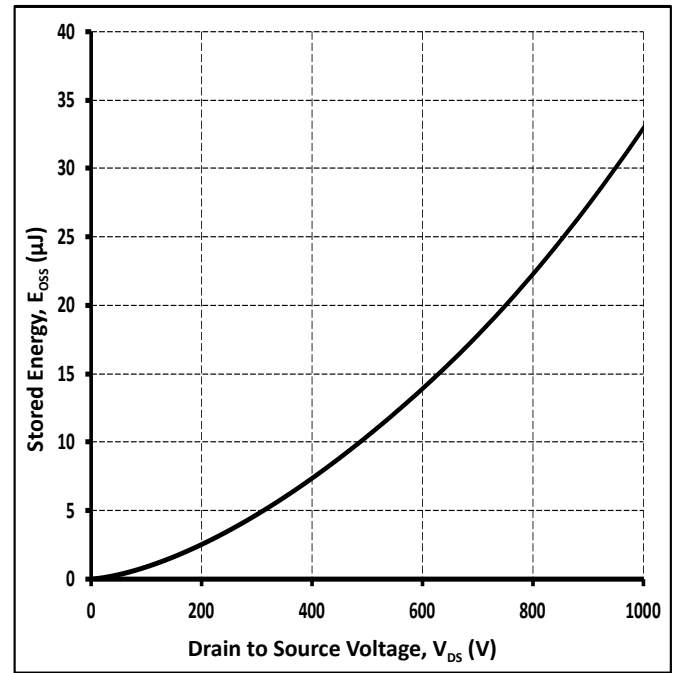


Figure 16. Output Capacitor Stored Energy

Typical Performance

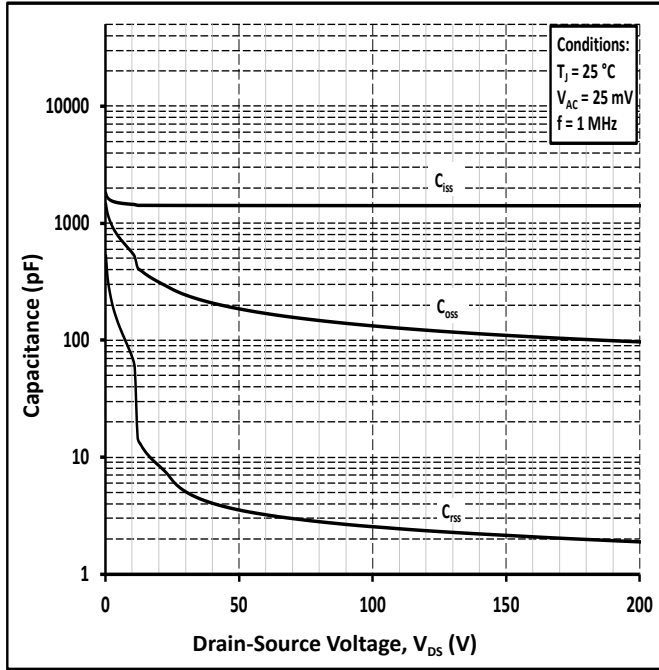


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

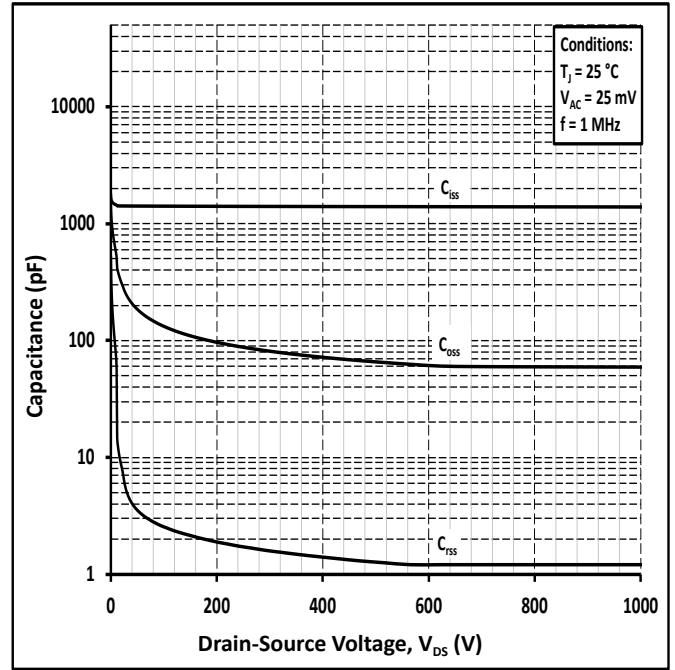


Figure 18. Capacitances vs Drain-Source Voltage (0-1000 V)

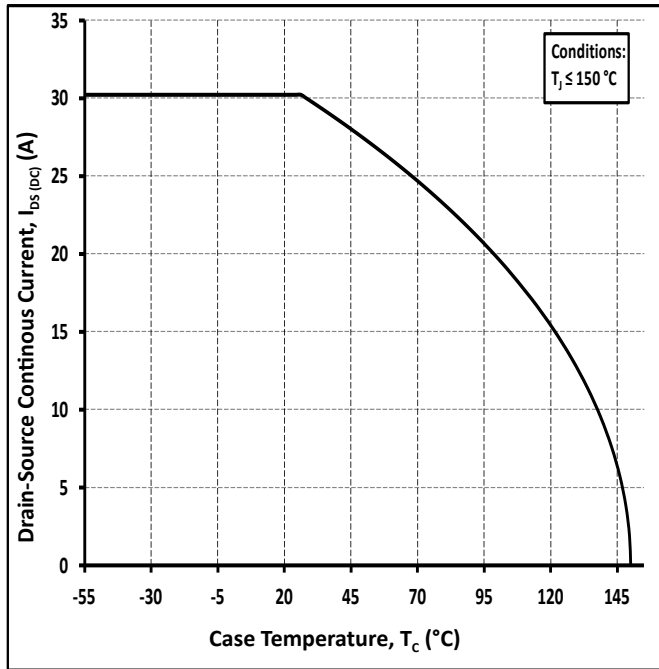


Figure 19. Continuous Drain Current Derating vs Case Temperature

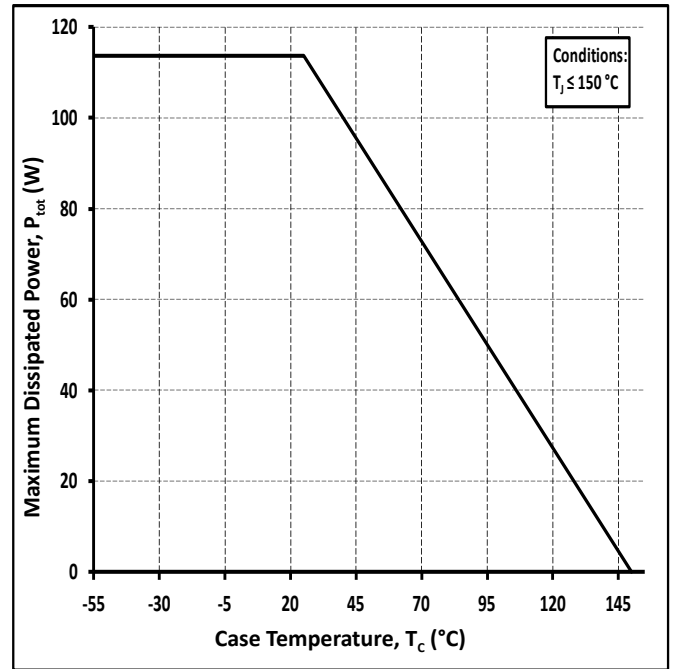


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

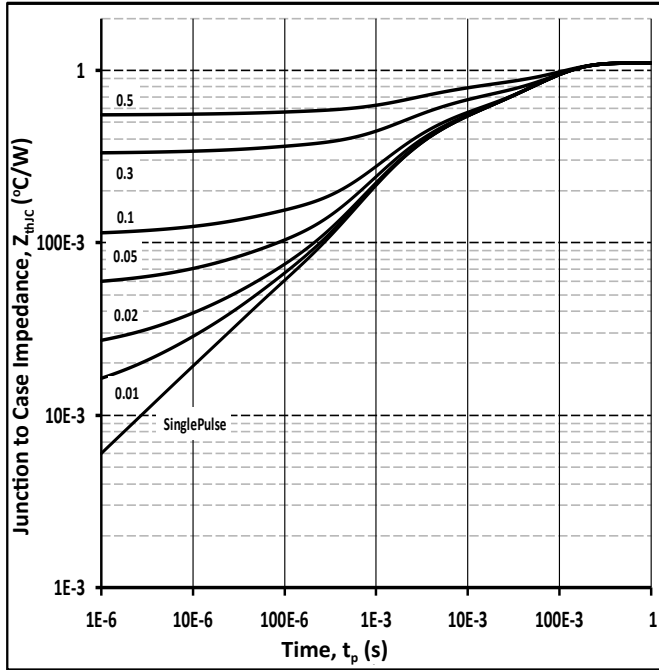


Figure 21. Transient Thermal Impedance (Junction - Case)

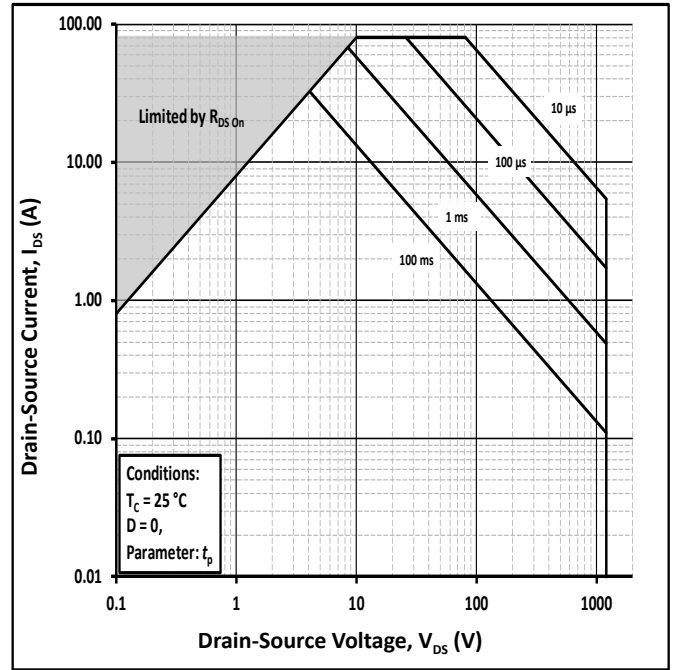


Figure 22. Safe Operating Area

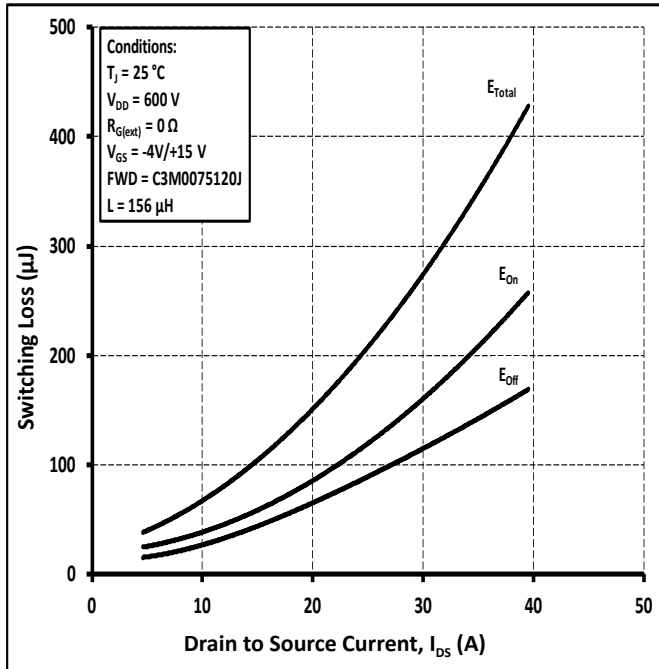


Figure 23. Clamped Inductive Switching Energy vs Drain Current ( $V_{DD} = 600\text{ V}$ )

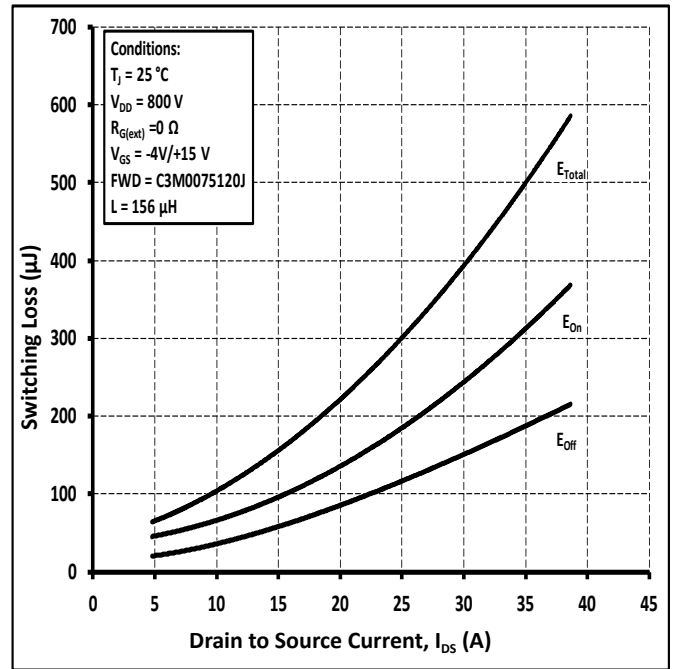


Figure 24. Clamped Inductive Switching Energy vs Drain Current ( $V_{DD} = 800\text{ V}$ )



Typical Performance

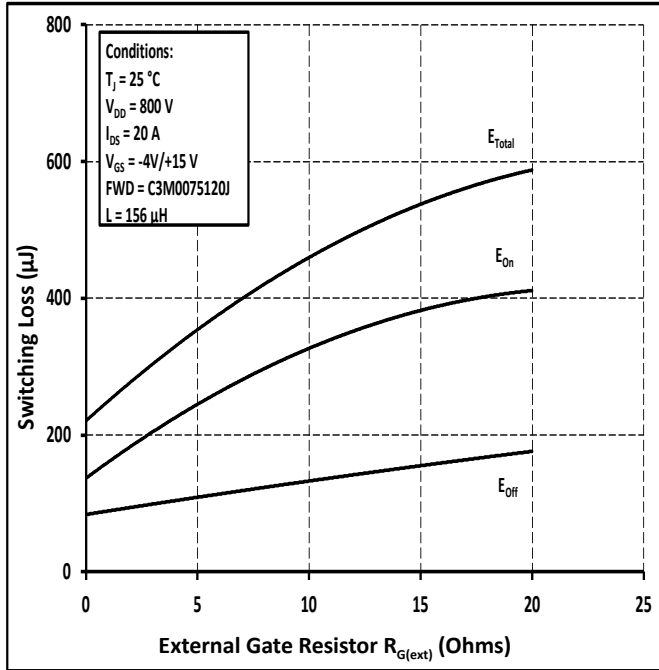


Figure 25. Clamped Inductive Switching Energy vs  $R_{G(ext)}$

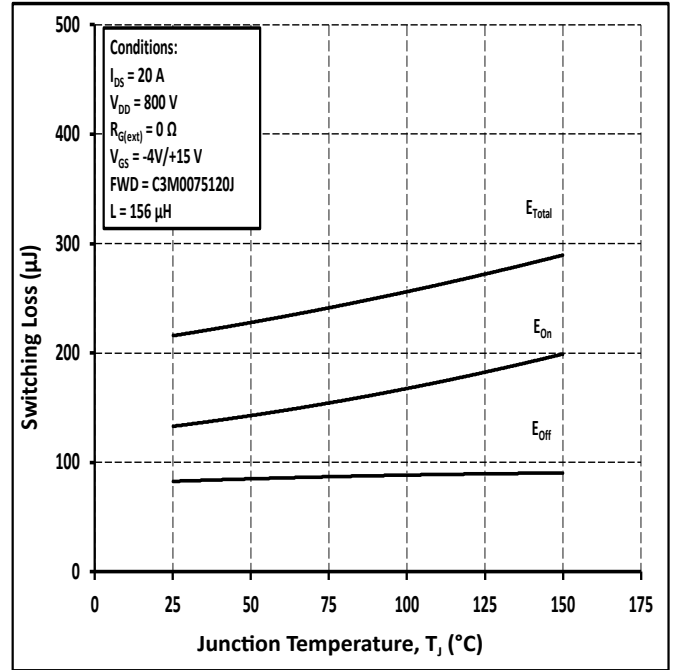


Figure 26. Clamped Inductive Switching Energy vs Temperature

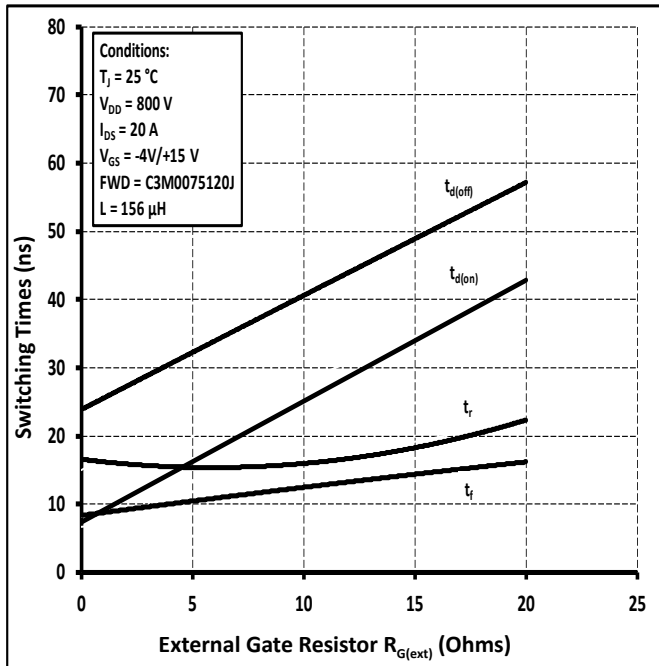


Figure 27. Switching Times vs  $R_{G(ext)}$

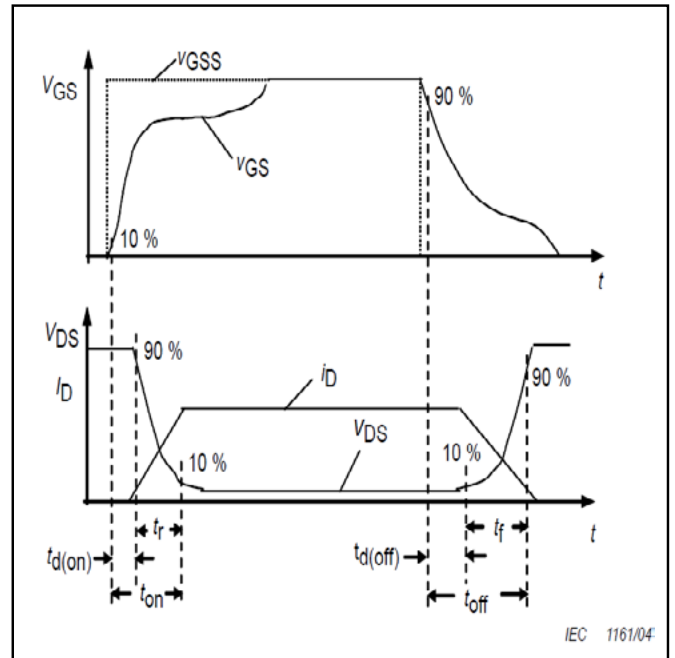


Figure 28. Switching Times Definition

## Test Circuit Schematic

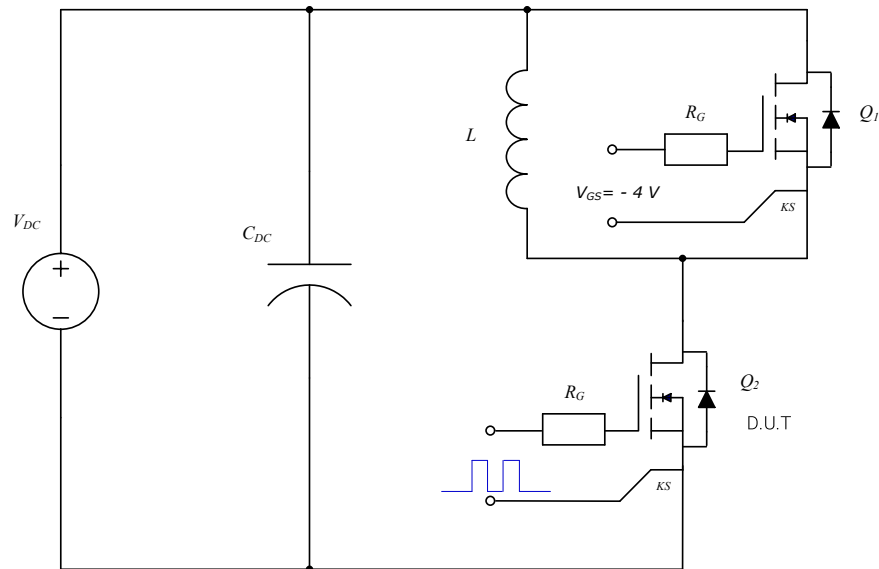


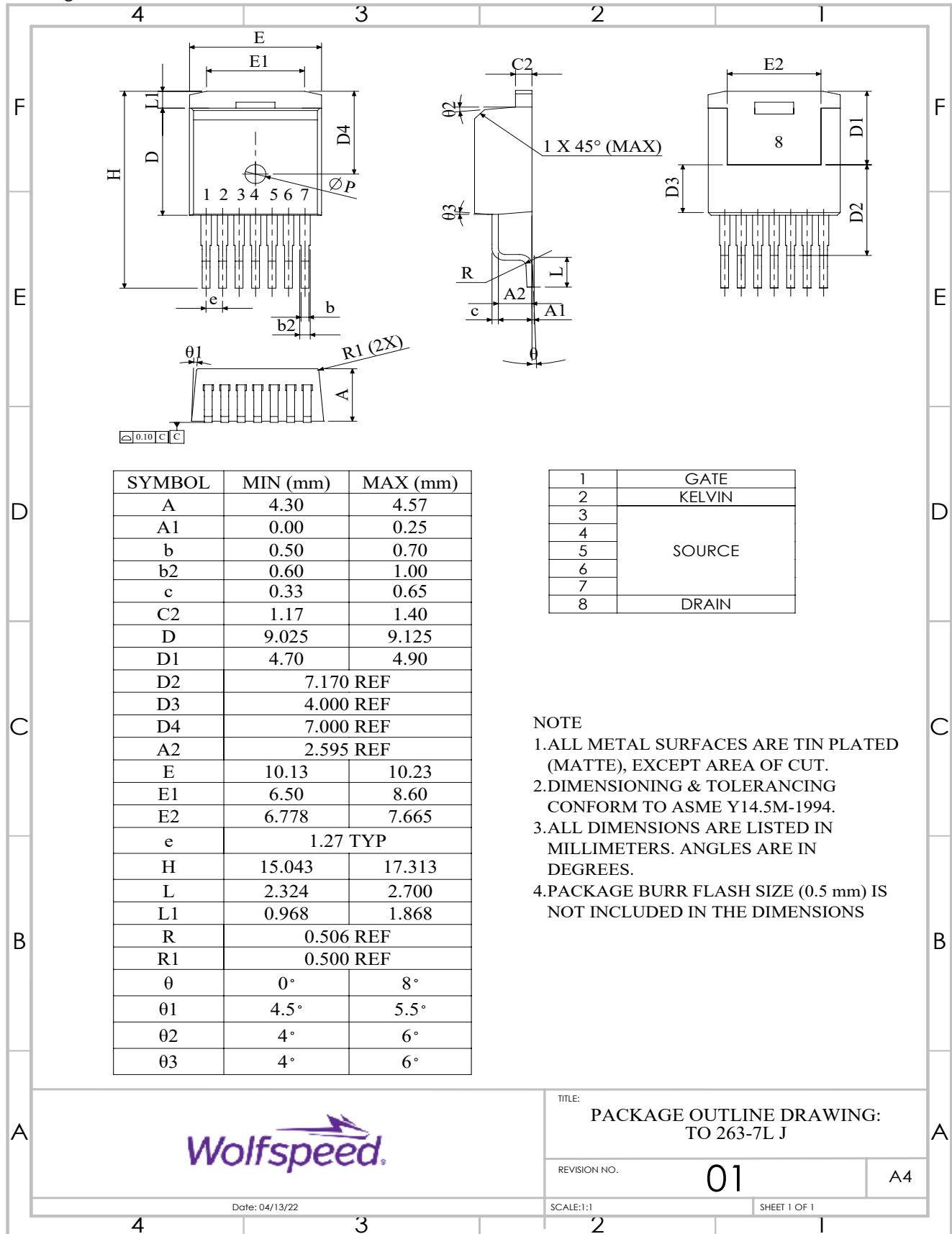
Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET body diode as shown above.



**Package Dimensions**

Package: TO-263-7L



**NOTE**  
 1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.  
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.  
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.  
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



TITLE:  
**PACKAGE OUTLINE DRAWING:  
 TO 263-7L J**

REVISION NO. **01** A4

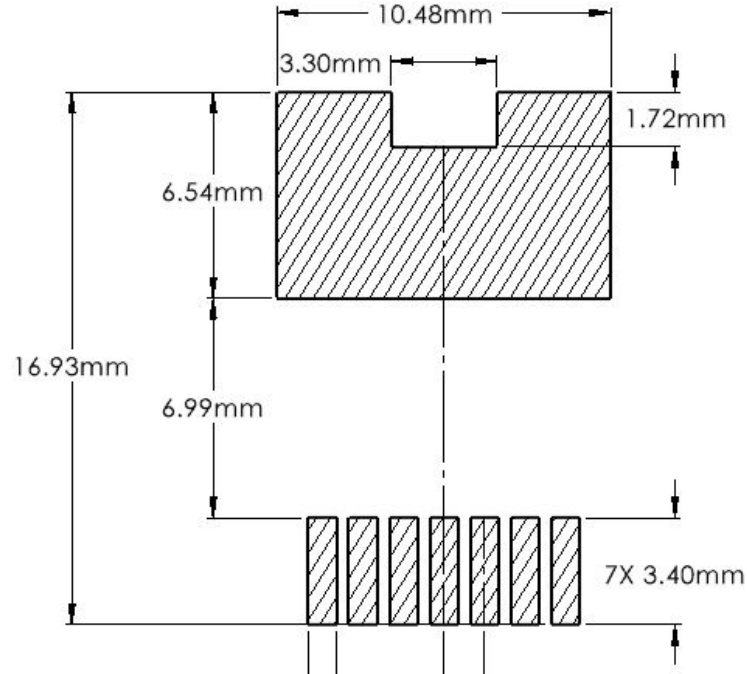
Date: 04/13/22

SCALE: 1:1

SHEET 1 OF 1



## Recommended Solder Pad Layout



## Revision History

Current Revision	Date of Release	Description of Changes
B	July-2019	N/A
3	December-2023	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised

## Related Links

- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)



## Notes & Disclaimer

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### **RoHS Compliance**

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of [www.wolfspeed.com](http://www.wolfspeed.com).

### **REACH Compliance**



REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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[www.wolfspeed.com/power](http://www.wolfspeed.com/power)

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