



**THE DATASHEET OF
NTMTSC002N10MCTXG**



MOSFET - Power, Single N-Channel

100 V, 2.0 mΩ, 236 A

NTMTSC002N10MC

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- New Power 88 Dual Cool Package
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	100	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 236	A
		$T_C = 100^\circ\text{C}$	167	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D 255	W
		$T_C = 100^\circ\text{C}$	128	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D 29	A
		$T_A = 100^\circ\text{C}$	20	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D 3.9	W
		$T_A = 100^\circ\text{C}$	1.9	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM} 900	A	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	213	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 18.2 \text{ A}$)	E_{AS}	2223	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

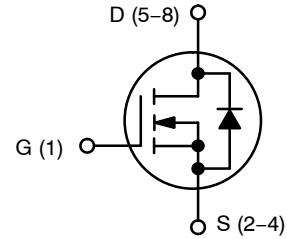
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

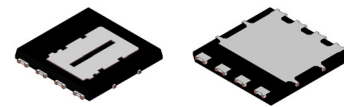
Parameter	Symbol	Value	Unit
Junction-to-Case, Bottom - Steady State	$R_{\theta JCB}$	0.6	$^\circ\text{C}/\text{W}$
Junction-to-Case, Top - Steady State	$R_{\theta JCT}$	0.9	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	2.0 mΩ @ 10 V	236 A

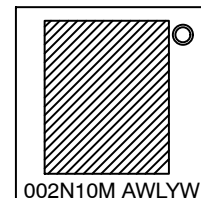


N-CHANNEL MOSFET



TDFNW8
CASE 507AN

MARKING DIAGRAM



002N10M = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTSC002N10MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			68.7		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25 °C		5	μA
			T _J = 125°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 520 μA	2.0		4.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-9.86		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 6 V	I _D = 46 A		5.3	mΩ
		V _{GS} = 10 V	I _D = 90 A		1.7	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 93 A		180		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V		6305		pF
Output Capacitance	C _{OSS}			3405		
Reverse Transfer Capacitance	C _{RSS}			37		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 93 A		89		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 50 V; I _D = 93 A		17		
Gate-to-Source Charge	Q _{GS}			28		
Gate-to-Drain Charge	Q _{GD}			21		
Plateau Voltage	V _{GP}			4.8		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 50 V, I _D = 93 A, R _G = 6 Ω		29		ns
Rise Time	t _r			19		
Turn-Off Delay Time	t _{d(OFF)}			59		
Fall Time	t _f			26		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 90 A	T _J = 25°C	0.84	1.2	V
			T _J = 125°C	0.72		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 46 A		49		ns
Charge Time	t _a			24		
Discharge Time	t _b			26		
Reverse Recovery Charge	Q _{RR}			44		nC
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 1000 A/μs, I _S = 46 A		38		ns
Charge Time	t _a			21		
Discharge Time	t _b			18		
Reverse Recovery Charge	Q _{RR}			310		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

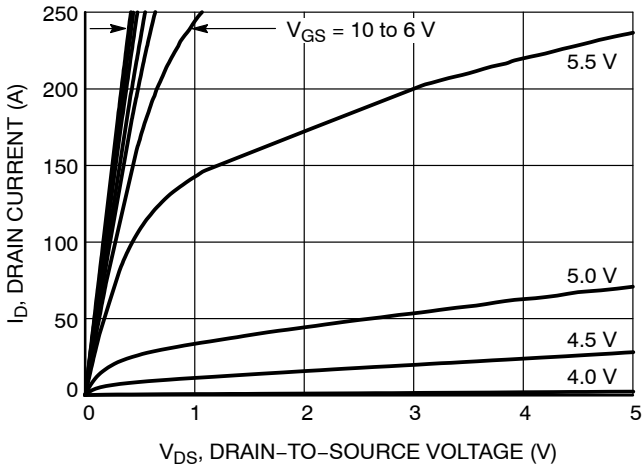


Figure 1. On-Region Characteristics

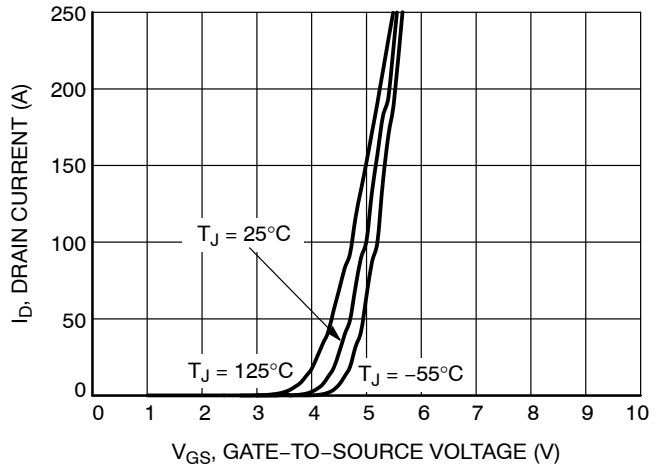


Figure 2. Transfer Characteristics

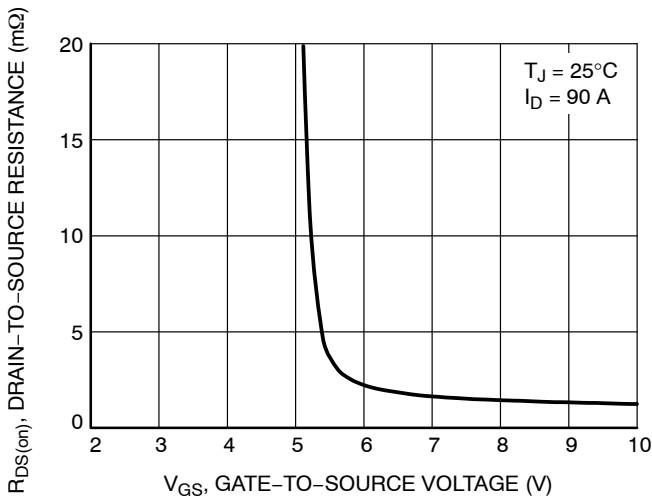


Figure 3. On-Resistance vs. Gate-to-Source Voltage

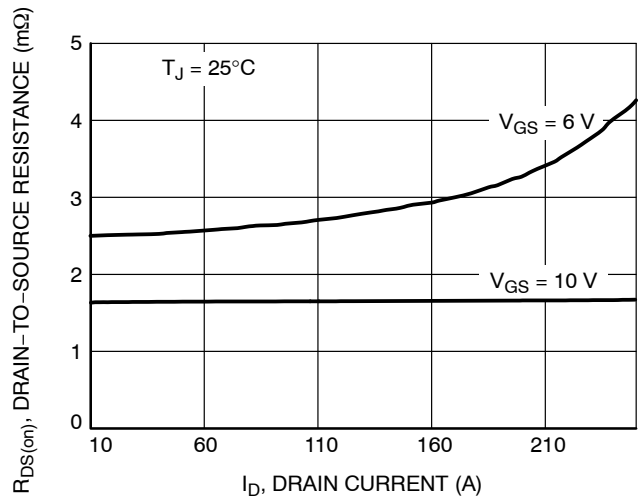


Figure 4. On-Resistance vs. Drain Current

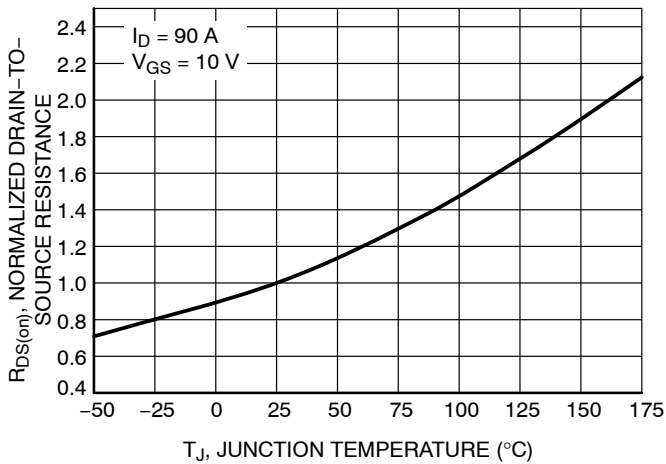


Figure 5. On-Resistance Variation with Temperature

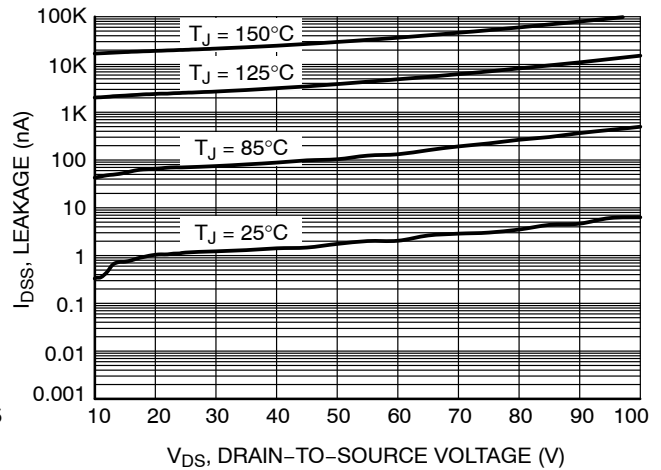


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

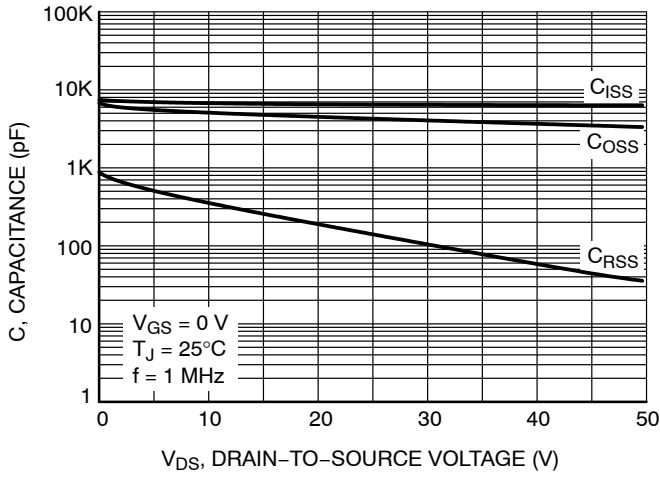


Figure 7. Capacitance Variation

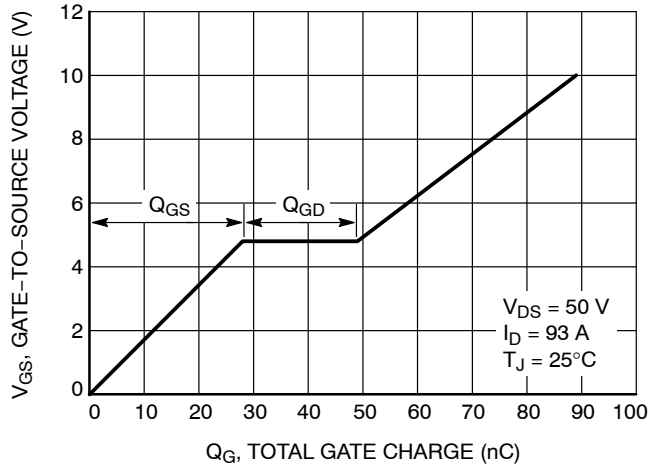


Figure 8. Gate-to-Source Voltage vs. Total Charge

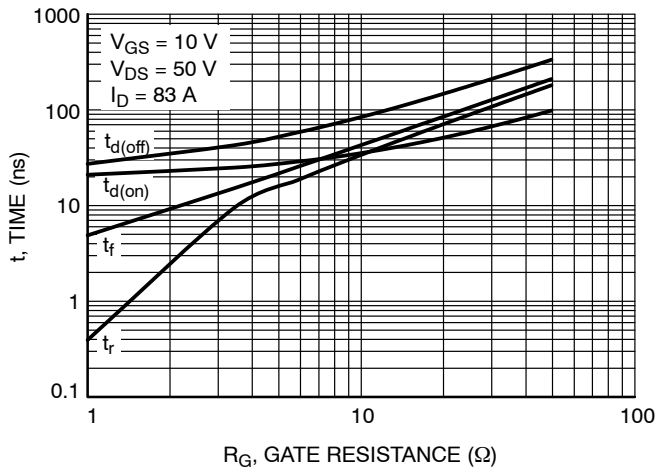


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

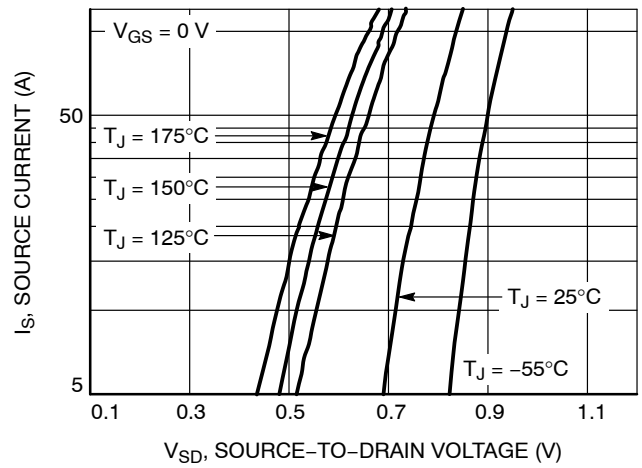


Figure 10. Diode Forward Voltage vs. Current

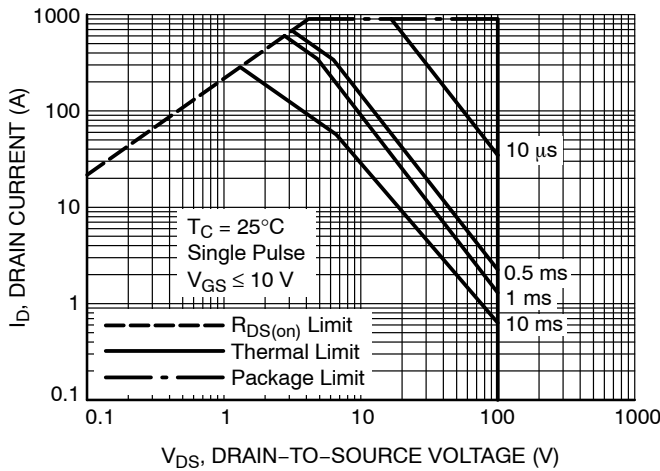


Figure 11. Maximum Rated Forward Biased Safe Operating Area

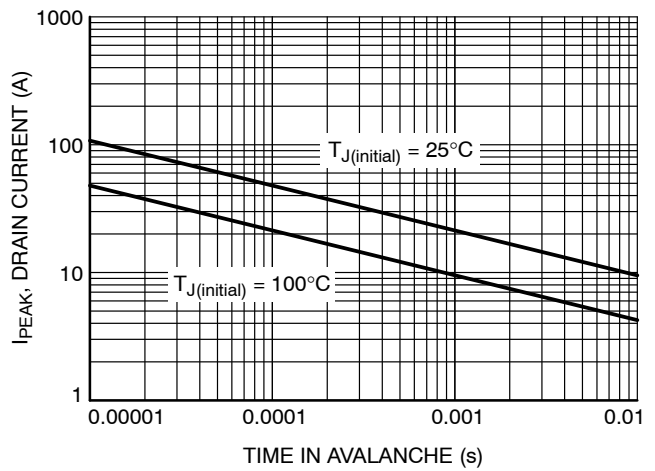


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

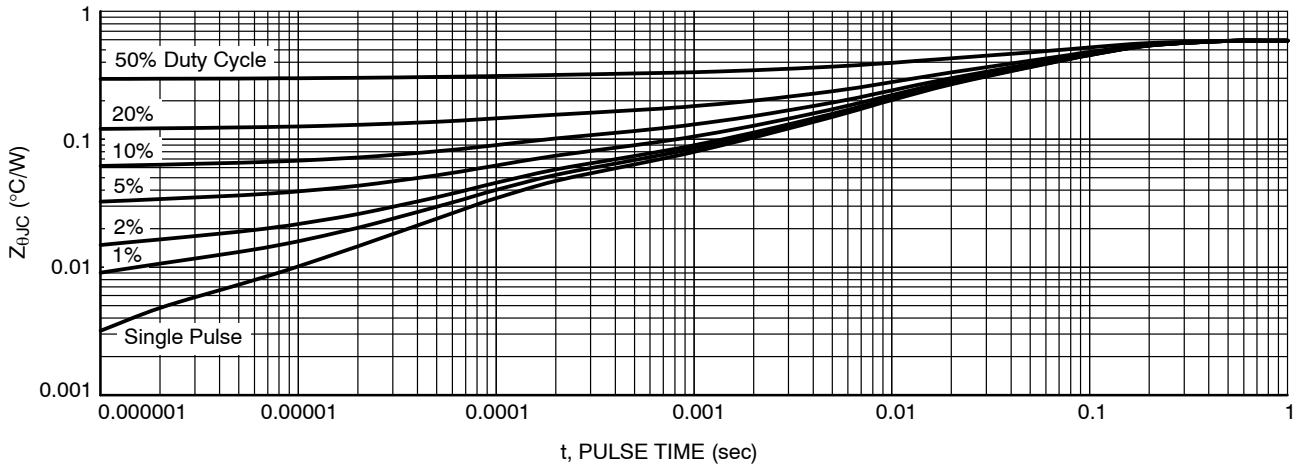


Figure 13. Junction-to-Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

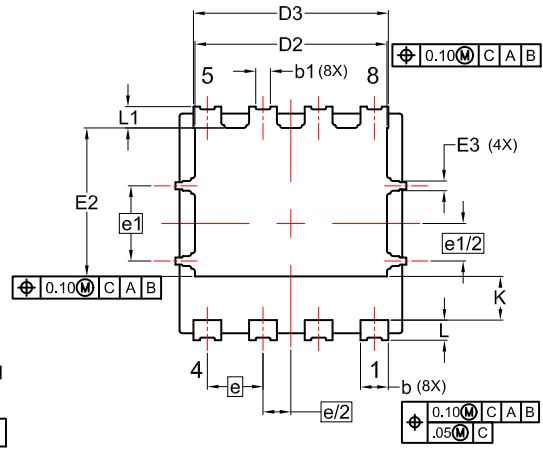
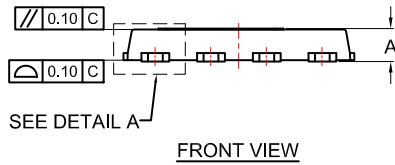
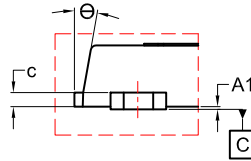
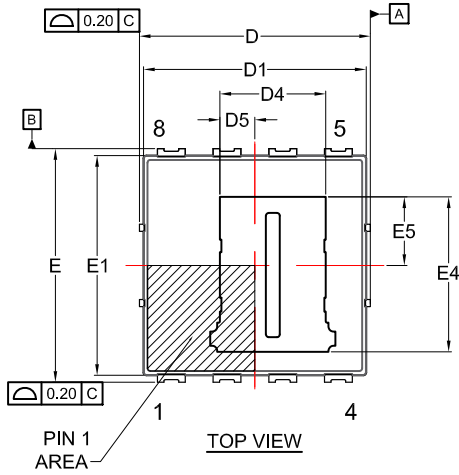
Device	Marking	Package	Shipping [†]
NTMTSC002N10MCTXG	002N10M	POWER 88 Dual Cool (Pb-Free)	3,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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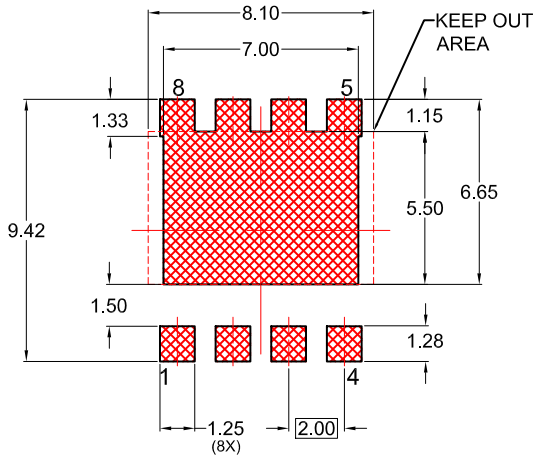
PACKAGE DIMENSIONS

TDFNW8 8.3x8.4, 2P
CASE 507AN
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED LAND PATTERN
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.43	0.53	0.63
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	3.60	3.80	4.00
D5	1.00	1.25	1.50
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	5.47	5.57	5.67
E5	2.25	2.50	2.75
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
θ	0°	—	12°

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Europe, Middle East and Africa Technical Support:

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- ✓ Obsolete Management
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- ✓ Shortage Management
- ✓ Alternative Solution
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