THE DATASHEET OF

DCR011203U

TEXAS INSTRUMENTS

DCR010503, DCR012405, DCR010505
DCR011203, DCR011205, DCR012403

SBVS013D – OCTOBER 2001 – REVISED JUNE 2016

DCR01 Series, 1-W, 1000-Vrms Isolated, Regulated DC–DC Converter Modules

1 Features

- 1000-Vrms Isolation (Operational)
- UL1950 Recognized Component
- 53 W/in^3 (3.3W/cm^3) Power Density
- 10-Pin PDIP and 12-Pin SOP Packages
- Device-to-Device Synchronization
- Thermal Protection
- 400-kHz Switching
- 125 FITs at 55ºC
- ±10% Input Range
- Short-Circuit Protected
- 5-V, 12-V, and 24-V Inputs
- 3.3-V and 5-V Outputs
- High Efficiency

2 Applications

- Point-of-Use Power Conversion
- Digital Interface Power
- Ground Loop Elimination
- Power-Supply Noise Reduction

3 Description

The DCR01 family is a series of high-efficiency, input-isolated, output-regulated DC–DC converters. In addition to 1 W nominal, galvanically-isolated output power capability, this range of DC–DCs offer very low output noise, thermal protection, and high accuracy.

This combination of features and small size makes the DCR01 series of devices suitable for a wide range of applications, and is an easy-to-use solution in applications requiring signal path isolation.

CAUTION

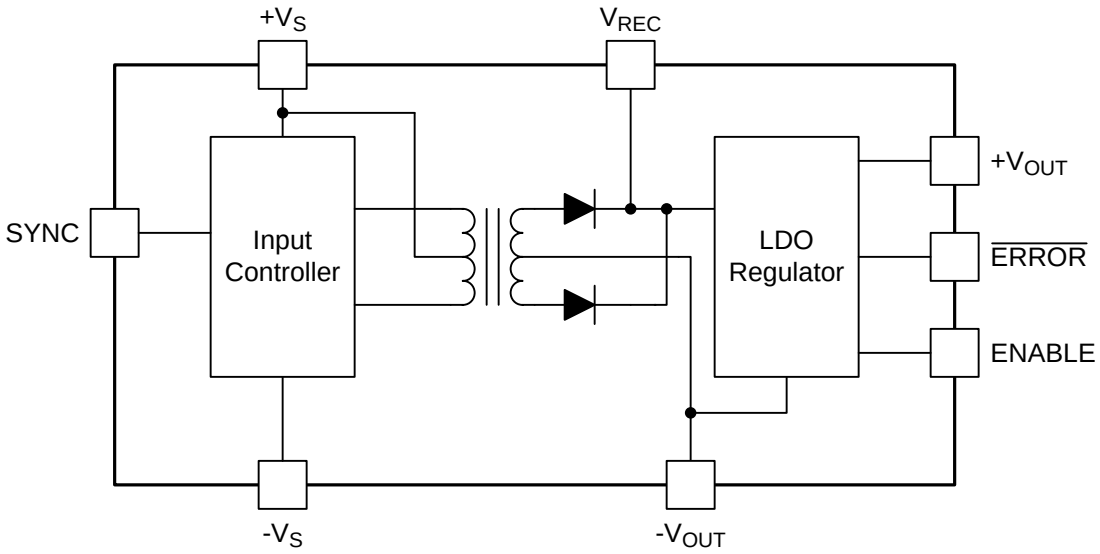
This product has operational isolation and is intended for signal isolation only. It must not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in *Feature Description*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DCR01	PDIP (10)	22.86 mm × 6.61 mm
	SOP (12)	17.90 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DCR01 Block Diagram



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4 Revision History

Changes from Revision C (May 2003) to Revision D **Page**

- Added *Device Information* table, *Device Comparison* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Package/Ordering Information* table, see POA at the end of the data sheet ... 1
- Added additional graphs to the *Typical Characteristics* section ... 7
- Added *Isolation* section to the *Feature Description* section ... 11
- Added a typical application design to the *Application Information* section ... 15

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5 Device Comparison Table

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2-µF ceramic, C_{FILTER} = 1-µF ceramic, C_{OUT} = 0.1-µF ceramic (unless otherwise noted)

DEVICE NUMBER (1)	INPUT VOLTAGE V_S (V)	OUTPUT VOLTAGE V_O (V)	OUTPUT CURRENT (mA)	RIPPLE (2) (mVp-p)	NOISE (3) (mVp-p)	SUPPLY CURRENT (mA)		
						I_O = 0 mA	I_O = 10 mA	I_O = 100% LOAD
	TYP	TYP	MAX	TYP	TYP	TYP	TYP	TYP
DCR010503P	5	3.3	300	5	35	18	28	335
DCR010503U				8	23	24	33	339
DCR010505P		5	200	6	20	25	40	306
DCR010505U				9	20	25	40	306
DCR011203P	12	3.3	390	10	54	13	17	173
DCR011203U			300	8	22	13	17	136
DCR011205P		5	200	6	45	13	18	125
DCR011205U				6	21	14	19	123
DCR012403P	24	3.3	390	10	22	17	18	97
DCR012403U			300	8	22	15	17	75
DCR012405P		5	200	10	22	15	18	69
DCR012405U				13	32	15	18	67

(1) The last character in the part number denotes the package type; P = PDIP, U = SOP
(2) 20-MHz Bandwidth, 50% Load
(3) 100-MHz Bandwidth, 50% Load

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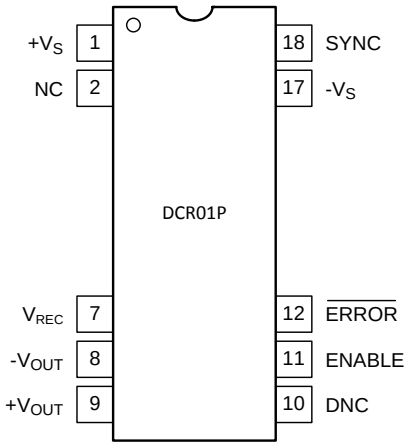
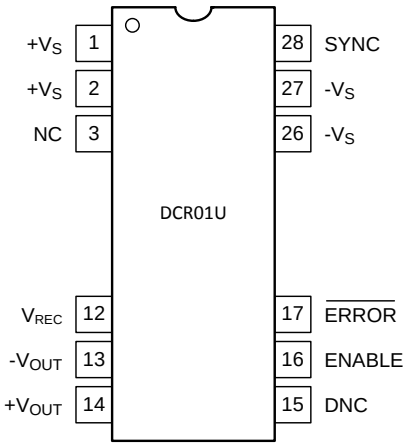
6 Pin Configuration and Functions

NVE Package
10-Pin PDIP
Top View



DVB Package
12-Pin SOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP	SOP		
ENABLE	11	16	I	Output Voltage Enable
$\overline{\text{ERROR}}$	12	17	O	Error Flag Active Low
DNC	10	15	—	Do Not Connect
NC	2	3	—	No Connection
SYNC	18	28	I	Synchronization Input
$-V_{OUT}$	8	13	O	Output Ground
$+V_{OUT}$	9	14	O	Voltage Output
V_{REC}	7	12	O	Rectified Output
$-V_S$	17	26, 27	I	Input Ground
$+V_S$	1	1, 2	I	Voltage Input

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Input voltage	5-V input devices			7	V
	12-V input devices			15	
	24-V input devices			29	
Lead temperature	PDIP package	Surface temperature of device body or pins (maximum 10 s)		270	°C
Reflow solder temperature	SOP package	Surface temperature of device body or pins		260	°C
Storage temperature, T_{stg}			–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the package option addendum at the end of the datasheet for additional package information.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	5-V input devices	4.5	5	5.5	V
	12-V input devices	10.8	12	13.2	
	24-V input devices	21.6	24	26.4	
Operating temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		DCR01		UNIT
		NVE (PDIP)	DVB (SOP)	
		10 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	24	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2-µF ceramic, C_{FILTER} = 1-µF ceramic, C_{OUT} = 0.1-µF ceramic (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Nominal output voltage ($+V_{OUT}$)	DCR01xx03			3.3		V
	DCR01xx05			5		
Setpoint accuracy				0.5%	2%	
Output short-circuit protected	Duration			Infinite		
Line regulation				1		mV/V
Over line and load	I_O = 10 mA to Full Load, Over $+V_S$ range			1%	2.5%	
Temperature variation	–40°C ≤ T_A ≤ +85°C			1%		
INPUT						
Nominal input voltage ($+V_S$)	DCR0105xx			5		V
	DCR0112xx			12		
	DCR0124xx			24		
Voltage range			–10%		10%	
Reflected ripple current	20-MHz Bandwidth, I_O = 100% Load			8		mAp-p
ISOLATION						
Isolation	1-s Flash Test	Voltage	1			kVrms
		dV/dt			500	V/s
		Leakage Current			30	nA
	Continuous working voltage across isolation barrier	DC			60	VDC
		AC			42.5	VAC
Barrier capacitance				25		pF
OUTPUT ENABLE CONTROL						
Logic high input voltage			2		V_{REC}	V
Logic high input current	2 < V_{ENABLE} < V_{REC}			100		nA
Logic low input voltage			–0.2		0.5	V
Logic low input current	0 < V_{ENABLE} < 0.5			100		nA
Rectified output, V_{REC}	All 3.3-V Outputs			3.3		V
	All 5-V Outputs			5		
ERROR FLAG						
Logic high open-collector leakage	V_{ERROR} = 5 V				10	µA
Logic low output voltage	Sinking 2 mA				0.4	V
THERMAL SHUTDOWN						
Junction temperature	Temperature Activated			150		°C
	Temperature Deactivated			130		
SYNCHRONIZATION PIN						
Max external capacitance on SYNC pin					3	pF
Internal oscillator frequency			720	800	880	kHz
External synchronization frequency			720		880	kHz
External synchronization signal high			2.5		3	V
External synchronization signal low			0		0.4	V
TEMPERATURE RANGE						
Operating			–40		85	°C

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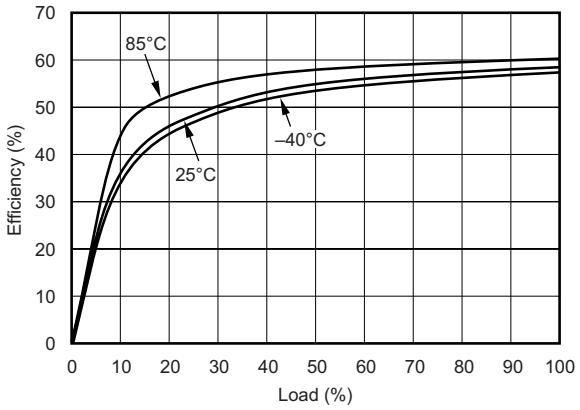
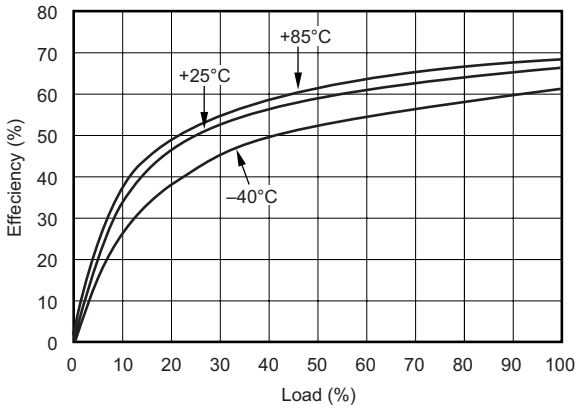
7.6 Typical Characteristics

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2 µF, C_{FILTER} = 1 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)



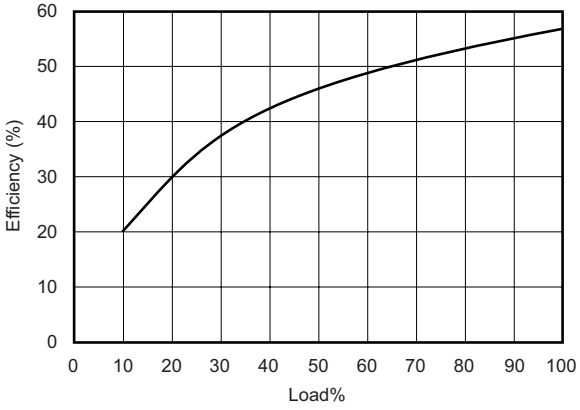
DCR010503P, DCR010503U
DCR011205P, DCR011205U

Figure 1. Efficiency vs Load



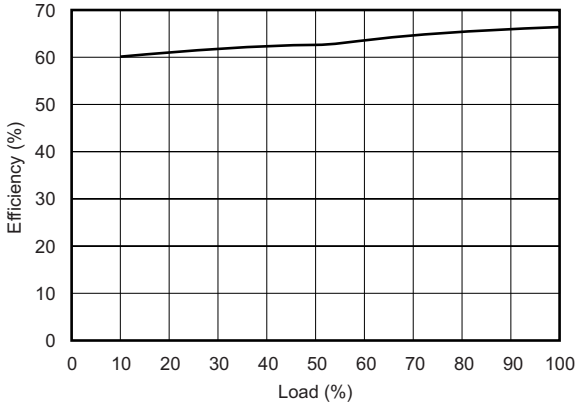
DCR010505P, DCR010505U
DCR011205P, DCR011205U

Figure 2. Efficiency vs Load



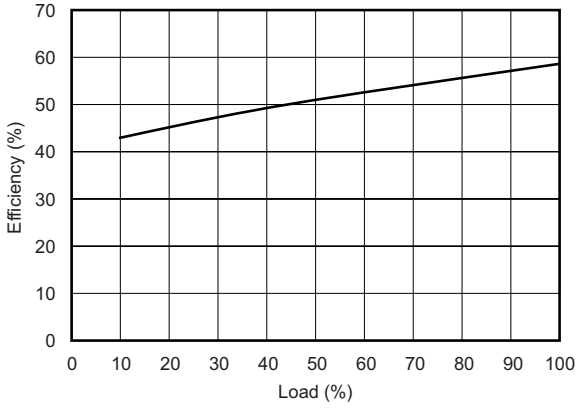
DCR012403P DCR012403U

Figure 3. Efficiency vs Load



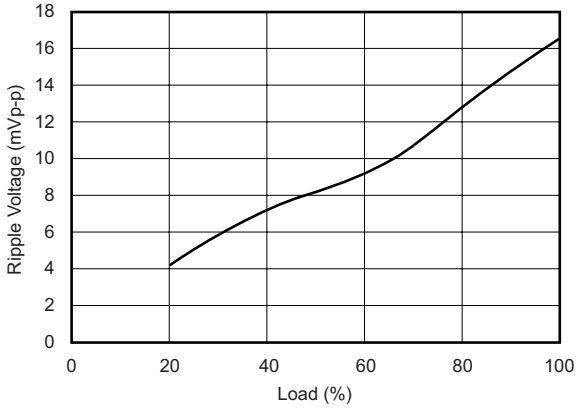
DCR010505U DCR011205U

Figure 4. Efficiency vs Load



DCR012405P DCR012405U

Figure 5. Efficiency vs Load



All devices except for DCR011203P & DCR012403P
20-MHz Bandwidth

Figure 6. Output Voltage Ripple

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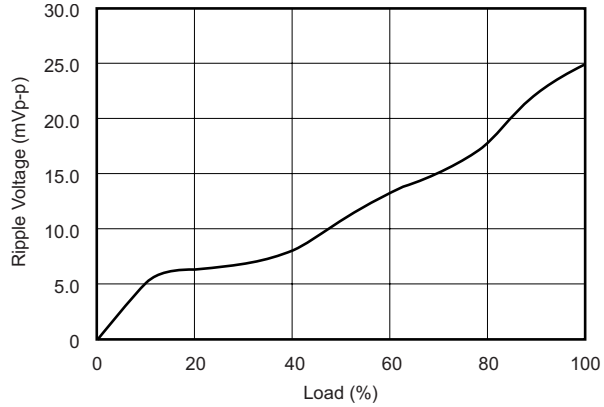
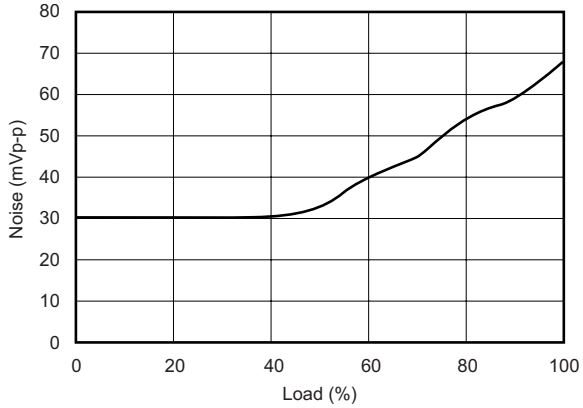
Typical Characteristics (continued)

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2 µF, C_{FILTER} = 1 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)



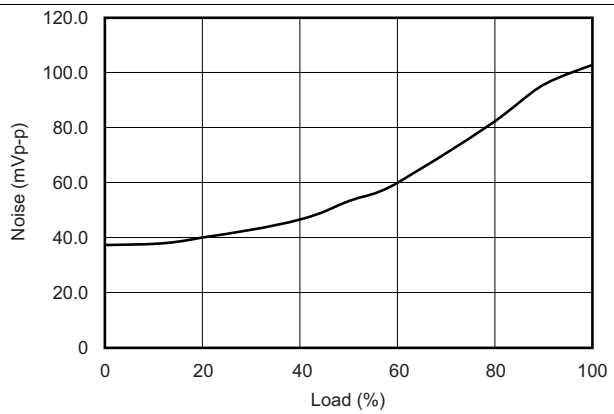
DCR011203P 20-MHz Bandwidth
DCR012403P

Figure 7. Output Voltage Ripple



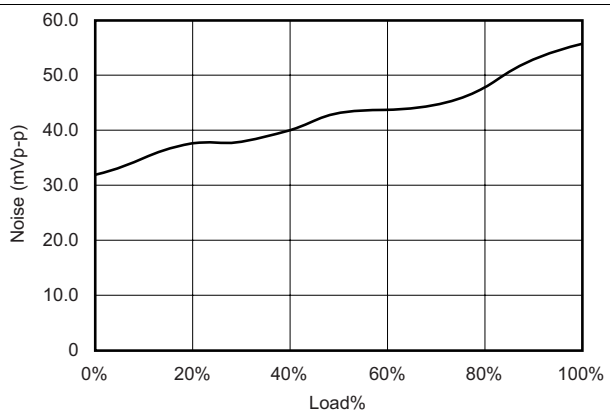
All 5-V Input Devices 100-MHz Bandwidth

Figure 8. Output Voltage Noise



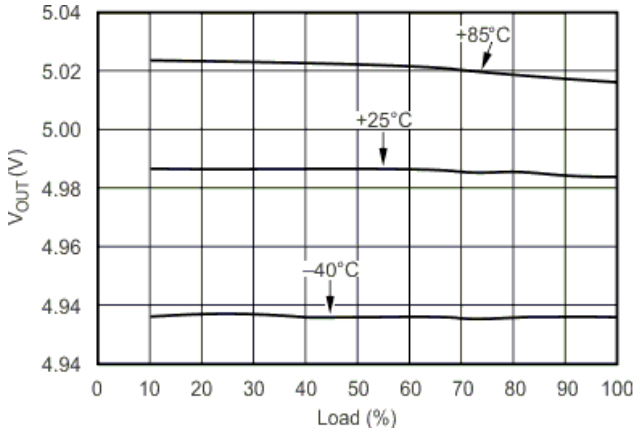
DCR011203P 100-MHz Bandwidth

Figure 9. Output Voltage Noise



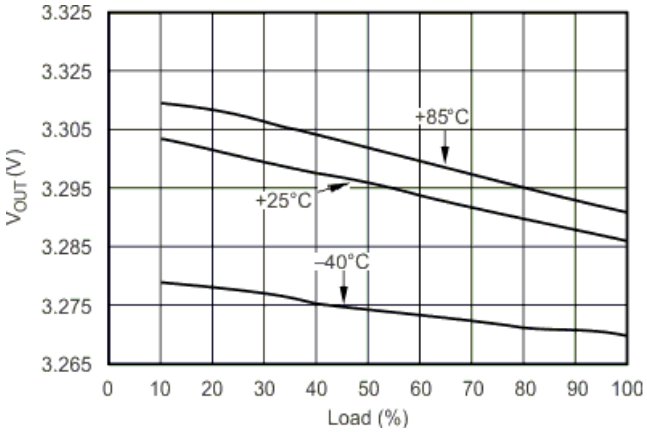
DCR011205P 100-MHz Bandwidth

Figure 10. Output Voltage Noise



All 5-V Output Devices

Figure 11. 5-V Output Load Regulation



All 3.3-V output devices except DCR010503P

Figure 12. 3.3-V Output Load Regulation

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Typical Characteristics (continued)

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2 µF, C_{FILTER} = 1 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)

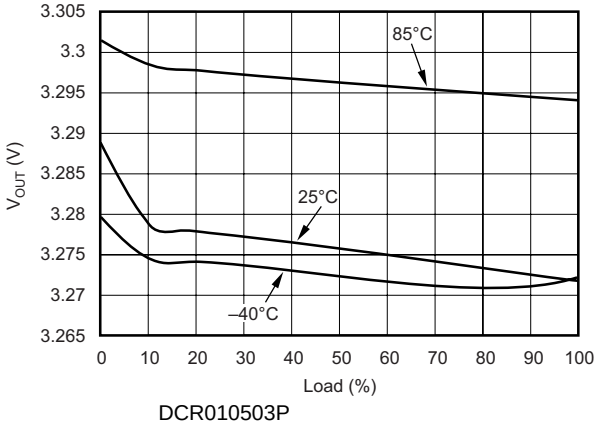

Figure 13. 3.3-V Output Load Regulation

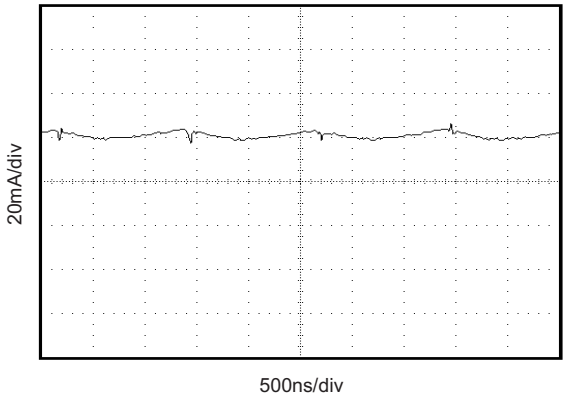

Figure 14. Input Current Reflected Ripple

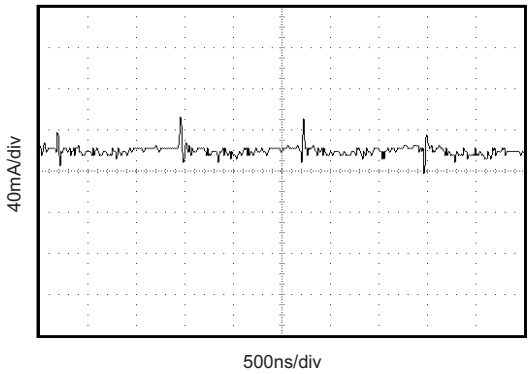

Figure 15. Input Current Reflected Ripple

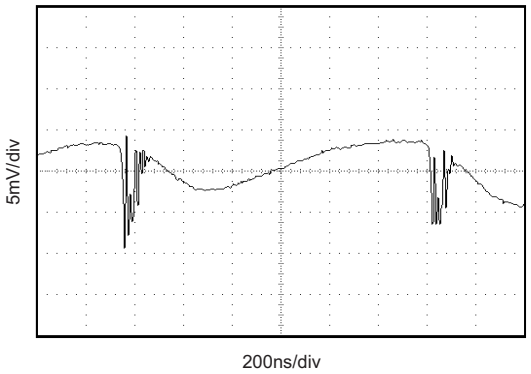

Figure 16. DCR010505P Output Voltage Ripple at 100% Load

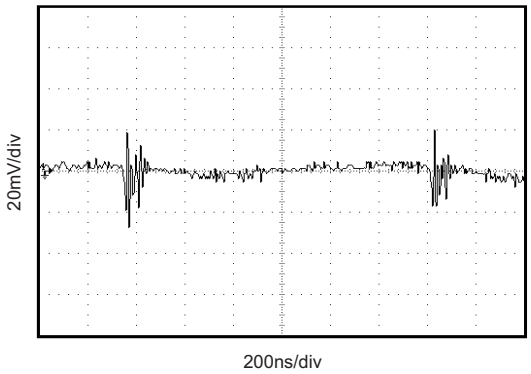

Figure 17. DCR010505P Output Voltage Noise at 100% Load

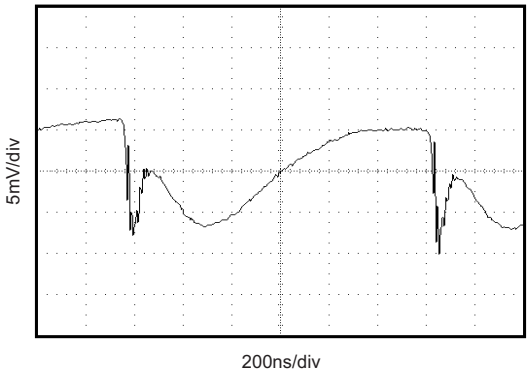

Figure 18. DCR010503P Output Voltage Ripple at 100% Load

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Typical Characteristics (continued)

at T_A = 25°C, $+V_S$ = nominal, I_O = 10 mA, C_{IN} = 2.2 µF, C_{FILTER} = 1 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)

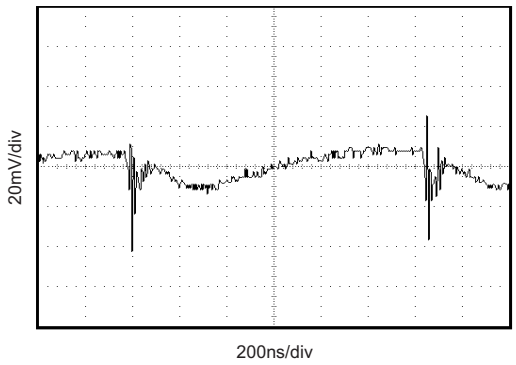

Figure 19. DCR010503P Output Voltage Noise at 100% Load

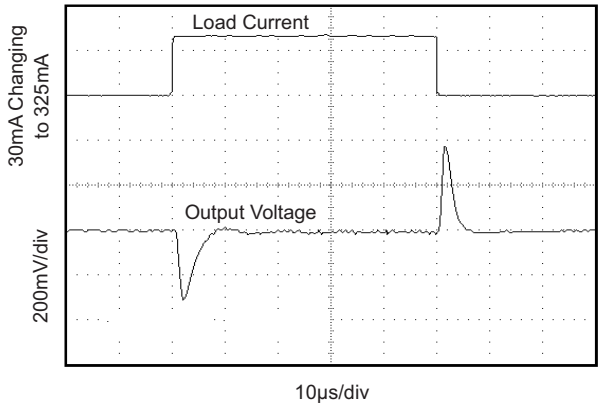

Figure 20. DCR010503P Load Transient Response

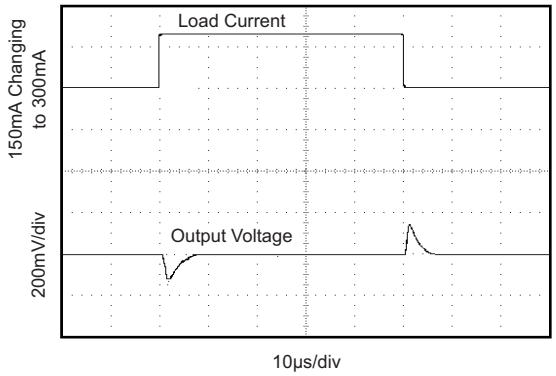

Figure 21. DCR010503P Load Transient Response

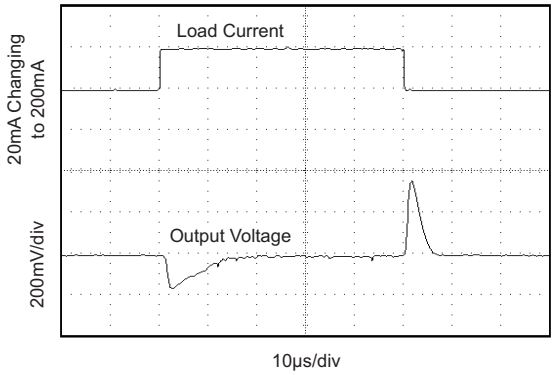

Figure 22. DCR010505P Load Transient Response

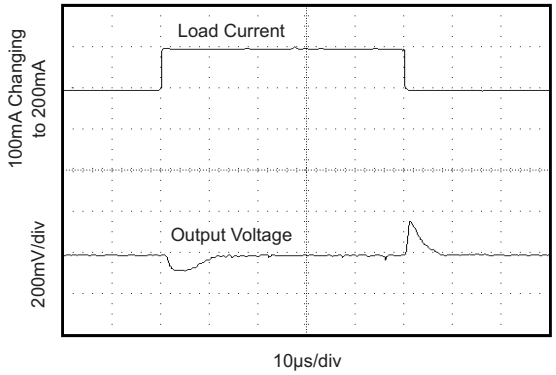

Figure 23. DCR010505P Load Transient Response

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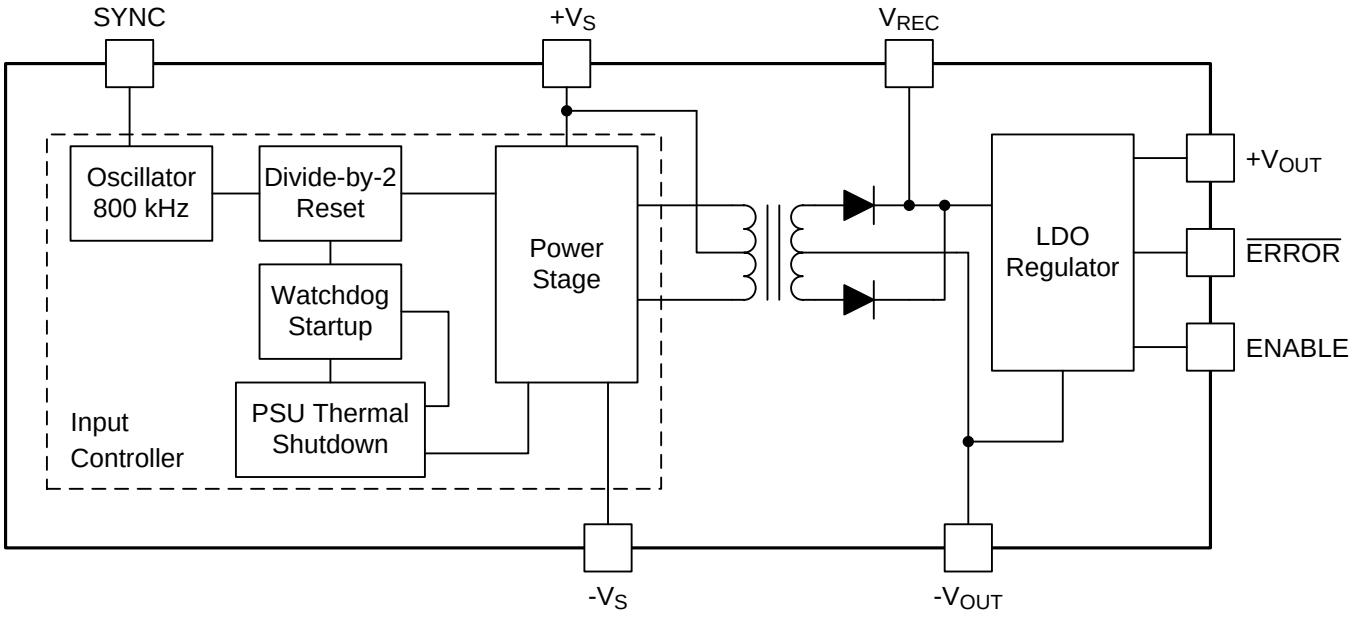
8 Detailed Description

8.1 Overview

The DCR01 series of power modules offer isolation from a regulated power supply operating from a choice of input voltages. The DCR01s provide a regulated 3.3-V or 5-V output voltage at a nominal output power of 1 W or above. The DCR01 devices include a low dropout linear regulator internal to the device to achieve a well-regulated output voltage. The DCR01 devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS/DMOS process.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Isolation

Underwriters Laboratories, UL™, defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.4 V_{RMS} or 60 V_{DC} peak.

8.3.1.1 Operation or Functional Isolation

The type of isolation used in the DCR01 products is referred to as operational or functional isolation. Insulated wire used in the construction of the transformer acts as the primary isolation barrier. A high-potential (hipot), one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

8.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

Feature Description (continued)

NOTE

The DCR01 products DO NOT provide basic or enhanced isolation.

8.3.1.3 Working Voltage

For a device with operational isolation, the continuous working voltage that can be applied across the device in normal operation must be less than 42.4 V_{RMS} or 60 V_{DC}, (SELV limits).

WARNING

Do not use the device as an element of a safety isolation system if SELV is exceeded.

If the device is expected to function correctly with more than 42.4 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

8.3.1.4 Isolation Voltage Rating

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* are all terms that relate to the same thing; a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCR01 series of DC-DC converters are all 100% production tested at 1 kV_{AC} for one second.

8.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCV01 series of DC–DC converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

8.3.2 Power Stage

The DCR01 series of devices use a push-pull, center-tapped topology. The DCV01 devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator).

8.3.3 Rectification

The transformer's output is full wave rectified and filtered by the external 1-μF ceramic capacitor connected to V_{REC}.

8.3.4 Regulator

The internal low dropout linear regulator provides a well-regulated output voltage throughout the operating range of the device.

8.3.5 Oscillator and Watchdog

The onboard, 800-kHz oscillator generates the switching frequency through a divide-by-2 circuit. The oscillator can be synchronized to other DCR01 device circuits or an external source, and is used to minimize system noise.

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Feature Description (continued)

A watchdog circuit monitors the operation of the oscillator circuit. The oscillator can be disabled by pulling the SYNC pin low. When the SYNC pin goes low, the output pins transition into tri-state mode, which occurs within 2 μs.

8.3.6 $\overline{\text{ERROR}}$ Flag

The DCR01 has an $\overline{\text{ERROR}}$ pin which provides a *power good* flag, as long as the internal regulator is in regulation. If the $\overline{\text{ERROR}}$ output is required, place a 10-kΩ resistor between the $\overline{\text{ERROR}}$ pin and the output voltage.

8.3.7 Synchronization

When more than one DC–DC converter is switching in an application, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC–DC converters.

The DCR01 series of devices overcome this interference by allowing devices to be synchronized to one another. Synchronize up to eight devices by connecting the SYNC pins of each device, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) reduces the switching frequency, or can sometimes stop the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3 V.

For an application that uses more than eight synchronized devices use an external device to drive the SYNC pins. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes this configuration.

NOTE

During the start-up period, all synchronized devices draw maximum current from the input simultaneously. If the input voltage falls below approximately 4 V, the devices may not start up. A ceramic capacitor should be connected close to each device's input pin. Use a 2.2-μF capacitor for 5-V input devices, and a 0.47-μF capacitor for the 12-V and 24-V devices.

8.3.8 Construction

The basic construction of the DCR01 series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCV01 series of devices are constructed using an IC, low dropout linear regulator, rectifier diodes, and a wound magnetic toroid on a leadframe. Because the package contains no solder, the devices do not require any special printed-circuit board (PCB) assembly processing. This architecture results in an isolated DC–DC converter with inherently high reliability.

8.3.9 Thermal Considerations

Due to the high power density of this device, it is advisable to provide ground planes on the input and output rails. The output regulator is mounted on a copper leadframe, and a ground plane serves as an efficient heatsink.

8.3.10 Decoupling – Ripple Reduction

Due to the very low forward resistance of the DMOS switching transistors, high current demands are placed upon the input supply for a short time. By using a good quality low Equivalent Series Resistance (ESR) capacitor of 2.2 μF (minimum) for the 5-V input devices and a 0.47-μF capacitor for the 12-V and 24-V devices, placed close to the IC supply input pins, the effects on the power supply can be minimized.

The high switching frequency of 400 kHz allows relatively small values of capacitors to be used for filtering the rectified output voltage. A good-quality, low-ESR, 1-μF ceramic capacitor placed close to the VREC pin and output ground is required and reduces the ripple. The output at VREC is full wave rectified and produces a ripple of 800 kHz.

TI recommends that a 0.1-μF, low-ESR, ceramic capacitor is connected close to the output pin and ground to reduce noise on the output. The capacitor values listed are minimum values. If lower ripple is required, the filter capacitor should be increased in value to 2.2 μF.

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Feature Description (continued)

As with all switching power supplies, the best performance is obtained with low ESR,ceramic capacitors connected close to the device pins. If low ESR, ceramic capacitors are not used, the ESR generates a voltage drop when the capacitor is supplying the load power. Often a larger capacitor is chosen for this purpose, when a low ESR, smaller capacitor would perform as well.

NOTE

TI does not recommend that the DCR01 be fitted using an IC socket, as this degrades performance.

8.4 Device Functional Modes

8.4.1 Device Disable and Enable

Each of the DCR01 series devices can be disabled or enabled by driving the SYNC pin using an open-drain CMOS gate. If the SYNC pin is pulled low, the DCR01 becomes disabled. The disable time depends upon the external loading. The internal disable function is implemented in 2 μs. Removal of the pulldown causes the DCR01 to be enabled.

Capacitive loading on the SYNC pin must be minimized (≤ 3 pF) to prevent a reduction in the oscillator frequency. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes disable and enable control circuitry. This document contains information on how to null the effects of additional capacitance on the SYNC pin. The oscillator's frequency can be measured at V_{REC}, as this is the fundamental frequency of the ripple component.

8.4.2 Regulated Output Disable and Enable

The regulated output of the DCR01 can be disabled by pulling the ENABLE pin LOW. Disabling the output voltage this way still produces a voltage on the V_{REC} pin. When using the ENABLE control, TI recommends placing a 10-kΩ resistor between the V_{REC} and ENABLE pins. The ENABLE pin only controls the internal linear regulator.

If disabling the regulated output is not required, pull the ENABLE pin HIGH by shorting it directly to the V_{REC} pin. This enables the regulated output voltage, thus allowing the output to be controlled from the isolated side.

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9 Application and Implementation

NOTE

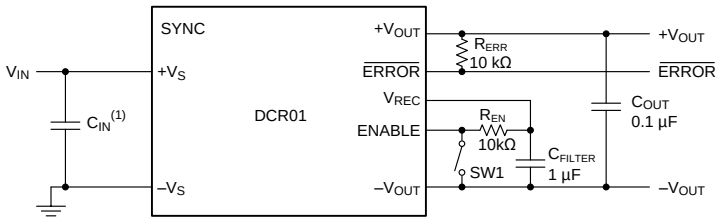
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DCR01 Single Voltage Output

The DCR01 can be used to provide a single voltage output by connecting it as shown in Figure 24. The $\overline{\text{ERROR}}$ output signal will be pulled up to the value of V_{OUT} . The value of R_{ERR} will depend on the loading on the $\overline{\text{ERROR}}$ line; however, the total load on the $\overline{\text{ERROR}}$ line must not exceed the value given in *Electrical Characteristics*.

The output may be permanently enabled by connecting the ENABLE pin to the V_{REC} pin. The DCR01 may be enabled remotely by connecting the ENABLE pin to V_{REC} through a pullup resistor (R_{EN}); the value of this resistor is not critical for the DCR01 as only a small current flows. The switch SW1 can be used to pull the ENABLE pin LOW, thus disabling the output. The switching devices can be a bipolar transistor, FET, or a mechanical device; the main load that it sees is R_{EN}.



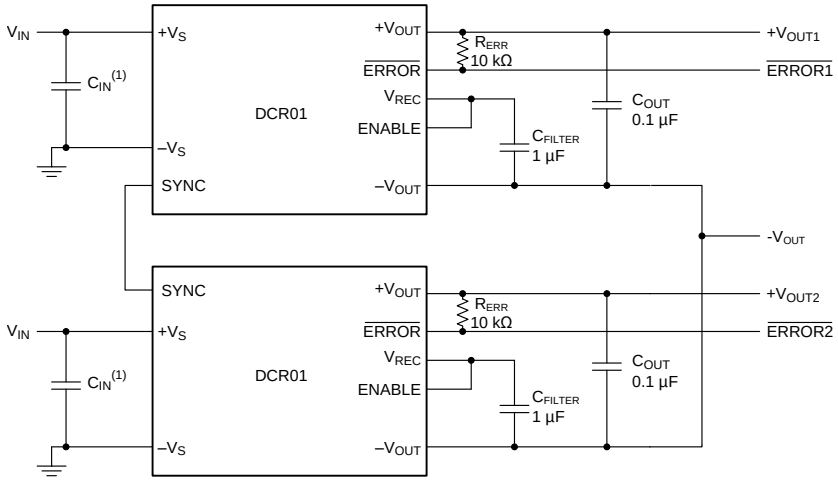
(1) C_{IN} = 2.2 µF for 5-V input devices and 0.47 µF for 12-V and 24-V input devices. Low ESR, ceramic capacitors are required.

Figure 24. DCR01 Single Output Voltage

Application Information (continued)

9.1.2 Generating Two Positive Output Voltages

Two DCR01s can be used to create output voltages of +3.3 V and +5 V, as shown in Figure 25. The two DCR01s are connected in self-synchronization, thus locking the oscillators of both devices to a single frequency. The $\overline{\text{ERROR}}$ and ENABLE facilities may be used in a similar configuration for a single DCR01. The filter capacitors connected to the V_{REC} pins (C_{FILTER}) must be kept separate from each other and connected in close proximity to their respective DCR01.



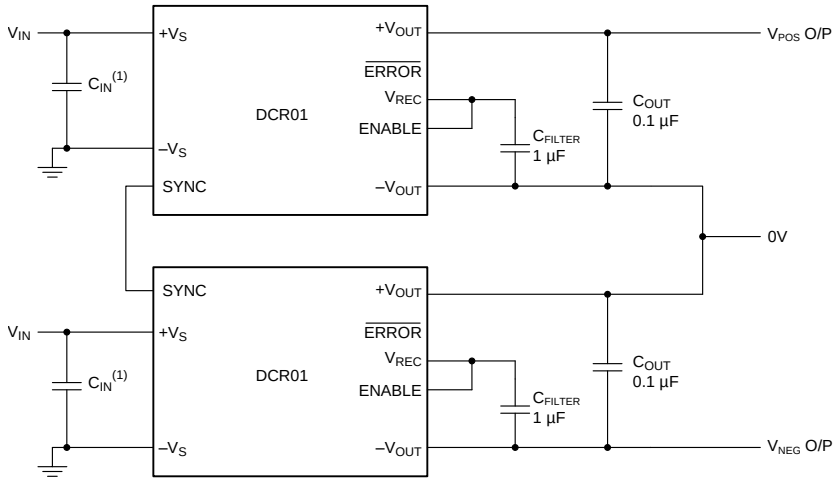
(1) C_{IN} = 2.2 µF for 5-V input devices and 0.47 µF for 12-V and 24-V input devices. Low ESR, ceramic capacitors are required.

Figure 25. Two Positive Voltages from Self-Synchronized DCR01s

9.1.3 Generation of Dual Polarity Voltages from Two Self-Synchronized DCR01s

Two DCR01s can be configured to produce a dual polarity supply (that is, ±5 V); the circuit must be connected as shown in Figure 26.

It must be observed that both devices are producing a positive regulated output; therefore the ERROR, ENABLE, and VREC are all relative to that particular device's $–V_{OUT}$ pin and must not be directly connected together, or in the case of the negative output device, connected to the common 0-V output.



(1) C_{IN} = 2.2 µF for 5-V input devices and 0.47 µF for 12-V and 24-V input devices. Low ESR, ceramic capacitors are required.

Figure 26. Dual Polarity Voltage Generation

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9.2 Typical Application

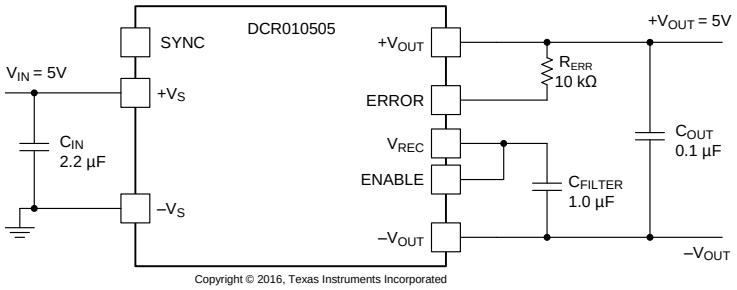

Figure 27. DCR01 Typical Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 and follow the design procedure.

Table 1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input Voltage V_{IN}	5 V typical
Output Voltage V_{OUT}	5 V regulated
Output Current Rating	200 mA
Isolation	1000-V operational

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor

For this design, a 2.2-µF, ceramic capacitor is required for the input decoupling capacitor.

9.2.2.2 Output Capacitor

For this design, a 0.1-µF, ceramic capacitor is required for between $+V_{OUT}$ and $–V_{OUT}$.

9.2.2.3 Filter Capacitor

A high-quality, low-ESR, 1-µF, ceramic capacitor placed close to the VREC pin and output ground is required to reduce output voltage ripple.

9.2.2.4 $\overline{\text{ERROR}}$ Flag

Place a 10-kΩ resistor between the $\overline{\text{ERROR}}$ pin and the output voltage to provide a *power good* signal when the internal regulator is in regulation.

9.2.3 Application Curves

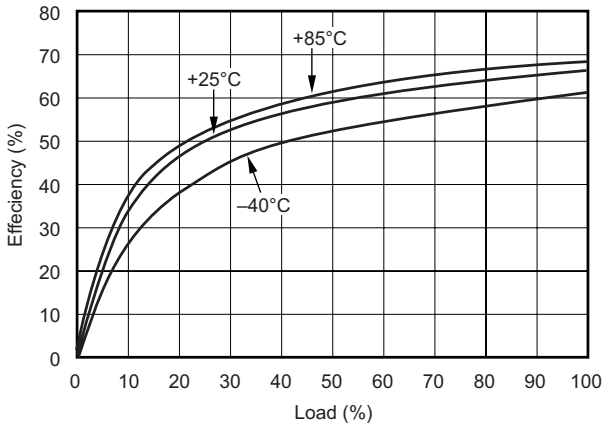

Figure 28. DCR010505 Efficiency

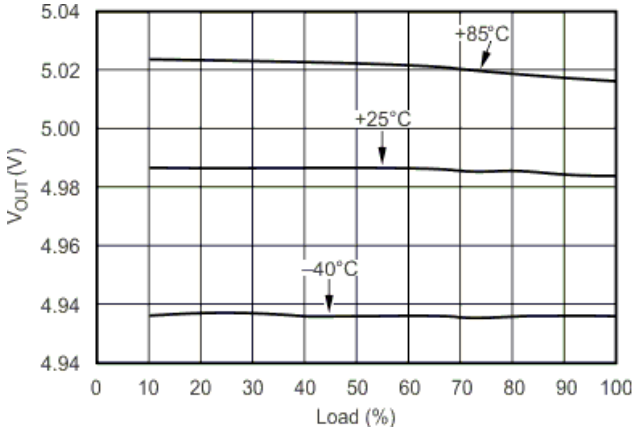

Figure 29. DCR010505 Load Regulation

10 Power Supply Recommendations

The DCR01 is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCR01. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

11 Layout

11.1 Layout Guidelines

Carefully consider the layout of the PCB in order for the best results to be obtained.

Input and output power and ground planes provide a low-impedance path for the input and output power. For the output, the positive and negative voltage outputs conduct through wide traces to minimize losses.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensure a smooth start-up.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

If the SYNC pin is being used, the tracking between device SYNC pins must be short to avoid stray capacitance. Never connect a capacitor to the SYNC pin. If the SYNC pin is not being used it is advisable to place a guard ring (connected to input ground) around this pin to avoid any noise pick-up. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

Figure 30 shows a schematic for a single DCR01, SOP package device. Figure 31 and Figure 32 show a typical layout for the SOP package DCR01 device. The layout shows proper placement of capacitors and power planes.

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11.2 Layout Examples

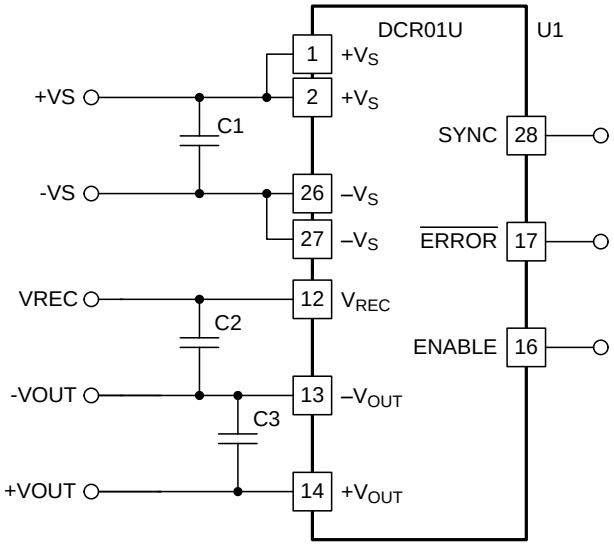

Figure 30. DCR01 PCB Schematic, U Package

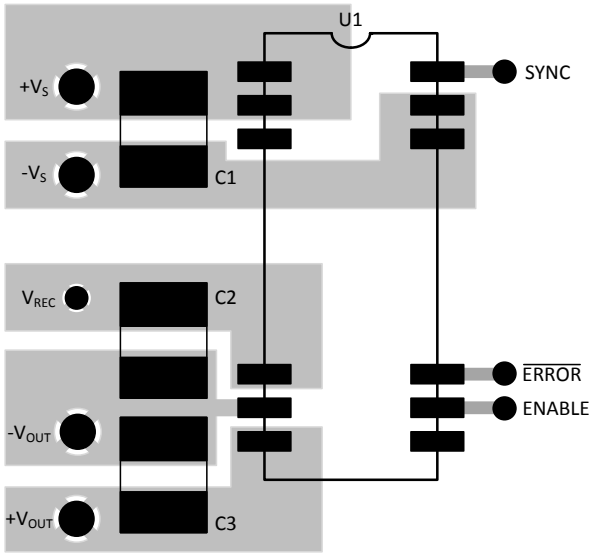

Figure 31. PCB Layout Example, Component-Side View

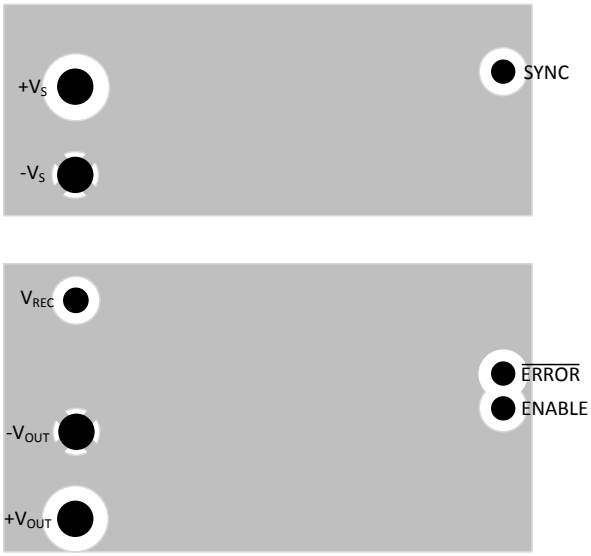

Figure 32. PCB Layout Example, Non-Component-Side View

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DCR010503	Click here	Click here	Click here	Click here	Click here
DCR012405	Click here	Click here	Click here	Click here	Click here
DCR010505	Click here	Click here	Click here	Click here	Click here
DCR011203	Click here	Click here	Click here	Click here	Click here
DCR011205	Click here	Click here	Click here	Click here	Click here
DCR012403	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCR010503P	ACTIVE	PDIP	NVE	10	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR010503P	Samples
DCR010503U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010503U	Samples
DCR010503U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010503U	Samples
DCR010503UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010503U	Samples
DCR010505P	ACTIVE	PDIP	NVE	10	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR010505P	Samples
DCR010505U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010505U	Samples
DCR010505U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010505U	Samples
DCR010505U/1KE4	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010505U	Samples
DCR010505UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR010505U	Samples
DCR011203P	ACTIVE	PDIP	NVE	10	20	TBD	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR011203P	Samples
DCR011203U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011203U	Samples
DCR011203U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011203U	Samples
DCR011203UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011203U	Samples
DCR011205P	ACTIVE	PDIP	NVE	10	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR011205P	Samples
DCR011205U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011205U	Samples
DCR011205U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011205U	Samples
DCR011205UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR011205U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCR012403P	ACTIVE	PDIP	NVE	10	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR012403P	Samples
DCR012403U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR012403U	Samples
DCR012405P	ACTIVE	PDIP	NVE	10	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	DCR012405P	Samples
DCR012405U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR012405U	Samples
DCR012405U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR012405U	Samples
DCR012405UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DCR012405U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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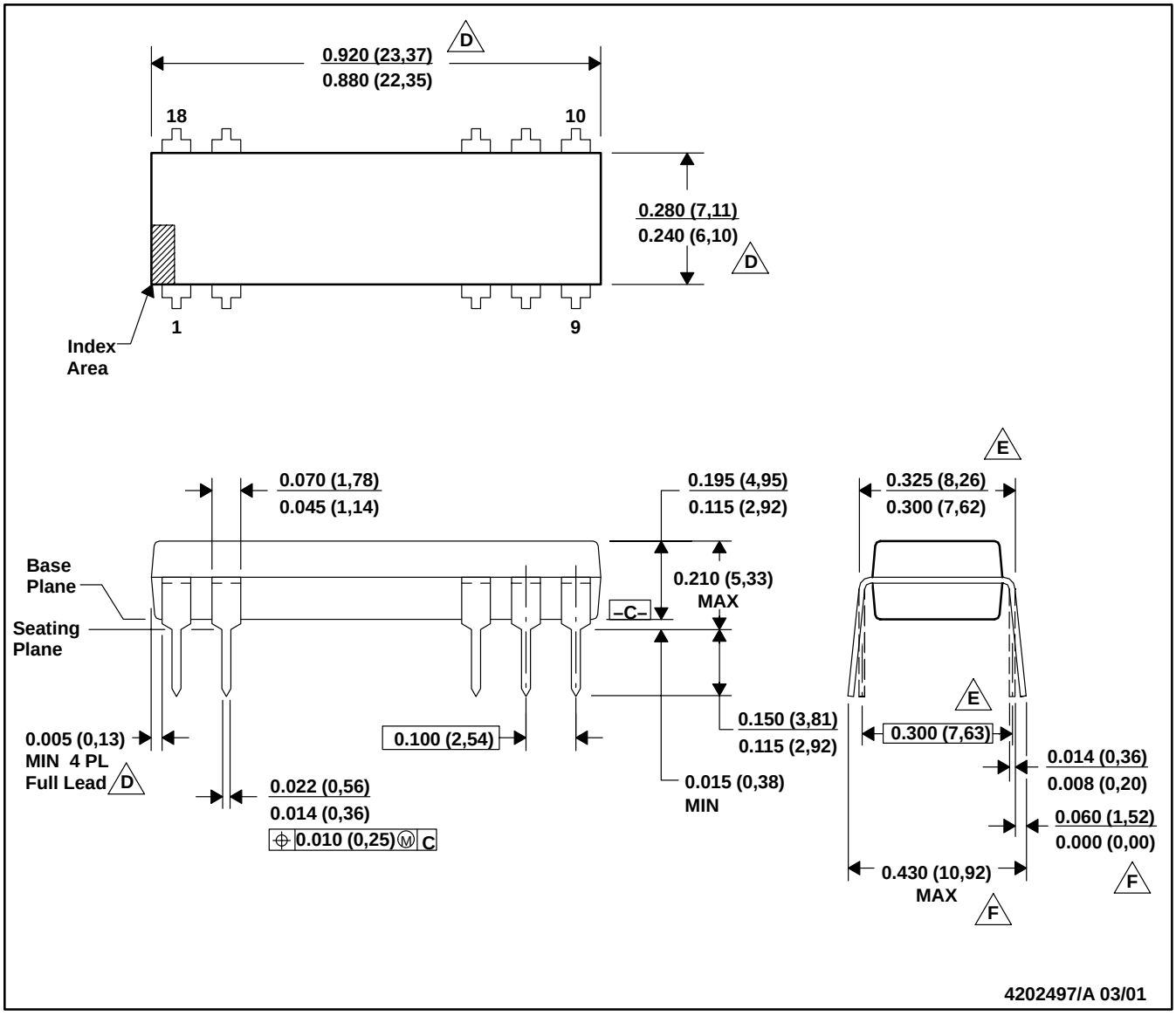
MPDI055 – APRIL 2001

NVE (R-PDIP-T10/18) **PLASTIC DUAL-IN-LINE**



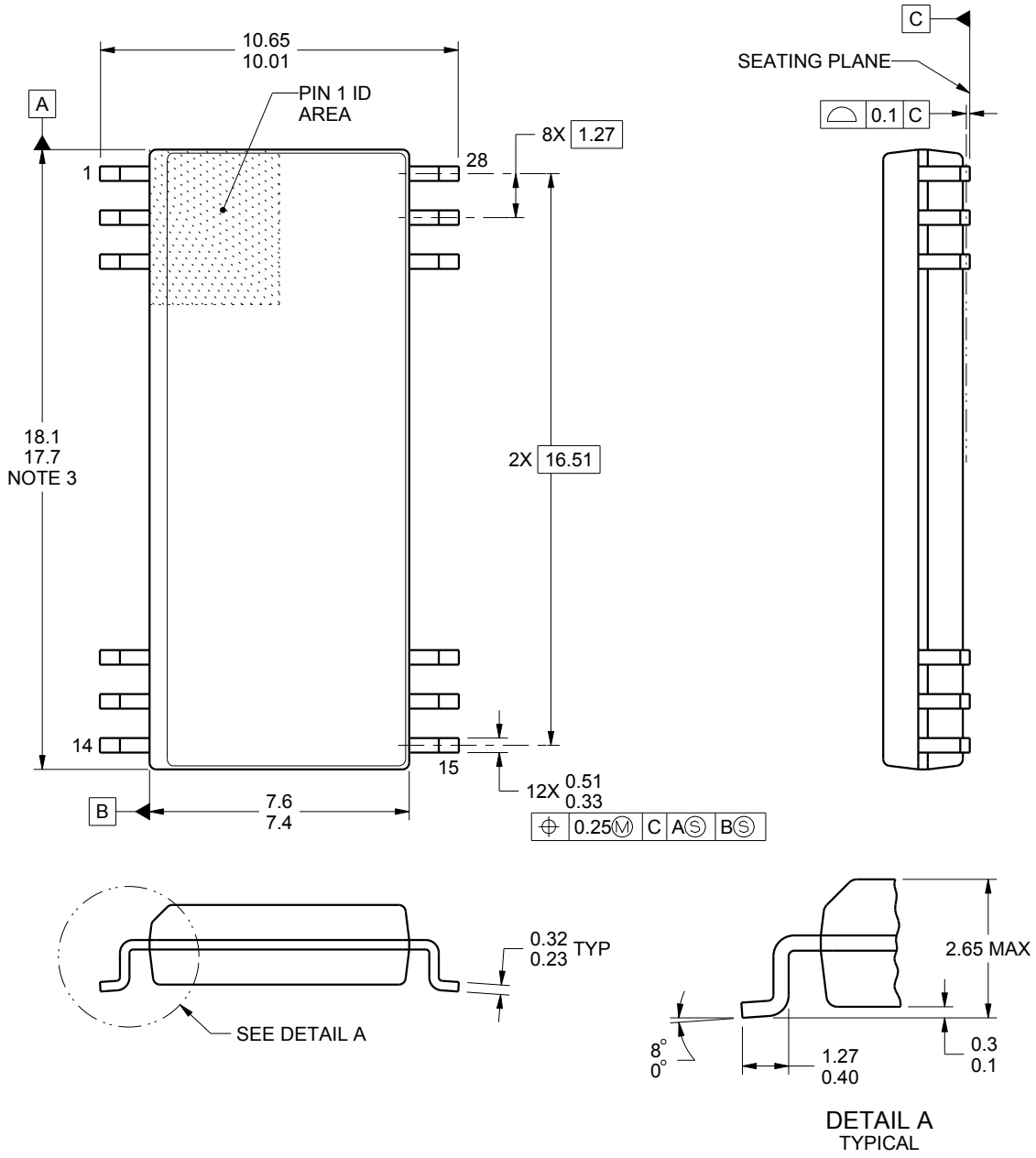
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001-AC with the exception of lead count.
D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
F. Dimensions are measured at the lead tips with the leads unconstrained.
G. A visual index feature must be located within the cross-hatched area.

PACKAGE OUTLINE

DVB0012A

SOP - 2.65 mm max height

PLASTIC SMALL OUTLINE



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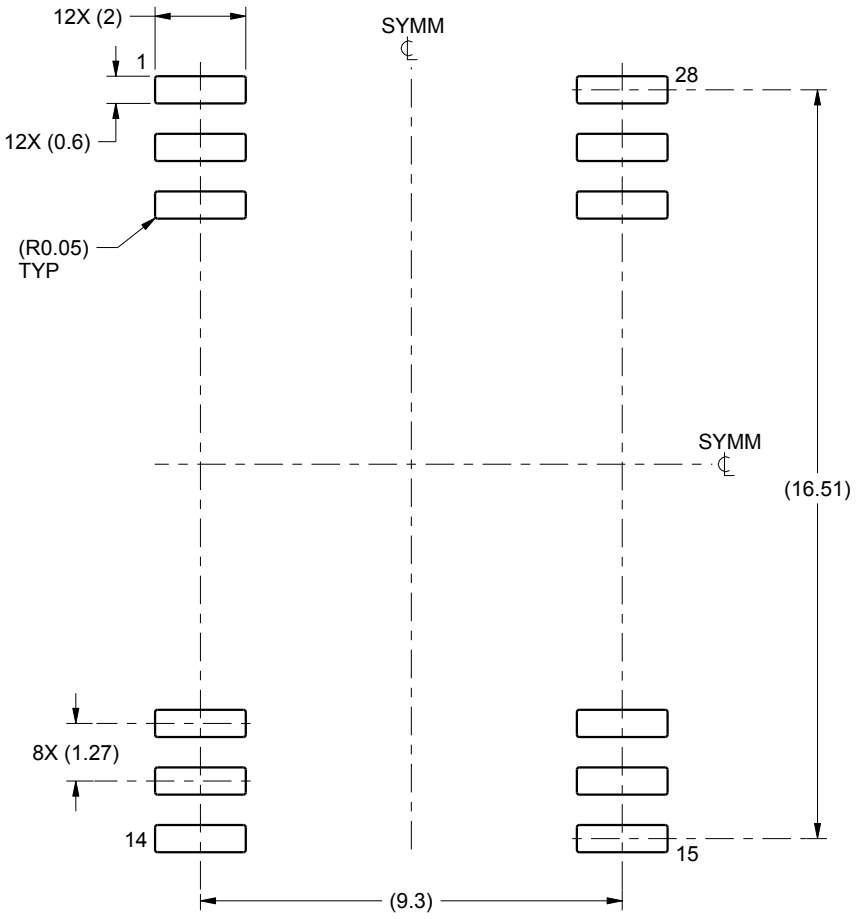
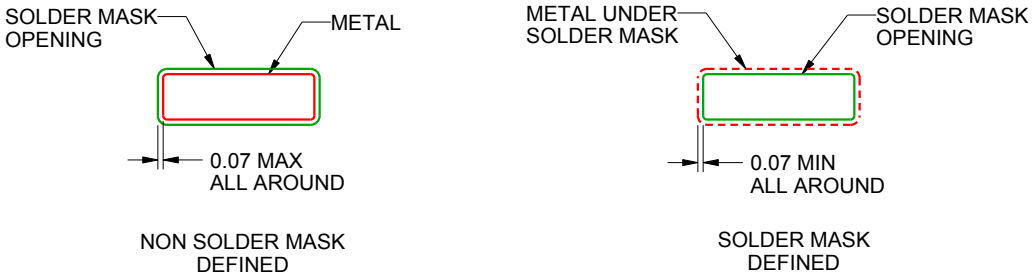
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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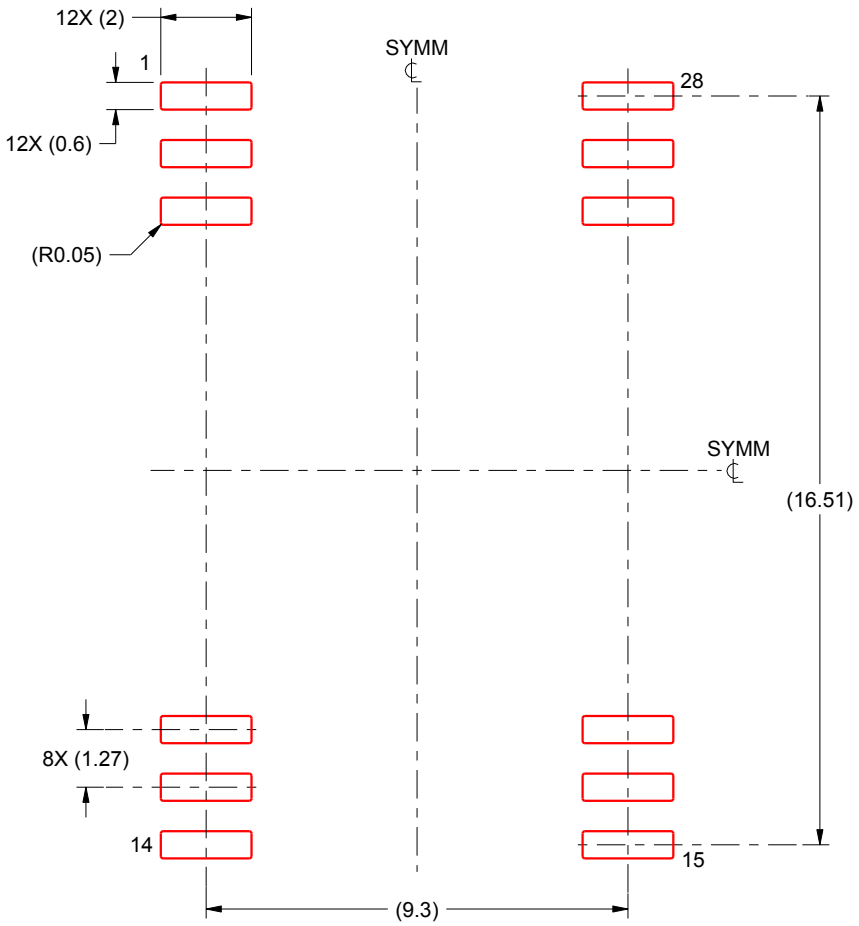
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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