



**THE DATASHEET OF  
PBSS4140U,115**



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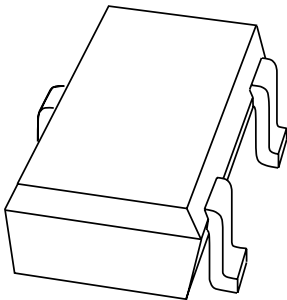
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Kind regards,

Team Nexperia

# DATA SHEET



## **PBSS4140U** 40 V low $V_{CEsat}$ NPN transistor

Product data sheet  
Supersedes data of 2001 Mar 27

2001 Jul 13

# 40 V low $V_{CEsat}$ NPN transistor

# PBSS4140U

### FEATURES

- Low collector-emitter saturation voltage
- High current capabilities.
- Improved device reliability due to reduced heat generation.
- Enhanced performance over SOT231A general purpose packaged transistors.

### APPLICATIONS

- General purpose switching and muting
- LCD backlighting
- Supply line switching circuits
- Battery driven equipment (mobile phones, video cameras and hand-held devices).

### DESCRIPTION

NPN low  $V_{CEsat}$  transistor in a SOT323 plastic package. PNP complement: PBSS5140U.

### MARKING

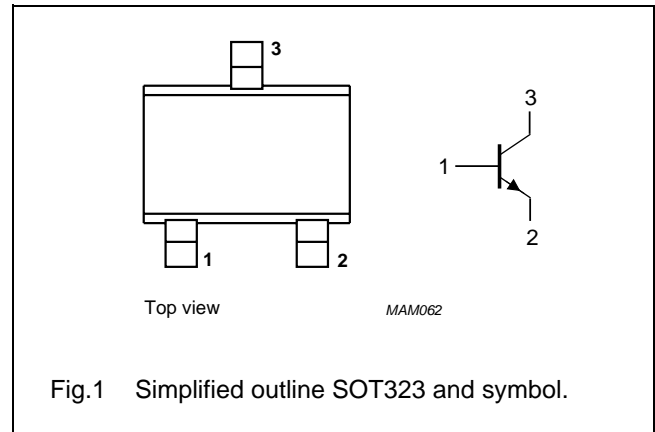
TYPE NUMBER	MARKING CODE
PBSS4140U	41t

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	40	V
$I_{CM}$	peak collector current	2	A
$R_{CEsat}$	equivalent on-resistance	<500	$m\Omega$

### PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	40	V
$V_{CEO}$	collector-emitter voltage	open base	–	40	V
$V_{EBO}$	emitter-base voltage	open collector	–	5	V
$I_C$	collector current (DC)		–	1	A
$I_{CM}$	peak collector current		–	2	A
$I_{BM}$	peak base current		–	1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$ ; note 1	–	250	mW
		$T_{amb} \leq 25\text{ }^\circ\text{C}$ ; note 2	–	350	mW
$T_{stg}$	storage temperature		–65	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$
$T_{amb}$	operating ambient temperature		–65	+150	$^\circ\text{C}$

### Notes

1. Device mounted on a printed-circuit board; single sided copper; tinplated; standard footprint.
2. Device mounted on a printed-circuit board; single sided copper; tinplated; mounting pad for collector 1 cm.

40 V low  $V_{CEsat}$  NPN transistor

## PBSS4140U

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	500	K/W
		in free air; note 2	357	K/W

## Notes

1. Device mounted on a printed-circuit board, single sided copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.

## CHARACTERISTICS

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

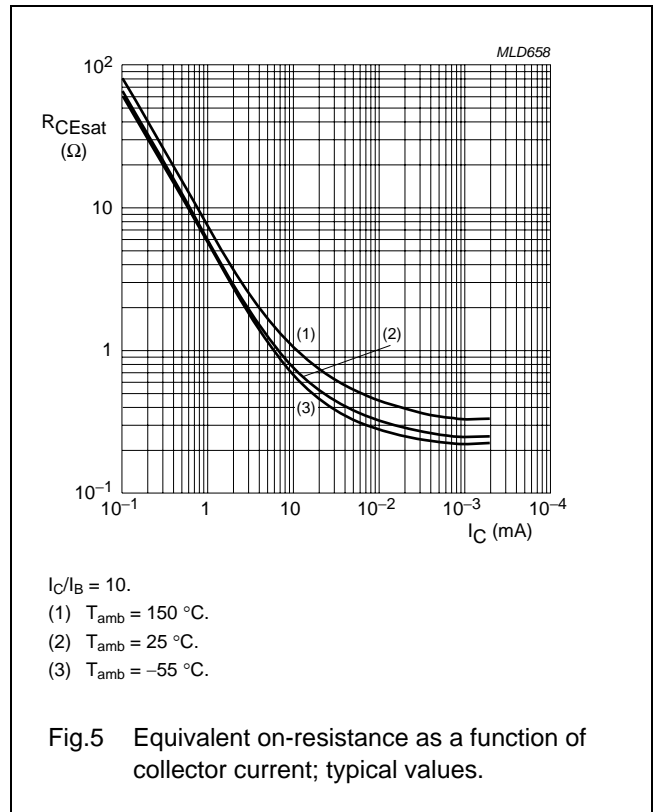
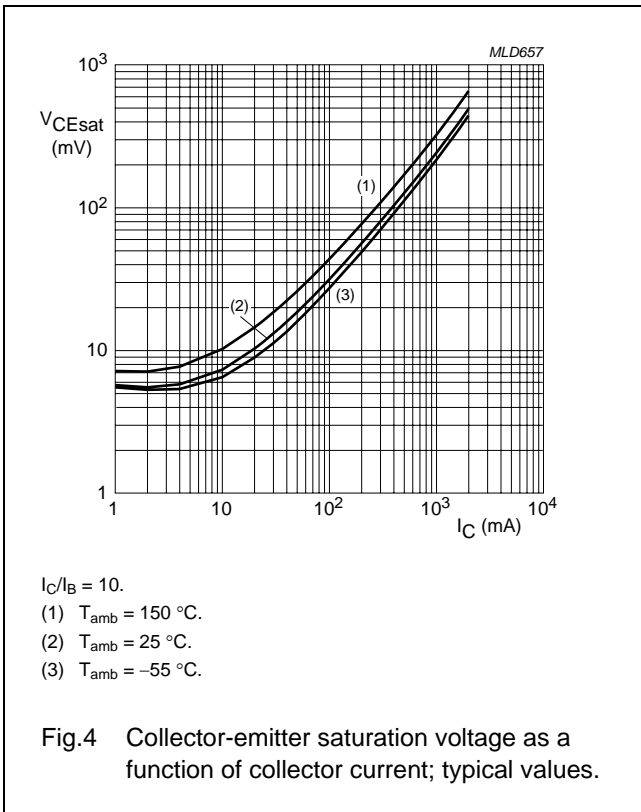
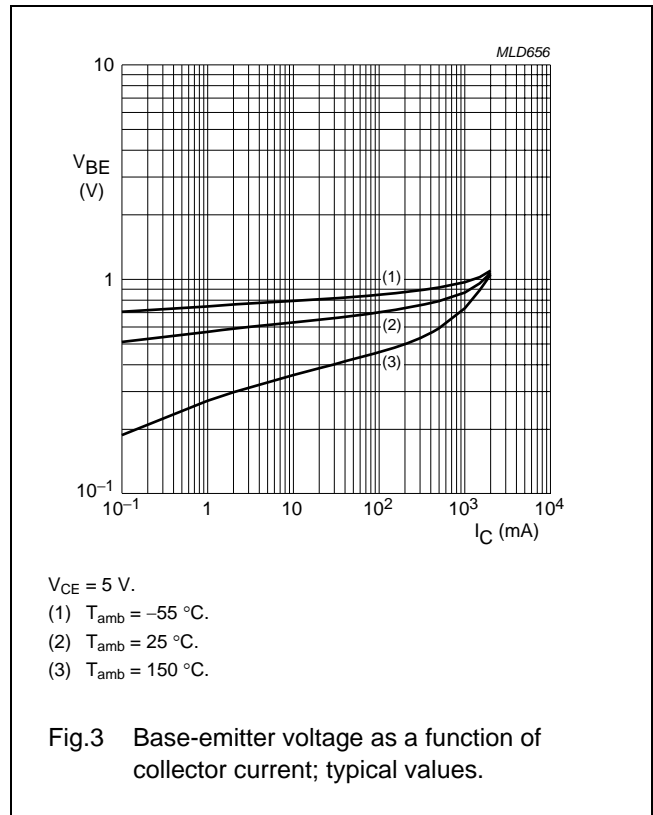
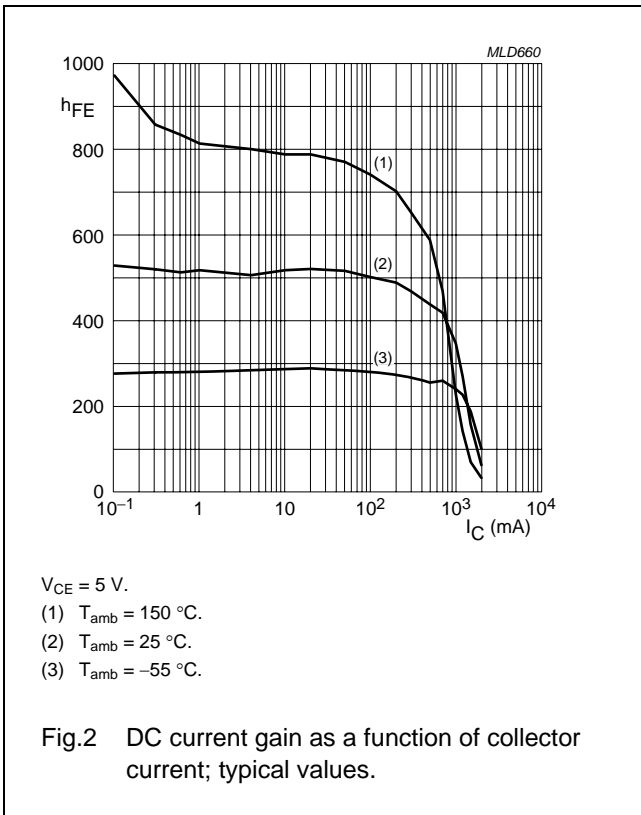
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 40\text{ V}; I_C = 0$	–	–	100	nA
		$V_{CB} = 40\text{ V}; I_C = 0; T_{amb} = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0$	–	–	100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	300	–	–	
		$V_{CE} = 5\text{ V}; I_C = 500\text{ mA}$	300	–	900	
		$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	200	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 1\text{ mA}$	–	–	200	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	–	250	mV
		$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	500	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = 500\text{ mA}; I_B = 50\text{ mA}; \text{note 1}$	–	260	<500	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 100\text{ mA}$	–	–	1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	–	–	1.1	V
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	150	–	–	MHz
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_C = 0; f = 1\text{ MHz}$	–	–	10	pF

## Note

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .

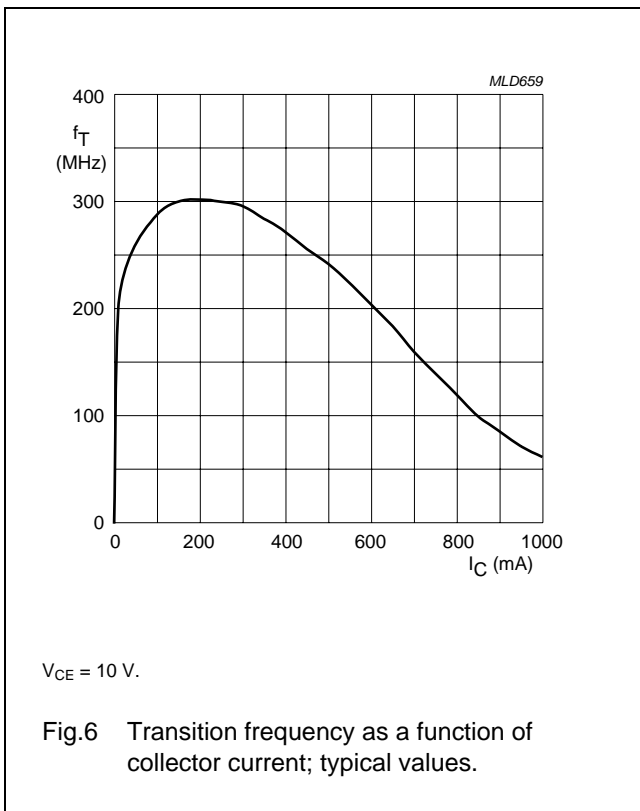
40 V low  $V_{CEsat}$  NPN transistor

PBSS4140U



40 V low  $V_{CEsat}$  NPN transistor

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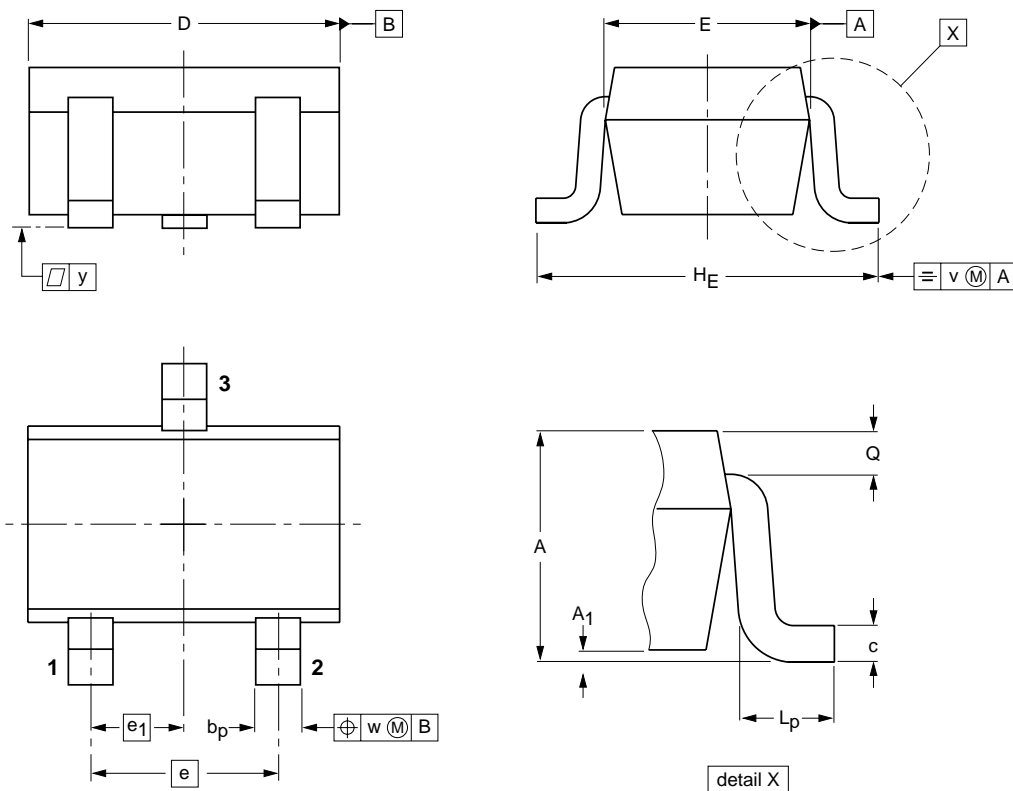
40 V low  $V_{CEsat}$  NPN transistor

PBSS4140U

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

40 V low  $V_{CEsat}$  NPN transistor

PBSS4140U

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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## **Contact information**

For additional information please visit: **<http://www.nxp.com>**

For sales offices addresses send e-mail to: **[salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)**

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