



**THE DATASHEET OF  
BD9G102G-LBTR**



# 6V to 42V, 0.5A 1ch Simple Buck Converter Integrated FET

## BD9G102G-LB

### General Description

This product guarantees long time support in Industrial market.

The BD9G102G-LB is a 42V, 0.5A non-synchronous buck converter with integrated internal high-side 42V Power MOSFET. Operating frequency is 1.0MHz fixed by inner circuit. The components of phase compensation are built in. Additional protection features are included such as Over Current Protection, Thermal Shutdown and Under Voltage Lockout.

### Features

- Long Time Support Product for Industrial Applications
- Wide Operating Input Range 6V to 42V
- 45V/800mΩ Internal Power MOSFET
- 1.0MHz Fixed Operating Frequency
- Feedback Pin Voltage  $0.75V \pm 2.0\%$
- Accurate EN Threshold  $1.8V \pm 0.1V$
- Current Mode
- Internal Compensation
- Over Current Protection (OCP)
- Under Voltage Locked Out (UVLO)
- Over Voltage Protection (OVP)
- Thermal Shutdown (TSD)
- 0μA Low Shutdown Supply Current

### Key Specifications

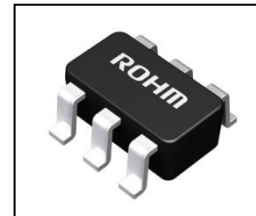
- |                             |                |
|-----------------------------|----------------|
| ■ Input Voltage Range:      | 6V to 42V      |
| ■ Ref. Precision (Ta=25°C): | ±2.0 %         |
| ■ Max Output Current:       | 0.5A (Max)     |
| ■ Switching Frequency:      | 1.0MHz (Typ)   |
| ■ Shutdown Current:         | 0μA (Typ)      |
| ■ Operating Temperature:    | -40°C to +85°C |

### Package

SSOP6

W(Typ) x D(Typ) x H(Max)

2.90mm x 2.80mm x 1.25mm



SSOP6

### Applications

- Industrial Equipment
- Battery Powered Equipment
- OA Instrument

### Typical Application Circuit

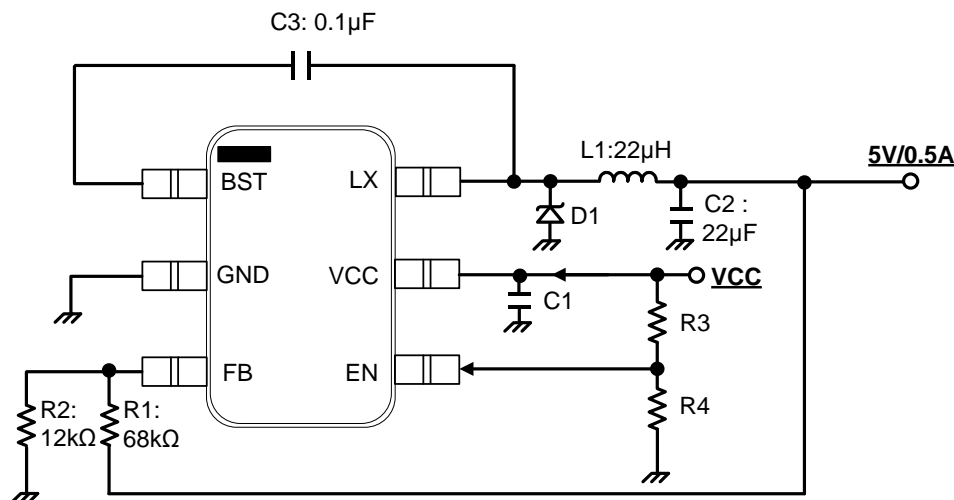


Figure 1. Typical Application Circuit

Pin Configuration

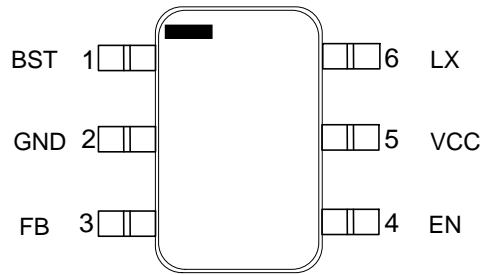


Figure 2. Pin Configuration (TOP VIEW)

Pin Description

Pin No.	Pin Name	Description
1	BST	The pin is power supply for floating Power MOSFET driver. Connect bypass capacitor between the pin and the LX pin for bootstrap operation. A 0.1μF ceramic capacitor is recommended.
2	GND	Ground.
3	FB	Voltage feedback pin. This pin is error-amp inverted input. This pin voltage is set to 0.75V by feedback loop in application.
4	EN	The BD9G102G-LB is shut down when this pin is smaller than 0.5 V and non-switching mode when this pin is between 0.5 V and 1.5 V, active when this pin is 1.8V or more.
5	VCC	Input supply. Place bypass capacitor as close as possible to this pin.
6	LX	Switching Node. Place schottky barrier diode and inductor as close as possible to this pin.

Block Diagram

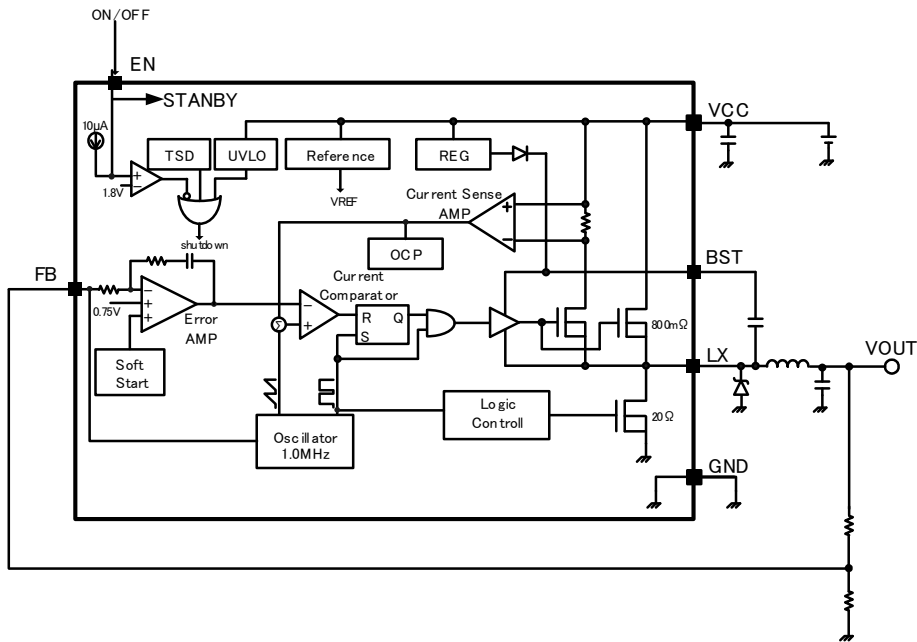


Figure 3. Block Diagram

**Description of Blocks**

1. Reference  
This block generates reference voltage and current.  
It provides reference voltage and current to error-amp, oscillator, and etc.
2. REG  
This is a gate drive voltage generator and 5.0V regulator for internal circuit power supply.
3. OSC  
It is generated rectangular wave of 1.0MHz with operation frequency of normal time.  
To protect over current from output shorted to GND, the frequency is changed depending on FB voltage by the Frequency fold-back function.
4. Soft Start  
This block does Soft Start to the output voltage of DC/DC converter, and prevents in-rush current during Start-up.  
Soft Start Time depends on application and start-condition because frequency fold-back function is built-in.
5. ERROR AMP  
This is an error amplifier which detects output signal, and outputs PWM control signal.  
Internal reference voltage is set to 0.75V. Also, the BD9G102G-LB has internal phase compensated element between error amp's input and output.
6. ICOMP  
This is a comparator that outputs PWM signal from current feed-back signal and error-amp output for current-mode.
7. Power MOSFET  
This is a 45V/800mΩ Nch Power MOSFET SW that converts inductor current of DC/DC converter.
8. UVLO  
This is a low voltage error prevention circuit.  
This prevents internal circuit error during increase of power supply voltage and during decline of power supply voltage.  
It monitors VCC pin voltage and internal REG voltage, and when VCC voltage becomes 5.3V and below, it turns OFF all output FET and DC/DC converter's output, and Soft Start circuit resets.  
Now this threshold has hysteresis of 200mV.
9. EN  
If the voltage from this pin is below 0.5V, IC operation is OFF. If it is between 0.5V and 1.5V, internal REG circuit turns ON. If it is greater than 1.8V(Typ), the IC is operational and a hysteresis generation current of 10 μA (Typ) is sourced from the EN pin. To turn off the IC, source current should be removed.  
When the situation without a signal to control the EN pin at the time of start up is assumed, pull down the EN pin by resistor to prevent becoming the high impedance.  
Arbitrary UVLO is possible by connecting the EN pin to a voltage divider from the input voltage.
10. TSD  
Circuit for preventing malfunction at high Temperature.  
When it detects an abnormal temperature, it turns OFF DC/DC Converter Output. The threshold of TSD has hysteresis.  
When the temperature is decreased, the IC automatically returns to normal operation.
11. OVP  
Over Voltage Protection.  
Output voltage is monitored with the FB pin, and output FET is turned off when it becomes 113% of set-point voltage.
12. OCP  
Over Current Protection.  
It monitors current of Power MOSFET. If the current is 1.2A (Typ) or more, this function reduce duty by pulse-by-pulse and restrict the input current.

**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Rating	Unit
VCC to GND	V <sub>CC</sub>	-0.3 to +45	V
BST to GND	V <sub>BST</sub>	-0.3 to +52	V
BST to LX	ΔV <sub>BST</sub>	7	V
EN to GND	V <sub>EN</sub>	-0.3 to +45	V
LX to GND	V <sub>LX</sub>	-0.3 to +45	V
FB to GND	V <sub>FB</sub>	-0.3 to +7	V
Power MOSFET Drain Current	I <sub>DH</sub>	I <sub>OCF</sub>	A
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Maximum Junction Temperature	T <sub>Jmax</sub>	150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Thermal Resistance**(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
SSOP6				
Junction to Ambient	θ <sub>JA</sub>	376.5	185.4	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	40	30	°C/W

(Note 1)Based on JESD51-2A(Still-Air).

(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V <sub>CC</sub>	6	-	42	V
Output Voltage	V <sub>OUT</sub>	0.75 <sup>(Note 5)</sup>	-	V <sub>CC</sub> ×0.8	V
Output Current <sup>(Note 6)</sup>	I <sub>OUT</sub>	-	-	500	mA
Input Capacitance	C <sub>IN</sub>	2.2 <sup>(Note 7)</sup>	-	-	μF
Output Capacitance	C <sub>OUT</sub>	22 <sup>(Note 8)</sup>	-	-	μF
Inductance	L	15 <sup>(Note 9)</sup>	-	-	μH
Operating Temperature	Topr	-40	-	+85	°C

(Note 5) Restricted by minimum duty = F<sub>SW</sub> × Minimum-On Time (F: frequency; Minimum-On Time typ : 80ns)

If the voltage of V<sub>CC</sub> × minimum duty is lower than 0.75V, this value is minimum output.

(Note 6) If the output Current is lower than ΔIL/2, there is possibility that BD9G102G-LB operates in the PFM mode. (ΔIL: Output ripple current)

For improving the stability, it's recommended to load current more than ΔIL/2 during normal operation.

(Note 7) The ceramic capacitance is selected in the range including temperature characteristics and DC bias voltage effect. Refer to P.19.

(Note 8) The ceramic capacitance is selected in the range including temperature characteristics and DC bias voltage effect. Refer to P.18.

(Note 9) Restricted by output voltage setting. Refer to P.18.

Timing Chart

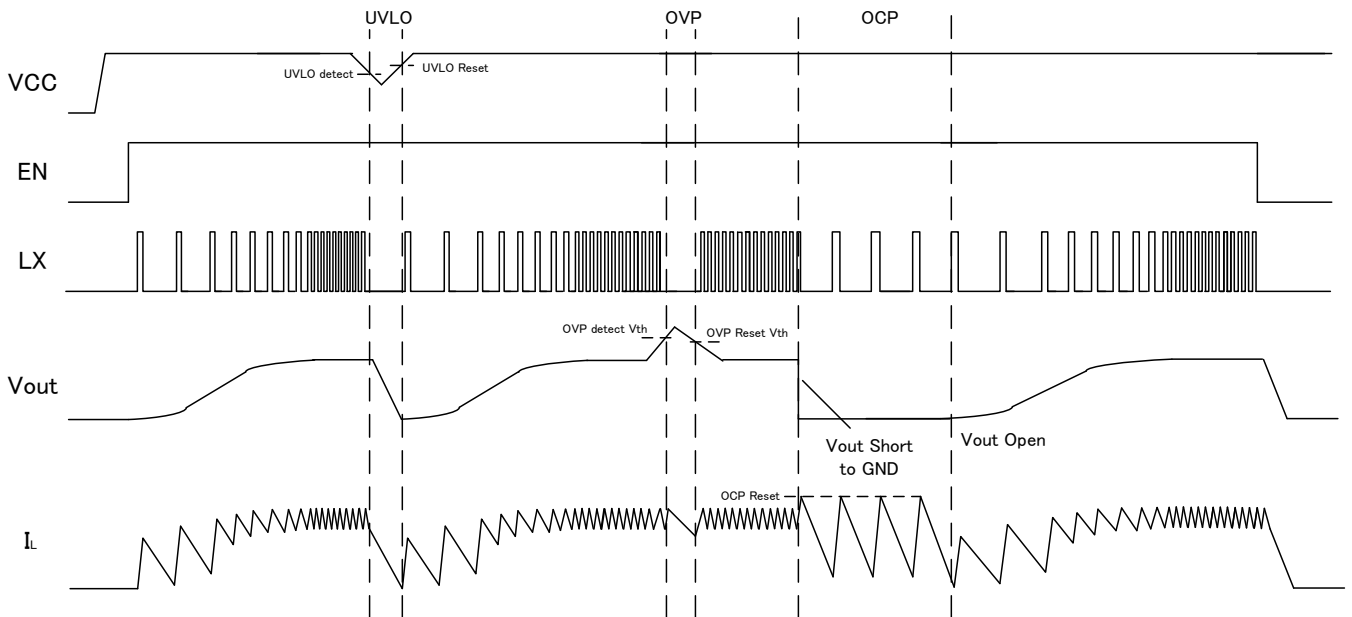


Figure 4. Timing Chart

**Electrical Characteristics** (Unless otherwise specified Ta=25°C, VCC=18V, VOUT=5.0V, EN=3V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<b>Circuit Current</b>						
Shutdown supply current	I <sub>ST</sub>	-	0	10	μA	EN = 0 V
Operating non-switching supply current	I <sub>CC</sub>	-	0.5	1.0	mA	FB = 1.2 V (Non-switching)
<b>Under voltage lockout</b>						
Detect threshold voltage	V <sub>UV</sub>	5.0	5.3	5.6	V	VCC falling
Hysteresis width	V <sub>UVHY</sub>	-	200	400	mV	
<b>Oscillator</b>						
Oscillating frequency	F <sub>SW</sub>	0.80	1.00	1.20	MHz	
<b>Error amplifier</b>						
FB Pin Reference Voltage	V <sub>FBN</sub>	0.735	0.750	0.765	V	Ta=25°C
	V <sub>FBA</sub>	0.730	0.750	0.770	V	Ta=-40°C to 85°C
FB Pin Bias Current	I <sub>FB</sub>	-1.0	0	+1.0	μA	V <sub>FB</sub> = 0 V
<b>Power MOSFET</b>						
On resistance	R <sub>onH</sub>	-	800	-	mΩ	
Minimum On Time	T <sub>MIN</sub>	-	80	-	ns	
Over current detect threshold	I <sub>OC</sub>	0.8	1.2	-	A	
<b>EN control</b>						
EN inner Reg threshold	V <sub>ENOF</sub>	-0.3	-	+0.5	V	Shut down
	V <sub>ENON1</sub>	0.5	-	1.5	V	Non switching mode
EN pin output active threshold	V <sub>ENON2</sub>	1.7	1.8	1.9	V	Output active
EN pin current	I <sub>EN</sub>	-12.0	-10.0	-8.0	μA	V <sub>EN</sub> = 3V

Typical Performance Characteristics (Unless otherwise specified, Ta=25°C, VCC=24V, VOUT=5V, EN=3V)

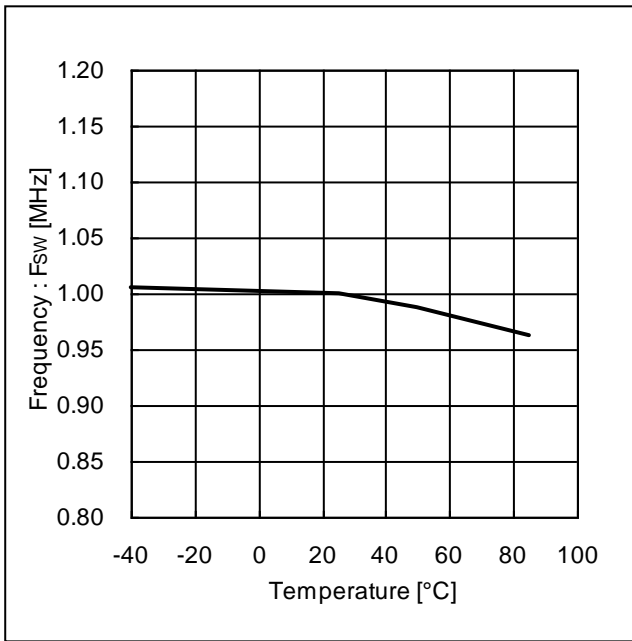


Figure 5. Oscillator Frequency - Temperature

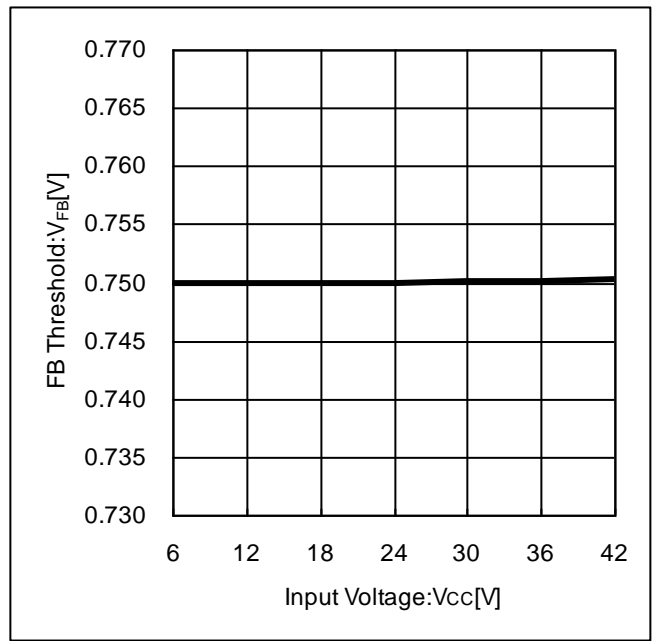


Figure 6. FB Threshold Voltage – Input Voltage

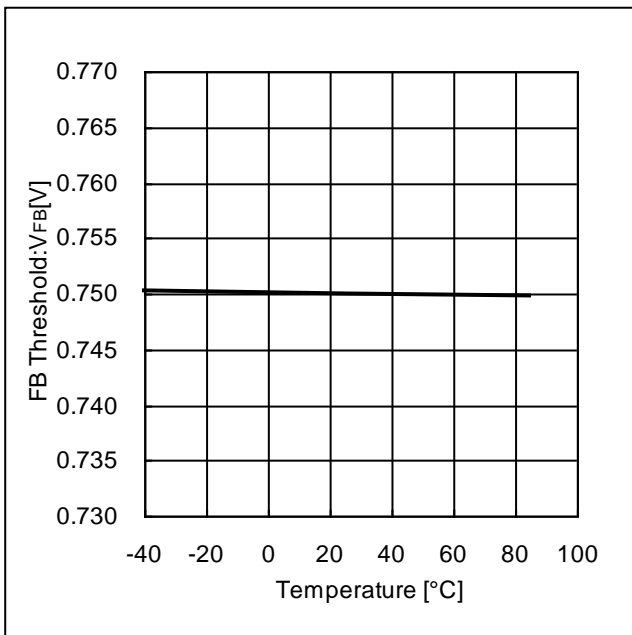


Figure 7. FB Threshold Voltage - Temperature

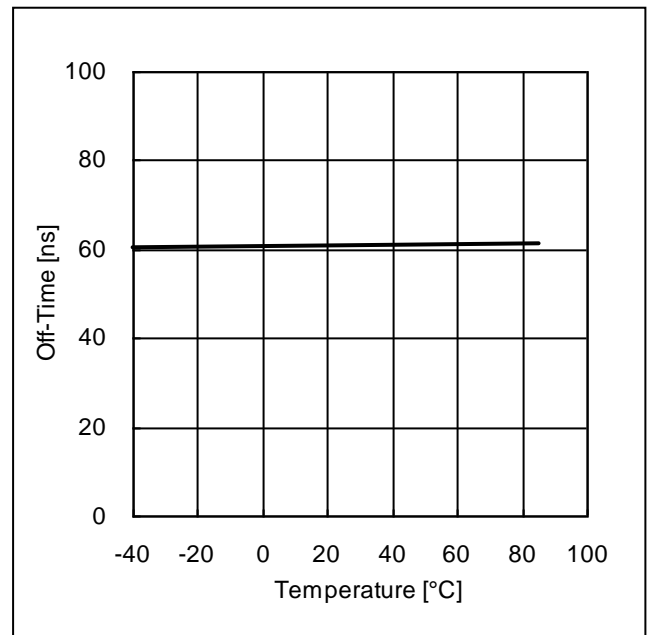


Figure 8. PWMCLK Off-Time - Temperature

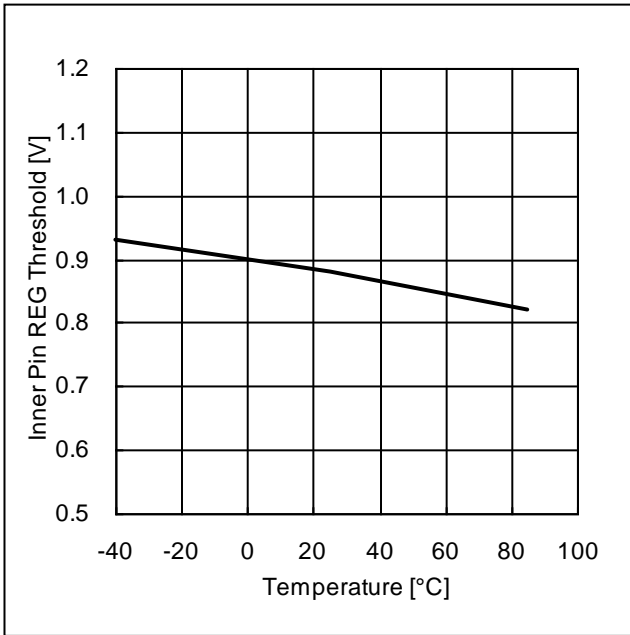


Figure 9. EN Inner REG ON Threshold - Temperature

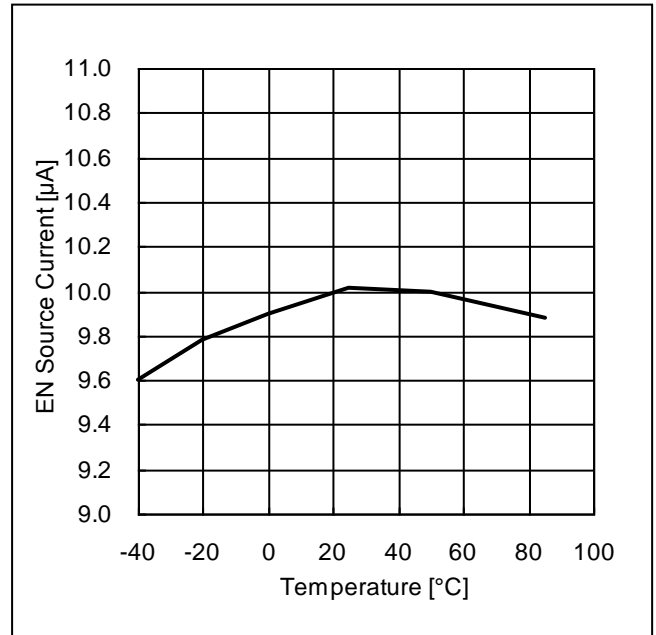


Figure 10. EN Source Current - Temperature

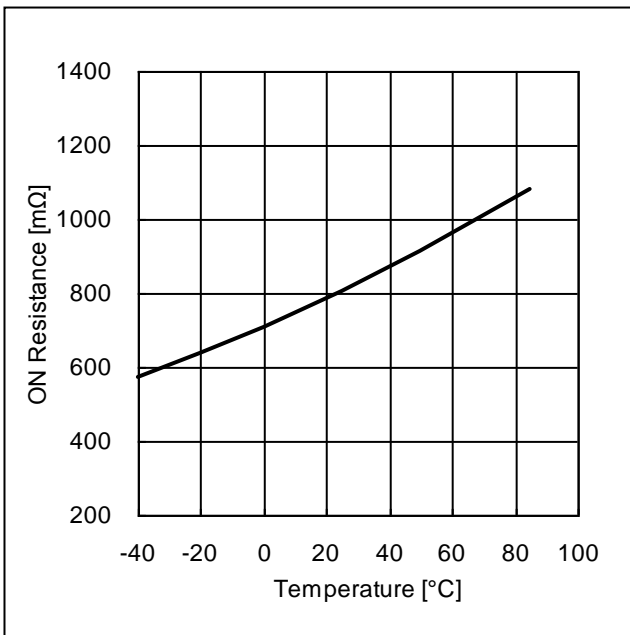


Figure 11. NMOS ON Resistance - Temperature

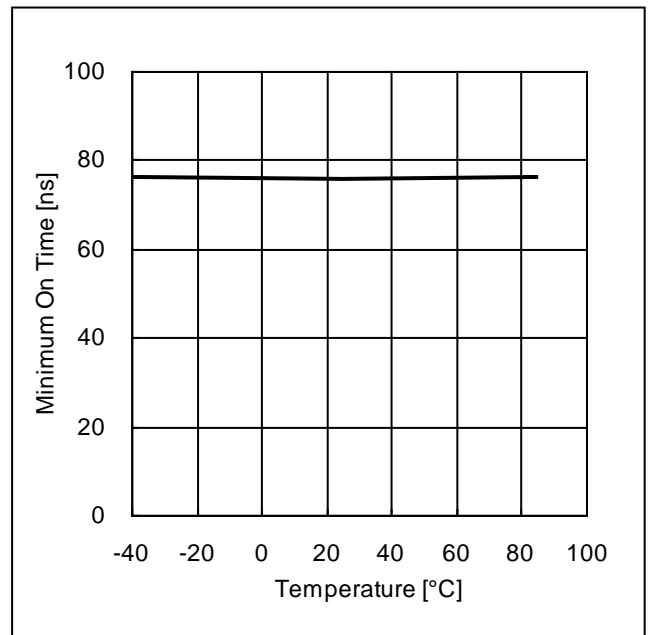


Figure 12. Minimum ON Time - Temperature

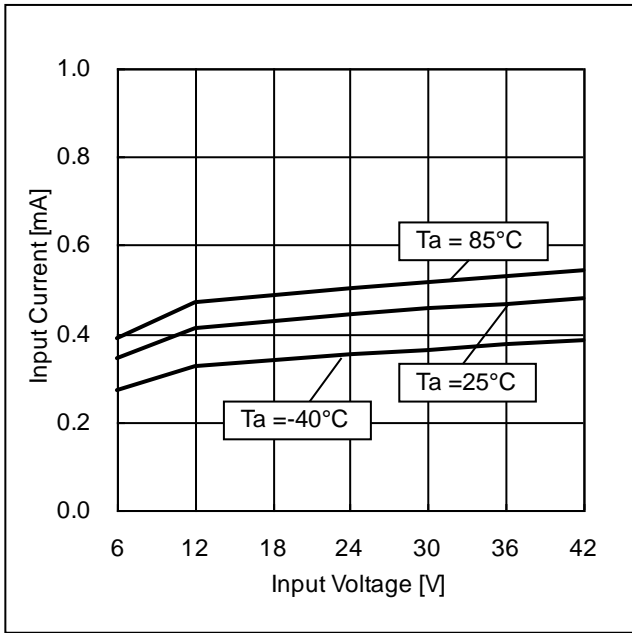


Figure 13. Operating Current – Input Voltage

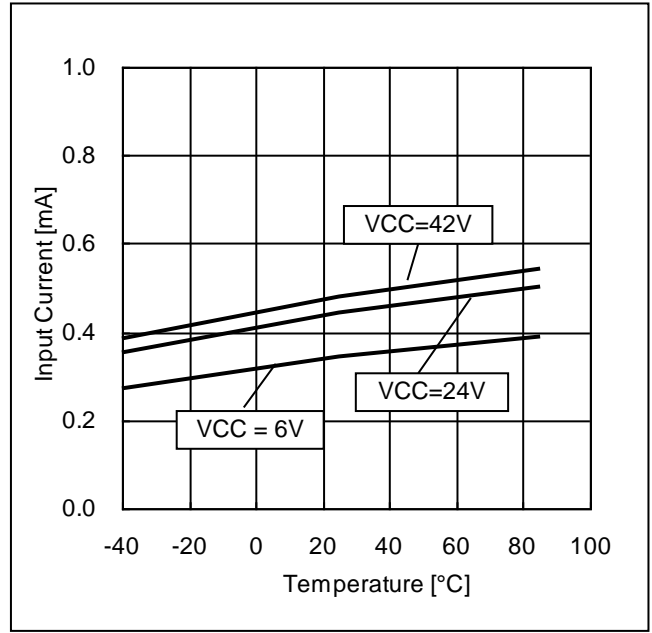


Figure 14. Operating Current – Temperature

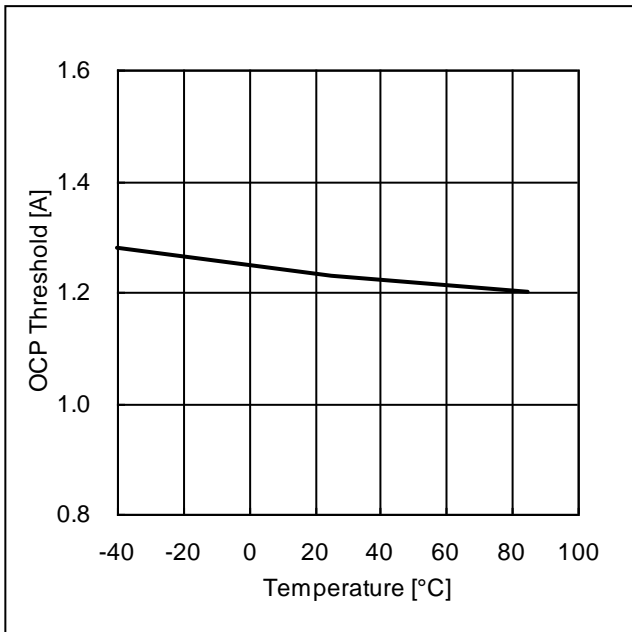


Figure 15. OCP Detect Current - Temperature

Reference Characteristics of Typical Application Circuits

V<sub>OUT</sub>=3.3V

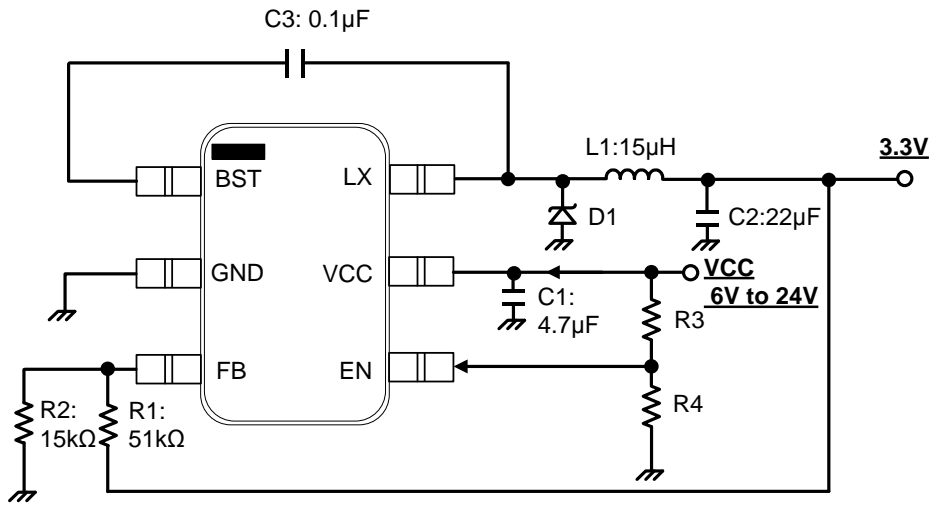


Figure 16. Typical Application Circuit (V<sub>OUT</sub>=3.3V)

Parts	L1:	TDK	CLF5030NIT-150M-D	15µH
	C1:	Murata	GRM32EB31H475KA87	4.7µF/50V
	C2:	Murata	GRM31CR61E226ME15	22µF/25V
	C3:	Murata	GRM155R71E104ME14	0.1µF/25V
	D1:	ROHM	RB060MM-60	

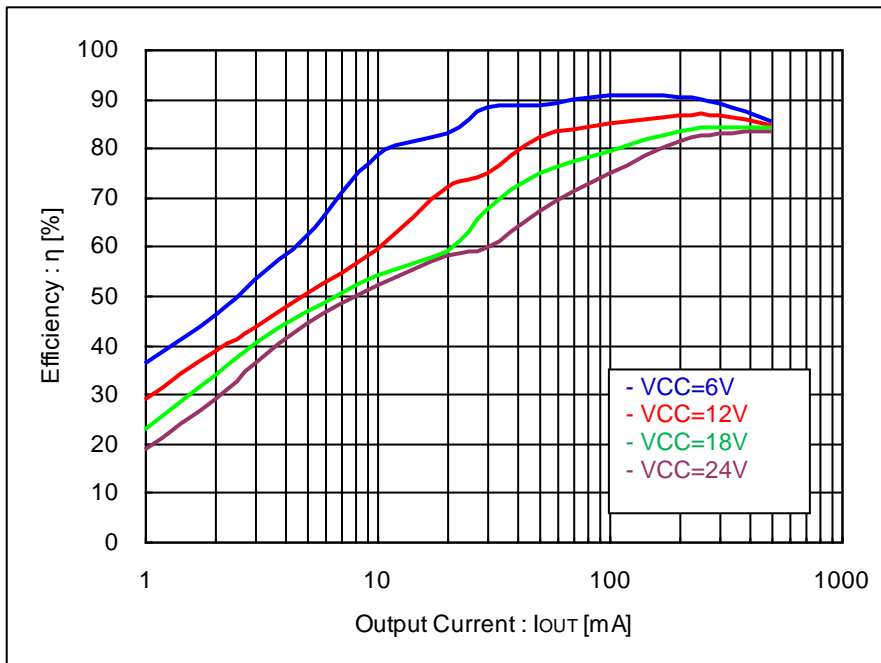


Figure 17. Efficiency-Output Current (V<sub>OUT</sub>=3.3V)

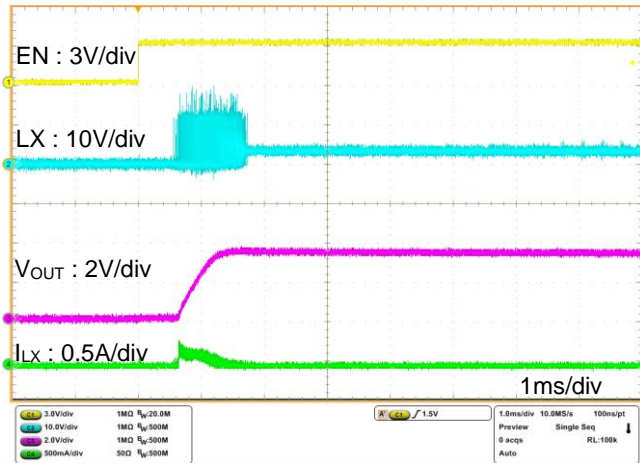


Figure 18. Start-up Characteristics  
(VCC=12V, IOUT=0mA, VOUT=3.3V)

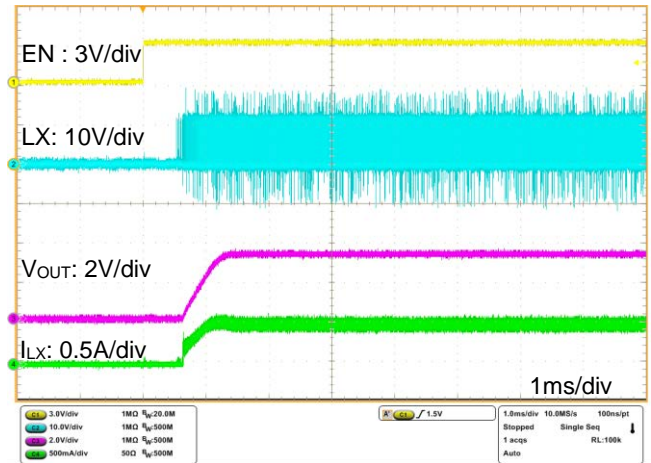


Figure 19. Start-up Characteristics  
(VCC=12V, IOUT=500mA, VOUT=3.3V)

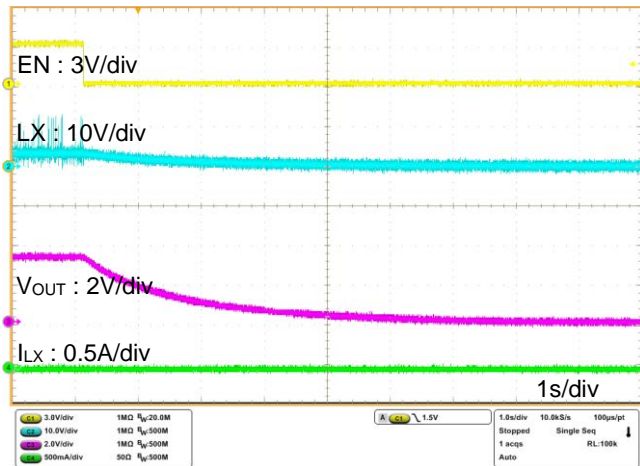


Figure 20. Shut-down Characteristics  
(VCC=12V, IOUT=0mA, VOUT=3.3V)

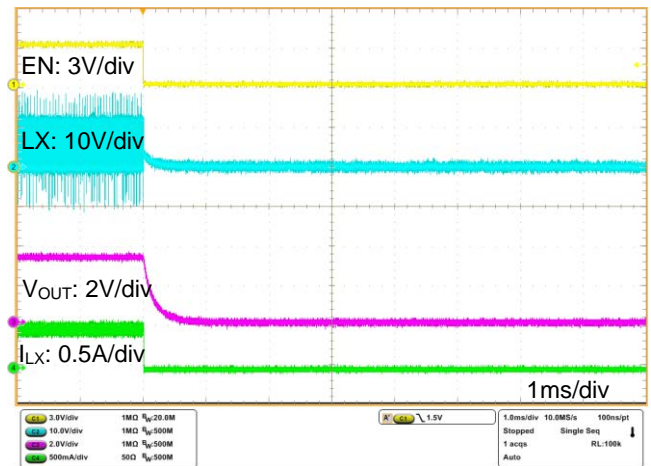


Figure 21. Shut-down Characteristics  
(VCC=12V, IOUT=500mA, VOUT=3.3V)

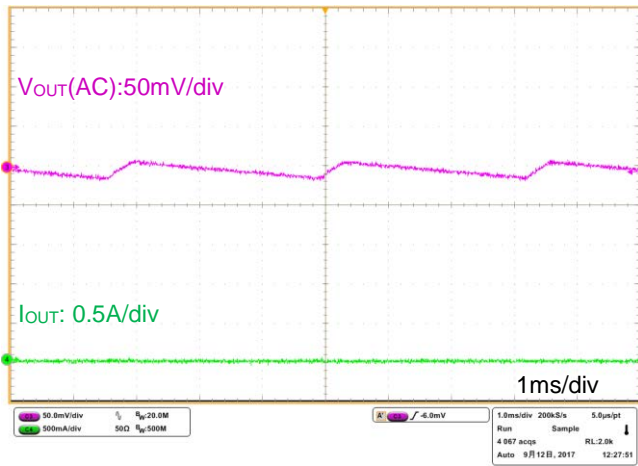


Figure 22.  $V_{out}$  Ripple  
( $V_{CC}=12V$ ,  $I_{out}=0mA$ ,  $V_{out}=3.3V$ )

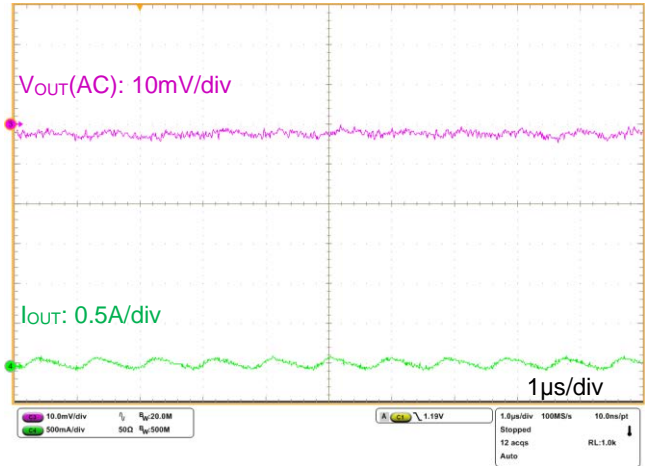


Figure 23.  $V_{out}$  Ripple  
( $V_{CC}=12V$ ,  $I_{out}=50mA$ ,  $V_{out}=3.3V$ )

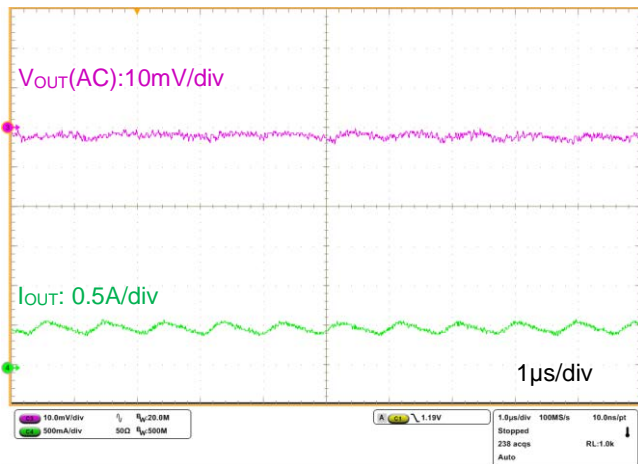


Figure 24.  $V_{out}$  Ripple  
( $V_{CC}=12V$ ,  $I_{out}=500mA$ ,  $V_{out}=3.3V$ )

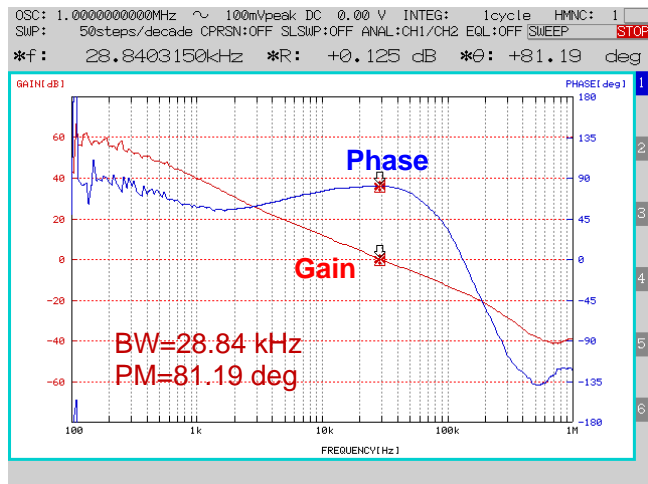


Figure 25. Frequency Response  
( $V_{CC}=12V$ ,  $I_{out}=100mA$ ,  $V_{out}=3.3V$ )

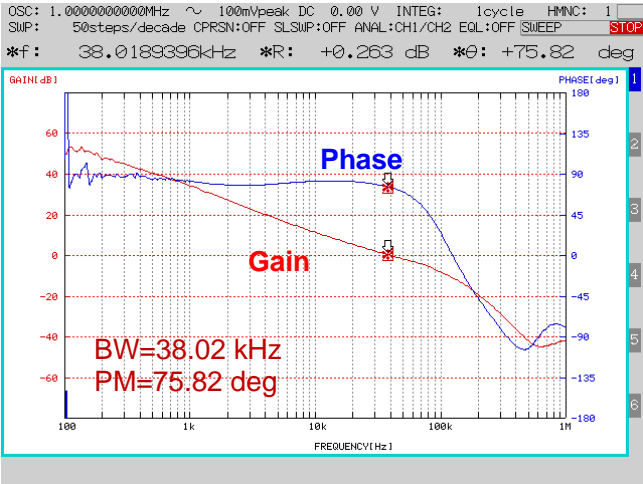


Figure 26. Frequency Response  
 (V<sub>CC</sub>=12V, I<sub>OUT</sub>=500mA, V<sub>OUT</sub>=3.3V)

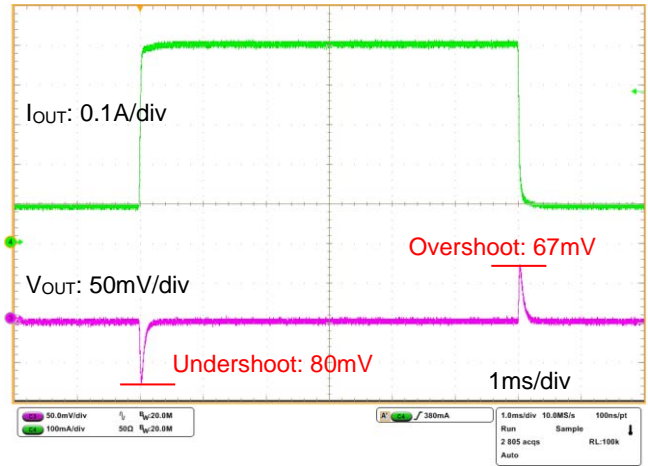


Figure 27. Load Response  
 (V<sub>CC</sub>=12V, I<sub>OUT</sub>=100mA↔500mA, V<sub>OUT</sub>=3.3V)

Reference Characteristics of Typical Application Circuits

V<sub>OUT</sub> = 5.0V

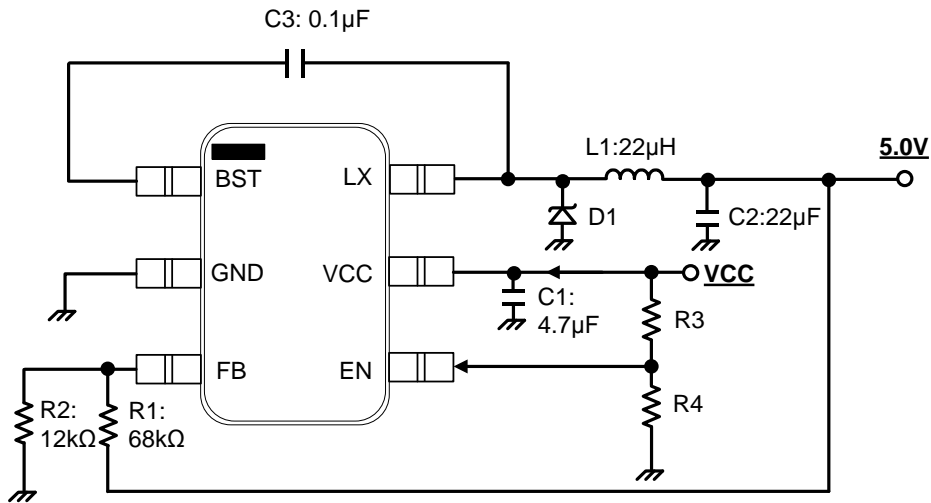


Figure 28 Typical Application Circuit (V<sub>OUT</sub>=5V)

Parts	L1:	TDK	CLF5030NIT-220M-D	22μH
	C1:	Murata	GRM32EB31H475KA87	4.7μF/50V
	C2:	Murata	GRM31CR61E226ME15	22μF/25V
	C3:	Murata	GRM155R71E104ME14	0.1μF/25V
	D1:	ROHM	RB060MM-60	

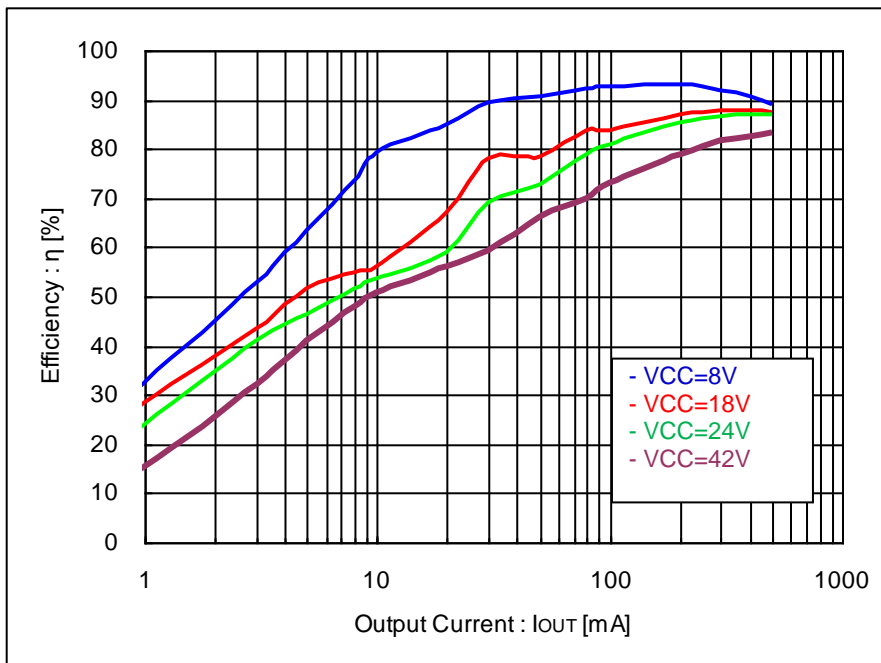


Figure 29 Efficiency-Output Current (V<sub>OUT</sub>=5V)

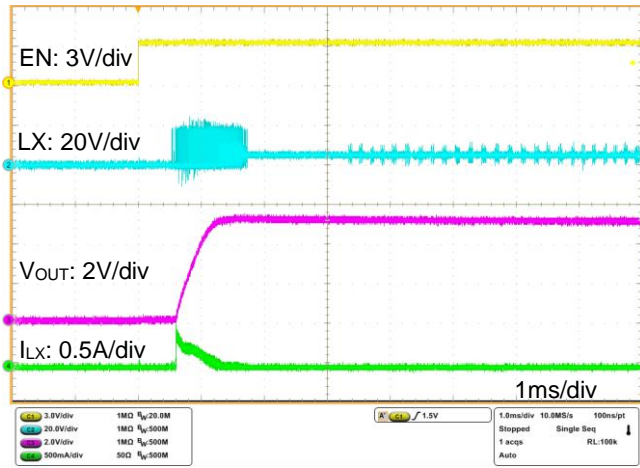


Figure 30. Start-up Characteristics  
(VCC=18V, IOUT=0mA, VOUT=5V)

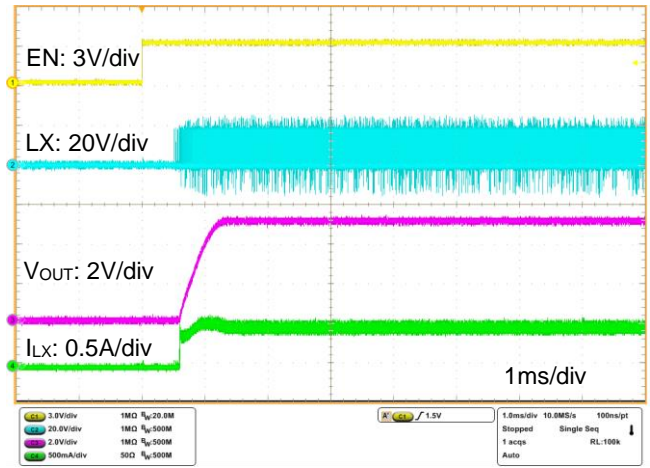


Figure 31. Start-up Characteristics  
(VCC=18V, IOUT=500mA, VOUT=5V)

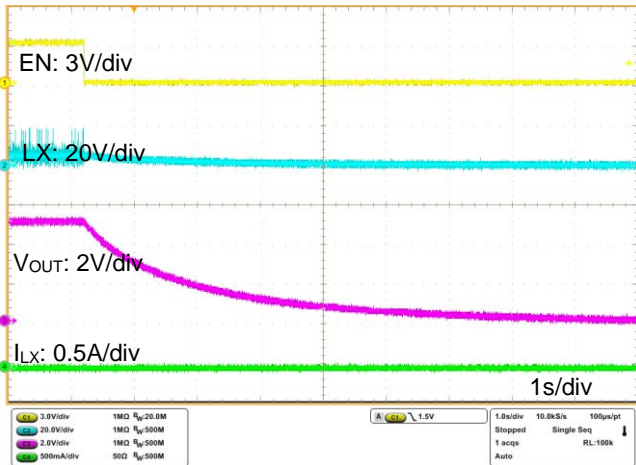


Figure 32. Shut-down Characteristics  
(VCC=18V, IOUT=0mA, VOUT=5V)

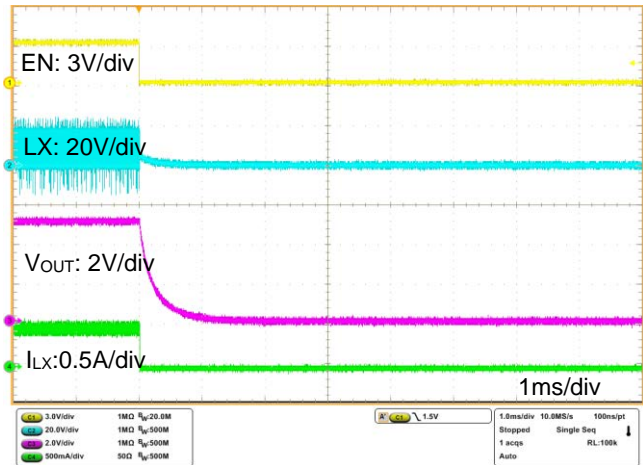


Figure 33. Shut-down Characteristics  
(VCC=18V, IOUT=500mA, VOUT=5V)

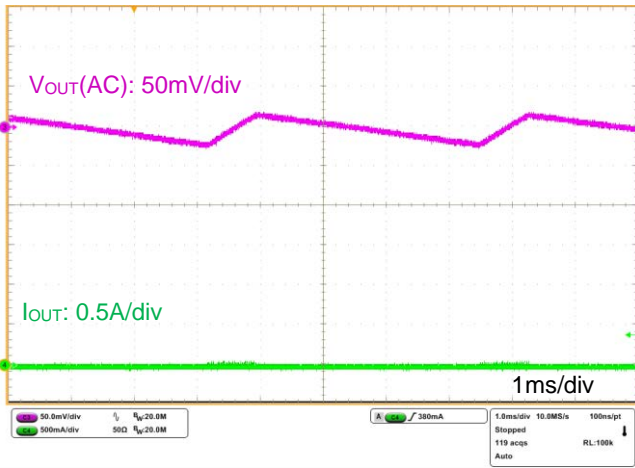


Figure 34.  $V_{out}$  Ripple  
( $V_{CC}=18V$ ,  $I_{out}=0mA$ ;  $V_{out}=5V$ )

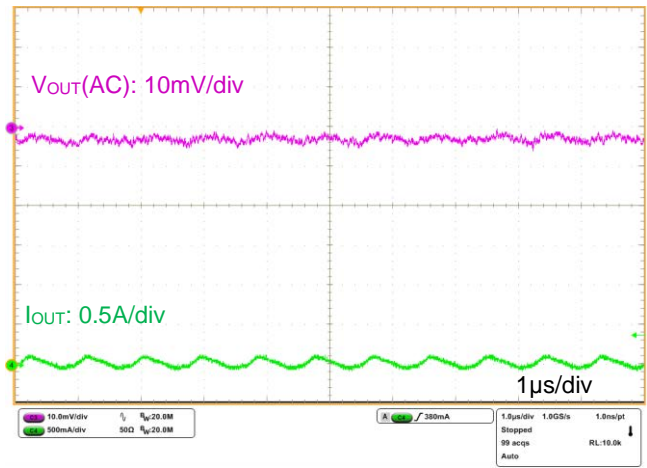


Figure 35.  $V_{out}$  Ripple  
( $V_{CC}=18V$ ,  $I_{out}=50mA$ ,  $V_{out}=5V$ )

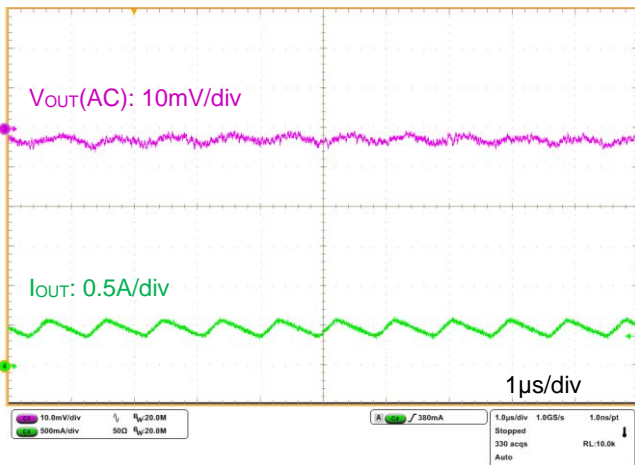


Figure 36. Frequency Response  
( $V_{CC}=18V$ ,  $I_{out}=500mA$ ,  $V_{out}=5V$ )

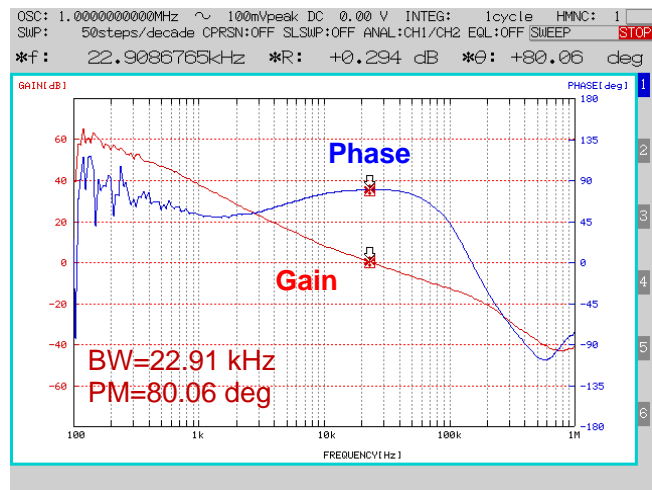


Figure 37. Frequency Response  
( $V_{CC}=18V$ ,  $I_{out}=100mA$ ,  $V_{out}=5V$ )

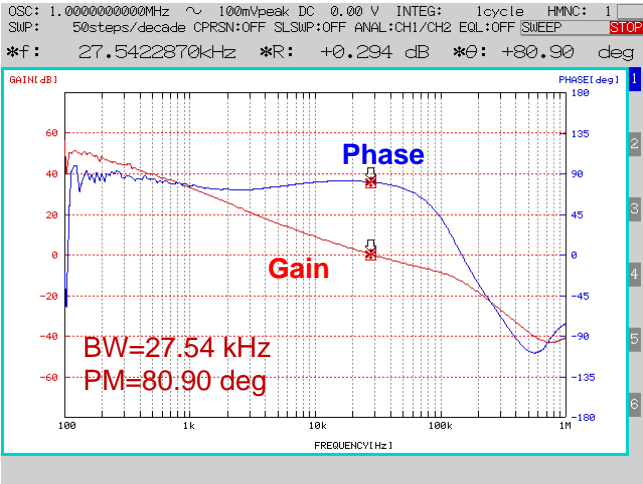


Figure 38. Frequency Response  
(V<sub>CC</sub>=18V, I<sub>OUT</sub>=500mA, V<sub>OUT</sub>=5V)

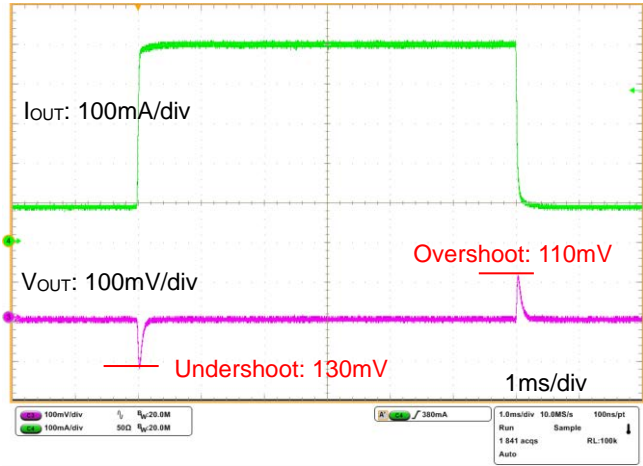


Figure 39. Load Response  
(V<sub>CC</sub>=18V, V<sub>OUT</sub>=5V, I<sub>OUT</sub>=100mA ← 500mA)

**Selection of Components Externally Connected**

**(1) Inductors**

Something of the shield type that fulfills the current rating (Current value lpeak below), with low DCR (DC Resistance) is recommended. Value of Inductance influences Inductor Ripple Current and becomes the cause of Output Ripple. In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

$$I_{peak} = I_{OUT} + \frac{\Delta I_L}{2} \tag{1}$$

$$\Delta I_L = \frac{V_{CC} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{CC}} \times \frac{1}{f} \tag{2}$$

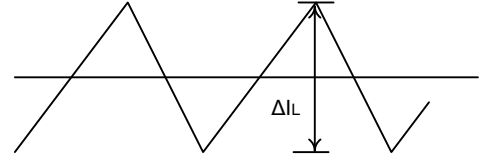


Figure 40. Inductor Current

Where:

ΔIL is the Output Ripple Current.

VCC is the Input Voltage.

VOUT is the Output Voltage.

f is the Switching Frequency.

**Recommended Inductor**

**TDK CLF5030NIT-D Series**

When the duty cycle greater than 50% due to input-output voltage setting, there is possibility of occurring sub-harmonic oscillation. Please design the value of Inductance that will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions. The minimum value of inductance in the case of a duty cycle is greater than 50% is shown in the following figure.

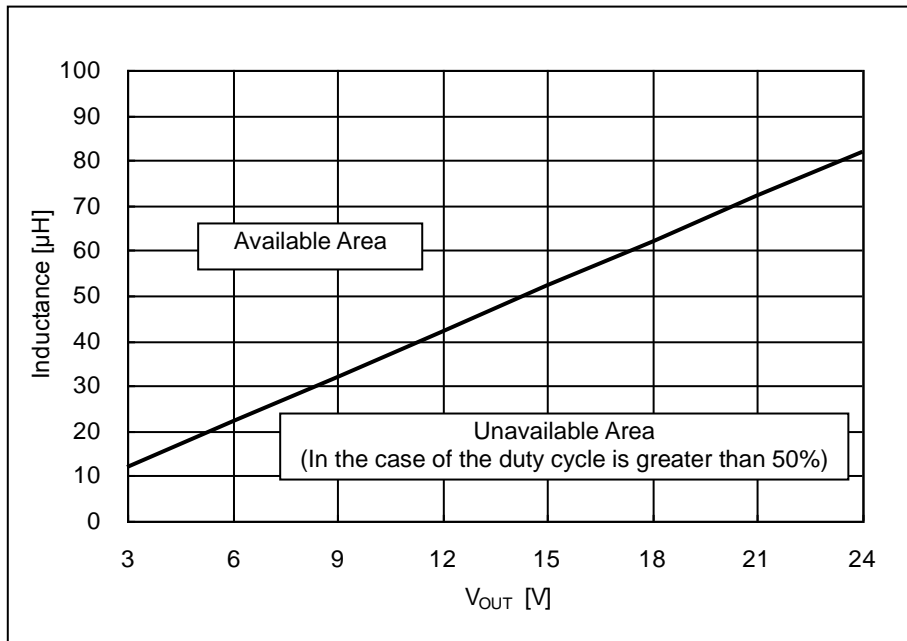


Figure 41. Recommended V<sub>OUT</sub> vs Inductance

※When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

**(2) Output Capacitor**

In order for capacitor to be used in output to reduce output ripple, Low ceramic capacitor of ESR is recommended. Also, for capacitor rating, on top of putting into consideration DC Bias characteristics, please use something whose maximum rating has sufficient margin with respect to the Output Voltage. The output ripple voltage can be estimated by the following formula.

$$V_{Ripple} = \Delta I_L \times \frac{1}{2\pi \times f \times C_{OUT}} + \Delta I_L \times R_{ESR} \tag{3}$$

The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the crossover frequency at less than 1/20 of the switching frequency. With high switching frequencies such as the 1.0MHz frequency of this design, internal circuit limitations of the BD9G102G-LB limit the practical maximum crossover frequency to about 50kHz. In general, the crossover frequency should be higher than the corner frequency determined by the load impedance and the output capacitor. This limits the minimum capacitor value for the output filter to:

$$C_{OUT\_min} = \frac{1}{2\pi \times R_{Load} \times fc\_max} \quad (4)$$

Where:

$R_{Load}$  is the output load resistance.

$fc\_max$  is the maximum crossover frequency.

Please design in a way that it is held within Capacity Ripple Voltage.

In the BD9G102G-LB, it is recommended a ceramic capacitor more than 22 $\mu$ F.

### (3) Output Voltage Setting

ERROR AMP internal Standard Voltage is 0.75V.

Output Voltage is determined as seen in (5) formula

$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.75 \quad (5)$$

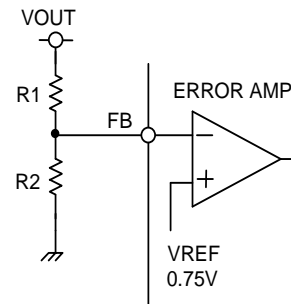


Figure 42. Output Voltage

### (4) Bootstrap Capacitor

Please connect from 0.01 $\mu$ F to 0.47 $\mu$ F (Ceramic Capacitor) between the BST pin and the LX pin.

### (5) Catch Diode

The BD9G102G-LB is designed to operate using an external catch diode between LX and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the LX pin, which is  $V_{CC\_max} + 0.5$  V. Peak current must be greater than  $I_{OUT\_max} + 1/2\Delta I_L$ . Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the power MOSFET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. It's necessary to use schottky barrier diode with the BD9G102G-LB.

### (6) Input Capacitor

The BD9G102G-LB requires an input capacitor for decoupling. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but low-ESR electrolytic capacitors may also suffice. Please place this capacitor as possible as close to the VCC pin. In the BD9G102G-LB, it is recommended a ceramic capacitor more than 2.2 $\mu$ F. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{CC\_Ripple} = \frac{I_{OUT}}{f \times C_{VCC}} \times \frac{V_{OUT}}{V_{CC}} \times \left[ 1 - \frac{V_{OUT}}{V_{CC}} \right] \quad (6)$$

Since the input capacitor ( $C_{VCC}$ ) absorbs the input switching current it requires an adequate ripple current rating. The RMS ripple current in the input capacitor can be estimated by:

$$I_{CVCC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{CC}} \times \left[ 1 - \frac{V_{OUT}}{V_{CC}} \right]} \quad (7)$$

RMS ripple current takes largest value at  $V_{CC} = 2V_{OUT}$ , where

$$I_{CVCC\_max} = \frac{I_{OUT}}{2} \quad (8)$$

**(7) External UVLO Threshold**

The high precision reset function is built in the EN pin of BD9G102G-LB, and arbitrary low-voltage malfunction prevention setup above the internal UVLO threshold is possible by connecting the EN pin to resistance divider of input voltage.

When you use, please set R3 and R4 to arbitrary UVLO threshold level( $V_{UV}$ ) and hysteresis( $V_{UVHY}$ ) like below.

$$R3 = \frac{V_{UVHY}}{I_{EN}} \quad (9)$$

$$R4 = \frac{V_{EN} \times R3}{V_{UV} - V_{EN}} \quad (10)$$

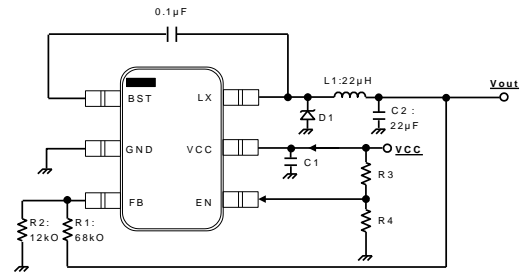


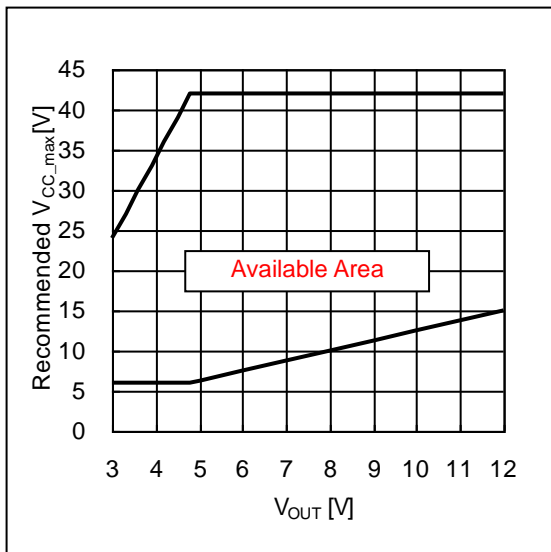
Figure 43. External UVLO Threshold Setting

$I_{EN}$ : EN pin source current 10µA(typ)       $V_{EN}$ : EN pin output on threshold 1.8V(typ)

As an example in typical sample, when VCC voltage which IC turned on 13V, hysteresis width 1V, the resistance divider set to R3=100kΩ, R4=16kΩ.

**(8) Recommended Input Voltage(vs.  $V_{OUT}$ )**

For improving the stability, it's recommended to operate BD9G102G-LB in the PWM mode. The  $V_{OUT}$  voltage operating under PWM mode is limited by minimum on time(typ: 80ns). When BD9G102G-LB operates with minimum ON time due to the large step-down ratio ( $V_{IN} \gg V_{OUT}$ ) the IC operates with PFM mode and there is possibility of oscillation depending on the setup condition. For considering the stability under PFM and PWM mode under all condition, it's recommended to set the  $V_{CC}$  smaller than  $V_{CC\_max}$ , and  $V_{CC\_max}$  is defined as below based on  $V_{OUT}$ . In case you use outside the available area, please conduct sufficient amount of operation verification in advance.



$V_{OUT}$ [V]	Recommended $V_{CC\_max}$ [V]
3.0	24
3.3	27
4.2	36
4.8	42
5.0	42
8.0	42
12.0	42

Figure 44. Recommended  $V_{CC\_max}$  vs  $V_{OUT}$

**Cautions on PCB board layout**

PCB Layout is a critical portion of good power supply design. Some paths that conduct fast current / voltage change may cause noises and degrade the power supplying performance due to leakage flux or interaction with parasitic capacitance. To help reducing these problems, the VCC pin should be bypassed to ground with a low ESR ceramic capacitor. Also, the large current is generated especially on the following 2 loops; Bypass input capacitor → Inductor → Output capacitor or Catch diode → Inductor → Output capacitor. Therefore, the distance between the output capacitor and the catch diode, or the distance between the output capacitor and the bypass input capacitor on the GND pattern should be as short as possible. The input bypass capacitor, the catch diode and the inductor should be located as close to the IC as possible. Please keep GND line on the top layer to avoid GND level fluctuation caused by external connection.

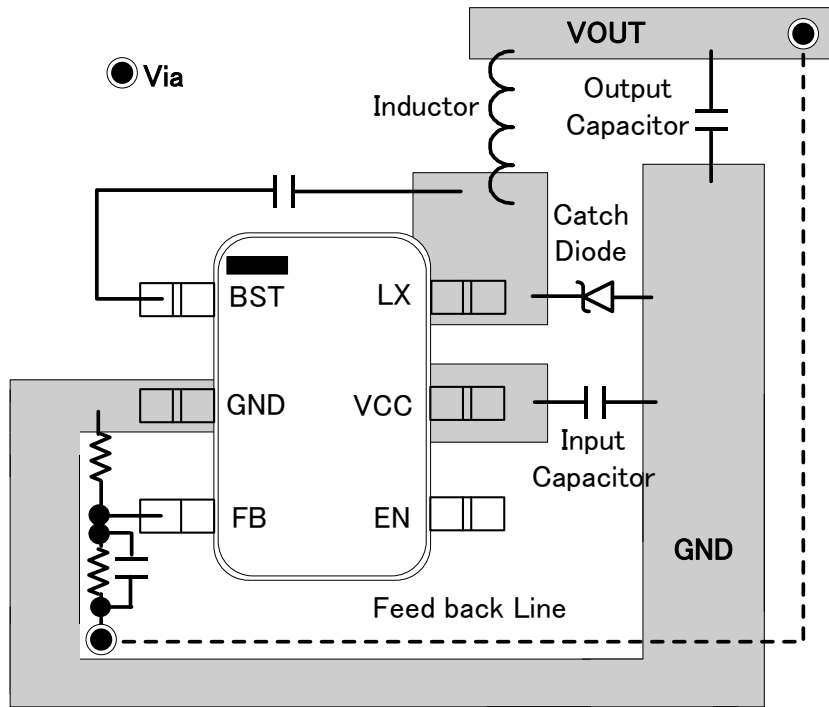


Figure 45. Reference PCB

I/O Equivalent Circuit

Pin. No	Pin Name	Pin Equivalent Circuit	Pin. No	Pin Name	Pin Equivalent Circuit
6 2 1 5	LX GND BST VCC		4	EN	
3	FB				

Figure 46. I/O Equivalent Circuit

**Operational Notes****1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

**2. Power Supply Lines**

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

**3. Ground Voltage**

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

**4. Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

**5. Recommended Operating Conditions**

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

**6. Inrush Current**

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

**7. Operation Under Strong Electromagnetic Field**

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

**8. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

**9. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

### 11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

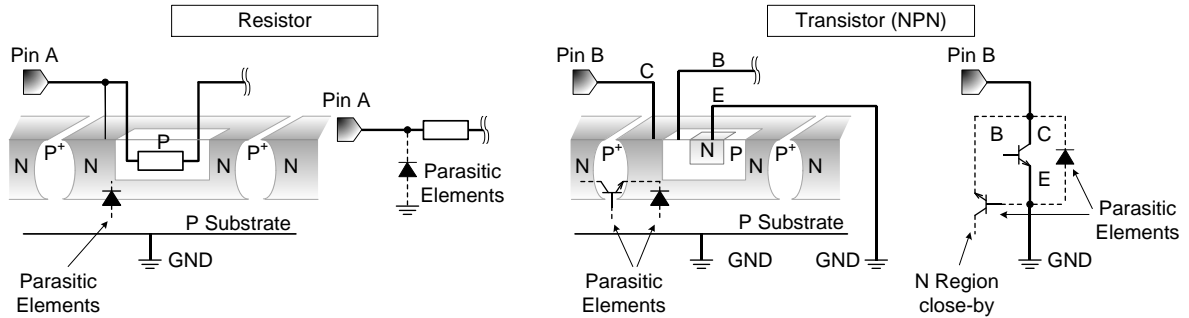


Figure 47. Example of monolithic IC structure

### 12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

### 13. Thermal Shutdown Circuit(TSD)

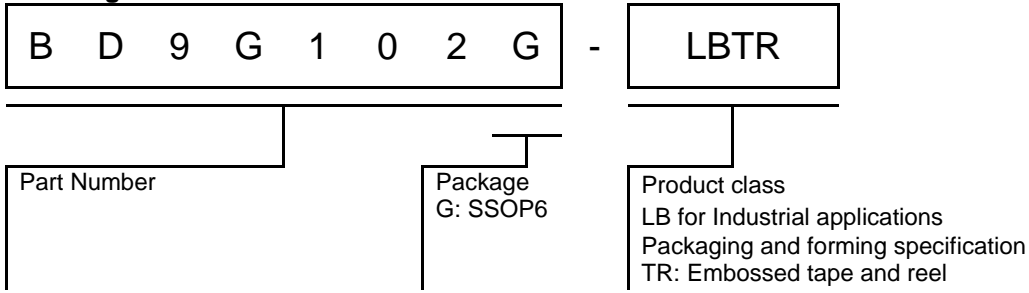
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage

### 14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information



Marking Diagram

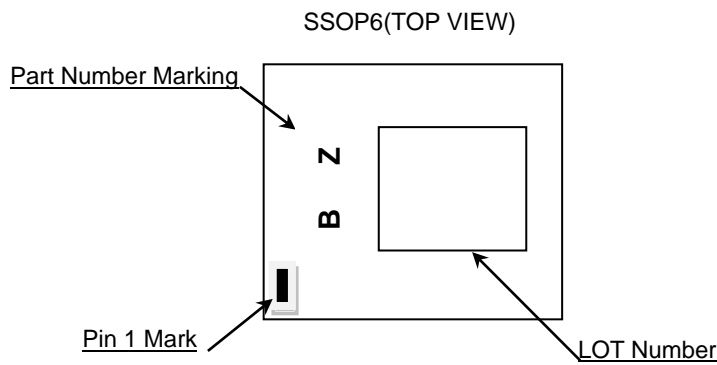
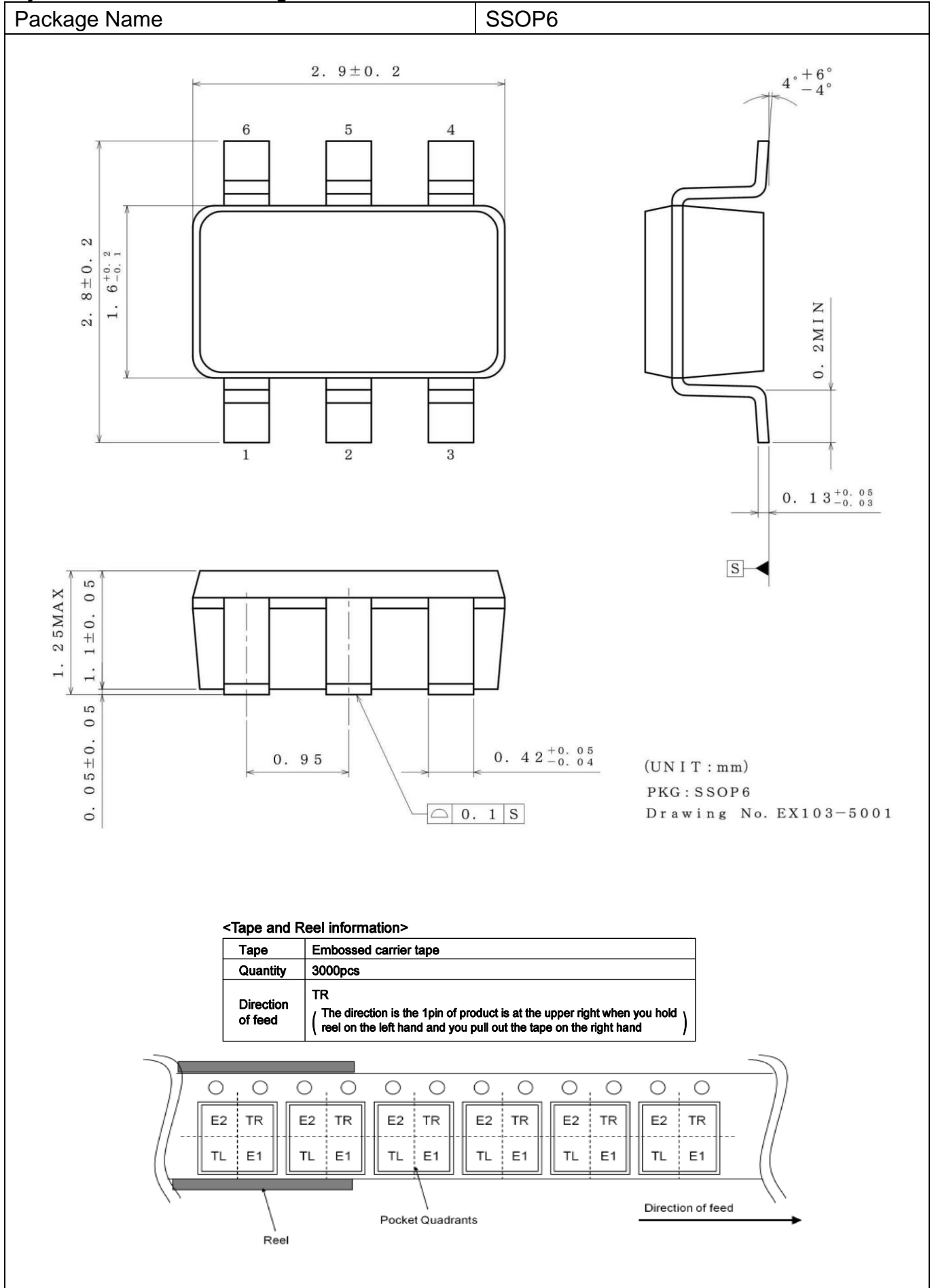


Figure 48. Marking Diagram

Physical Dimension and Packing Information



## Revision History

Date	Revision	Changes
29.Jun.2017	001	New Release
03.Dec.2021	002	<p>P1 Features: Partly changed.</p> <p>P2 Pin Description: Fixed some description.</p> <p>P2 Figure 3: Fixed the Block Diagram (added OCP block).</p> <p>P3 Changed writing: Nch FET SW → Power MOSFET (Also standardized the writing for the following part)</p> <p>P3 Description of Blocks: Partly changed the description and added the description about OCP.</p> <p>P5 Note 7 and Note 8: Partly changed the description.</p> <p>P18 Selection of Components Externally Connected (1)Inductors: Fixed and unified the symbol for inductance. Partly changed the description.</p> <p>P18 Figure 41: Fixed the typographic error: "Unvailable Area" → "Unavailable Area".</p> <p>P19 (6) Input Capacitor: Partly changed the description. "The worst case condition occurs" → "RMS ripple current takes largest value at".</p> <p>P20 (7) External UVLO Threshold: Changed writings.</p> <p>P21 Cautions on PCB board layout: Fixed some part of the description.</p> <p>P21 Figure 45: Changed figure.</p>

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