



# THE DATASHEET OF PMN20ENAX





# PMN20ENA

40 V, N-channel Trench MOSFET

30 April 2019

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic-level compatible
- Extended temperature range  $T_j = 175\text{ °C}$
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	40	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	6.2	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 6.2\text{ A}; T_j = 25\text{ °C}$	-	19	23	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<p>SC-74; TSOP6 (SOT457)</p>	<p>017aaa253</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN20ENA	SC-74; TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMN20ENA	3M

## 8. Limiting values

Table 5. Limiting values

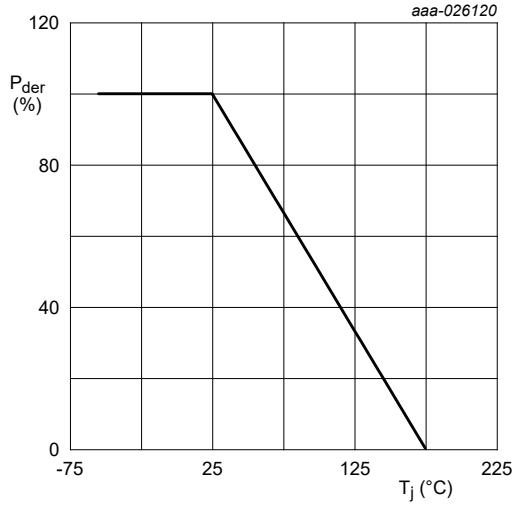
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	6.2	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	4.4	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	25	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	652	mW
			[1]	-	1.7	W
		$T_{sp} = 25\text{ °C}$		-	7.5	W
$T_j$	junction temperature			-55	175	°C
$T_{amb}$	ambient temperature			-55	175	°C
$T_{stg}$	storage temperature			-65	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	1.7	A
<b>ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	500	V
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}; I_D = 1.35\text{ A};$ DUT in avalanche (unclamped)		-	28.4	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

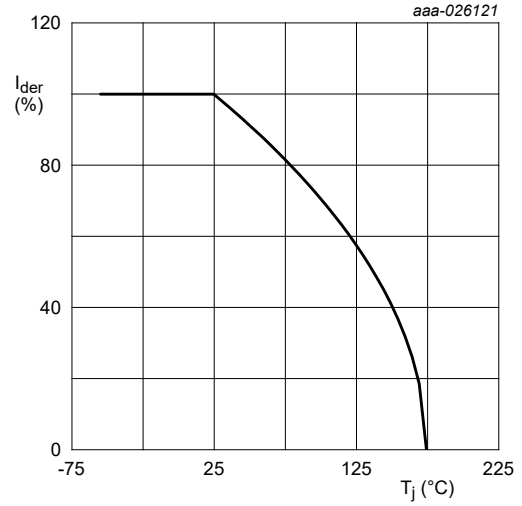
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature

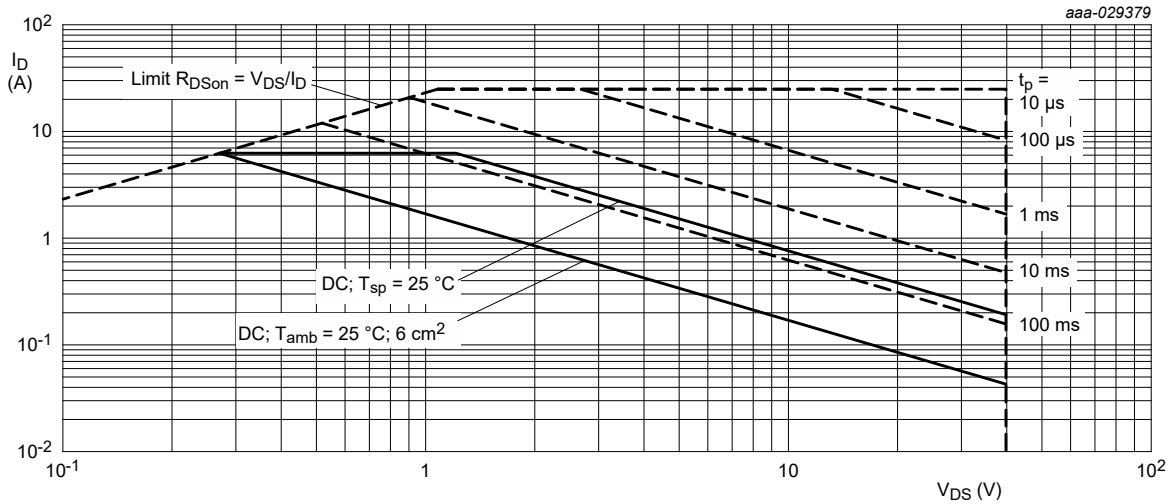


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	200	230	K/W
			[2]	-	78	90	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

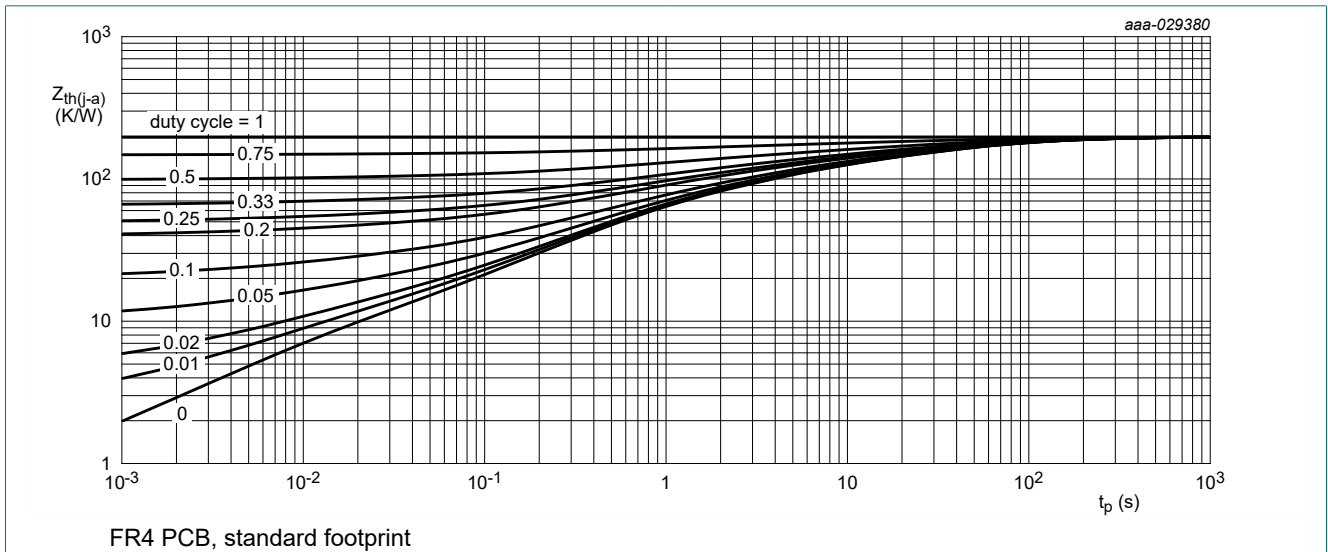


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

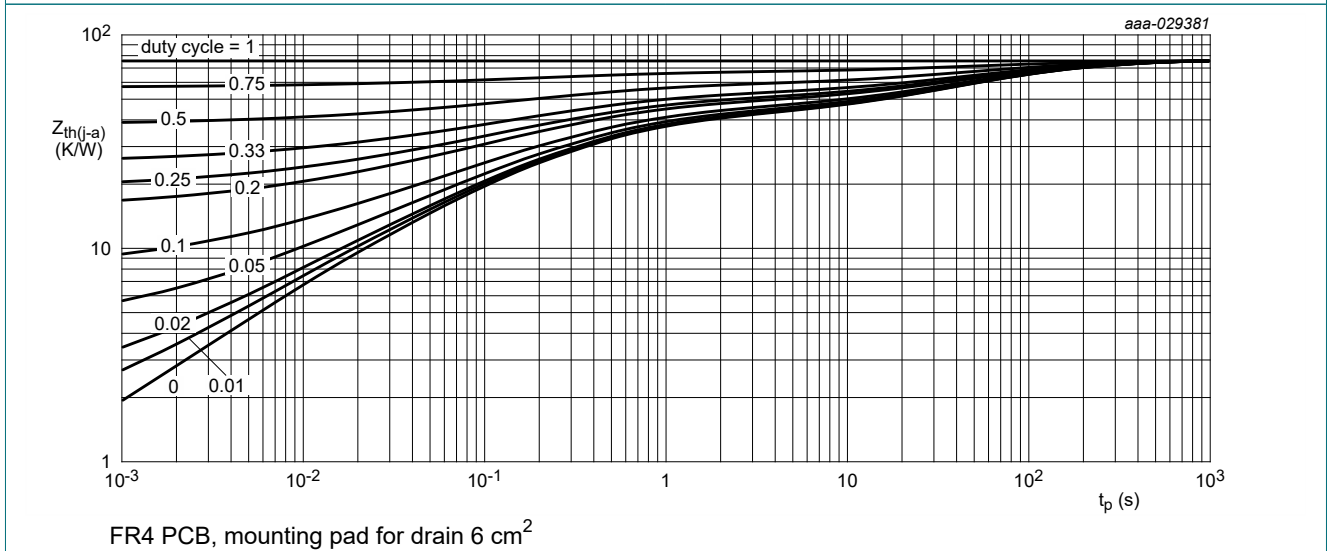


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	1.3	1.7	2.7	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	19	23	m $\Omega$
		$V_{GS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 175 \text{ }^\circ\text{C}$	-	36	44	m $\Omega$
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 5.4 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	23	30	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	33	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.8	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 20 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $V_{GS} = 10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	11	17	nC
$Q_{GS}$	gate-source charge		-	2	-	nC
$Q_{GD}$	gate-drain charge		-	2.4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 20 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	582	-	pF
$C_{oss}$	output capacitance		-	101	-	pF
$C_{rss}$	reverse transfer capacitance		-	58	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 20 \text{ V}$ ; $I_D = 6.2 \text{ A}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{G(ext)} = 6 \text{ }^\circ\Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	-
$t_r$	rise time	-		5	-	ns
$t_{d(off)}$	turn-off delay time	-		12	-	ns
$t_f$	fall time	-		5	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.7 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 2.3 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 20 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	12.8	-	ns
$Q_r$	recovered charge		-	5.4	-	nC

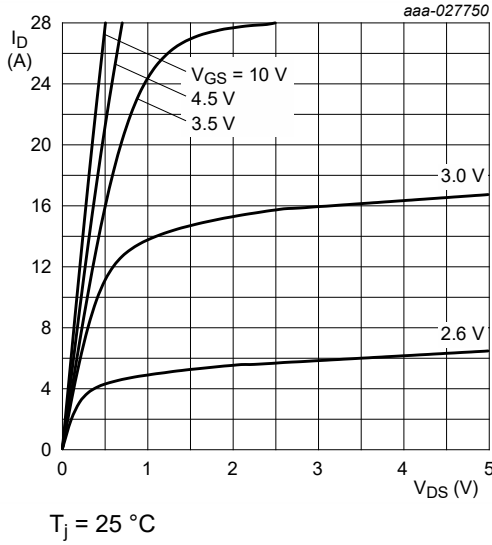


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

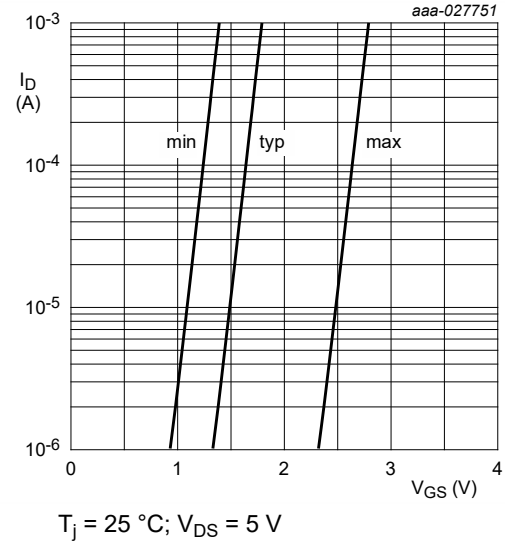


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

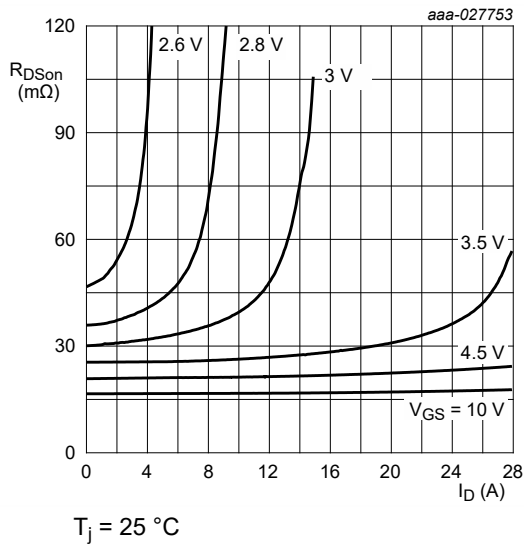


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

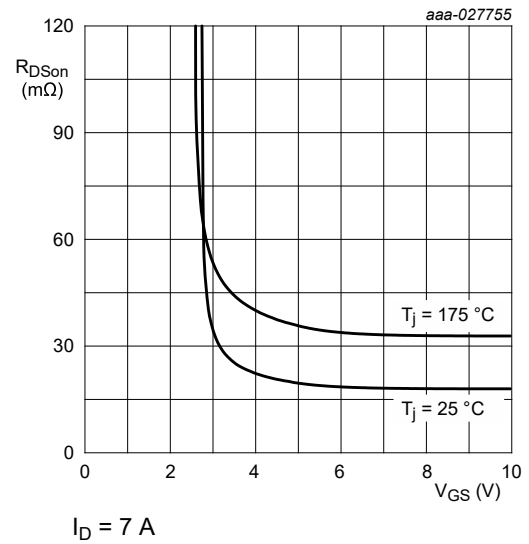
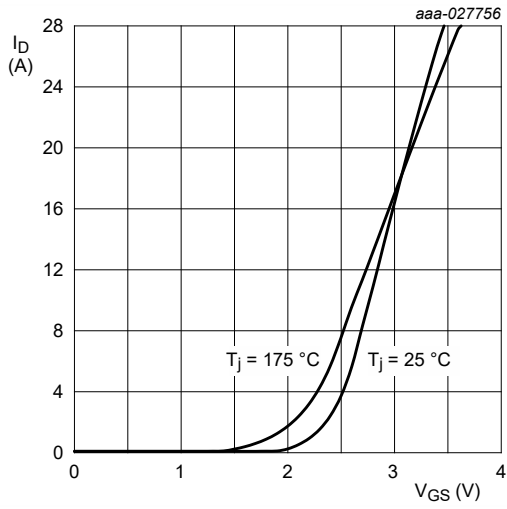
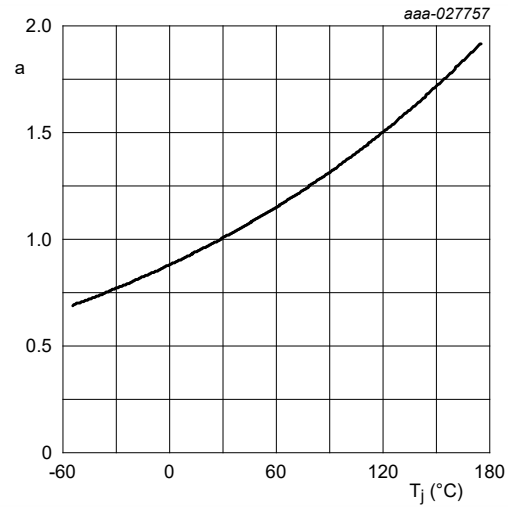


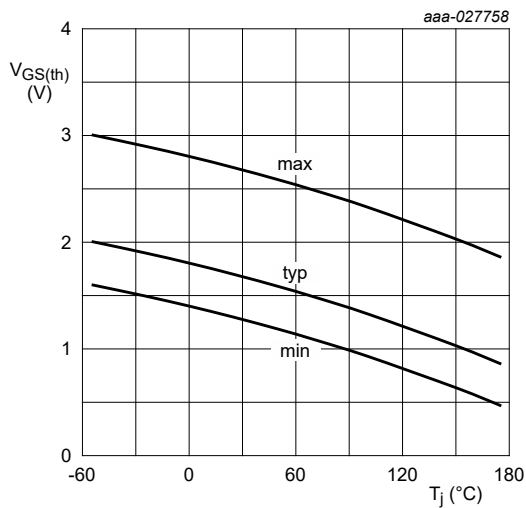
Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



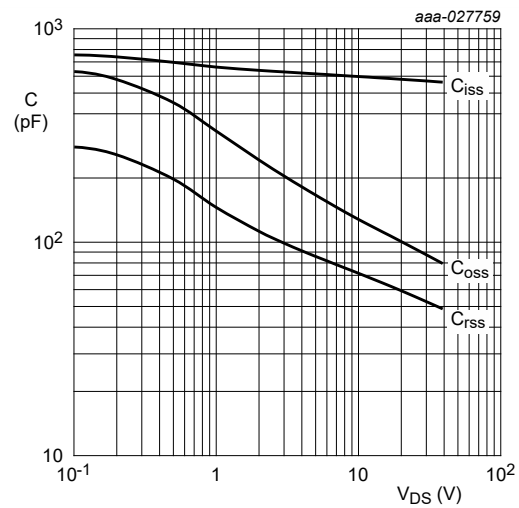
**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



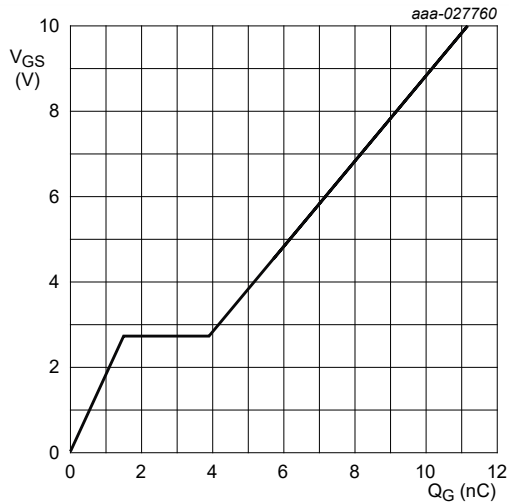
**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = 7 \text{ A}$ ;  $V_{DS} = 20 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

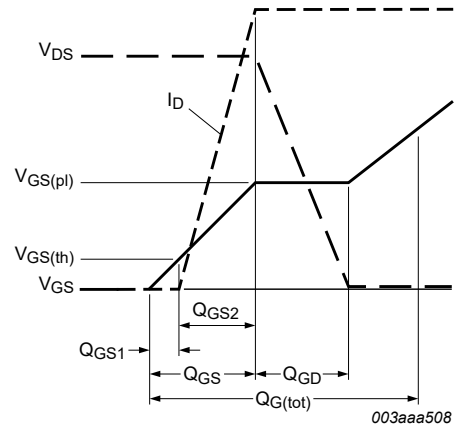
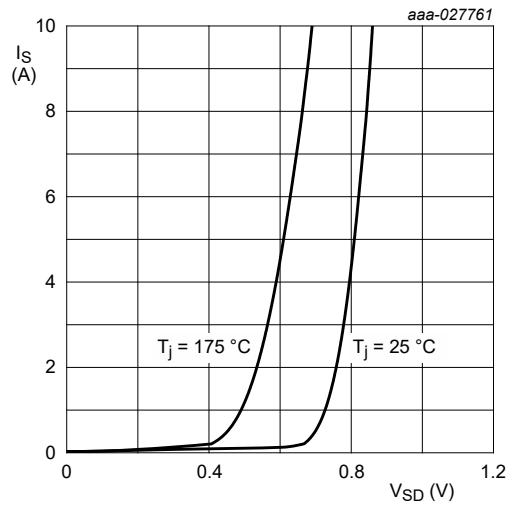


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

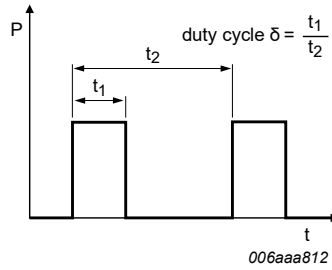


Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

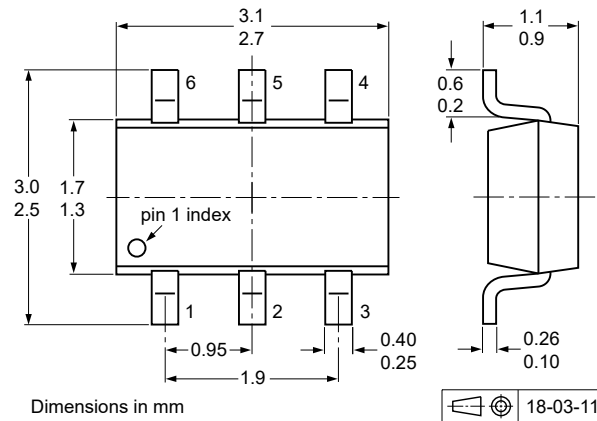


Fig. 18. Package outline SC-74; TSOP6 (SOT457)

13. Soldering

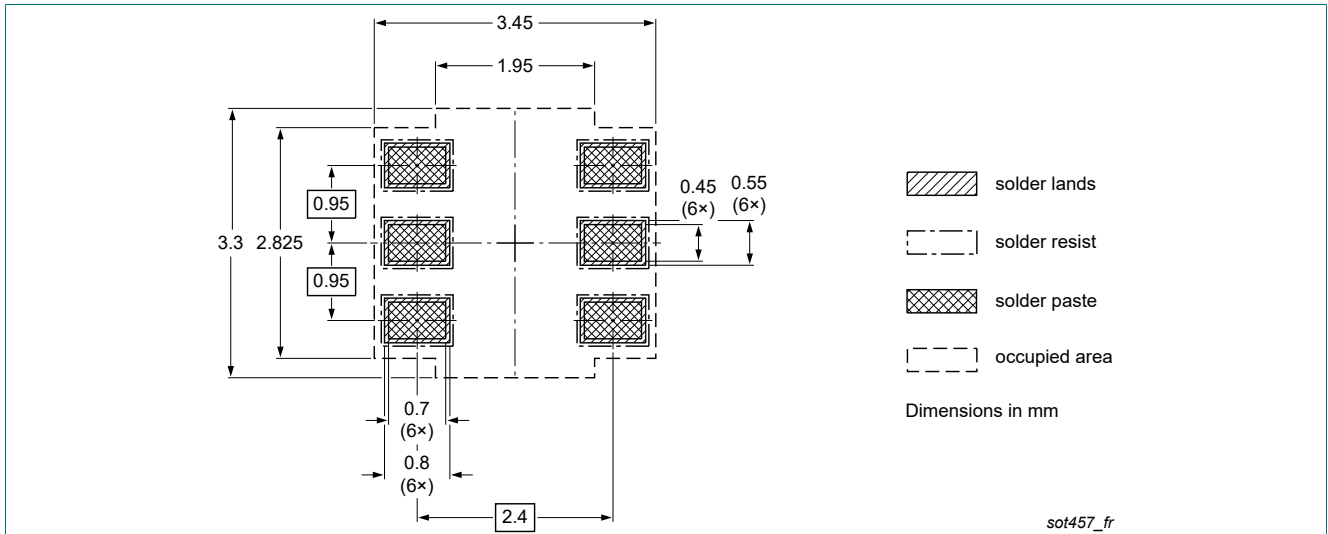


Fig. 19. Reflow soldering footprint for SC-74; TSOP6 (SOT457)

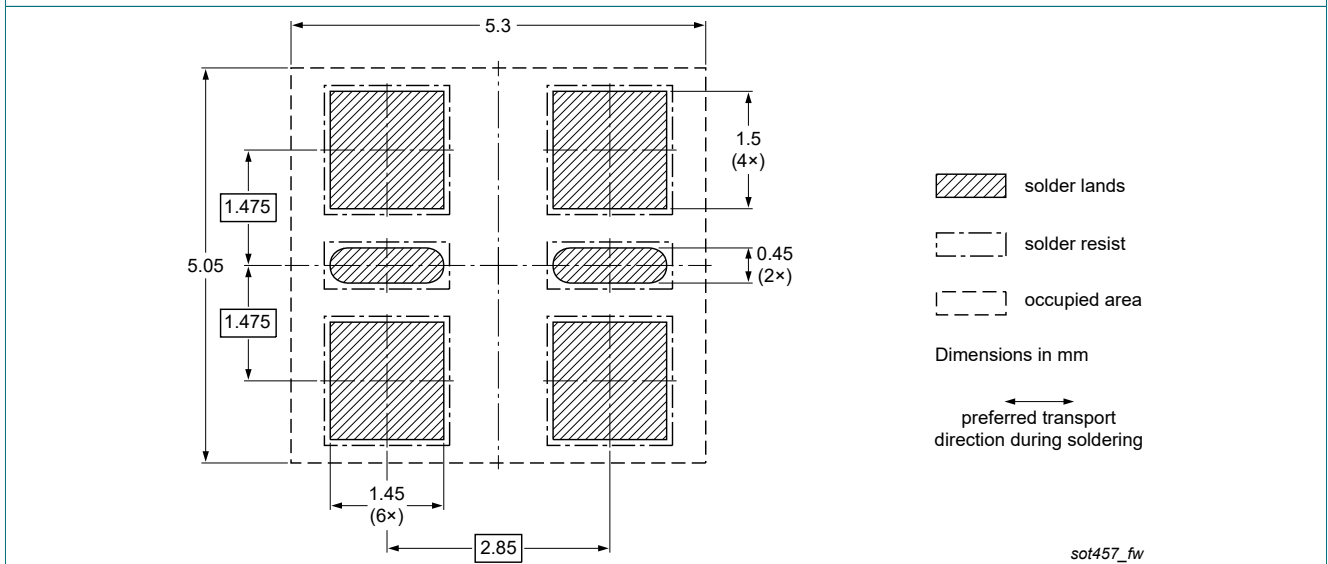


Fig. 20. Wave soldering footprint for SC-74; TSOP6 (SOT457)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN20ENA v.1	20190430	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 30 April 2019

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