



# THE DATASHEET OF TMUX8212PWR



# TMUX821x 100-V, Flat Ron, 1:1 (SPST), 4-Channel Switches with Latch-Up Immunity and 1.8-V Logic

## 1 Features

- High supply voltage capable:
  - Dual supply:  $\pm 10$  V to  $\pm 50$  V
  - Single supply: 10 V to 100 V
  - Asymmetric dual supply operation
- Consistent parametric across supply voltages
- [Latch-up immune](#)
- High continuous current: 200 mA
- Low crosstalk:  $-110$  dB
- Low input leakage: 10 pA
- Low On-Resistance flatness:  $0.05 \Omega$
- Low On-Resistance:  $5 \Omega$
- Low capacitance: 12 pF
- Removes need for additional logic rail ( $V_L$ )
- [1.8-V Logic capable](#)
- [Fail-safe logic: up to 48 V independent of supply](#)
- [Integrated Pull-Down resistor on logic pins](#)
- [Bidirectional signal path](#)
- Wide operating temperature  $T_A$ :  $-40^\circ\text{C}$  to  $125^\circ\text{C}$
- Industry-standard TSSOP and smaller WQFN packages

## 2 Applications

- High voltage bidirectional switching
- Analog and digital signal switching
- [Semiconductor test equipment](#)
- [LCD test equipment](#)
- [Battery test equipment](#)
- [Data acquisition systems \(DAQ\)](#)
- [Digital multi-meter \(DMM\)](#)
- [Factory automation and control](#)
- [Programmable logic controllers \(PLC\)](#)
- [Analog input modules](#)

## 3 Description

The TMUX8211, TMUX8212, and TMUX8213 are modern high voltage capable analog switches with Latch-Up immunity. Each device has four independently controllable 1:1, single-pole single-throw (SPST) switch channels. The devices work well with dual supplies, a single supply, or asymmetric supplies up to a maximum supply voltage of 100 V. The TMUX821x devices provide consistent analog parametric performance across the entire supply voltage range. The TMUX821x family supports bidirectional analog and digital signals on the source ( $S_x$ ) and drain ( $D_x$ ) pins.

All logic inputs support logic levels of 1.8 V, 3.3 V, and 5 V and can be connected as high as 48 V, allowing for system flexibility with control signal voltage. Fail-safe logic circuitry allows voltages on the logic pins to be applied before the supply pin, protecting the device from potential damage.

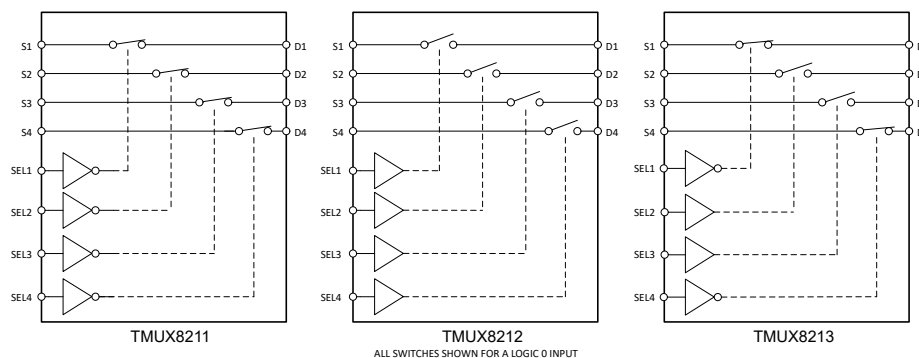
The device family provides Latch-Up immunity, preventing undesirable high current events between parasitic structures within the device. A Latch-Up condition typically continues until the power supply rails are turned off and can lead to device failure. The Latch-Up immunity feature allows this family of multiplexers to be used in harsh environments.

### Package Information<sup>(1) (2)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX8211	PW (TSSOP, 16)	5.00 mm × 4.40 mm
TMUX8212	RUM (WQFN, 16)	4.00 mm × 4.00 mm
TMUX8213		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) See the [Device Comparison Table](#).



**Functional Block Diagram**



## Table of Contents

<b>1 Features</b> .....	1	8.4 Device Turn-On and Turn-Off Time.....	19
<b>2 Applications</b> .....	1	8.5 Charge Injection.....	20
<b>3 Description</b> .....	1	8.6 Off Isolation.....	20
<b>4 Revision History</b> .....	2	8.7 Crosstalk.....	21
<b>5 Device Comparison Table</b> .....	3	8.8 Bandwidth.....	21
<b>6 Pin Configuration and Functions</b> .....	3	8.9 THD + Noise.....	22
<b>7 Specifications</b> .....	4	<b>9 Detailed Description</b> .....	23
7.1 Absolute Maximum Ratings: TMUX821x Devices.....	4	9.1 Overview.....	23
7.2 ESD Ratings.....	4	9.2 Functional Block Diagram.....	23
7.3 Recommended Operating Conditions:		9.3 Feature Description.....	23
TMUX821x Devices.....	4	9.4 Device Functional Modes.....	25
7.4 Source of Drain Continuous Current.....	5	<b>10 Application and Implementation</b> .....	26
7.5 Source of Drain Pulse Current.....	5	10.1 Application Information.....	26
7.6 Thermal Information.....	6	10.2 Typical Application.....	26
7.7 Electrical Characteristics (Global): TMUX821x		<b>11 Power Supply Recommendations</b> .....	28
Devices.....	6	<b>12 Layout</b> .....	29
7.8 Electrical Characteristics (±15-V Dual Supply).....	7	12.1 Layout Guidelines.....	29
7.9 Electrical Characteristics (±36-V Dual Supply).....	8	12.2 Layout Example.....	29
7.10 Electrical Characteristics (±50-V Dual Supply).....	9	<b>13 Device and Documentation Support</b> .....	30
7.11 Electrical Characteristics (72-V Single Supply).....	10	13.1 Documentation Support.....	30
7.12 Electrical Characteristics (100-V Single Supply).....	11	13.2 Receiving Notification of Documentation Updates.....	30
7.13 Switching Characteristics: TMUX821x Devices.....	12	13.3 Support Resources.....	30
7.14 Typical Characteristics.....	13	13.4 Trademarks.....	30
<b>8 Parameter Measurement Information</b> .....	18	13.5 Electrostatic Discharge Caution.....	30
8.1 On-Resistance.....	18	13.6 Glossary.....	30
8.2 Off-Leakage Current.....	18	<b>14 Mechanical, Packaging, and Orderable</b>	
8.3 On-Leakage Current.....	19	<b>Information</b> .....	30

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2021) to Revision B (March 2023)	Page
• Changed the status of the RUM package from: <i>preview</i> to: <i>active</i> .....	1

Changes from Revision * (October 2021) to Revision A (December 2021)	Page
• Changed the status of the data sheet from: <i>Advanced Information</i> to: <i>Production Data</i> .....	1

## 5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX8211	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic Low)
TMUX8212	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic High)
TMUX8213	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic Low + Logic High)

## 6 Pin Configuration and Functions

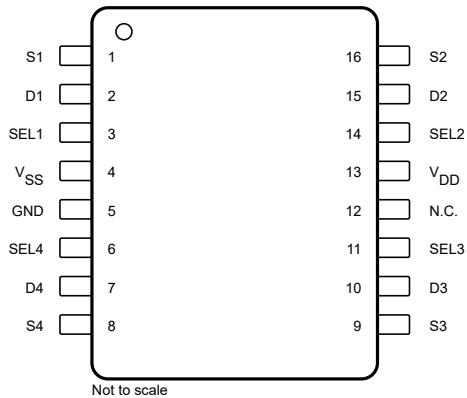


Figure 6-1. PW Package, 16-Pin TSSOP (Top View)

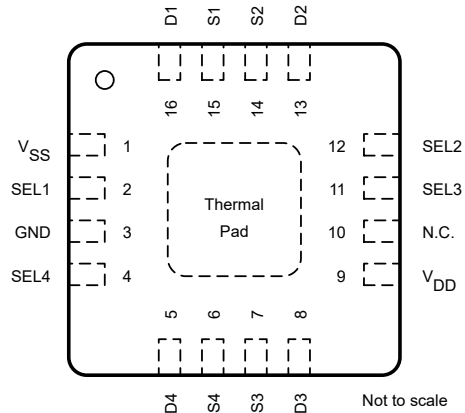


Figure 6-2. RUM Package, 16-Pin WQFN (Top View)

Table 6-1. Pin Functions

PIN			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	TSSOP	WQFN		
D1	2	16	I/O	Drain pin 1. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
GND	5	3	P	Ground (0 V) reference
S1	1	15	I/O	Source pin 1. Can be an input or output.
S2	16	14	I/O	Source pin 2. Can be an input or output.
S3	9	7	I/O	Source pin 3. Can be an input or output.
S3	9	7	I/O	Source pin 3. Can be an input or output.
S4	8	6	I/O	Source pin 4. Can be an input or output.
SEL1	3	2	I	Logic control input 1.
SEL2	14	12	I	Logic control input 2.
SEL3	11	11	I	Logic control input 3.
SEL4	6	4	I	Logic control input 4.
N.C.	12	10	—	No internal connection.
V <sub>DD</sub>	13	9	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 1 μF to 10 μF between V <sub>DD</sub> and GND.
V <sub>SS</sub>	4	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 1 μF to 10 μF between V <sub>SS</sub> and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or V <sub>SS</sub> for best performance.

(1) I = input, O = output, I/O = input and output, P = power

## 7 Specifications

### 7.1 Absolute Maximum Ratings: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{DD}-V_{SS}$	Supply voltage		110	V
$V_{DD}$		-0.5	110	V
$V_{SS}$		-110	0.5	V
$V_{SELx}$	Logic control input pin voltage (SELx)	-0.5	50	V
$I_{SELx}$	Logic control input pin current (SELx)	-30	30	mA
$V_S$ or $V_D$	Source or drain voltage (Sx, Dx)	$V_{SS}-2$	$V_{DD}+2$	V
$I_{DC}$	Source or drain continuous current (Sx, Dx)	-200	200	mA
$I_{IK}$ <sup>(2)</sup>	Diode clamp current at 85°C	-100	100	mA
	Diode clamp current at 125°C	-15	15	mA
$T_{stg}$	Storage temperature	-65	150	°C
$T_A$	Ambient temperature	-55	150	°C
$T_J$	Junction temperature		150	°C
$P_{tot}$ <sup>(3)</sup>	Total power dissipation (QFN)		1680	mW
$P_{tot}$ <sup>(4)</sup>	Total power dissipation (TSSOP)		720	mW

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Signal path pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) For QFN package:  $P_{tot}$  derates linearly above  $T_A = 70^\circ\text{C}$  by 24.0 mW/°C
- (4) For TSSOP package:  $P_{tot}$  derates linearly above  $T_A = 70^\circ\text{C}$  by 10.5 mW/°C

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ <sup>(1)</sup>	Power supply voltage differential	10		100	V
$V_{DD}$	Positive power supply voltage	10		100	V
$V_S$ or $V_D$ <sup>(2)</sup>	Signal path input/output voltage (source or drain pin)	$V_{SS}$		$V_{DD}$	V
$V_{SEL}$	Logic input pin voltage	0		48	V
$T_A$	Ambient temperature	-40		125	°C
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, D)			$I_{DC}$ <sup>(3)</sup>	mA

- (1)  $V_{DD}$  and  $V_{SS}$  can be any value as long as  $10\text{ V} \leq (V_{DD} - V_{SS}) \leq 100\text{ V}$ , and the minimum  $V_{DD}$  is met.
- (2)  $V_S$  or  $V_D$  is the voltage on any Source or Drain pins.
- (3) Refer to *Source or Drain Continuous Current* table for  $I_{DC}$  specifications.

## 7.4 Source of Drain Continuous Current

over operating free-air temperature range (unless otherwise noted)

	Package		MIN	NOM	MAX	UNIT
$I_{DC}$ 1 ch <sup>(1)</sup>	PW (TSSOP) RUM (WQFN)	Continuous current through switch for 1 channel	$T_A = 25^\circ\text{C}$		200	mA
			$T_A = 85^\circ\text{C}$		200	
			$T_A = 125^\circ\text{C}$		200	
$I_{DC}$ All ch <sup>(2)</sup>	PW (TSSOP)	Continuous current through switch on all channels at the same time	$T_A = 25^\circ\text{C}$		185	mA
			$T_A = 85^\circ\text{C}$		125	
			$T_A = 125^\circ\text{C}$		65	
$I_{DC}$ All ch <sup>(2)</sup>	RUM (WQFN)	Continuous current through switch on all channels at the same time	$T_A = 25^\circ\text{C}$		200	mA
			$T_A = 85^\circ\text{C}$		190	
			$T_A = 125^\circ\text{C}$		100	

(1) Max continuous current shown for a single channel at a time.

(2) Max continuous current shown for all channels at a time. Refer to max power dissipation ( $P_{tot}$ ) to ensure package limitations are not violated.

## 7.5 Source of Drain Pulse Current

over operating free-air temperature range (unless otherwise noted)

	Package		MIN	NOM	MAX	UNIT
$I_{DC}$ 1 ch <sup>(1)</sup>	PW (TSSOP)	Pulse <sup>(3)</sup> current through switch on 1 channel	$T_A = 25^\circ\text{C}$		370	mA
			$T_A = 85^\circ\text{C}$		310	
			$T_A = 125^\circ\text{C}$		240	
$I_{DC}$ All ch <sup>(2)</sup>	PW (TSSOP)	Pulse <sup>(3)</sup> current through switch on all channels at the same time	$T_A = 25^\circ\text{C}$		185	mA
			$T_A = 85^\circ\text{C}$		155	
			$T_A = 125^\circ\text{C}$		120	
$I_{DC}$ 1 ch <sup>(1)</sup>	RUM (WQFN)	Pulse <sup>(3)</sup> current through switch on 1 channel	$T_A = 25^\circ\text{C}$		560	mA
			$T_A = 85^\circ\text{C}$		470	
			$T_A = 125^\circ\text{C}$		365	
$I_{DC}$ All ch <sup>(2)</sup>	RUM (WQFN)	Pulse <sup>(3)</sup> current through switch on all channels at the same time	$T_A = 25^\circ\text{C}$		280	mA
			$T_A = 85^\circ\text{C}$		235	
			$T_A = 125^\circ\text{C}$		180	

(1) Max continuous current shown for a single channel at a time.

(2) Max continuous current shown for all channels at a time. Refer to max power dissipation ( $P_{tot}$ ) to ensure package limitations are not violated.

(3) Pulsed at 1 ms, 10% duty cycle

## 7.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX821x	TMUX821x	UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	25.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.7	16.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.2	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	42.0	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics (Global): TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)  
typical at  $V_{DD} = +36\text{ V}$ ,  $V_{SS} = -36\text{ V}$ ,  $GND = 0\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>LOGIC INPUTS</b>							
$V_{IH}$	Logic voltage high		$-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.3		48	V
$V_{IL}$	Logic voltage low		$-40^\circ\text{C}$ to $+125^\circ\text{C}$	0		0.8	V
$I_{IH}$	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.4	3.8	$\mu\text{A}$
$I_{IL}$	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	-0.2	-0.005		$\mu\text{A}$
$C_{IN}$	Logic input capacitance		$-40^\circ\text{C}$ to $+125^\circ\text{C}$		3		pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	Logic inputs = 0 V, 5 V, or 48 V	$25^\circ\text{C}$		350	800	$\mu\text{A}$
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			800	$\mu\text{A}$
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			900	$\mu\text{A}$
$I_{SS}$	$V_{SS}$ supply current	Logic inputs = 0 V, 5 V, or 48 V	$25^\circ\text{C}$		350	800	$\mu\text{A}$
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			800	$\mu\text{A}$
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			900	$\mu\text{A}$

## 7.8 Electrical Characteristics ( $\pm 15$ -V Dual Supply)

 $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

 Typical at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = -10\text{ V to }+10\text{ V}$ $I_D = -10\text{ mA}$	25°C		5	7	$\Omega$
			-40°C to +85°C			8	
			-40°C to +125°C			10	
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = -10\text{ V to }+10\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.2	0.3	$\Omega$
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = -10\text{ V to }+10\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.07		$\Omega$
$R_{ON\ DRIFT}$	On-resistance drift	$V_S = 0\text{ V}$ , $I_S = -10\text{ mA}$	-40°C to +125°C		0.03		$\Omega/^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Switch state is off $V_S = +10\text{ V} / -10\text{ V}$ $V_D = -10\text{ V} / +10\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Switch state is off $V_S = +10\text{ V} / -10\text{ V}$ $V_D = -10\text{ V} / +10\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current <sup>(2)</sup>	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Switch state is on $V_S = V_D = \pm 10\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-1	1	
			-40°C to +125°C		-2	2	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels <sup>(2)</sup>	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Switch state is on $V_S = V_D = \pm 10\text{ V}$	25°C		5		pA
			85°C		35		
			125°C		120		

(1) When  $V_S$  is positive,  $V_D$  is negative. And when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating. And when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 7.9 Electrical Characteristics (±36-V Dual Supply)

$V_{DD} = +36\text{ V} \pm 10\%$ ,  $V_{SS} = -36\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = -25\text{ V to }+25\text{ V}$ $I_D = -10\text{ mA}$	25°C		5	7	$\Omega$
			-40°C to +85°C			8	
			-40°C to +125°C			10	
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = -25\text{ V to }+25\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.1	0.3	$\Omega$
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = -25\text{ V to }+25\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.12		$\Omega$
$R_{ON\ DRIFT}$	On-resistance drift	$V_S = 0\text{ V}$ , $I_S = -10\text{ mA}$	-40°C to +125°C		0.03		$\Omega/^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = -39.6\text{ V}$ Switch state is off $V_S = +25\text{ V / }-25\text{ V}$ $V_D = -25\text{ V / }+25\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = -39.6\text{ V}$ Switch state is off $V_S = +25\text{ V / }-25\text{ V}$ $V_D = -25\text{ V / }+25\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current <sup>(2)</sup>	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = -39.6\text{ V}$ Switch state is on $V_S = V_D = \pm 25\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-1	1	
			-40°C to +125°C		-2	2	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels <sup>(2)</sup>	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = -39.6\text{ V}$ Switch state is on $V_S = V_D = \pm 25\text{ V}$	25°C		5		pA
			85°C		35		
			125°C		120		

(1) When  $V_S$  is positive,  $V_D$  is negative. And when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating. And when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 7.10 Electrical Characteristics ( $\pm 50$ -V Dual Supply)

 $V_{DD} = +50$  V,  $V_{SS} = -50$  V, GND = 0 V (unless otherwise noted)

 Typical at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = -45$ V to 45 V $I_D = -10$ mA	25°C		5	7	$\Omega$
			-40°C to +85°C			8	
			-40°C to +125°C			10	
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = -45$ V to 45 V $I_D = -10$ mA	25°C		0.2	0.3	$\Omega$
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = -45$ V to 45 V $I_D = -10$ mA	25°C		0.13		$\Omega$
$R_{ON\ DRIFT}$	On-resistance drift	$V_S = 0$ V, $I_S = -10$ mA	-40°C to +125°C		0.03		$\Omega/^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 50$ V, $V_{SS} = -50$ V Switch state is off $V_S = +45$ V / -45 V $V_D = -45$ V / +45 V	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	$V_{DD} = 50$ V, $V_{SS} = -50$ V Switch state is off $V_S = +45$ V / -45 V $V_D = -45$ V / +45 V	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current <sup>(2)</sup>	$V_{DD} = 50$ V, $V_{SS} = -50$ V Switch state is on $V_S = V_D = \pm 45$ V	25°C		0.01		nA
			-40°C to +85°C		-2	2	
			-40°C to +125°C		-5	5	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels <sup>(2)</sup>	$V_{DD} = 50$ V, $V_{SS} = -50$ V Switch state is on $V_S = V_D = \pm 45$ V	25°C		10		pA
			85°C		50		
			125°C		220		

(1) When  $V_S$  is positive,  $V_D$  is negative. And when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating. And when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 7.11 Electrical Characteristics (72-V Single Supply)

$V_{DD} = +72\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }60\text{ V}$ $I_D = -10\text{ mA}$	25°C		5	7	$\Omega$
			-40°C to +85°C			8	
			-40°C to +125°C			10	
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = 0\text{ V to }60\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.2	0.3	$\Omega$
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = 0\text{ V to }60\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.05		$\Omega$
$R_{ON\ DRIFT}$	On-resistance drift	$V_S = 0\text{ V}$ , $I_S = -10\text{ mA}$	-40°C to +125°C		0.03		$\Omega/^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	Switch state is off $V_S = +60\text{ V} / 1\text{ V}$ $V_D = 1\text{ V} / +60\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	Switch state is off $V_S = +60\text{ V} / 1\text{ V}$ $V_D = 1\text{ V} / +60\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current <sup>(2)</sup>	Switch state is on $V_S = V_D = 1\text{ V} / +60\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-2	2	
			-40°C to +125°C		-5	5	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels <sup>(2)</sup>	Switch state is on $V_S = V_D = 1\text{ V} / +60\text{ V}$	25°C		15		pA
			85°C		75		
			125°C		300		

(1) When  $V_S$  is 60 V,  $V_D$  is 1 V. Or when  $V_S$  is 1 V,  $V_D$  is 60 V.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating. Or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 7.12 Electrical Characteristics (100-V Single Supply)

 $V_{DD} = +100\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

 Typical at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }+95\text{ V}$ $I_D = -10\text{ mA}$	25°C		5	7	$\Omega$
			-40°C to +85°C			8	
			-40°C to +125°C			10	
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = 0\text{ V to }+95\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.2	0.3	$\Omega$
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = 0\text{ V to }+95\text{ V}$ $I_D = -10\text{ mA}$	25°C		0.07		$\Omega$
$R_{ON\ DRIFT}$	On-resistance drift	$V_S = 50\text{ V}$ , $I_S = -10\text{ mA}$	-40°C to +125°C		0.03		$\Omega/^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	Switch state is off $V_S = +95\text{ V} / 1\text{ V}$ $V_D = 1\text{ V} / +95\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{D(OFF)}$	Drain off leakage current <sup>(1)</sup>	Switch state is off $V_S = +95\text{ V} / 1\text{ V}$ $V_D = 1\text{ V} / +95\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-40	40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current <sup>(2)</sup>	Switch state is on $V_S = V_D = 1\text{ V} / +95\text{ V}$	25°C		0.01		nA
			-40°C to +85°C		-4	4	
			-40°C to +125°C		-10	10	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels <sup>(2)</sup>	Switch state is on $V_S = V_D = 1\text{ V} / +95\text{ V}$	25°C		15		pA
			85°C		100		
			125°C		450		

(1) When  $V_S$  is 95 V,  $V_D$  is 1 V. Or when  $V_S$  is 1 V,  $V_D$  is 95 V.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating. Or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

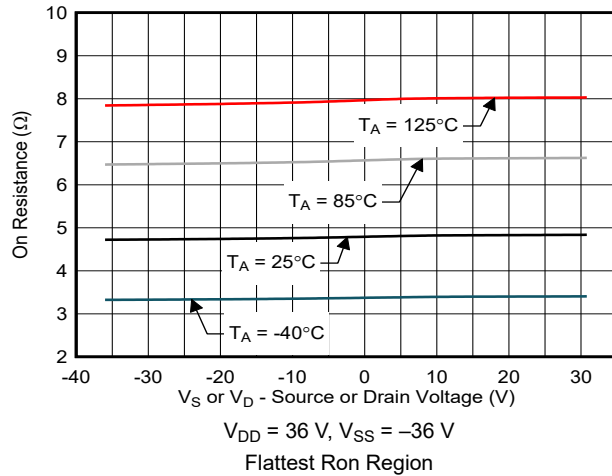
### 7.13 Switching Characteristics: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)  
 typical at  $V_{DD} = +36\text{ V}$ ,  $V_{SS} = -36\text{ V}$ ,  $GND = 0\text{ V}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

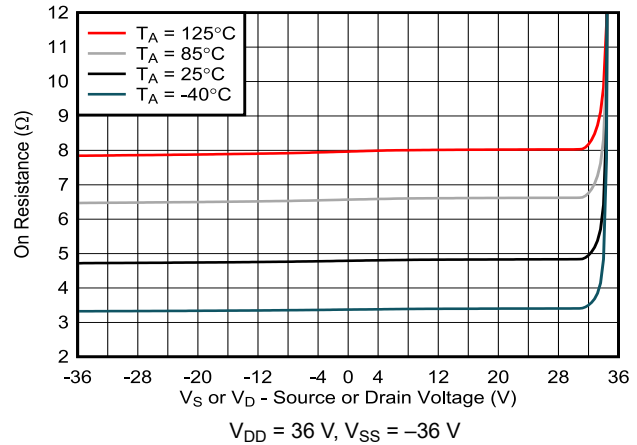
PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{ON(EN)}$	Turn-on time from enable	$V_S = 10\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 15\text{ pF}$	25°C		4		$\mu\text{s}$
			-40°C to +85°C			10	
			-40°C to +125°C			12	
$t_{OFF(EN)}$	Turn-off time from enable	$V_S = 10\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 15\text{ pF}$	25°C		100		ns
			-40°C to +85°C			600	
			-40°C to +125°C			700	
$t_{ON(VDD)}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ ramp rate = 1 V/ $\mu\text{s}$ , $V_S = 10\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 15\text{ pF}$	25°C		60		$\mu\text{s}$
$t_{PD}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	25°C		190		ps
$Q_{INJ}$	Charge injection	$V_S = (V_{DD} + V_{SS}) / 2$ , $C_L = 1\text{ nF}$	25°C		-1.3		nC
$O_{ISO}$	Off isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = (V_{DD} + V_{SS}) / 2$ , $f = 100\text{ kHz}$	25°C		-110		dB
$X_{TALK}$	Inter-channel crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = (V_{DD} + V_{SS}) / 2$ , $f = 100\text{ kHz}$	25°C		-110		dB
BW	-3 dB bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = (V_{DD} + V_{SS}) / 2$	25°C		420		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = (V_{DD} + V_{SS}) / 2$ , $f = 1\text{ MHz}$	25°C		-0.4		dB
THD+N	Total harmonic distortion + Noise	Dual supply voltage $V_{PP} = 5\text{ V}$ , $V_{BIAS} = (V_{DD} + V_{SS}) / 2$ $R_L = 1\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz to } 20\text{ kHz}$	25°C		0.0008		%
$C_{S(OFF)}$	Source off capacitance	$V_S = (V_{DD} + V_{SS}) / 2\text{ V}$ , $f = 1\text{ MHz}$	25°C		12		pF
$C_{D(OFF)}$	Drain off capacitance	$V_S = (V_{DD} + V_{SS}) / 2\text{ V}$ , $f = 1\text{ MHz}$	25°C		12		pF
$C_{S(ON)}$ , $C_{D(ON)}$	On capacitance	$V_S = (V_{DD} + V_{SS}) / 2\text{ V}$ , $f = 1\text{ MHz}$	25°C		14		pF

### 7.14 Typical Characteristics

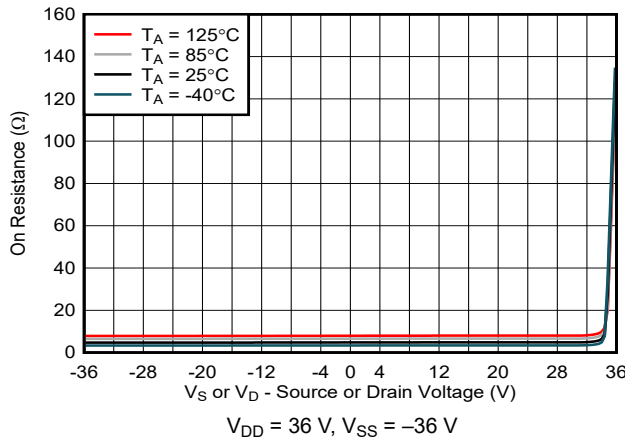
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +36\text{ V}$ , and  $V_{SS} = -36\text{ V}$  (unless otherwise noted)



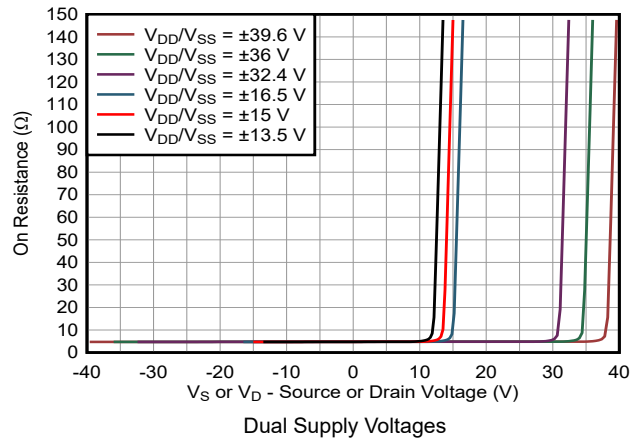
**Figure 7-1. On-Resistance vs Source or Drain Voltage**



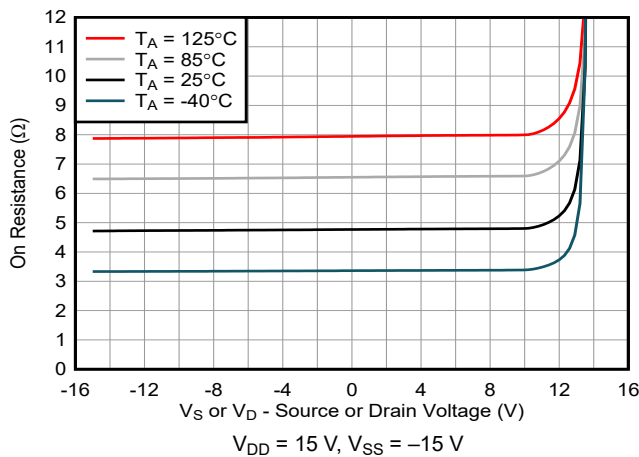
**Figure 7-2. On-Resistance vs Source or Drain Voltage**



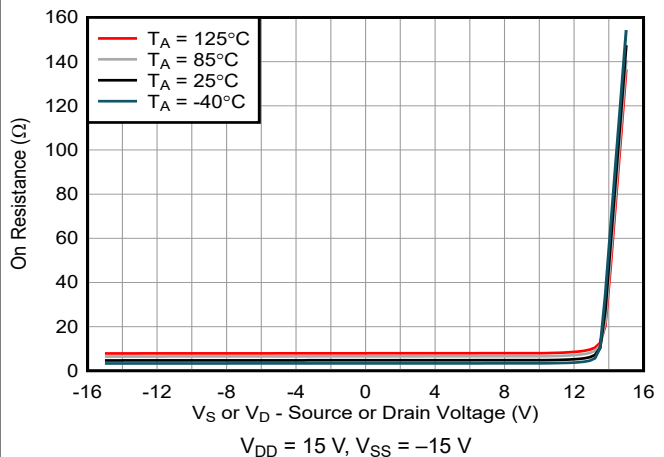
**Figure 7-3. On-Resistance vs Source or Drain Voltage**



**Figure 7-4. On-Resistance vs Source or Drain Voltage**



**Figure 7-5. On-Resistance vs Source or Drain Voltage**



**Figure 7-6. On-Resistance vs Source or Drain Voltage**

## 7.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +36\text{ V}$ , and  $V_{SS} = -36\text{ V}$  (unless otherwise noted)

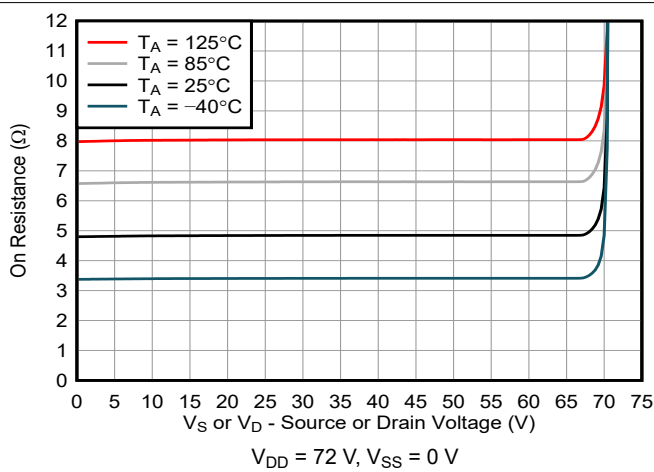


Figure 7-7. On-Resistance vs Source or Drain Voltage

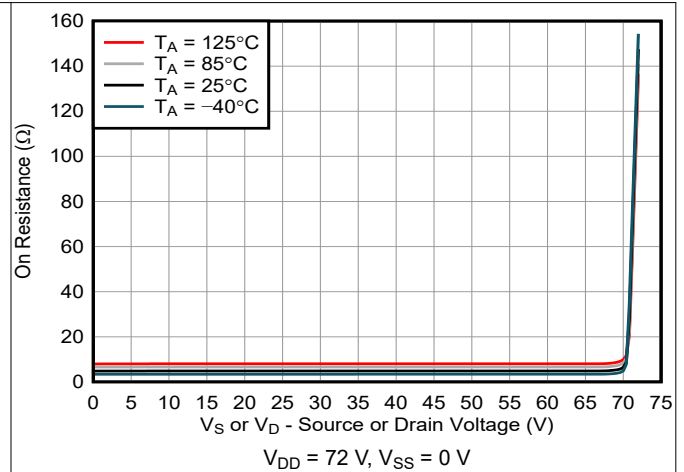


Figure 7-8. On-Resistance vs Source or Drain Voltage

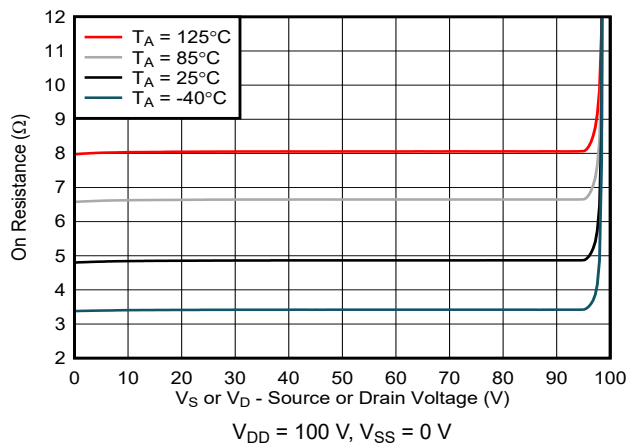


Figure 7-9. On-Resistance vs Source or Drain Voltage

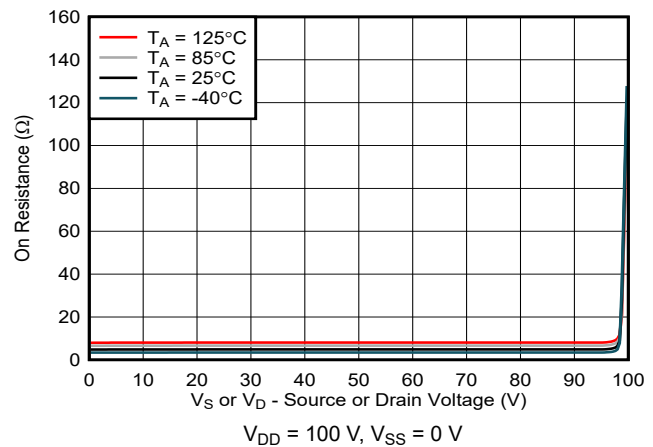


Figure 7-10. On-Resistance vs Source or Drain Voltage

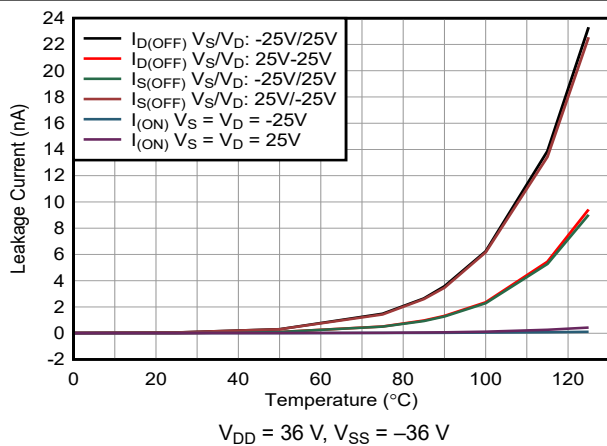


Figure 7-11. Leakage Current vs Temperature

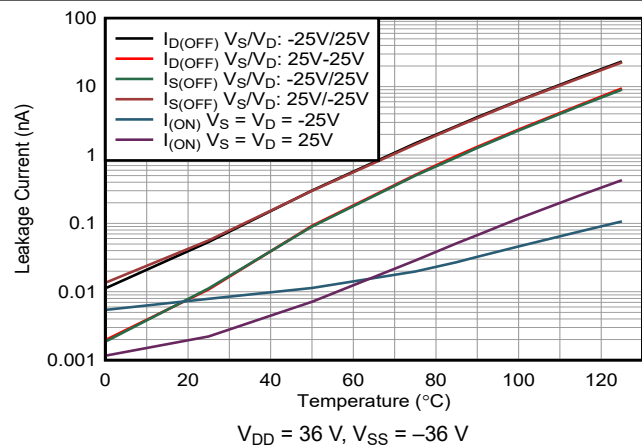
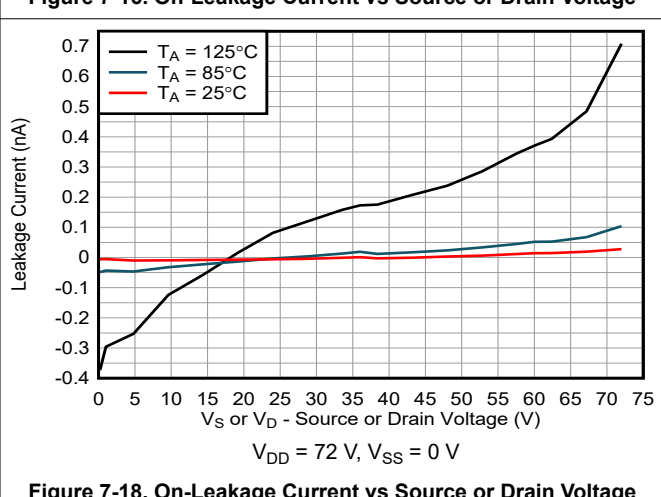
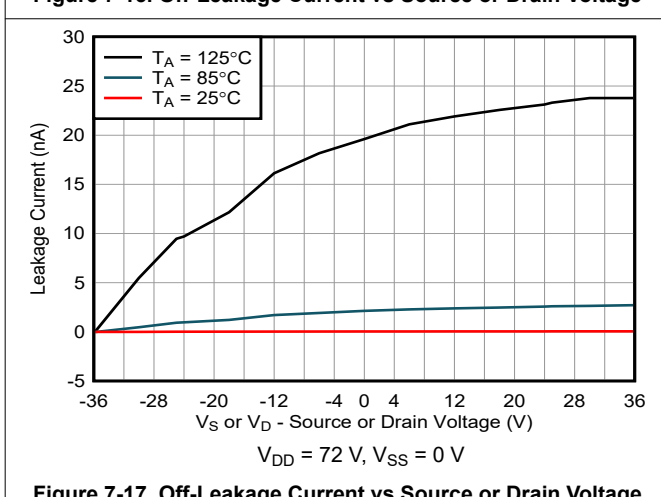
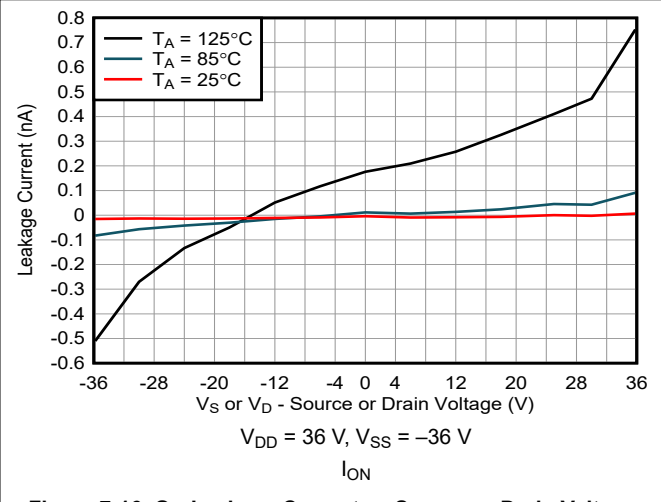
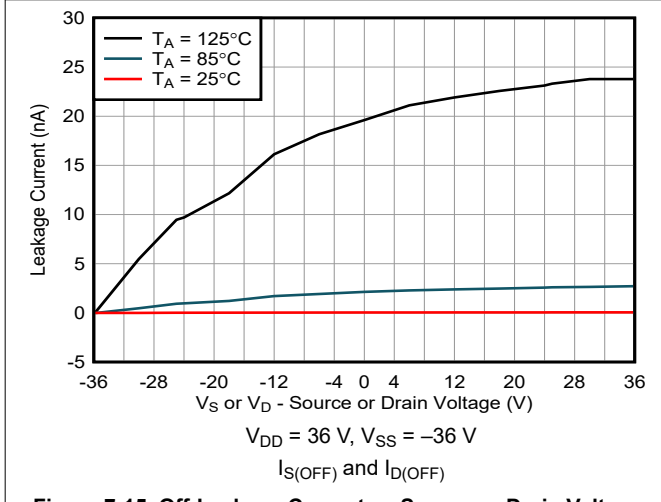
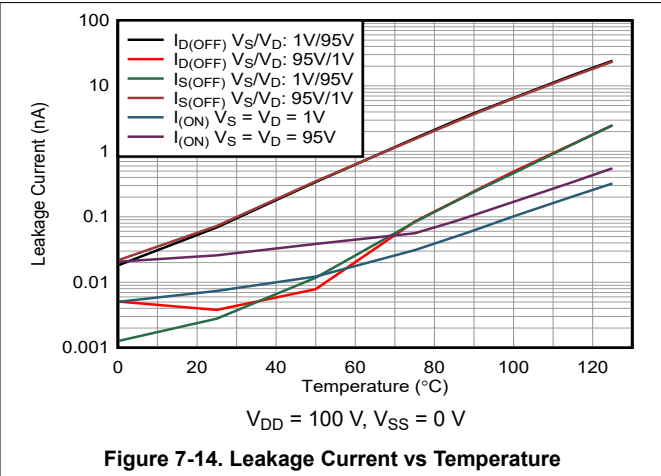
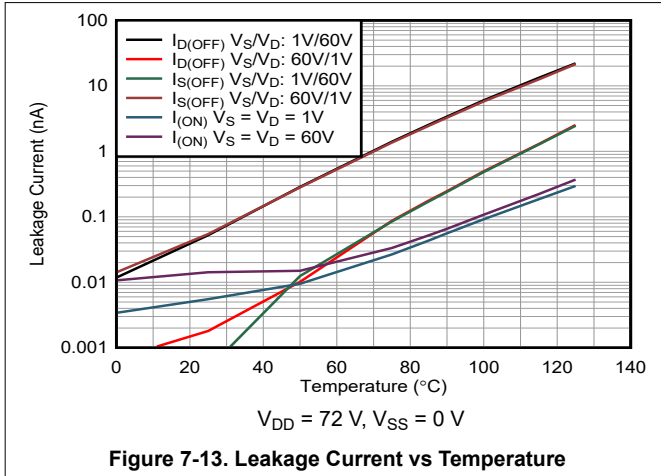


Figure 7-12. Leakage Current vs Temperature

### 7.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +36\text{ V}$ , and  $V_{SS} = -36\text{ V}$  (unless otherwise noted)



## 7.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +36\text{ V}$ , and  $V_{SS} = -36\text{ V}$  (unless otherwise noted)

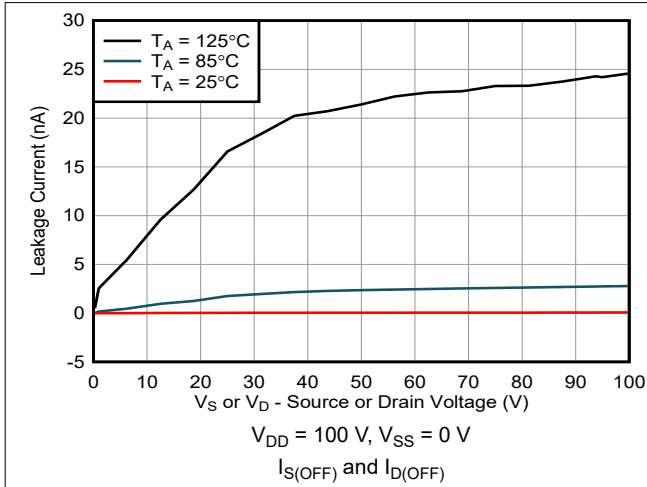


Figure 7-19. Off-Leakage Current vs Source or Drain Voltage

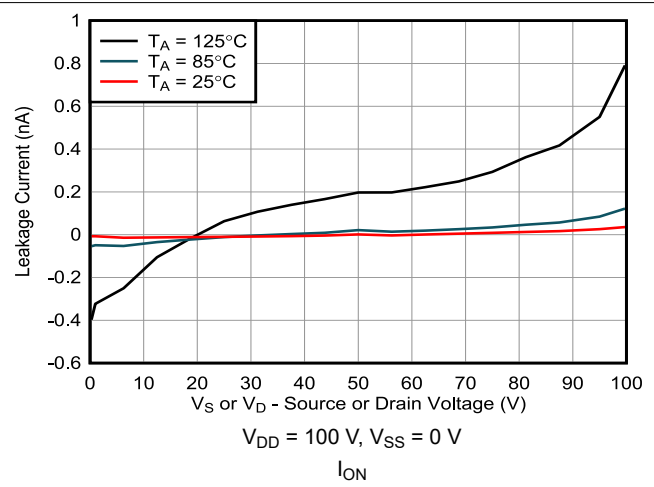


Figure 7-20. On-Leakage Current vs Source or Drain Voltage

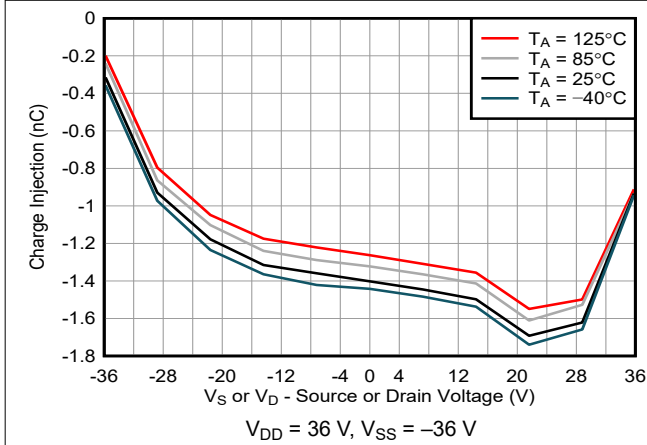


Figure 7-21. Charge Injection vs Source Voltage

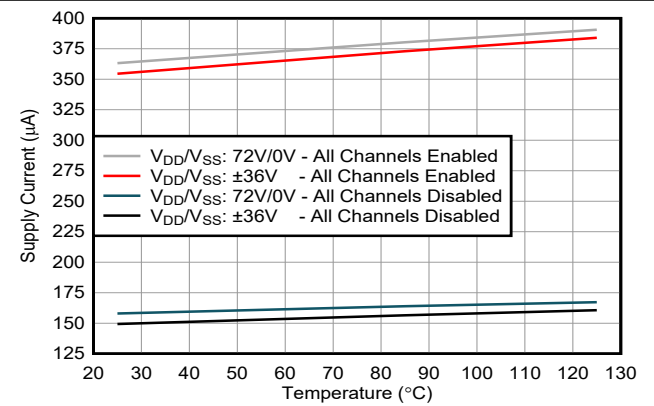


Figure 7-22. Supply Current vs Temperature

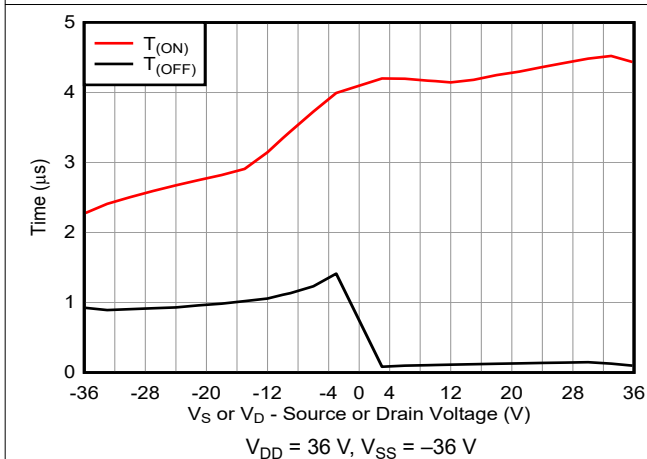


Figure 7-23. Turn-On and Turn-Off Times vs Source Voltage

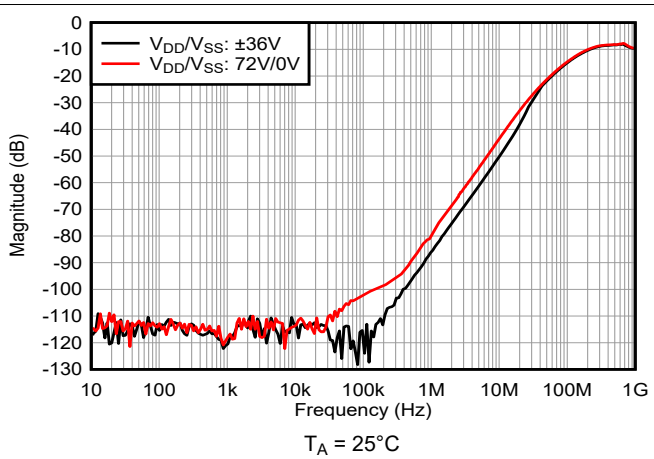
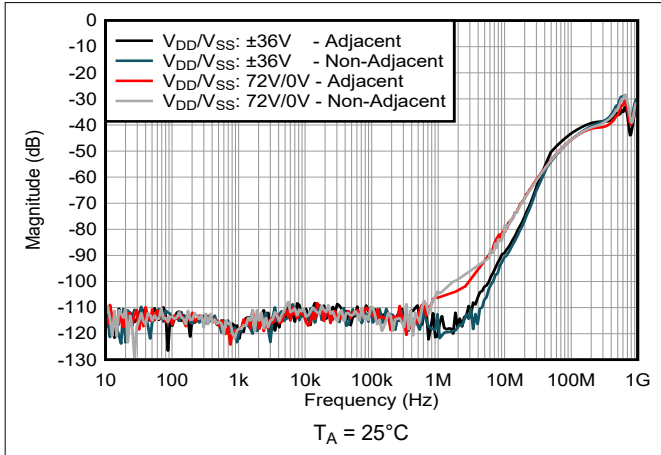


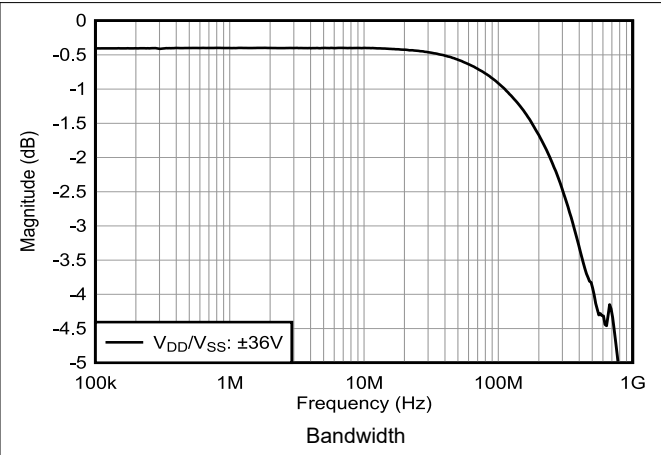
Figure 7-24. Off Isolation vs Frequency

### 7.14 Typical Characteristics (continued)

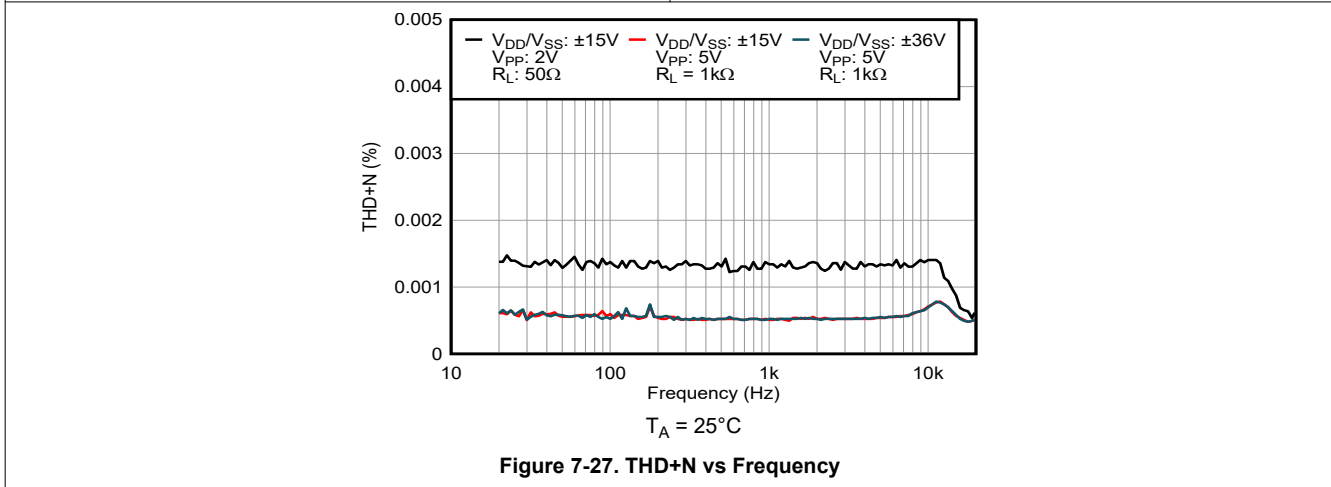
at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = +36\text{ V}$ , and  $V_{SS} = -36\text{ V}$  (unless otherwise noted)



**Figure 7-25. Crosstalk vs Frequency**



**Figure 7-26. Insertion Loss vs Frequency**



**Figure 7-27. THD+N vs Frequency**

## 8 Parameter Measurement Information

### 8.1 On-Resistance

The On-Resistance of the TMUX821x is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The On-Resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote On-Resistance. Figure 8-1 shows the measurement setup used to measure  $R_{ON}$ .  $\Delta R_{ON}$  represents the difference between the  $R_{ON}$  of any two channels, while  $R_{ON\_FLAT}$  denotes the flatness that is defined as the difference between the maximum and minimum value of On-Resistance measured over the specified analog signal range.

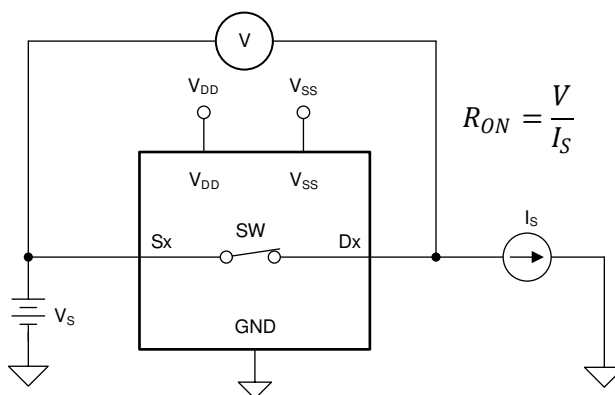


Figure 8-1. On-Resistance Measurement Setup

### 8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source Off-Leakage current  $I_{S(OFF)}$ : the leakage current flowing into or out of the source pin when the switch is off.
2. Drain Off-Leakage current  $I_{D(OFF)}$ : the leakage current flowing into or out of the drain pin when the switch is off.

Figure 8-2 shows the setup used to measure both Off-Leakage currents.

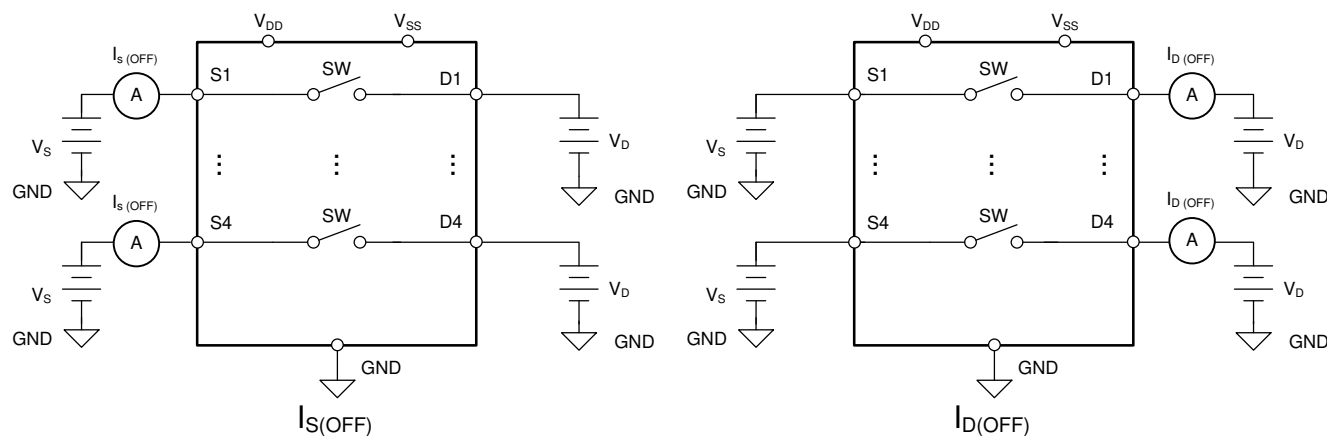


Figure 8-2. Off-Leakage Measurement Setup

### 8.3 On-Leakage Current

Source On-Leakage current ( $I_{S(ON)}$ ) and drain On-Leakage current ( $I_{D(ON)}$ ) denote the channel leakage currents when the switch is in the on state.  $I_{S(ON)}$  is measured with the drain floating, while  $I_{D(ON)}$  is measured with the source floating. Figure 8-3 shows the circuit used for measuring the On-Leakage currents.

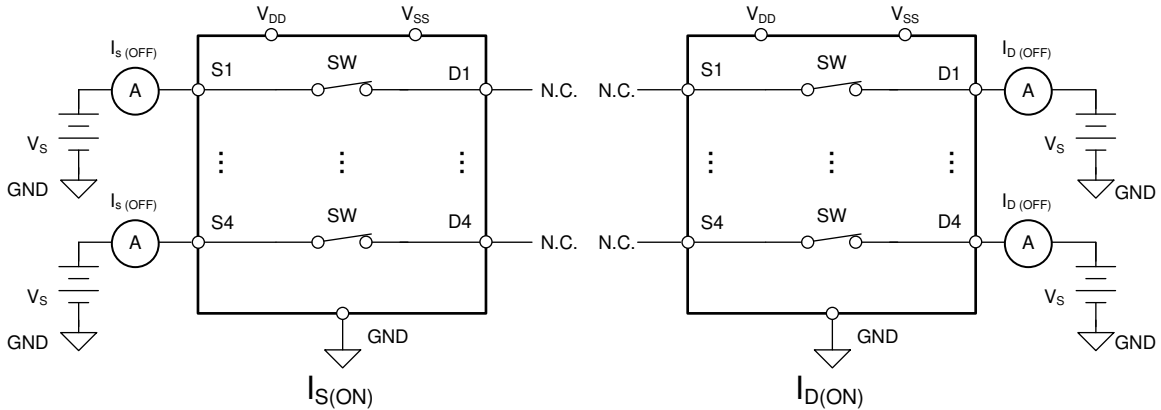


Figure 8-3. On-Leakage Measurement Setup

### 8.4 Device Turn-On and Turn-Off Time

Turn-On time ( $t_{ON}$ ) is defined as the time taken by the output of the TMUX8211, TMUX8212, and TMUX8213 to rise to a 90% final value after the SELx signal has risen (for NC switches) or fallen (for NO switches) to a 50% final value. Turn-Off time ( $t_{OFF}$ ) is defined as the time taken by the output of the TMUX8211, TMUX8212, and TMUX8213 to fall to a 10% initial value after the SELx signal has fallen (for NC switches) or risen (for NO switches) to a 50% initial value. Figure 8-4 shows the setup used to measure  $t_{ON}$  and  $t_{OFF}$ .

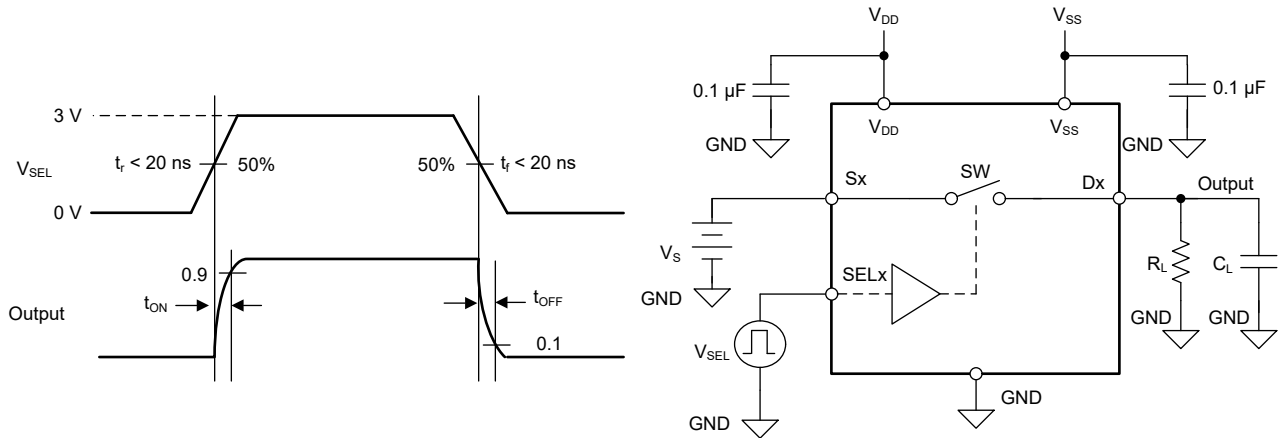


Figure 8-4. Enable Delay Measurement Setup

## 8.5 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol  $Q_{INJ}$ . Figure 8-5 shows the setup used to measure charge injection from the source to drain.

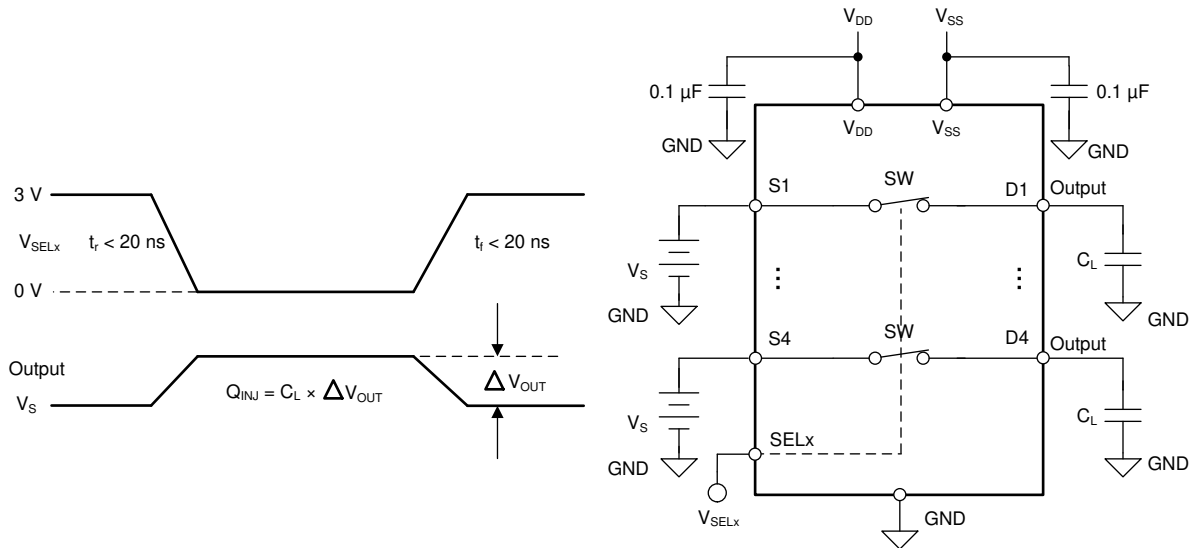


Figure 8-5. Charge-Injection Measurement Setup

## 8.6 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance,  $Z_0$ , for the measurement is 50 Ω. Figure 8-6 and Equation 1 shows the setup used to measure off isolation.

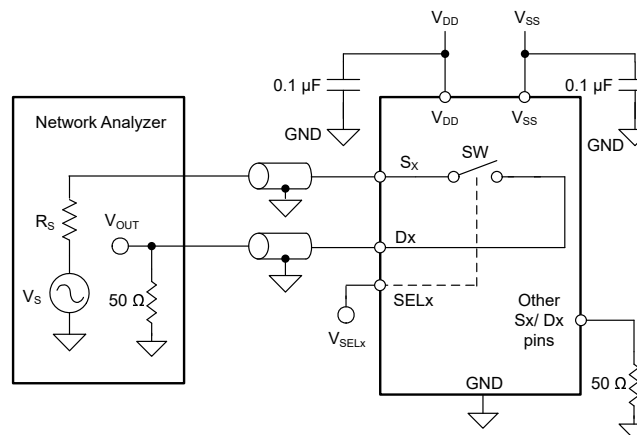
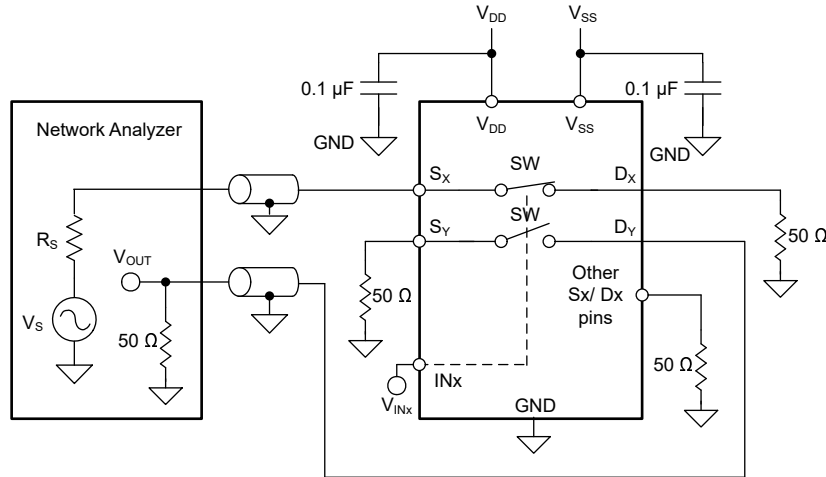


Figure 8-6. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \quad (1)$$

### 8.7 Crosstalk

Crosstalk ( $X_{TALK}$ ) is defined as the ratio of the signal at the drain pin ( $D_x$ ) of a different channel, when a signal is applied at the source pin ( $S_x$ ) of an on-channel. The characteristic impedance,  $Z_O$ , for the measurement is  $50\ \Omega$ , as shown in [Figure 8-7](#) and [Equation 2](#).

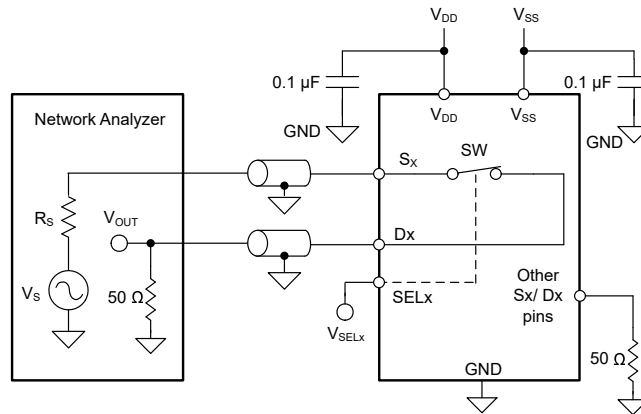


**Figure 8-7. Inter-channel Crosstalk Measurement Setup**

$$Inter - channel\ Crosstalk = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \tag{2}$$

### 8.8 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by  $< 3\ \text{dB}$  when the input is applied to the source pin ( $S_x$ ) of an on-channel, and the output is measured at the drain pin ( $D_x$ ). [Figure 8-8](#) and [Equation 3](#) shows the setup used to measure bandwidth of the switch.

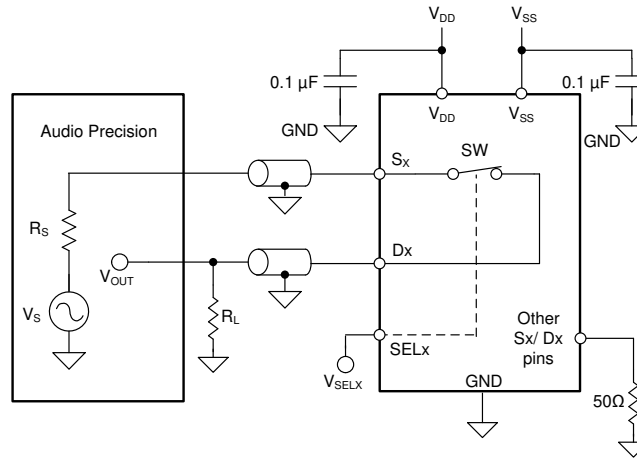


**Figure 8-8. Bandwidth Measurement Setup**

$$Bandwidth = 20 \times \text{Log} \frac{V_{OUT}}{V_S} \tag{3}$$

## 8.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The On-Resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. [Figure 8-9](#) shows the setup used to measure THD+N of the devices.



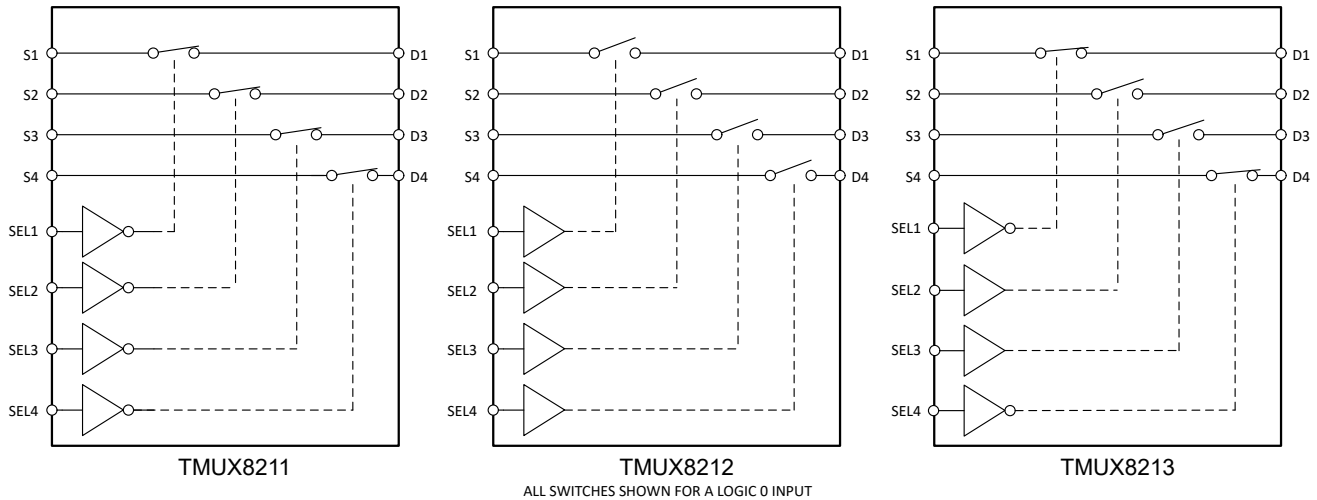
**Figure 8-9. THD+N Measurement Setup**

## 9 Detailed Description

### 9.1 Overview

The TMUX8211, TMUX8212 and TMUX8213 are a modern complementary metal-oxide semiconductor (CMOS) analog switches in quad single-pole single-throw configuration. The devices work well with dual supplies, a single supply, or asymmetric supplies.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Bidirectional Operation

The devices conduct equally well from source ( $S_x$ ) to drain ( $D_x$ ) or from drain ( $D_x$ ) to source ( $S_x$ ). Each signal path has similar characteristics in both directions.

#### 9.3.2 Flat On-Resistance

The TMUX821x devices are designed with a special switch architecture to produce ultra-flat On-Resistance ( $R_{ON}$ ) across most of the switch input operating region. The flat  $R_{ON}$  response allows the device to be used in precision sensor applications since the  $R_{ON}$  is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

The flattest On-Resistance region extends from  $V_{SS}$  to roughly 5 V below  $V_{DD}$ . Once the signal is within 5 V of  $V_{DD}$  the On-Resistance will exponentially increase and may impact desired signal transmission.

#### 9.3.3 Protection Features

These devices offer a number of protection features to enable robust system implementations.

##### 9.3.3.1 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. Additionally the fail safe logic feature allows the logic inputs of the mux to be interfaced with high voltages, allowing for simplified interfacing if only high voltage control signals are present. The logic inputs are protected against positive faults of up to +48 V in powered-off condition, but do not offer protection against negative over-voltage condition.

Fail-safe logic also allows the devices to interface with a voltage greater than  $V_{DD}$  on the control pins during normal operation to add maximum flexibility in system design. For example, with a  $V_{DD} = 15$  V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 48 V.

### 9.3.3.2 ESD Protection

All pins support HBM ESD protection level up to  $\pm 2$  kV, which helps protect the devices from ESD events during the manufacturing process.

### 9.3.3.3 Latch-Up Immunity

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or over-voltage), but once activated the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

In the TMUX821x devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are Latch-Up immune under all circumstances by device construction.

The TMUX821x devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to over-voltage or current injections. The Latch-Up immunity feature allows the TMUX821x to be used in harsh environments. For more information on Latch-Up immunity, refer to [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#).

### 9.3.4 1.8 V Logic Compatible Inputs

The TMUX821x devices have 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX821x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#).

### 9.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX821x have internal weak Pull-Down resistors to GND to ensure the logic pins are not left floating. The value of this Pull-Down resistor is approximately 4 M $\Omega$ , but is clamped to 1  $\mu$ A at higher voltages. This feature integrates up to four external components and reduces system size and cost.

## 9.4 Device Functional Modes

### 9.4.1 Normal Mode

In Normal Mode operation, signals of up to  $V_{DD}$  and  $V_{SS}$  can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The select (SELx) pins determine which switch path to turn on, according to the [Truth Table](#). The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies ( $V_{DD} - V_{SS}$ ) must be greater than or equal to 10 V. With a minimum  $V_{DD}$  of 10 V.
- The input signals on the source (Sx) or the drain (Dx) must be between  $V_{DD}$  and  $V_{SS}$ .
- The logic control (SELx) must have selected the switch.

### 9.4.2 Truth Tables

[Table 9-1](#), [Table 9-2](#), and [Table 9-3](#) show the truth tables for the TMUX8211, TMUX8212, and TMUX8213, respectively.

**Table 9-1. TMUX8211 Truth Table**

SEL # <sup>(1)</sup>	CHANNEL #
0	Channel # ON
1	Channel # OFF

(1) "#" designates the channel number controlled by SEL pin: "1, 2, 3, or 4"

**Table 9-2. TMUX8212 Truth Table**

SEL # <sup>(1)</sup>	CHANNEL #
0	Channel # OFF
1	Channel # ON

(1) "#" designates the channel number controlled by SEL pin: "1, 2, 3, or 4"

**Table 9-3. TMUX8213 Truth Table**

SEL1	SEL2	SEL3	SEL4	ON / OFF CHANNELS
0	X <sup>(1)</sup>	X	X	CHANNEL 1 ON
1	X	X	X	CHANNEL 1 OFF
X	0	X	X	CHANNEL 2 OFF
X	1	X	X	CHANNEL 2 ON
X	X	0	X	CHANNEL 3 OFF
X	X	1	X	CHANNEL 3 ON
X	X	X	0	CHANNEL 4 ON
X	X	X	1	CHANNEL 4 OFF

(1) "X" means "do not care."

If unused, then the SELx pins must be tied to GND or Logic High so that the devices do not consume additional current as highlighted in [Implications of Slow or Floating CMOS Inputs](#). Unused signal path inputs (Sx or Dx) should be connected to GND for best performance.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 10.1 Application Information

The TMUX821x are high voltage switches capable of supporting analog and digital signals. The high voltage capability of these multiplexers allow them to be used in systems with high voltage signal swings, or in systems with high common mode voltages.

Additionally, the TMUX821x devices provide consistent analog parametric performance across the entire supply voltage range allowing the devices to be powered by the most convenient supply rails in the system while still providing excellent performance.

### 10.2 Typical Application

A common feature of many PMUs (precision measurement units) is the ability to change current ranges. This allows for a system defined current clamp when testing devices and reduces possible damage to the PMU and DUT (device under test). In high voltage PMUs, large relays are often used to enable this switching, but this comes with the trade-off of size. To reduce system size, a multi-channel high voltage switch can be added to facilitate this switching with minimal impact to system size and performance. The TMUX821x allows for switching between multiple current ranges, and has the added flexibility to use multiple channels in parallel for high current applications.

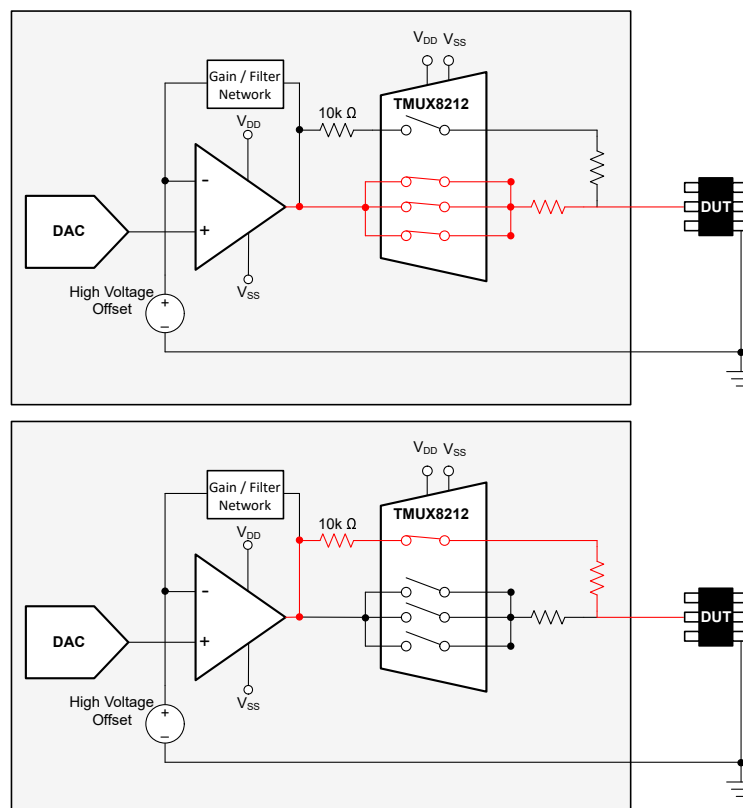


Figure 10-1. TMUX8212 Application Schematic

## 10.2.1 Design Requirements

**Table 10-1. Design Parameters**

PARAMETERS	VALUES
Positive supply ( $V_{DD}$ ) mux and Op Amps	36 V
Positive supply ( $V_{SS}$ ) mux and Op Amps	-36 V
Maximum input or output signals with common mode shift	-36 V to 36 V
Control logic thresholds	1.8 V compatible, up to 48 V
Temperature range	-40°C to +125°C

## 10.2.2 Detailed Design Procedure

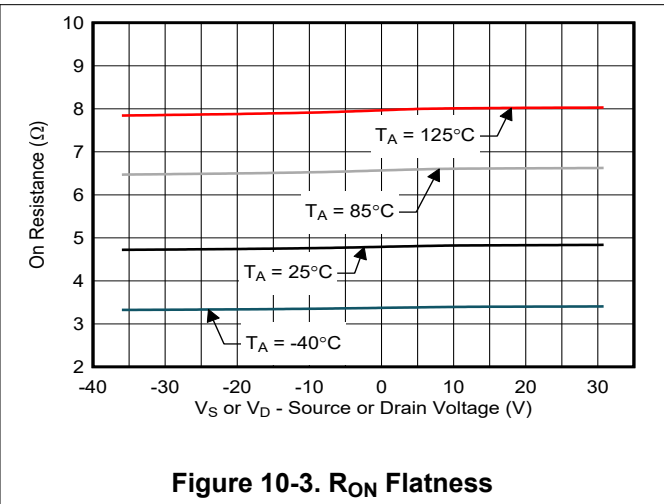
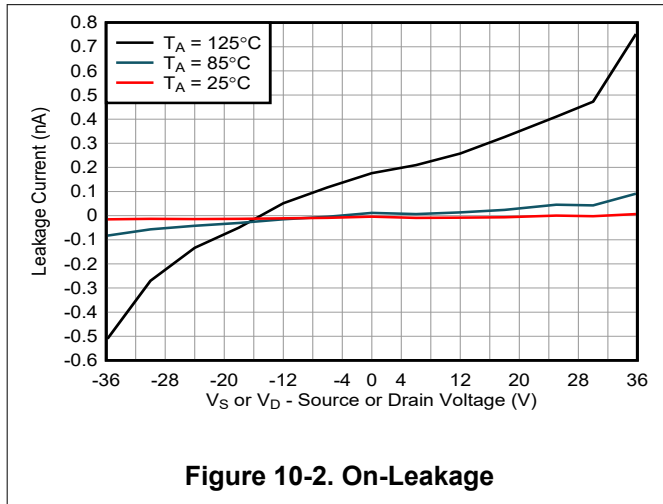
Multiplexing PMU systems enables a small, flexible solution that can be used over a wide range of current ranges. TI's high voltage multiplexers offer a size advantage over typical relay solutions while still achieving an extremely low level of distortion, noise, and leakage. This high voltage multiplexer can be use in tandem with high voltage operational amplifiers and DACs to create an accurate PMU with excellent signal-to-noise ratio.

In this example application, the TMUX8212 is paired with a high voltage amplifier and a DAC. The DAC generates an arbitrary voltage signal that feeds into the amplifier. An additional high voltage offset is also fed into the amplifier to add any needed common mode shift. This arbitrary signal is then passed through a current limiting resistor before reaching the DUT. To change the current range of the system, different current limiting resistors are added in series with each channel of the multiplexer. In this example, the first channel of the multiplexer uses a 10 k $\Omega$  resistor for the low current clamp. The maximum output current of the PMU in this range is 5 mA because of this design. During the system operation, the PMU is set to this lower current range in the beginning of the test routine. After the DUT is initially checked in this range and is operating normally with no unexpected shorts, the current range can be switched to high current. This way the PMU and DUT will not be unnecessarily damaged from excess current due to a short. In this example, the remaining three channels of the TMUX8212 are connected in parallel, increasing the maximum current through the device and reducing the low On-Resistance. Because of the flexibility of the TMUX8212, this could easily be modified to fit any system need. For example, if less maximum current is needed, then two channels could be connected in parallel instead of three, and the additional single channel could be used to add a third current range option. The additional input channels make this multiplexed application increasingly valuable by greatly reducing solution size.

The TMUX821x switches have exceptionally flat On-Resistance and low leakage currents across the signal voltage range. The ultra-flat On-Resistance keeps the current clamp constant across the signal voltage range, and the low leakage current reduces the potential noise/offset when measuring on the lowest current range. Additionally, excellent crosstalk and off-isolation performance allows the TMUX821x devices to perform well in multi-channel switching applications without having an unselected channel impact the measurement on selected channels.

### 10.2.3 Application Curves

The example application utilizes the excellent leakage and On-Resistance flatness performance of the TMUX821x devices. Figure 10-2 shows the leakage current for a channel that is ON across a varying source voltage. Figure 10-3 shows the extremely flat On-Resistance across source voltage while operating within the flattest  $R_{ON}$  range of the TMUX821x devices. These features make the devices an ideal solution for applications that require excellent linearity and low distortion.



## 11 Power Supply Recommendations

The TMUX821x devices operate across a wide supply range of  $\pm 10$  V to  $\pm 50$  V (10 V to 100 V in single-supply mode). They also perform well with asymmetrical supplies such as  $V_{DD} = 50$  V and  $V_{SS} = -10$  V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1  $\mu$ F to 10  $\mu$ F at both the  $V_{DD}$  and  $V_{SS}$  pins to ground. An additional 0.1  $\mu$ F capacitor placed closest to the supply pins will provide the best supply decoupling solution. Always ensure the ground (GND) connection is established before supplies are ramped.

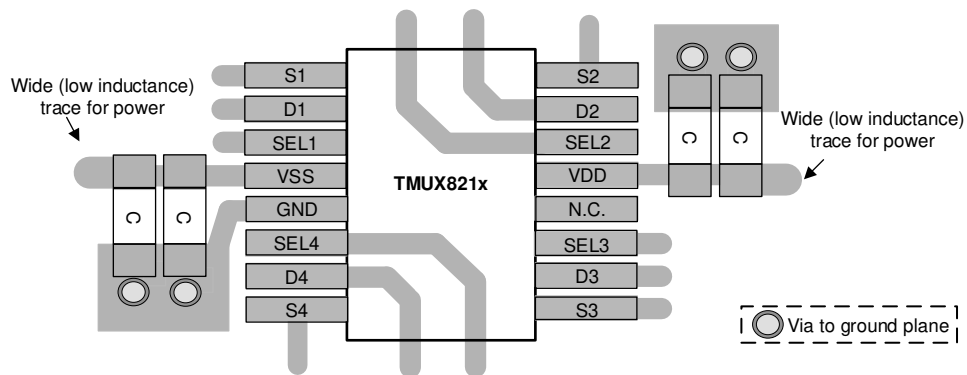
## 12 Layout

### 12.1 Layout Guidelines

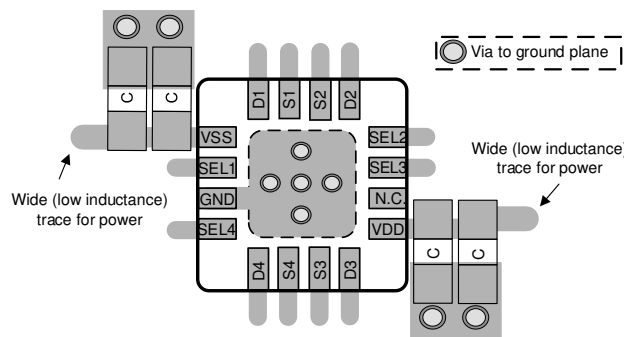
The image below illustrates an example of a PCB layout with the TMUX821x device. Some key considerations are:

- For reliable operation, connect at least one decoupling capacitor ranging from 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  between  $V_{\text{DD}}$  and  $V_{\text{SS}}$  to GND. We recommend a 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

### 12.2 Layout Example



**Figure 12-1. TMUX821x TSSOP Layout Example**



**Figure 12-2. TMUX821x QFN Layout Example**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application note
- Texas Instruments, [Multiplexers and Signal Switches Glossary](#) application report
- Texas Instruments, [Using Latch-Up Immune Multiplexers to Help Improve System Reliability](#) application report

#### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

#### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX8211PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8211	<a href="#">Samples</a>
TMUX8211RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8211	<a href="#">Samples</a>
TMUX8212PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8212	<a href="#">Samples</a>
TMUX8212RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8212	<a href="#">Samples</a>
TMUX8213PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8213	<a href="#">Samples</a>
TMUX8213RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8213	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

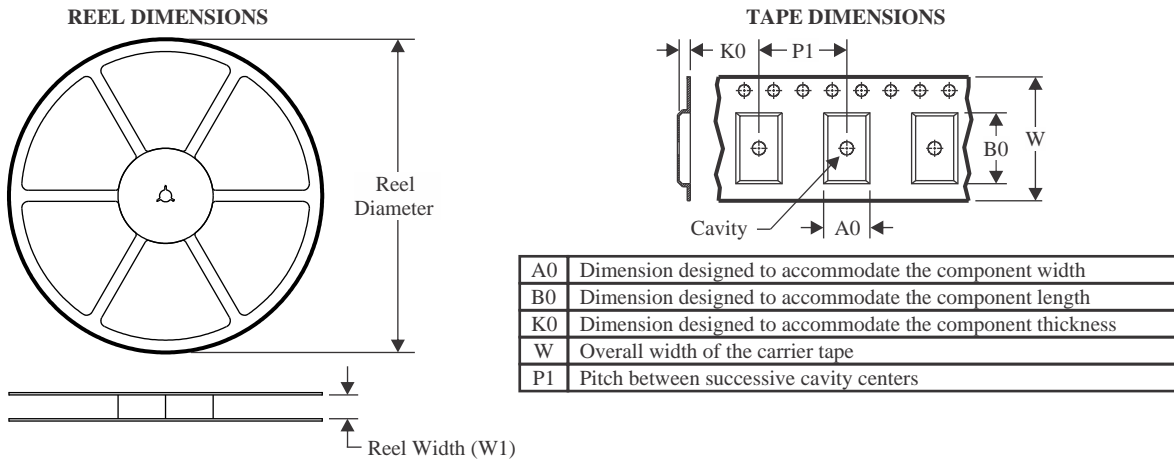
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

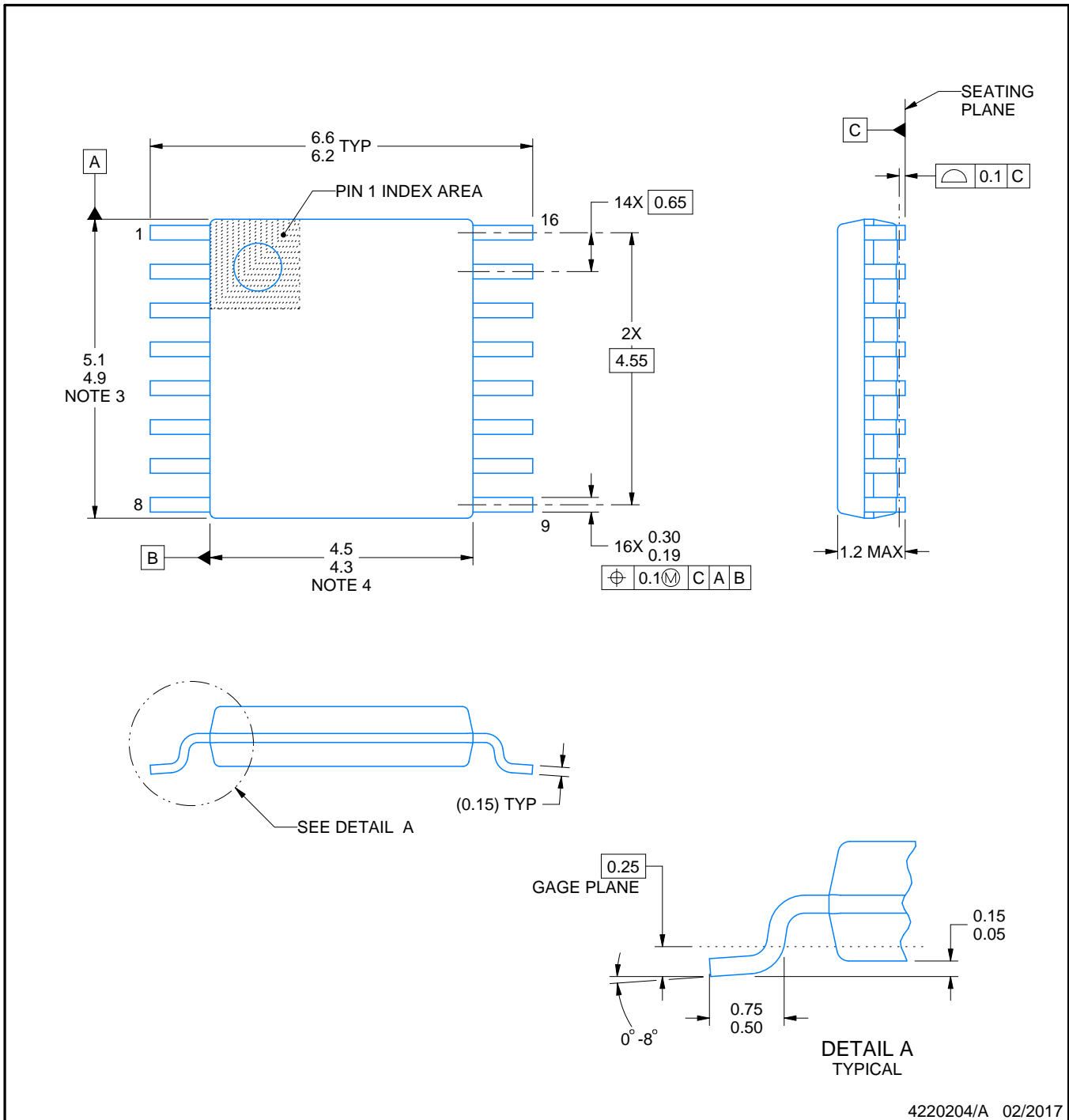

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX8211PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8211RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX8212PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8212RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX8213PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8213RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX8211PWR	TSSOP	PW	16	3000	356.0	356.0	35.0
TMUX8211RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX8212PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX8212RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX8213PWR	TSSOP	PW	16	3000	356.0	356.0	35.0
TMUX8213RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0



4220204/A 02/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

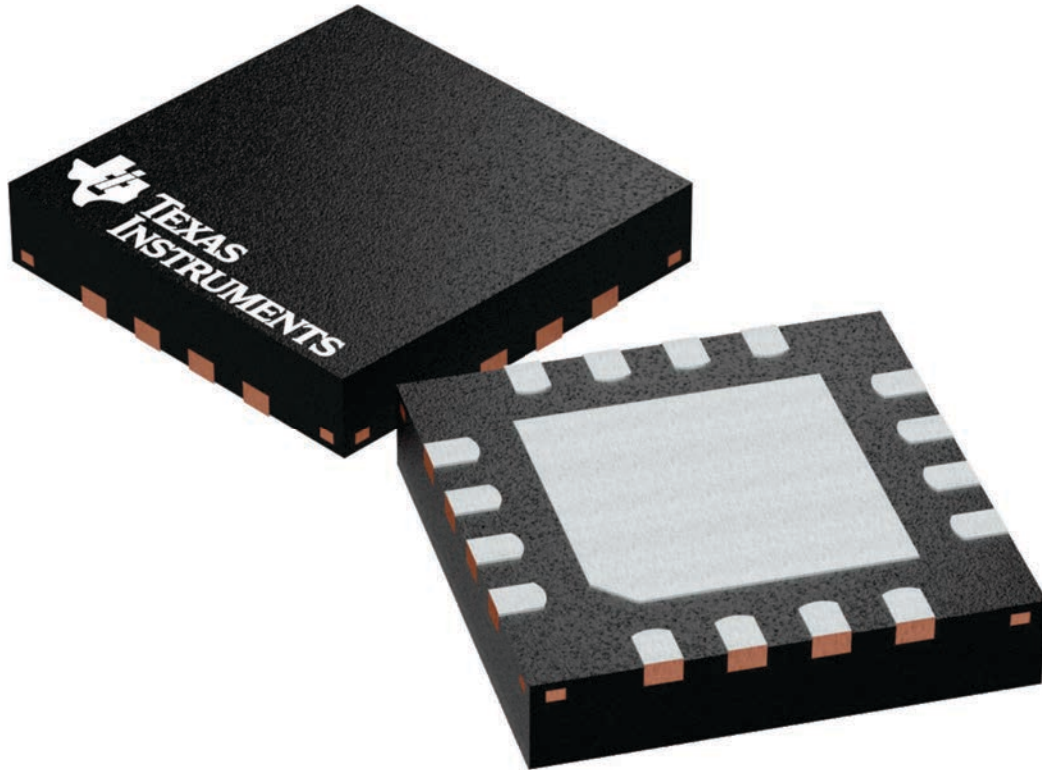
**RUM 16**

**WQFN - 0.8 mm max height**

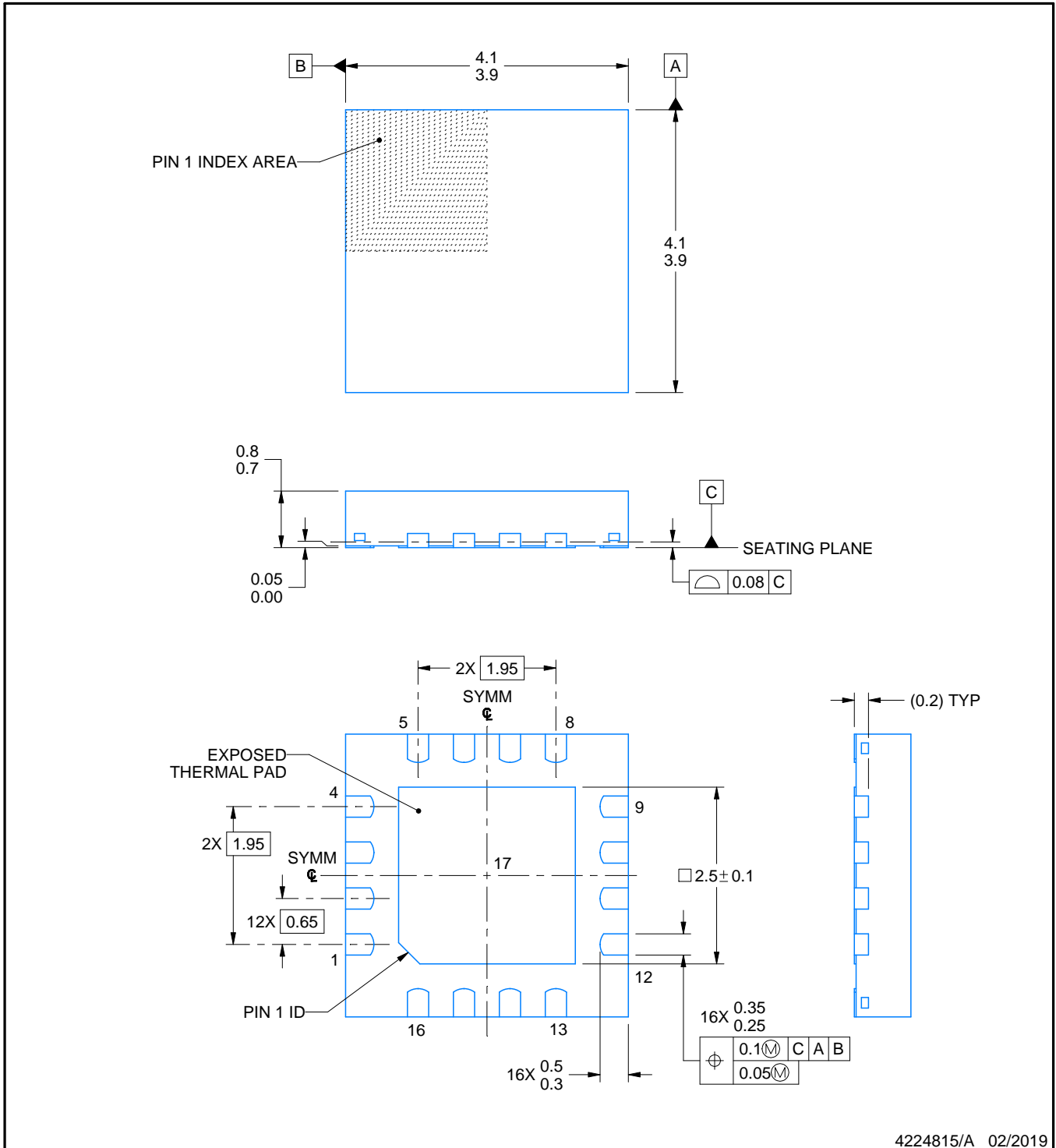
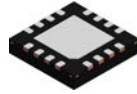
4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224843/A



4224815/A 02/2019

NOTES:

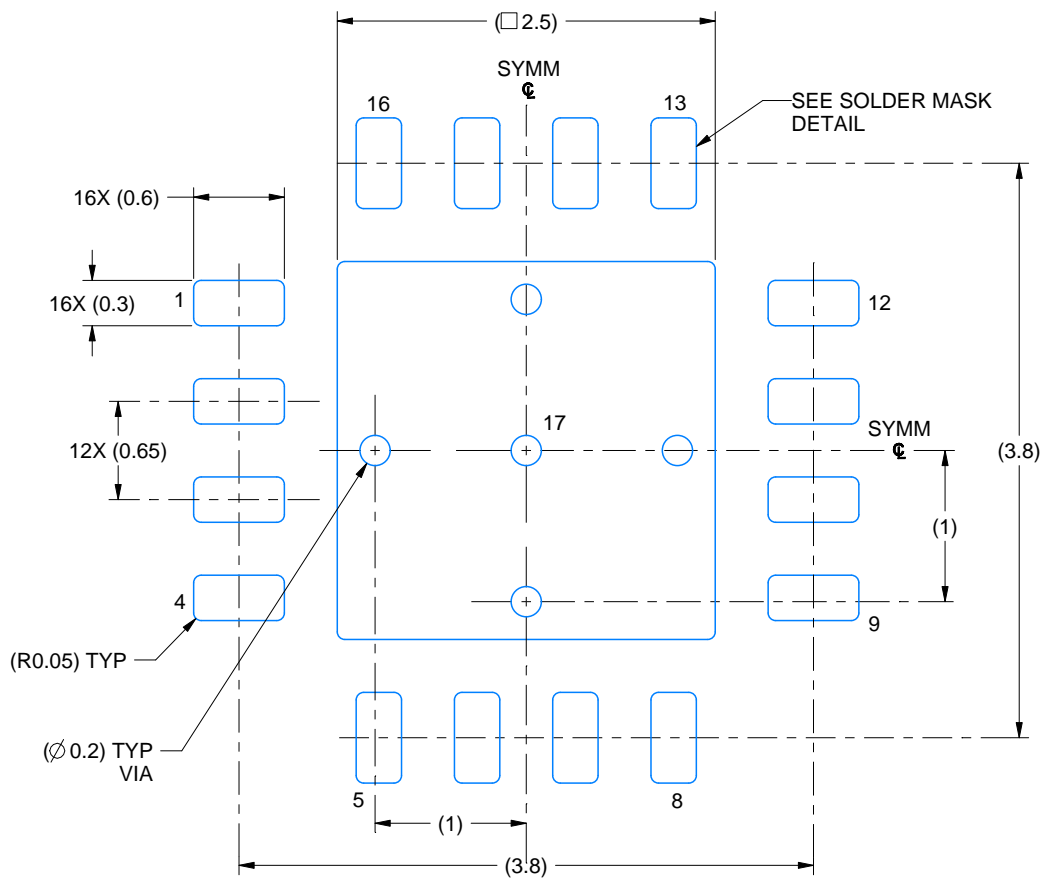
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

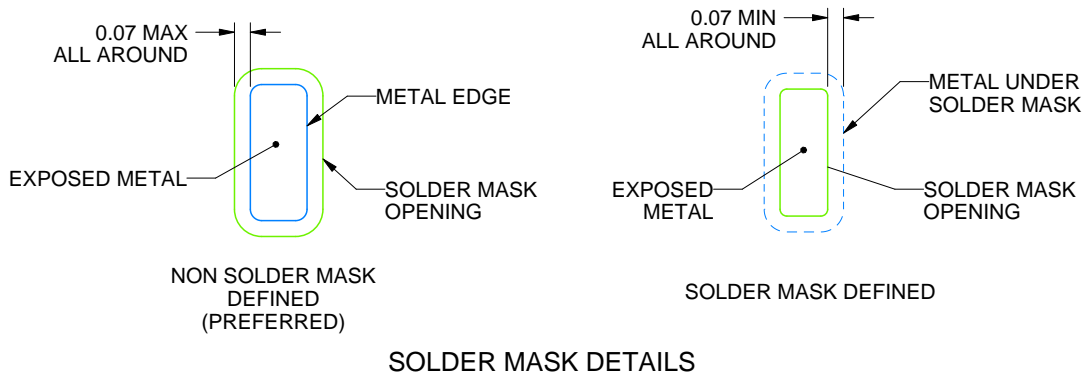
RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4224815/A 02/2019

NOTES: (continued)

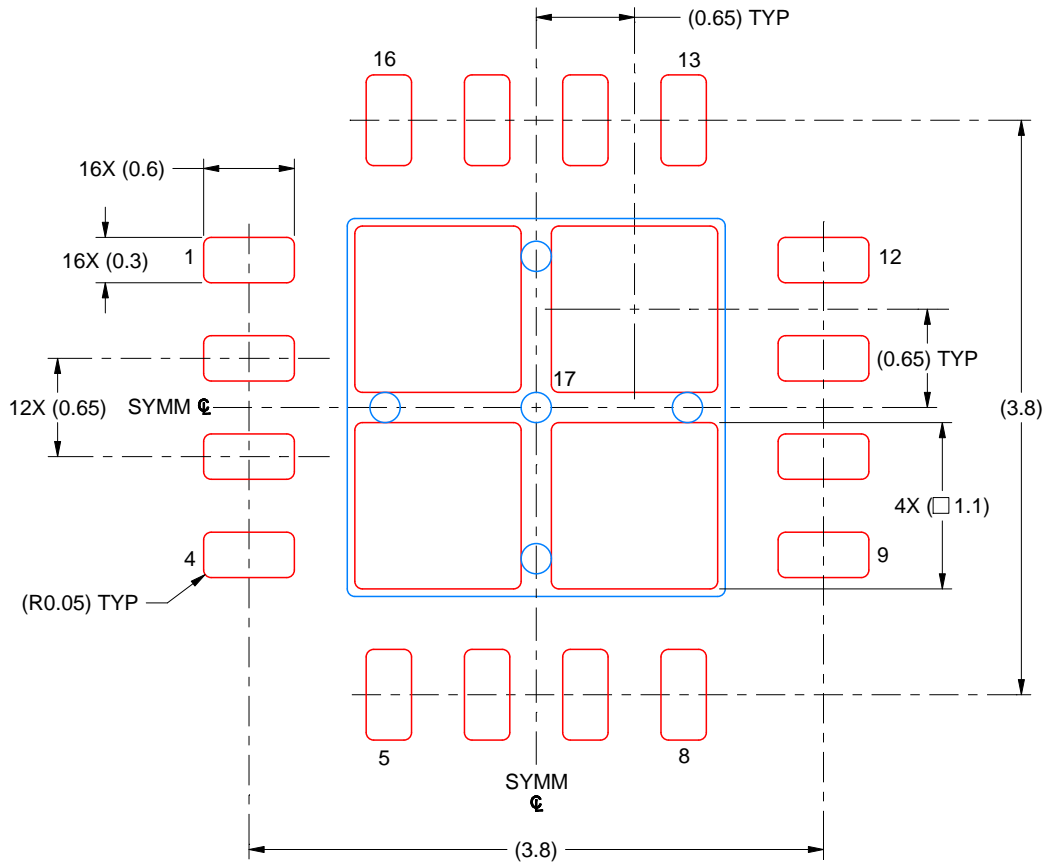
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 MM THICK STENCIL  
 SCALE: 20X

EXPOSED PAD 17  
 77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TMUX8212PWR on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management