



**THE DATASHEET OF  
PXP8R3-20QXJ**





# PXP8R3-20QX

20 V, P-channel Trench MOSFET

6 September 2021

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

## 3. Applications

- High-side load switch
- Battery management
- DC-to-DC conversion
- Switching circuits

## 4. Quick reference data

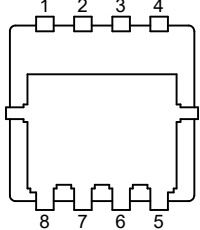
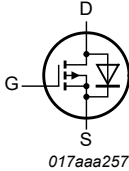
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-20.2	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -12.3\text{ A}; T_j = 25\text{ °C}$	-	6.6	8.3	mΩ
		$V_{GS} = -2.5\text{ V}; I_D = -9.7\text{ A}; T_j = 25\text{ °C}$	-	9.6	13.3	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-1)</p>	 <p>017aaa257</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXP8R3-20QX	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PXP8R3-20QX	9AW

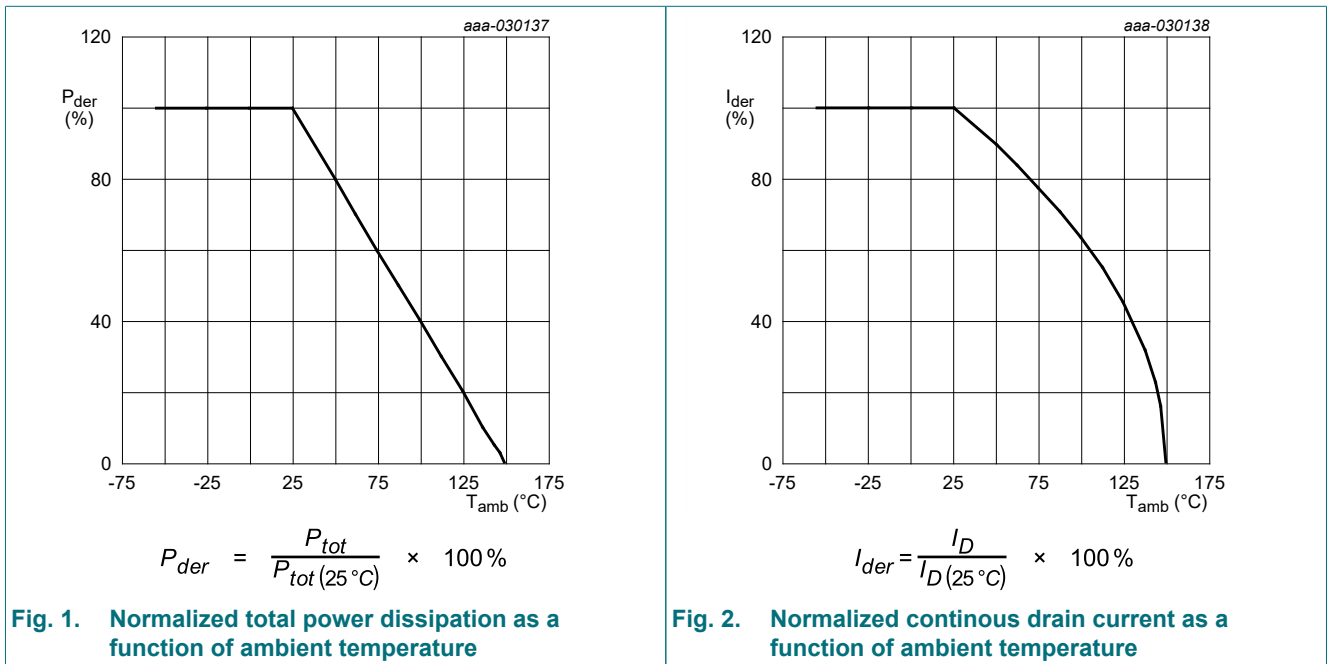
## 8. Limiting values

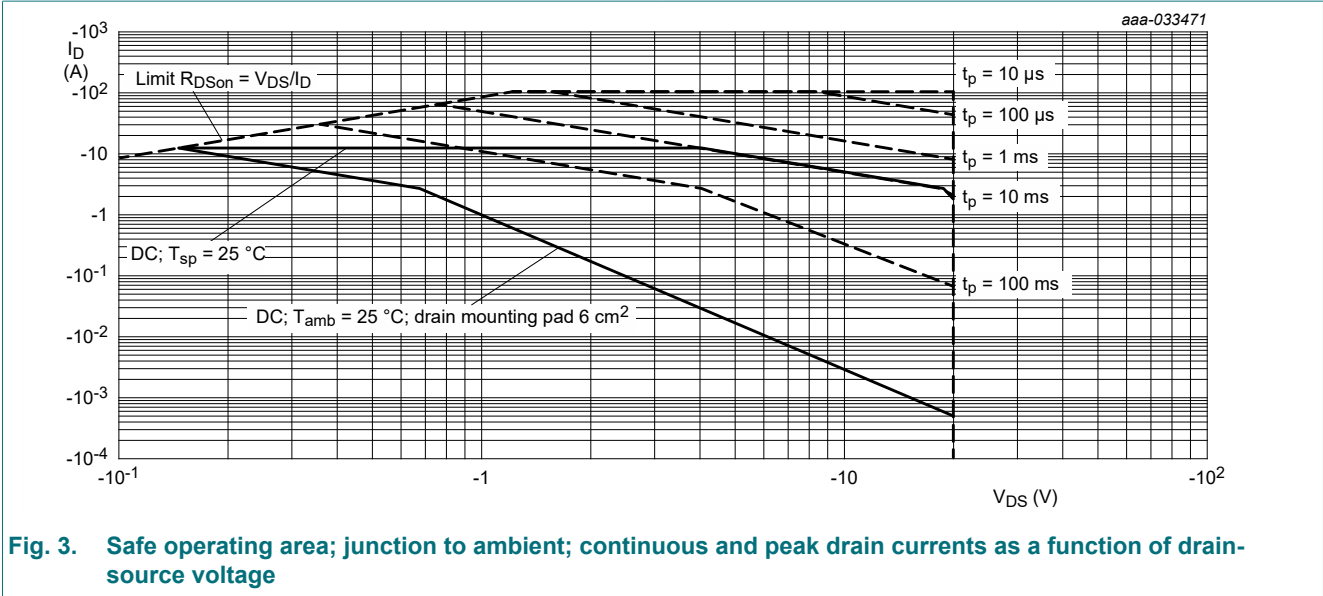
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-20	V	
V <sub>GS</sub>	gate-source voltage		-12	12	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-20.2	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-12.4	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-7.8	A
		V <sub>GS</sub> = -4.5 V; T <sub>sp</sub> = 25 °C		-	-65.1	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs	-	-102.8	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	4.8	W
		T <sub>amb</sub> = 25 °C	[1]	-	1.8	W
		T <sub>sp</sub> = 25 °C		-	50	W
T <sub>j</sub>	junction temperature		-55	150	°C	
T <sub>amb</sub>	ambient temperature		-55	150	°C	
T <sub>stg</sub>	storage temperature		-65	150	°C	
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.7	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.





### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	145	185	K/W
			[2]	-	55	70	K/W
		in free air; $t \leq 5$ s	[2]	-	21	26	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	1.5	2.5	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

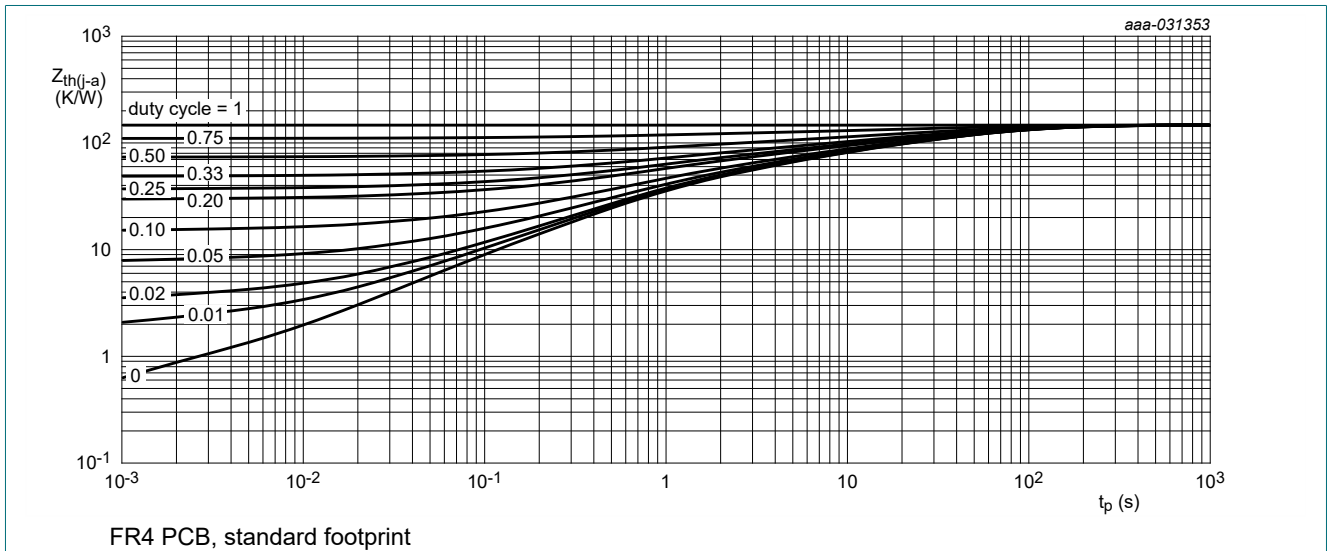


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

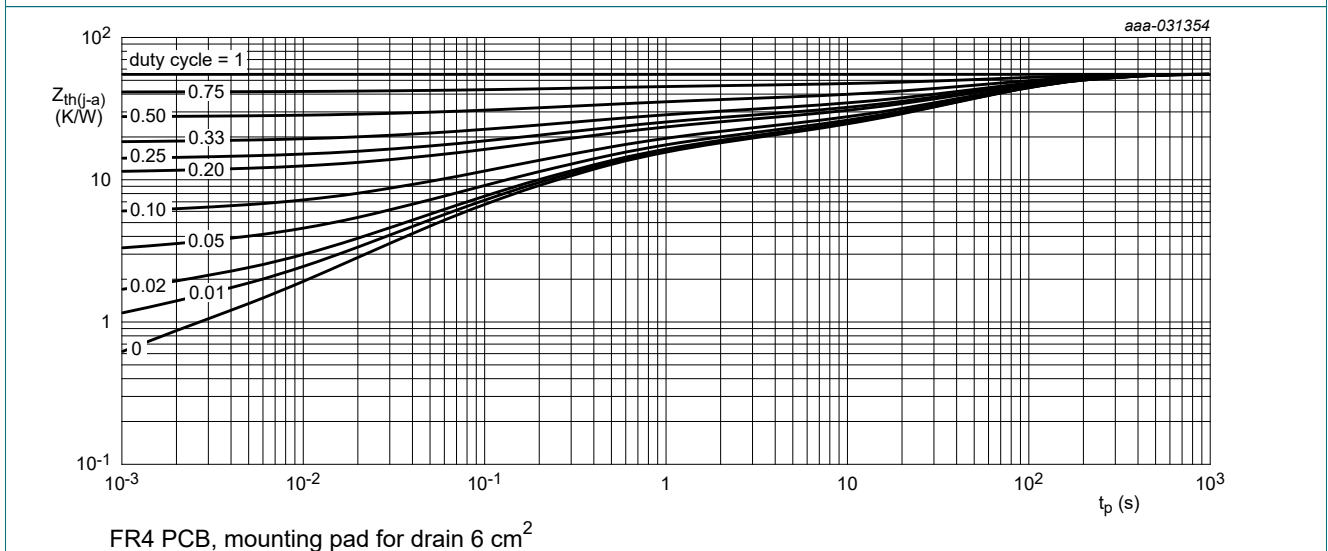


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.7	-0.9	-1.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-0.1	$\mu\text{A}$
		$V_{GS} = 12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	0.1	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -12.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6.6	8.3	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -12.3 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	9.4	11.8	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -9.7 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	9.6	13.3	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -12.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	43	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	2.4	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -12.3 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	61.2	91.8	nC
$Q_{GS}$	gate-source charge		-	10	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	5.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.9	-	nC
$Q_{GD}$	gate-drain charge		-	18.4	-	nC
$V_{GSpl}$	gate-source plateau voltage	$V_{DS} = -10 \text{ V}$ ; $I_D = -12.3 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-1.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6200	-	pF
$C_{oss}$	output capacitance		-	840	-	pF
$C_{rss}$	reverse transfer capacitance		-	780	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$ ; $I_D = -9.7 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 5 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	14	-	ns
$t_r$	rise time		-	42	-	ns
$t_{d(off)}$	turn-off delay time		-	101	-	ns
$t_f$	fall time		-	62	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.7 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V
$t_{rr}$	reverse recovery time	$I_S = -1.7 \text{ A}$ ; $dI_S/dt = 100 \text{ A}/\mu\text{s}$ ; $V_{GS} = -4.5 \text{ V}$ ; $V_{DS} = -10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	38	-	ns
$Q_r$	recovered charge		-	26	-	nC
$t_a$	reverse recovery rise time		-	13	-	ns
$t_b$	reverse recovery fall time		-	25	-	ns

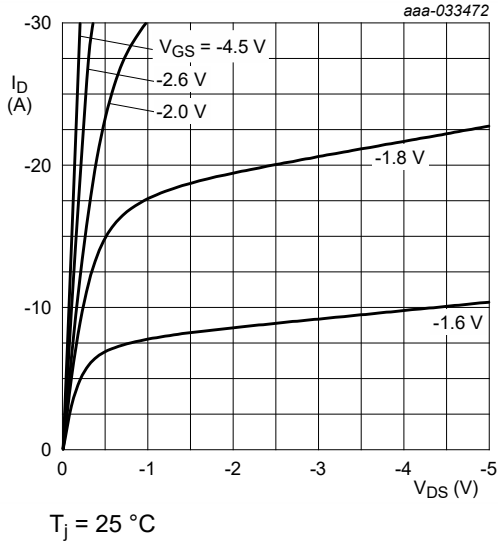


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

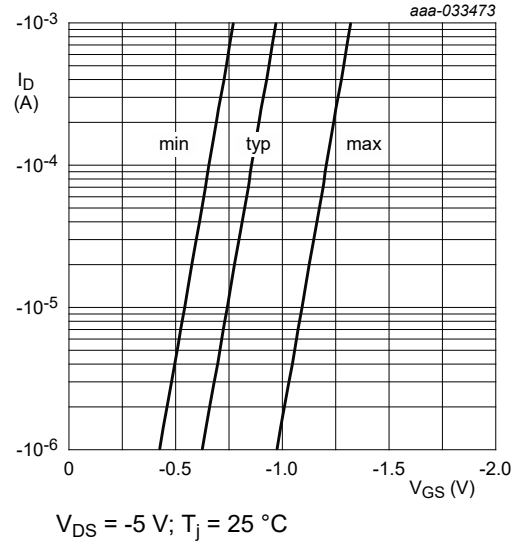


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

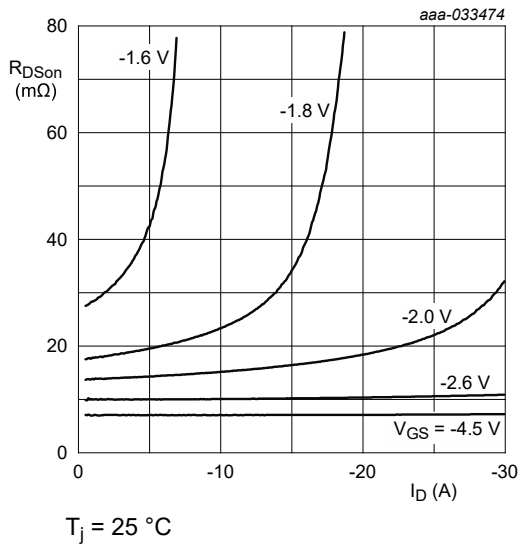


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

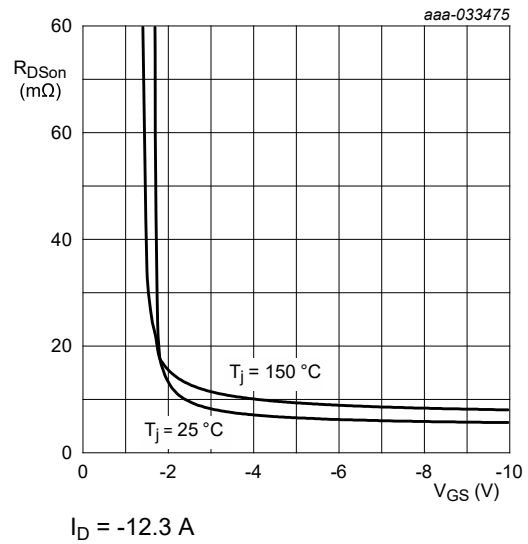


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

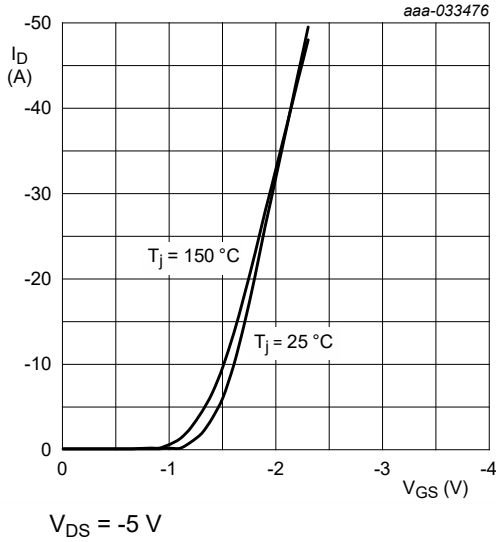


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

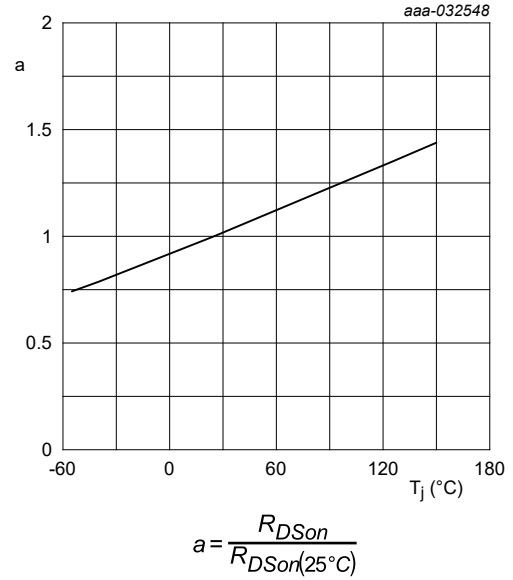


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

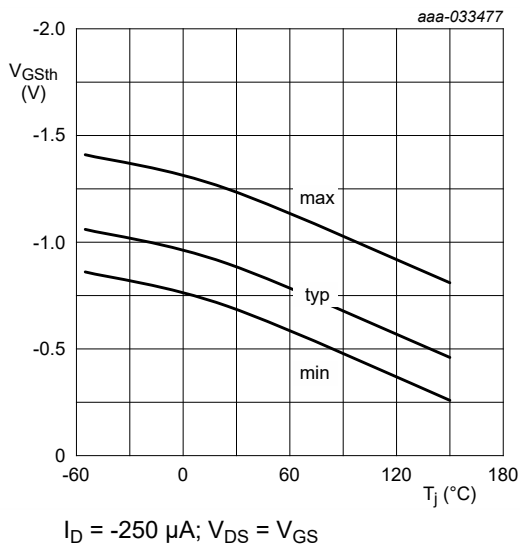


Fig. 12. Gate-source threshold voltage as a function of junction temperature

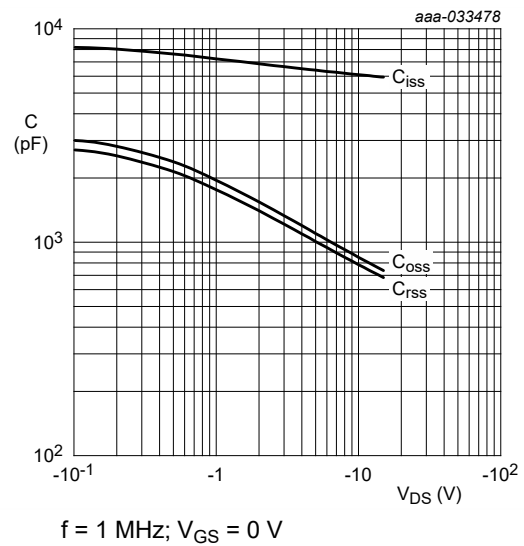
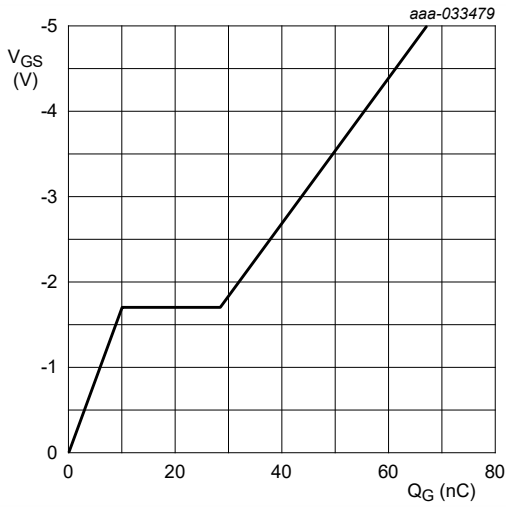


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -10\text{ V}; I_D = -12.3\text{ A}; T_j = 25\text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

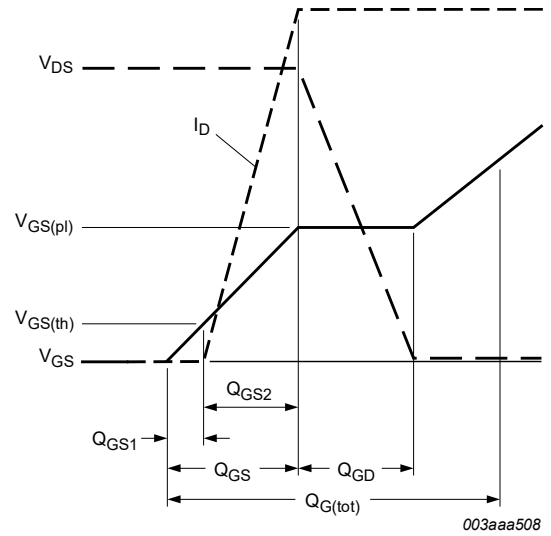


Fig. 15. Gate charge waveform definitions

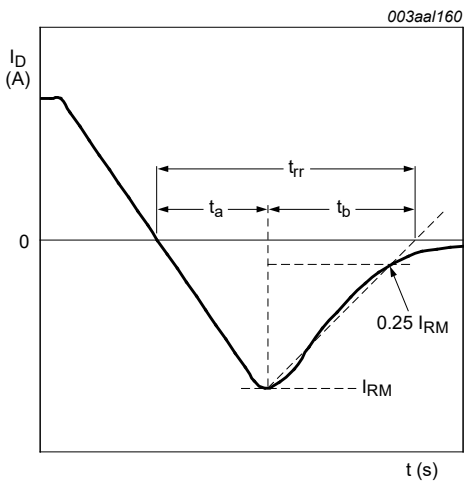
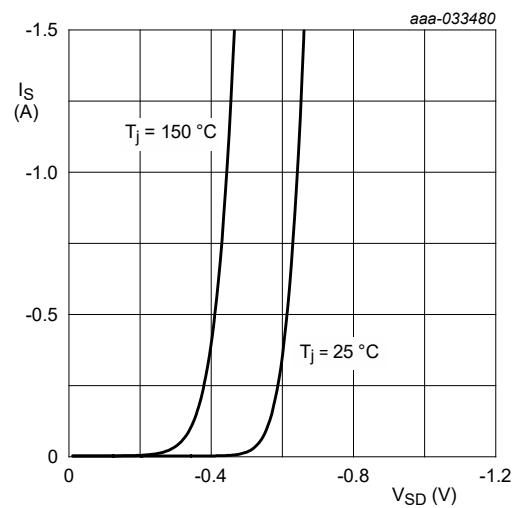


Fig. 16. Reverse recovery timing definition



$V_{GS} = 0\text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

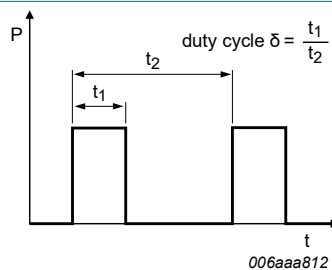


Fig. 18. Duty cycle definition

## 12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals;  
pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-1

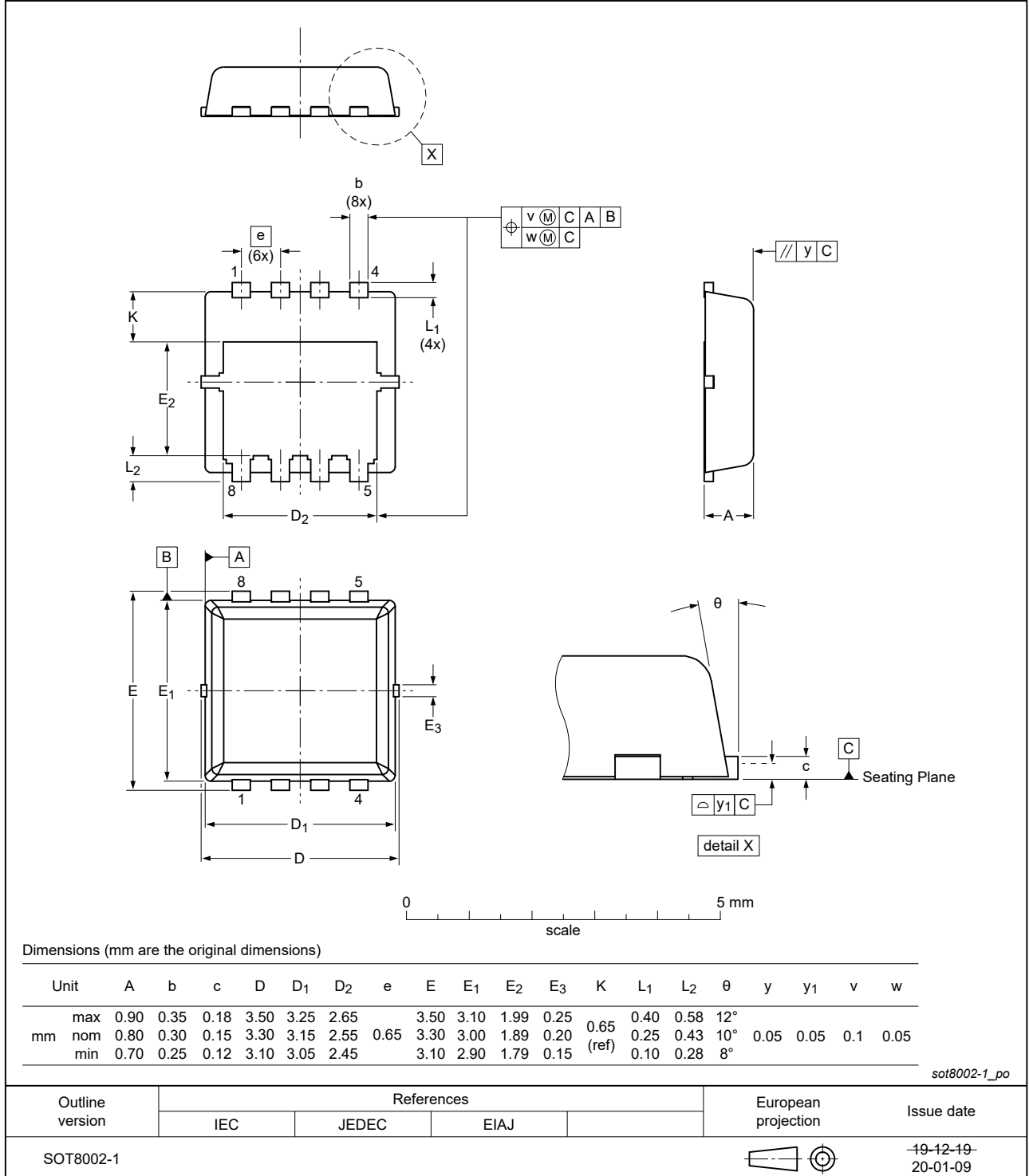


Fig. 19. Package outline MLPAK33 (SOT8002-1)

### 13. Soldering

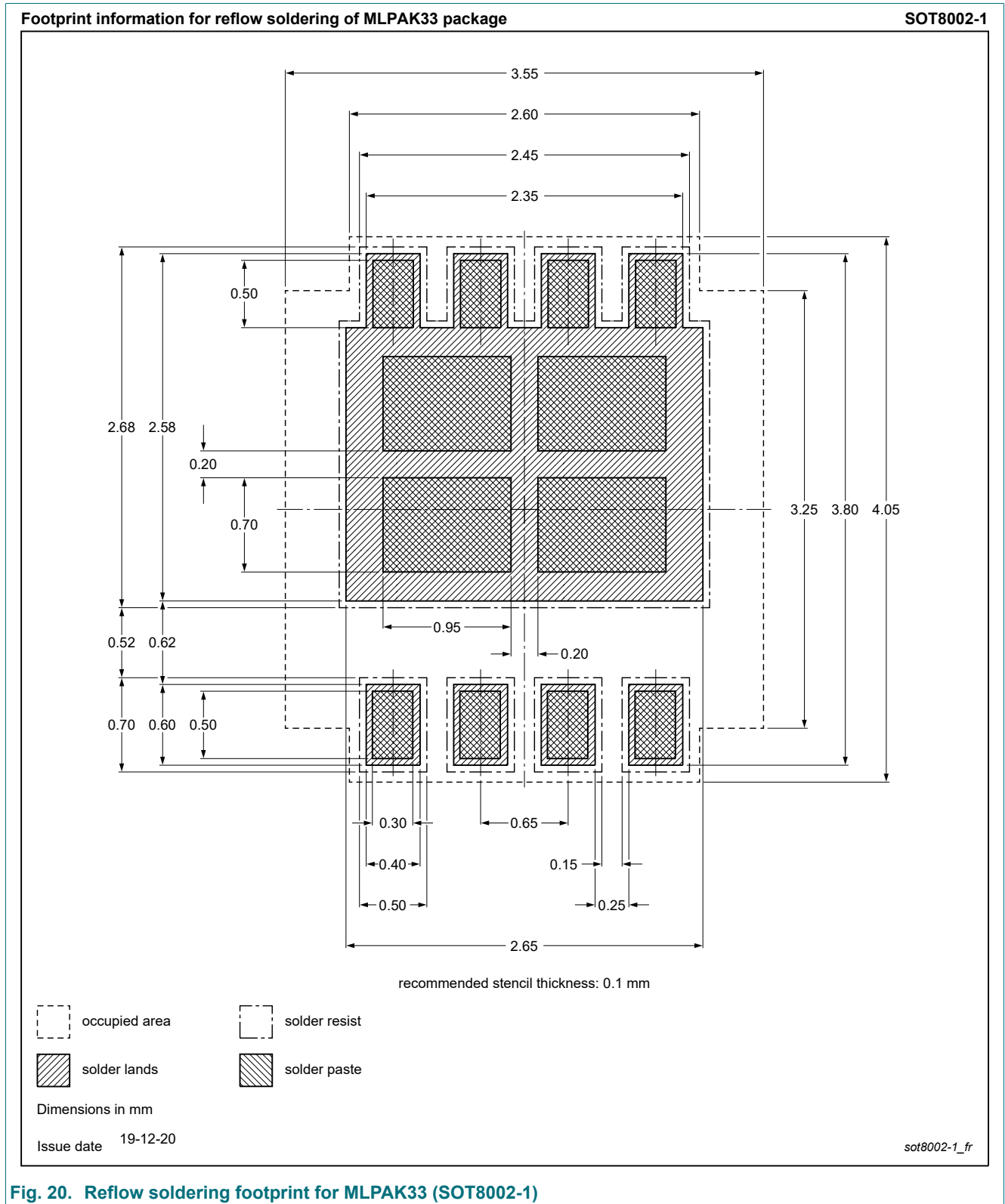


Fig. 20. Reflow soldering footprint for MLPAK33 (SOT8002-1)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXP8R3-20QX v.1	20210906	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
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## Contents

---

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	5
10. Characteristics.....	6
11. Test information.....	9
12. Package outline.....	10
13. Soldering.....	11
14. Revision history.....	12
15. Legal information.....	13

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Date of release: 6 September 2021

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