# THE DATASHEET OF

# NTTFD9D0N06HLTWG

DATA SHEET
www.onsemi.com

# MOSFET - Power, Single N-Channel

## 60 V, 9 mΩ, 38 A

# NTTFD9D0N06HL

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 60 V | 9 mΩ @ 10 V | 38 A |
| | 13 mΩ @ 4.5 V | |

### General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

### Features

Q1: N−Channel

- Max $r_{DS(on)}$ = 9.0 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10 A
- Max $r_{DS(on)}$ = 13 mΩ at $V_{GS}$ = 4.5, $I_D$ = 8.0 A

Q2: N−Channel

- Max $r_{DS(on)}$ = 9.0 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10 A
- Max $r_{DS(on)}$ = 13 mΩ at $V_{GS}$ = 4.5, $I_D$ = 8.0 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

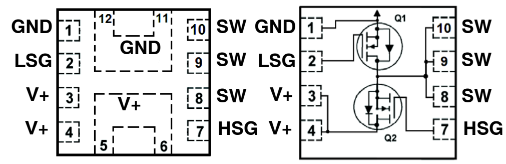
### Typical Applications

- Computing
- Communications
- General Purpose Point of Load

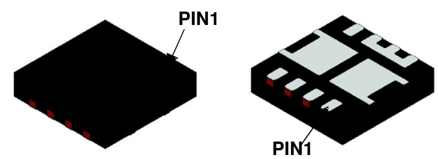
### PIN DESCRIPTION

| Pin | Name | Description |
|---|---|---|
| 1, 11, 12 | GND (LSS) | Low Side Source |
| 2 | LSG | Low Side Gate |
| 3, 4, 5, 6 | V + (HSD) | High Side Drain |
| 7 | HSG | High Side Gate |
| 8, 9, 10 | SW | Switching Node, Low Side Drain |

### ELECTRICAL CONNECTION

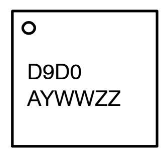



Dual N-Channel MOSFET




WQFN12, 3x3
CASE 510CJ

### MARKING DIAGRAM




D9D0 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTTFD9D0N06HLTWG | WQFN12 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**MOSFET MAXIMUM RATINGS** ($T_A$ = 25°C, Unless otherwise specified)

| Symbol | Parameter | | | | Q1 | Q2 | Units |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | Drain−to−Source Voltage | | | | 60 | 60 | V |
| $V_{GS}$ | Gate−to−Source Voltage | | | | ±20 | ±20 | V |
| $I_D$ | Drain Current | −Continuous | $T_C$ = 25°C | (Note 4) | 38 | 38 | A |
| | | −Continuous | $T_C$ = 100°C | (Note 4) | 23 | 23 | |
| | | −Continuous | $T_A$ = 25°C | | 9 (Note 1a) | 9 (Note 1b) | |
| | | −Pulsed | $T_A$ = 25°C | | 349 | 349 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | | (Note 3) | 46 | 46 | mJ |
| $P_D$ | Power Dissipation for Single Operation | | $T_C$ = 25°C | | 26 | 26 | W |
| | Power Dissipation for Single Operation | | $T_A$ = 25°C | | 1.7 (Note 1a) | 1.7 (Note 1b) | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | | −55 to +150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Q1 | Q2 | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case | 4.8 | 4.8 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1a), max copper | 70 (Note 1a) | 70 (Note 1b) | |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1c), min copper | 135 (Note 1a) | 135 (Note 1b) | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

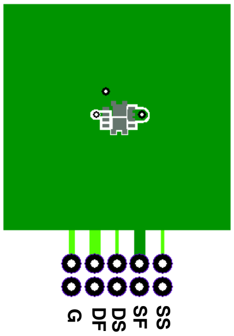
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain−to−Source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 V | Q1 | 60 | | | V |
| | | $I_D$ = 250 µA, $V_{GS}$ = 0 V | Q2 | 60 | | | |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, referenced to 25°C | Q1 | | 37.38 | | mV/°C |
| | | $I_D$ = 250 µA, referenced to 25°C | Q2 | | 37.38 | | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | Q1 | | | 10 | µA |
| | | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | Q2 | | | 10 | |
| $I_{GSS}$ | Gate−to−Source Leakage Current, Forward | $V_{GS}$ = +20/−16 V, $V_{DS}$ = 0 V | Q1 | | | ±100 | nA |
| | | $V_{GS}$ = +20/−16 V, $V_{DS}$ = 0 V | Q2 | | | ±100 | |
| **ON CHARACTERISTICS** | | | | | | | |
| $V_{GS(th)}$ | Gate−to−Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 50 µA | Q1 | 1.2 | 1.6 | 2.0 | V |
| | | $V_{GS}$ = $V_{DS}$, $I_D$ = 50 µA | Q2 | 1.2 | 1.6 | 2.0 | |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate−to−Source Threshold Voltage Temperature Coefficient | $I_D$ = 50 µA, referenced to 25°C | Q1 | | −6.19 | | mV/°C |
| | | $I_D$ = 50 µA, referenced to 25°C | Q2 | | −6.19 | | |
| $r_{DS(on)}$ | Drain−to−Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A | Q1 | | 7.3 | 9.0 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 8 A | | | 9.8 | 13 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 10 A, $T_J$ = 125°C | | | 12.7 | | |
| $r_{DS(on)}$ | Drain−to−Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A | Q2 | | 7.3 | 9.0 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 8 A | | | 9.8 | 13 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 10 A, $T_J$ = 125°C | | | 12.7 | | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 10 A | Q1 | | 53 | | S |
| | | $V_{DS}$ = 15 V, $I_D$ = 10 A | Q2 | | 53 | | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

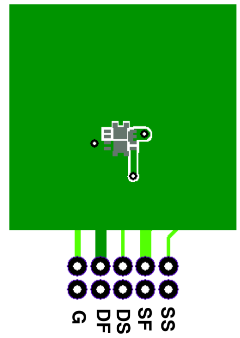
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{ISS}$ | Input Capacitance | Q1: $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1 Mhz<br>Q2: $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1 MHz | Q1 | | 948 | | pF |
| | | | Q2 | | 948 | | |
| $C_{OSS}$ | Output Capacitance | | Q1 | | 188 | | pF |
| | | | Q2 | | 188 | | |
| $C_{RSS}$ | Reverse Transfer Capacitance | | Q1 | | 12.3 | | pF |
| | | | Q2 | | 12.3 | | |
| $R_G$ | Gate Resistance | $T_A$ = 25°C | Q1 | | 2.0 | | Ω |
| | | | Q2 | | 2.0 | | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $td_{(ON)}$ | Turn−On Delay Time | Q1: $V_{DD}$ = 48 V, $I_D$ = 19 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 2.5 Ω<br>Q2: $V_{DD}$ = 48 V, $I_D$ = 19 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 2.5 Ω | Q1 | | 9.4 | | ns |
| | | | Q2 | | 9.4 | | |
| $t_r$ | Rise Time | | Q1 | | 5.8 | | ns |
| | | | Q2 | | 5.8 | | |
| $t_{D(OFF)}$ | Turn−Off Delay Time | | Q1 | | 12.8 | | ns |
| | | | Q2 | | 12.8 | | |
| $t_f$ | Fall Time | | Q1 | | 4.4 | | ns |
| | | | Q2 | | 4.4 | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V | Q1 | | 13.5 | | nC |
| | | | Q2 | | 13.5 | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V<br>Q1: $V_{DD}$ = 48 V, $I_D$ = 19 A<br>Q2: $V_{DD}$ = 48 V, $I_D$ = 19 A | Q1 | | 6.4 | | nC |
| | | | Q2 | | 6.4 | | |
| $Q_{gs}$ | Gate−to−Source Gate Charge | | Q1 | | 2.6 | | nC |
| | | | Q2 | | 2.6 | | |
| $Q_{gd}$ | Gate−to−Drain “Miller” Charge | | Q1 | | 2.8 | | nC |
| | | | Q2 | | 2.8 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10 A (Note 2) | Q1 | | 0.79 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 10 A (Note 2) | Q2 | | 0.79 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | Q1: $I_F$ = 19 A, di/dt = 100 A/μs<br>Q2: $I_F$ = 19 A, di/dt = 100 A/μs | Q1 | | 29 | | ns |
| | | | Q2 | | 29 | | |
| $Q_{rr}$ | Reverse Recovery Charge | | Q1 | | 14 | | nC |
| | | | Q2 | | 14 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

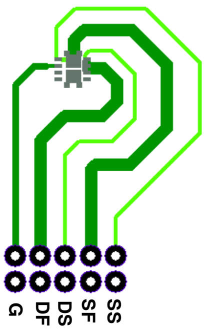
1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



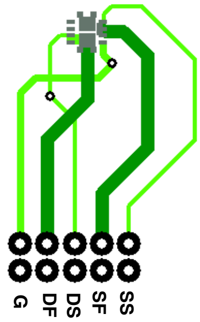

a) 70°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.




b) 70°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.




c) 135°C/W when mounted on a minimum pad of 2 oz copper.




d) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: $E_{AS}$ of 46 mJ is based on starting $T_J$ = 25°C; N−ch: L = 1 mH, $I_{AS}$ = 9.6 A, $V_{DD}$ = 60 V, $V_{GS}$ = 10 V. 100% test at L = 1 mH, $I_{AS}$ = 9.6 A.
   Q2: $E_{AS}$ of 46 mJ is based on starting $T_J$ = 25°C; N−ch: L = 1 mH, $I_{AS}$ = 9.6 A, $V_{DD}$ = 60 V, $V_{GS}$ = 10 V. 100% test at L = 1 mH, $I_{AS}$ = 9.6 A.
4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

## TYPICAL CHARACTERISTICS

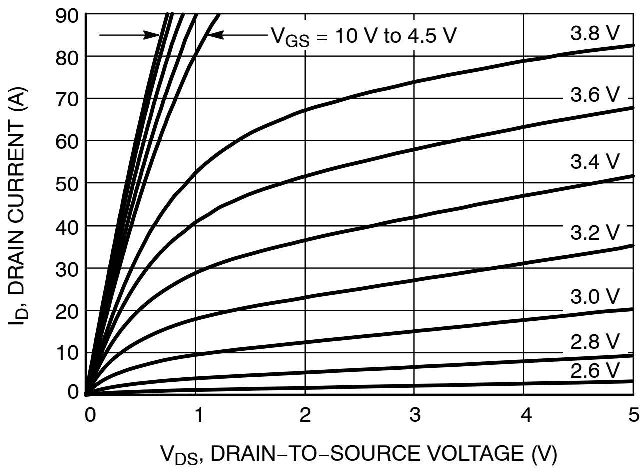



**Figure 1. On−Region Characteristics**

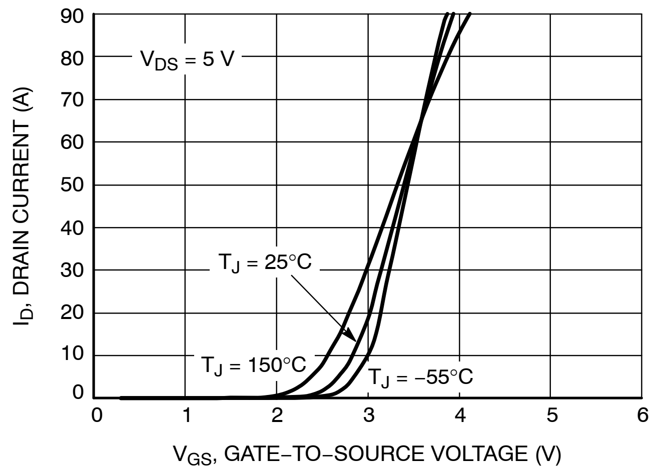



**Figure 2. Transfer Characteristics**

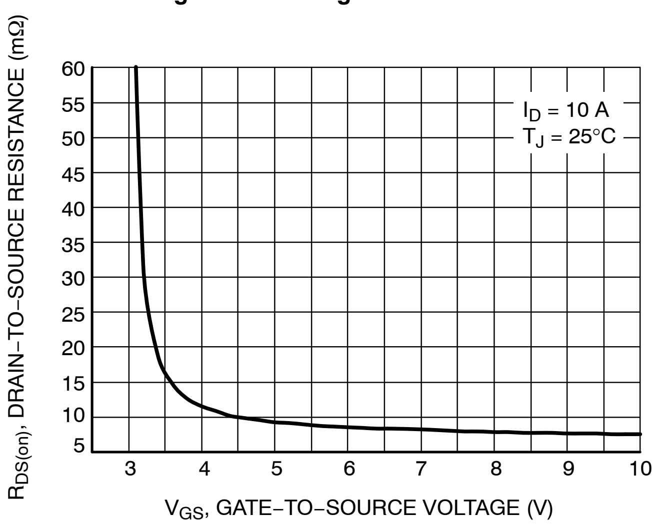



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

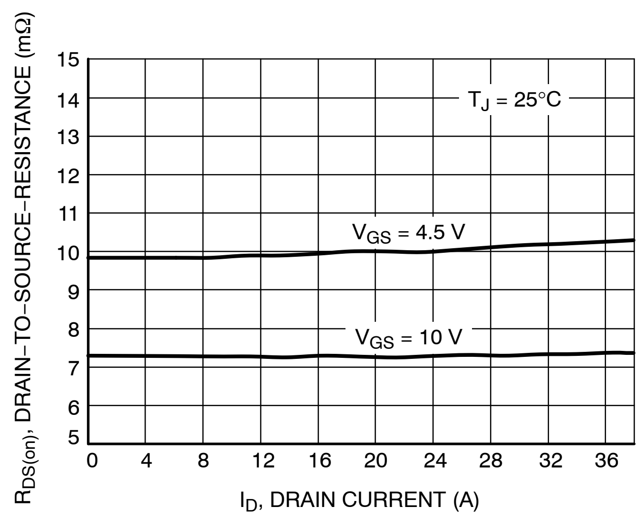



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

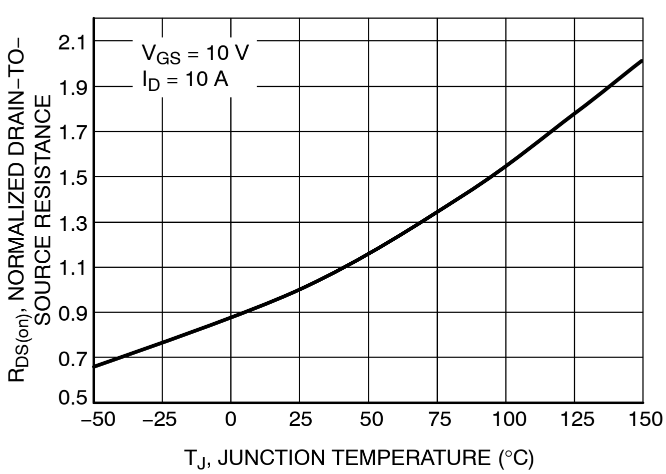



**Figure 5. On−Resistance Variation with Temperature**

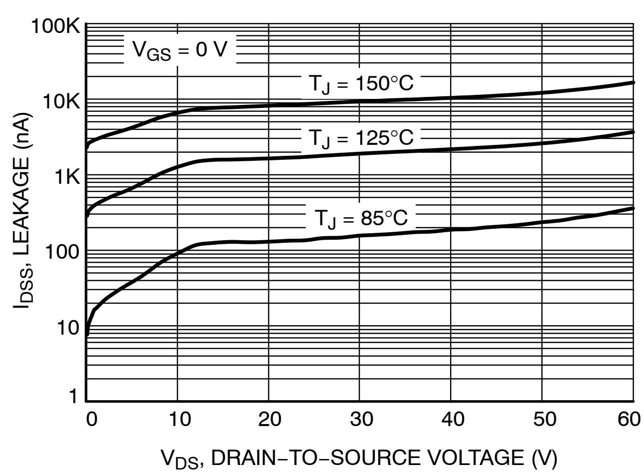



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

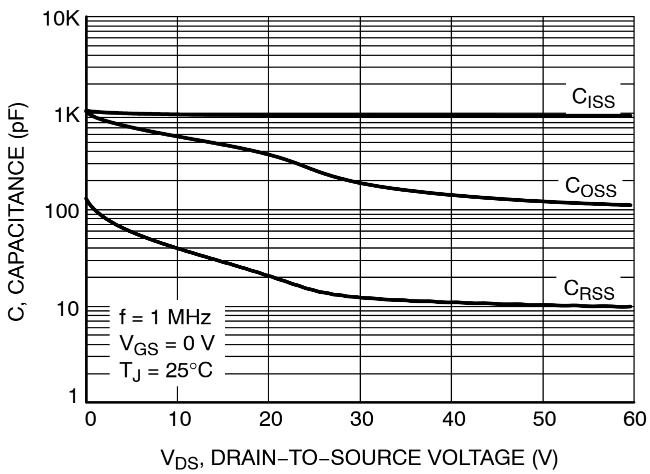



**Figure 7. Capacitance Variation**

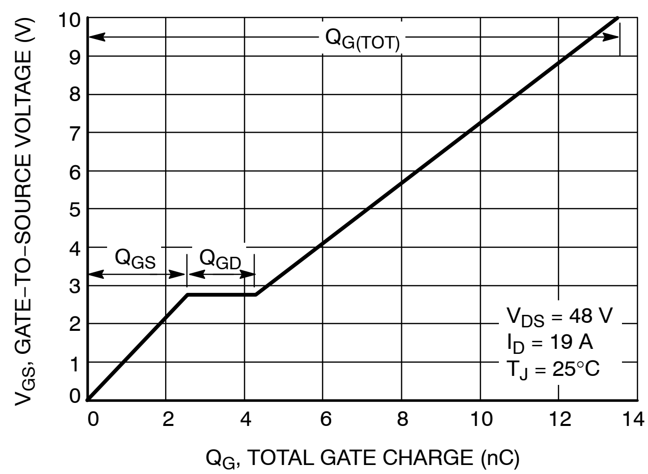



**Figure 8. Gate−to−Source vs. Total Charge**

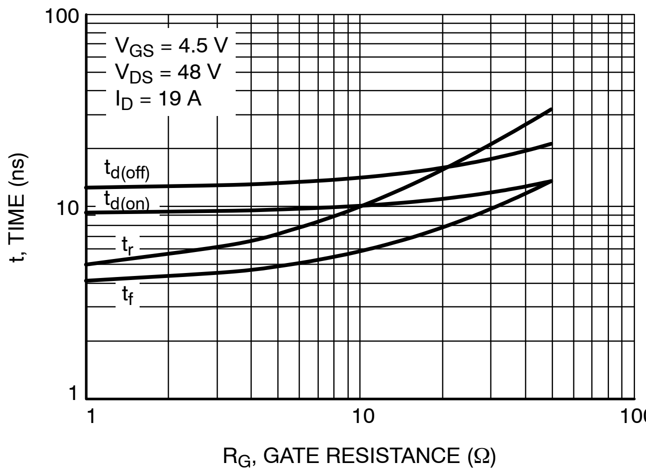



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

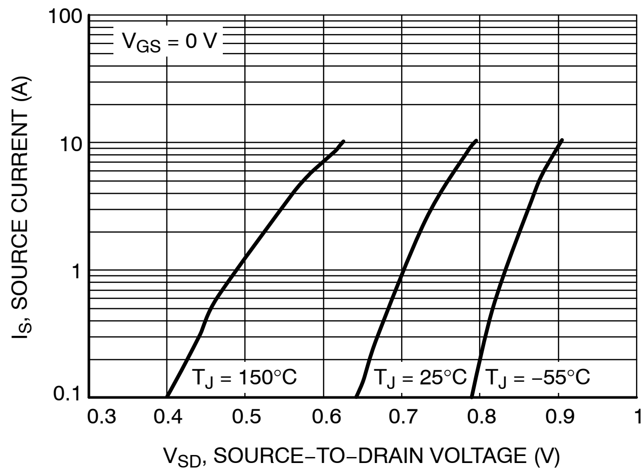



**Figure 10. Diode Forward Voltage vs. Current**

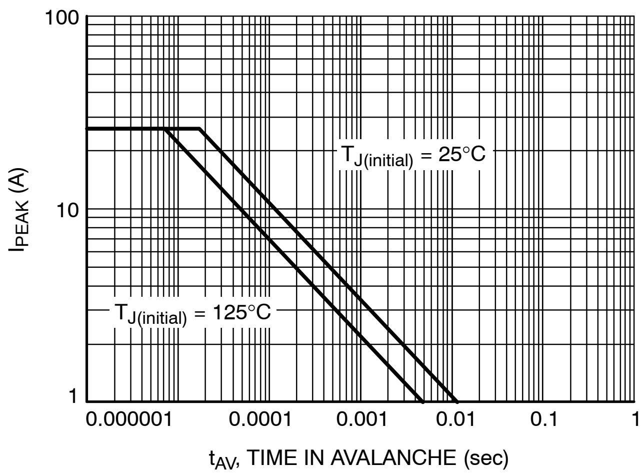



**Figure 11. Unclamped Inductive Switching Capability**

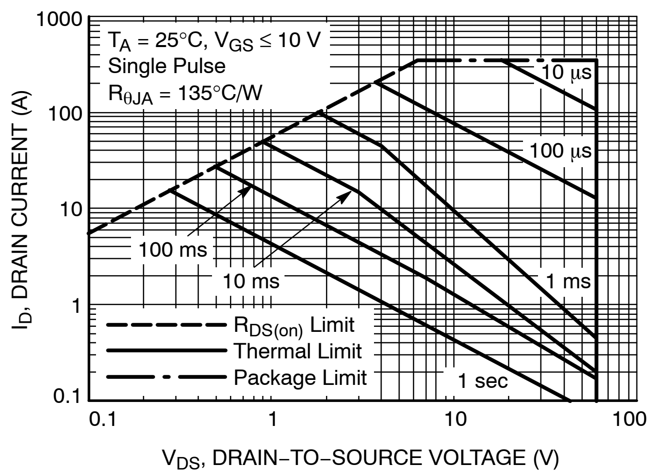



**Figure 12. Forward Bias Safe Operating Area**

## TYPICAL CHARACTERISTICS

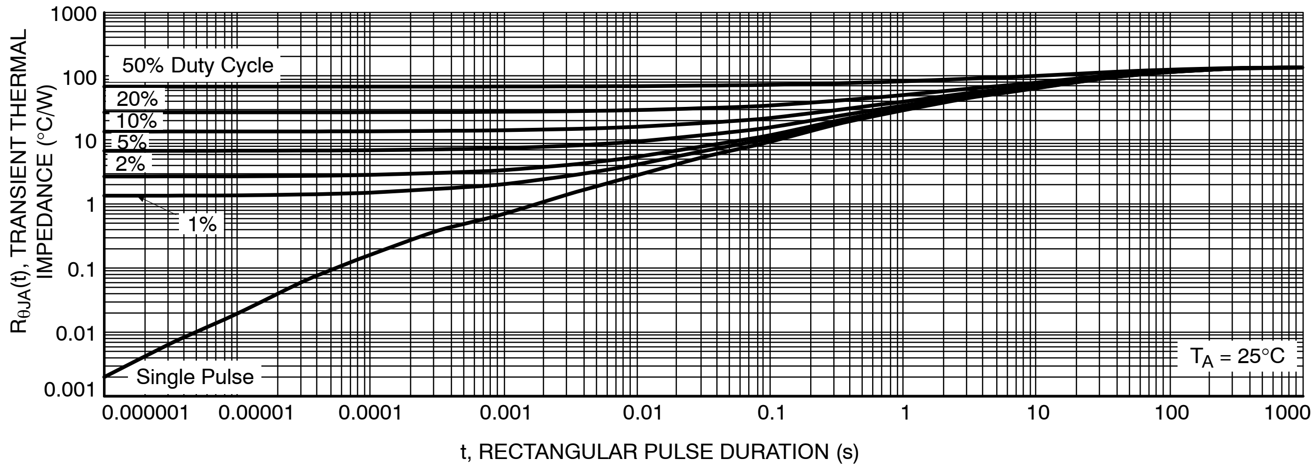



**Figure 13. Thermal Response**

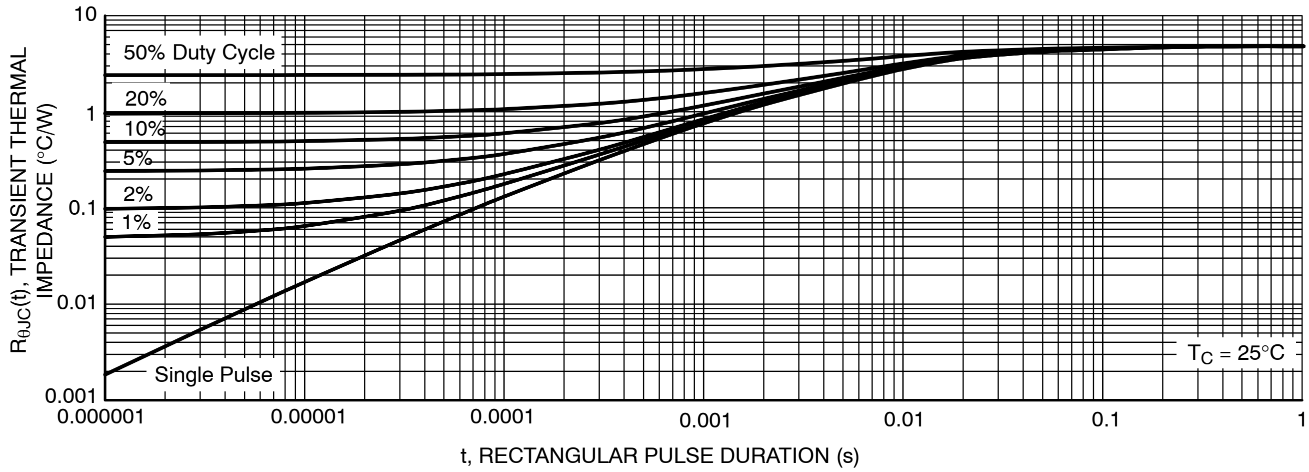



**Figure 14. Thermal Response**

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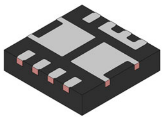
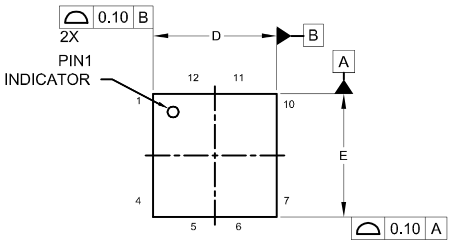


**WQFN12 3.3X3.3, 0.65P**
CASE 510CJ
ISSUE A

DATE 08 AUG 2022

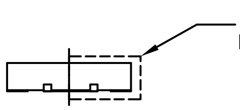



TOP VIEW

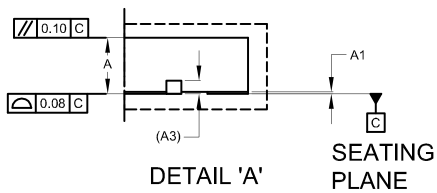
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

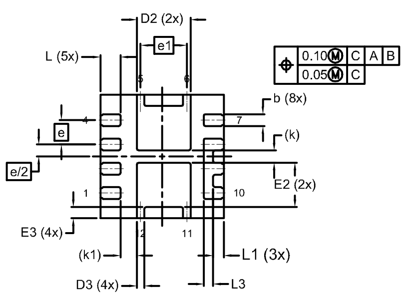
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | -- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.27 | 0.32 | 0.37 |
| D | 3.20 | 3.30 | 3.40 |
| D2 | 1.34 | 1.44 | 1.54 |
| D3 | 0.10 | 0.20 | 0.30 |
| E | 3.20 | 3.30 | 3.40 |
| E2 | 1.09 | 1.19 | 1.29 |
| E3 | 0.20 | 0.30 | 0.40 |
| e | 0.65 BSC | | |
| e/2 | 0.325 BSC | | |
| e1 | 1.24 BSC | | |
| k | 0.33 REF | | |
| k1 | 0.43 REF | | |
| L | 0.44 | 0.54 | 0.64 |
| L1 | 0.19 | 0.29 | 0.39 |
| L3 | 0.15 | 0.25 | 0.35 |



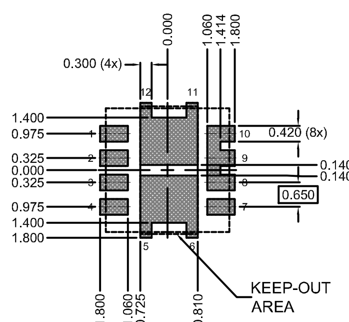

FRONT VIEW




DETAIL 'A'
SCALE 2:1



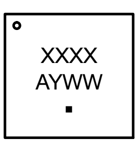

BOTTOM VIEW




LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON13806G | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | WQFN12 3.3X3.3, 0.65P | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT:** www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
www.onsemi.com/support/sales

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