THE DATASHEET OF

DK-START-5AGXB3N

Arria V GX Starter Kit

User Guide

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Additional Information

1. About This Kit

The Altera® Arria® V GX Starter Kit is a complete design environment that includes both the hardware and software you need to develop Arria V GX FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (up to 6.5536 Gbps).
- Develop and test PCI Express® (PCIe) 2.0 designs.
- Develop and test memory subsystems consisting of SyncFlash, SRAM, and DDR3.
- Develop and test SDI with the embedded 75-ohm 3G SDI transceivers.
- Develop embedded designs utilizing the Nios® II processor and external memory.
- Develop and test network designs utilizing Triple Speed Ethernet MegaCore® and external RJ-45 jack.
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 40 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO®, 10 Gigabit Ethernet, SONET, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI) and others.
- Measure the FPGA's power consumption.
- Control two programmable clock oscillators.
- Develop and test HDMI TX application with embedded TMDS level shifter capable of supporting data rate up to 2.7 Gbps.

Kit Features

This section briefly describes the Arria V GX Starter Kit contents.

Hardware

The Arria V GX Starter Kit includes the following hardware:

- Arria V GX starter board—A development platform that allows you to develop and prototype hardware designs running on the Arria V GX 5AGXFB3H4F35C4N FPGA.

  For detailed information about the board components and interfaces, refer to the *Arria V GX Starter Board Reference Manual*.

- Loopback and debug header daughter cards.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - 75 Ω SMB video cable
  - Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

Arria V GX Starter Kit Installer

The license-free Arria V GX Starter Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Installing the Arria V GX Starter Kit" on page 3–2.

The remaining chapters in this user guide lead you through the following Arria V GX starter board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the starter board
- Configuring the Arria V GX FPGA
- Running the Board Test System designs

For complete information about the starter board, refer to the *Arria V GX Starter Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Boards

To inspect the boards, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

In typical applications with the Arria V GX starter board, a heat sink is not necessary. However, under extreme conditions, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Arria V GX Starter Kit page.

- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Arria V GX device documentation, refer to the Documentation: Arria V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Arria V GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Arria V GX Starter Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including Qsys) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to the *Altera Software Installation and Licensing Manual*.

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the myAltera Account Sign In web page, and click **Sign In**.
2. On the myAltera Home web page, click the *Self-Service Licensing Center* link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code.

   The number consists of alphanumeric characters and does not contain hyphens: for example, *5xxxSoCxxxxxxx*.

4. On the Self-Service Licensing Center web page, click the *Find it with your License Activation Code* link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

For complete licensing details, refer to the *Altera Software Installation and Licensing Manual*.

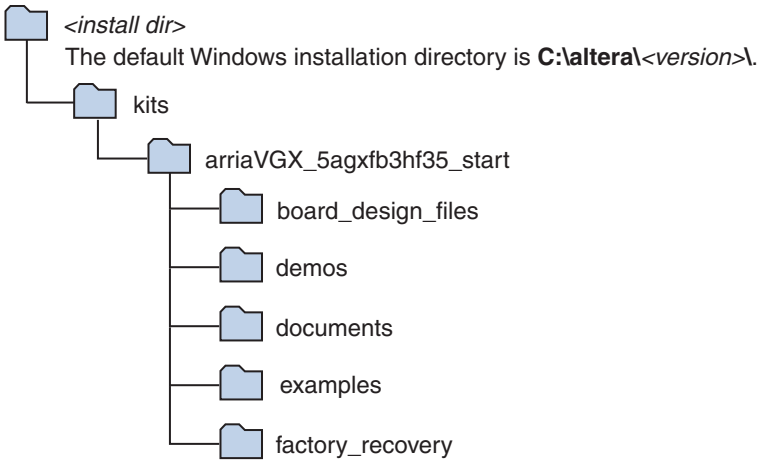
Installing the Arria V GX Starter Kit

To install the Arria V GX Starter Kit, perform the following steps:

1. Download the Arria V GX Starter Kit installer from the Arria V GX Starter Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Arria V GX Starter Kit installer **.exe** for Windows, or unzip the installation image for Linux.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Arria V GX Starter Kit directory structure shown in Figure 3–1.

Figure 3–1. Arria V GX Starter Kit Installed Directory Structure *(1)*



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Arria V GX Starter Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Arria V GX starter board includes integrated On-Board USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Starter Board Setup

The instructions in this chapter explain how to set up the Arria V GX starter board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Arria V GX starter board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The starter board ships with design examples stored in the flash memory device. Verify the DIP switch SW4.3 is set to the off (1) position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the DIP switch locations on the starter board.
3. Connect the +19 V, 6.32 A power adapter to the DC Power Jack (J17) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW5) to the on position. When power is supplied to the board, the blue LED (D30) illuminates indicating that the board has power.

The MAX V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. FAC_LOAD (SW4.3) controls which design to load. When the switch is in the factory off (1) position, the PFL loads the design from the factory portion of flash memory.

The kit includes a MAX V design which contains the MAX V PFL megafunction. The design resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples\max5** directory.

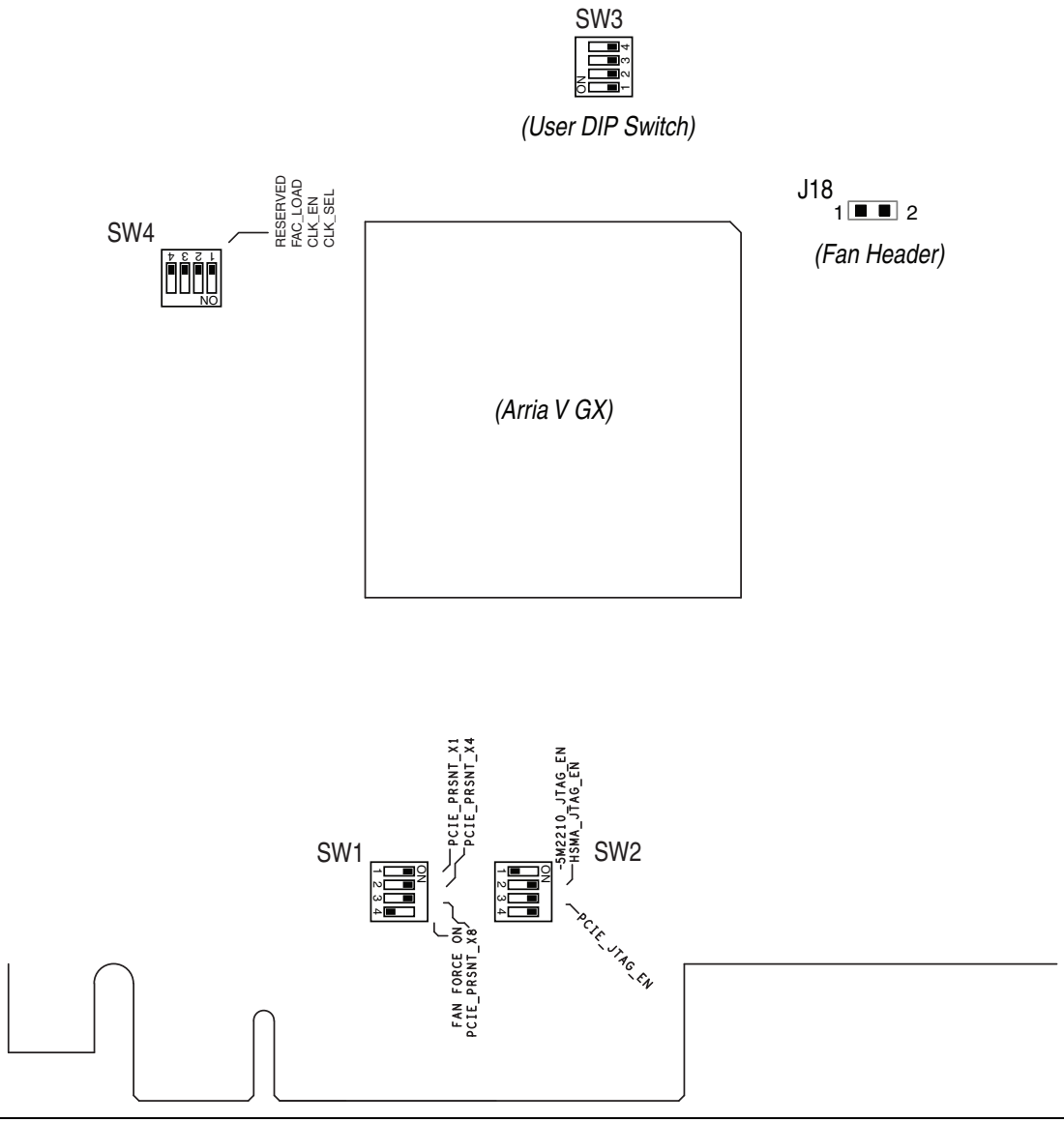
When configuration is complete, the Config Done LED (D12) illuminates, signaling that the Arria V GX device configured successfully.

For more information about the PFL megafunction, refer to the *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Arria V GX starter board. Figure 4–1 shows the switch locations and the default position of each switch.

Figure 4–1. Switch Locations and Default Settings (Detail)



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW1) to match Table 4–1 and Figure 4–1.

Table 4–1. SW1 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	PCIE_PRSNT_X1	Switch 1 has the following options: ■ When ON, x1 presence detect is enabled. ■ When OFF, x1 presence detect is disabled.	ON
2	PCIE_PRSNT_X4	Switch 2 has the following options: ■ When ON, x4 presence detect is enabled. ■ When OFF, x4 presence detect is disabled.	ON
3	PCIE_PRSNT_X8	Switch 3 has the following options: ■ When ON, x8 presence detect is enabled. ■ When OFF, x8 presence detect is disabled.	ON
4	FAN FORCE ON	Switch 4 has the following options: ■ When ON, a logic 0 is selected, fan is turned on. (Fan is not included in this kit.) ■ When OFF, logic 1 is selected, fan is turned off.	OFF

2. Set DIP switch bank (SW2) to match Table 4–2 and Figure 4–1.

Table 4–2. SW2 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	5M2210_JTAG_EN	Set to OFF to include the MAX V System Controller in the JTAG chain. Default is OFF (in chain).	OFF
2	HSMA_JTAG_EN	Set to OFF to include HSMC Port A in the JTAG chain. Default is ON (not in chain).	ON
3	PCIE_JTAG_EN	Set to OFF to include the PCI Express Edge Connector in the JTAG chain. Default is ON (not in chain).	ON
4	—	—	—

3. Set DIP switch bank (SW3) to match Table 4–3 and Figure 4–1.

Table 4–3. SW3 Dip Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	USER0	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
2	USER1	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Table 4–3. SW3 Dip Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	USER2	Switch 3 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
4	USER3	Switch 4 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

4. Set DIP switch bank (SW4) to match Table 4–4 and Figure 4–1.

Table 4–4. SW4 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	CLK_SEL	Switch 1 has the following options: ■ When ON, a logic 0 is selected, SMA input clock select. ■ When OFF, a logic 1 is selected, Programmable oscillator clock select.	OFF
2	CLK_EN	Switch 2 has the following options: ■ When ON, a logic 0 is selected, on-board oscillator disable. ■ When OFF, a logic 1 is selected, on-board oscillator enable.	OFF
3	FAC_LOAD	Switch 3 has the following options: ■ When OFF, a logic 1 is selected, load the factory design of Arria V device from flash at power up. ■ When ON, a logic 0 is selected, load the user design from flash at power up.	OFF
4	RESERVED	Switch 4 has no function.	OFF

For more information about the FPGA board settings, refer to the *Arria V GX Starter Board Reference Manual*.

5. Board Update Portal

The Arria V GX Starter Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the FAC_LOAD (SW4.3) in the factory off (1) position, the Arria V GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides useful kit-specific links and design resources.

After successfully updating the user hardware 1 flash memory, you can load the user design from flash memory into the FPGA. To do so, set the FAC_LOAD (SW4.3) to the user on (0) position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the FAC_LOAD (SW4.3) to the factory off (1) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   You can click *Arria V GX Starter Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Arria V GX Starter Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Arria V GX Starter Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the FAC_LOAD (SW4.3) to the user on (0) position, and power cycle the board.

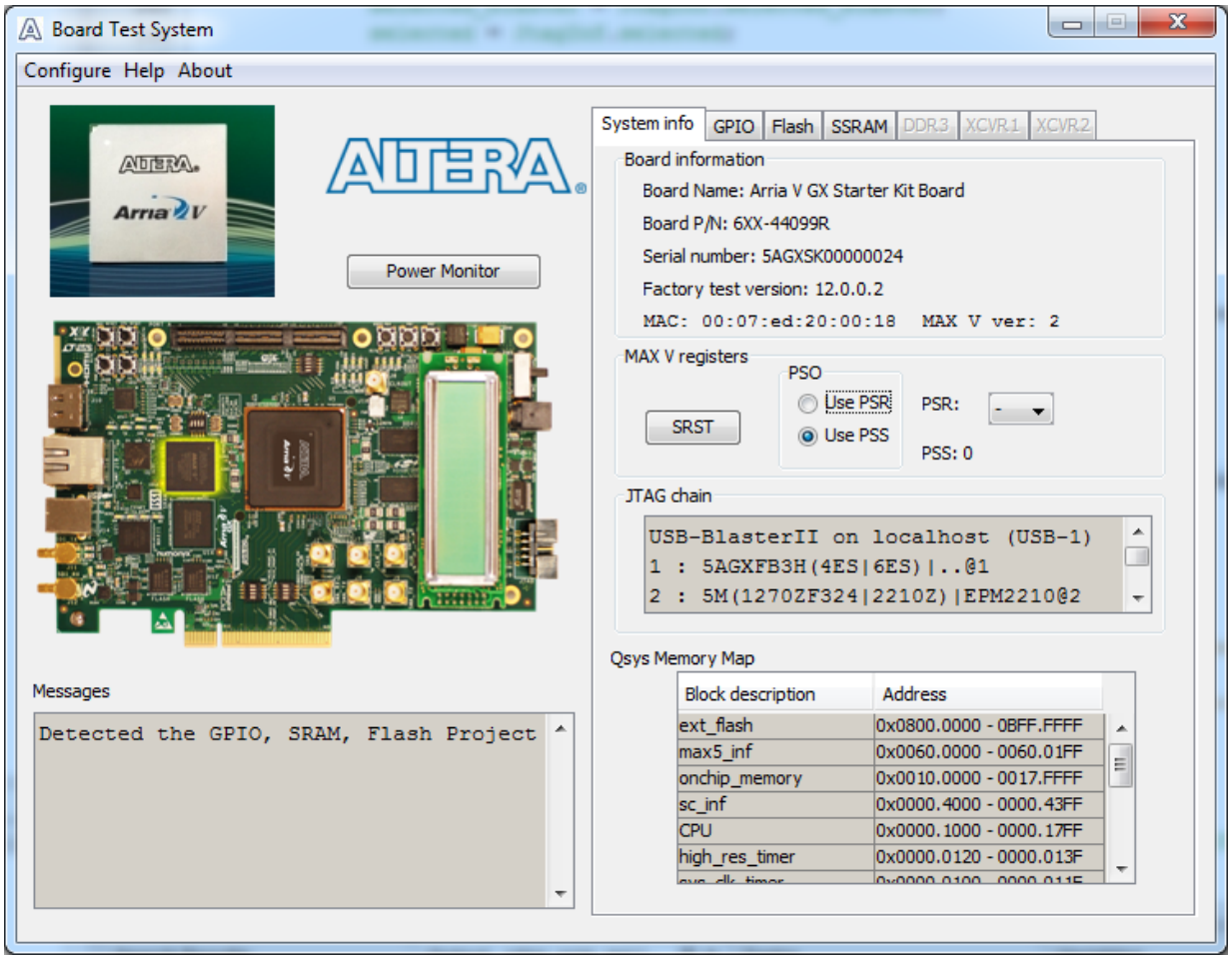
As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The development kit includes an application called the Board Test System (BTS) and related design examples. The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. (While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) To install the BTS, follow the steps in "Installing the Arria V GX Starter Kit" on page 3–2.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Arria V GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX V device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, following these steps:

1. Connect the USB cable to the board.
2. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch Settings" section starting on page 4–2, except for DIP switch SW4.3, which should be set the FAC_LOAD (SW4.3) to the user on (0) position.

   For more information about the board's DIP switch and jumper settings, refer to the *Arria V GX Starter Board Reference Manual*.

3. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO and flash memory tests.

   CAUTION

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GX Starter Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Arria V GX starter board's flash memory ships preconfigured with the design that corresponds to the GPIO, Flash, and SRAM tabs.

If you power up your board with the FAC_LOAD (SW4.3) in a position other than the user on (0) position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

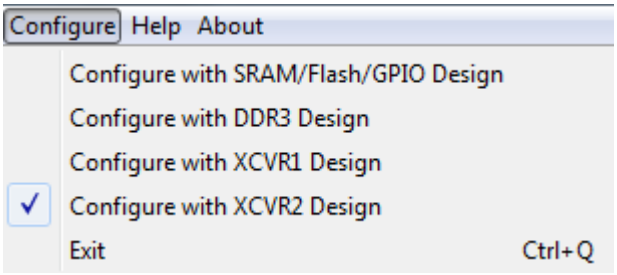
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 6–2) to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's Raw Binary File (**.rbf**) to the FPGA.
3. When configuration finishes, close the Quartus II Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Quartus II Programmer for configuration, rather than the Board Test System GUI, you may need to restart the Board Test System.

The System Info Tab

The **System Info** tab shows board's current configuration (Figure 6–1 on page 6–1). The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** controls display static information about your board.

- **Board Name**—Indicates the official name of the board, given by the Board Test System.
- **Board P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAC**—Indicates the MAC address of the board.
- **MAX V ver**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples** directory. Newer revisions of this code might be available on the Arria V GX Starter Kit page of the Altera website.

MAX V Registers

The **MAX V registers** control allows you to view and change the current MAX V register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX V Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the up to three (0-2) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PGM LED (D24-D26) based on the following encoding: ■ 0 = PGM LED (D24) and corresponds to the flash memory page for the factory hardware design ■ 1 = PGM LED (D25) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PGM LED (D26) and corresponds to the flash memory page for the user hardware 2 design

- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values. Refer to Table 6–1 for more information.

- **PSO**—Sets the MAX V PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX V PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.
- **PSS**—Displays the MAX V PSS register value. Refer to Table 6–1 for the list of available options.

Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Arria V GX device is always the first device in the chain. The JTAG chain is normally mastered by the On-board USB-Blaster II.

If the JTAG chain cannot be detected using the On-Board USB-Blaster II, refer to the initialization instructions on the USB-Blaster Driver for Windows 7 and Windows Vista web page or the USB-Blaster and USB-Blaster II Drivers for Windows XP web page.

If you plug in an external USB-Blaster cable to the JTAG header (J9), the On-Board USB-Blaster II is disabled.

DIP switch SW2 selects which interfaces are in the chain. Refer to Table 4–2 on page 4–3 for detailed settings.

For details on the JTAG chain, refer to the *Arria V GX Starter Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

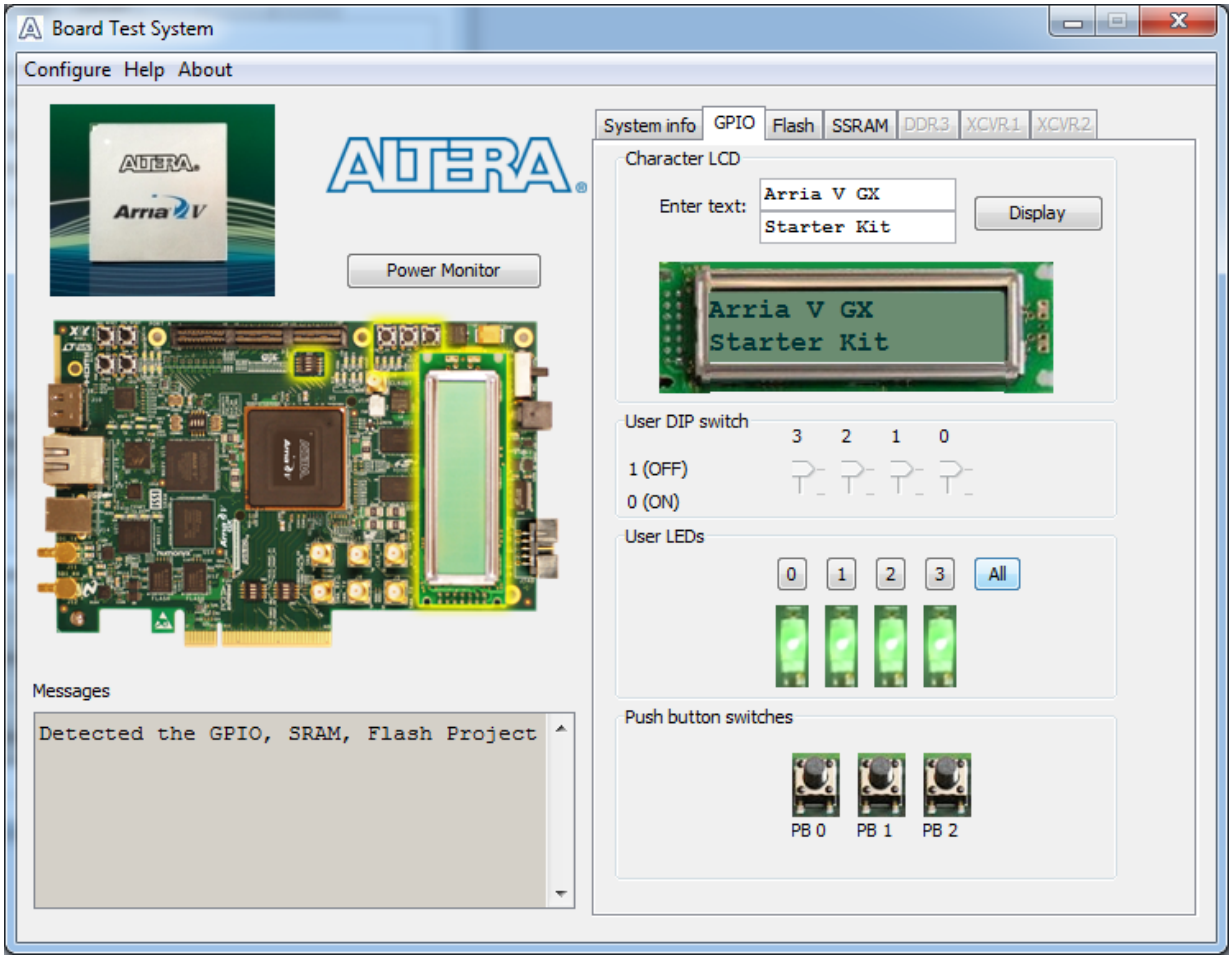
Qsys Memory Map

The **Qsys memory map** control shows the memory map of the Qsys system on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank (SW3). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Click the number buttons for the LEDs to turn the board LEDs on and off. You can click **ALL** to turn on and off all of the user LEDs at once.

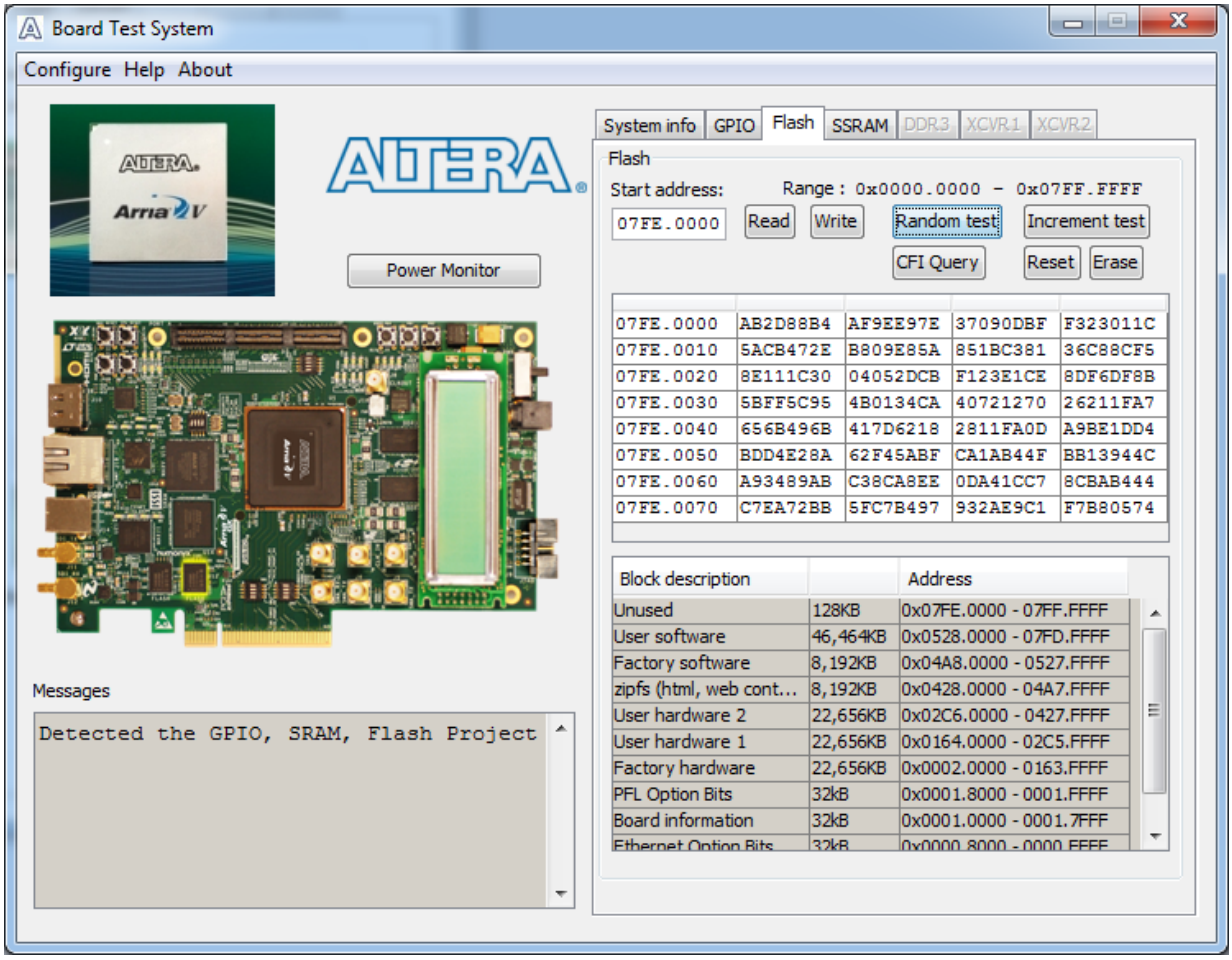
Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6–4 shows the **Flash** tab.

Figure 6–4. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.

If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory, which is limited to a scratch page in the upper 128K block.

Data Display/Entry Boxes

There are 8 rows and 4 columns. Each column contain 8 hexadecimal numbers. After entering the numbers in each cell, press Enter on your keyboard. Then click **Write** and **Read** button.

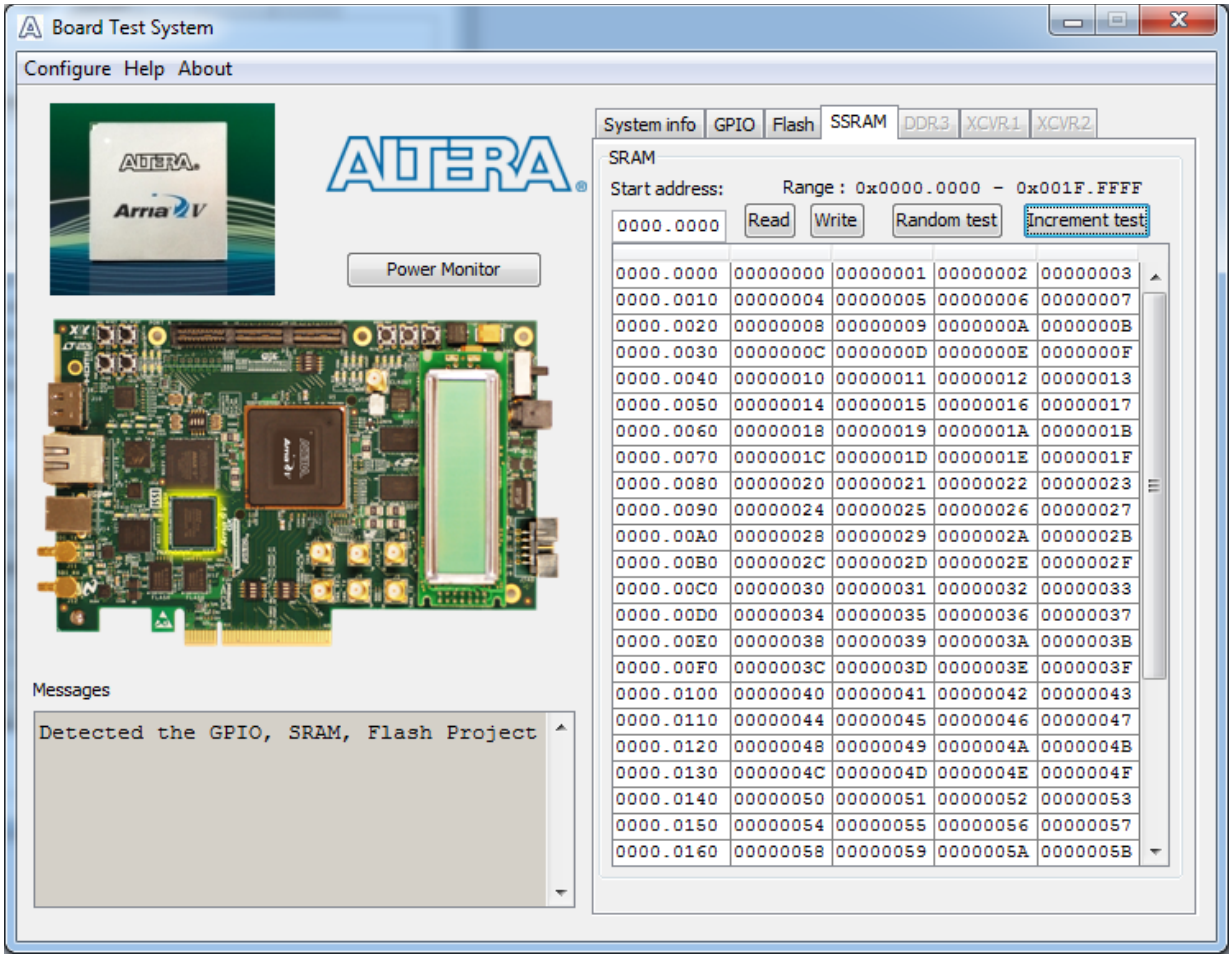
Flash Memory Map

Displays the U12 flash device memory map for the Arria V GX Starter Kit.

The SSRAM Tab

The **SSRAM** tab allows you to read and write SSRAM and flash memory on your board. Figure 6–5 shows the **SSRAM** tab.

Figure 6–5. The SSRAM Tab



The following sections describe the controls on the **SSRAM** tab.

Read

The **Read** control reads the SSRAM on your board. To see the SSRAM contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.

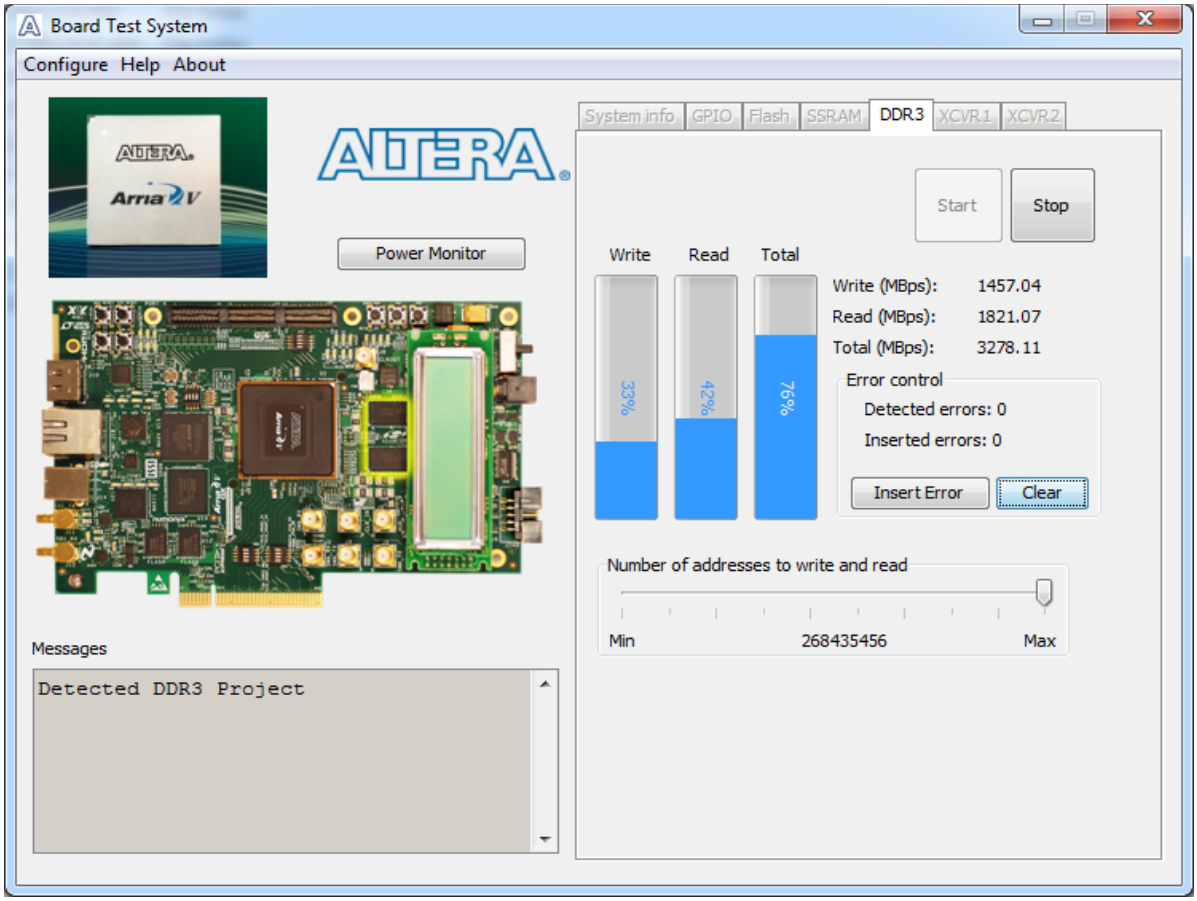
Write

The **Write** control writes the SSRAM on your board. To update the SSRAM contents, change values in the table and click **Write**. The application writes the new values to SSRAM and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

The DDR3 Tab

The **DDR3** tab allows you to read and write the DDR3 memory on your board. Figure 6–6 shows the **DDR3** tab.

Figure 6–6. The DDR3 Tab



The following sections describe the controls on the **DDR3** tab.

Start

The **Start** control initiates DDR3 memory transaction performance analysis.

Always click **Clear** before **Start**.

Stop

The **Stop** control terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last pressed **Start**:

- **Write**, **Read**, and **Total** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

- **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**—Show the number of bytes of data analyzed per second.

Error Control

The **Error Control** control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transaction stream.
- **Insert Error**—Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

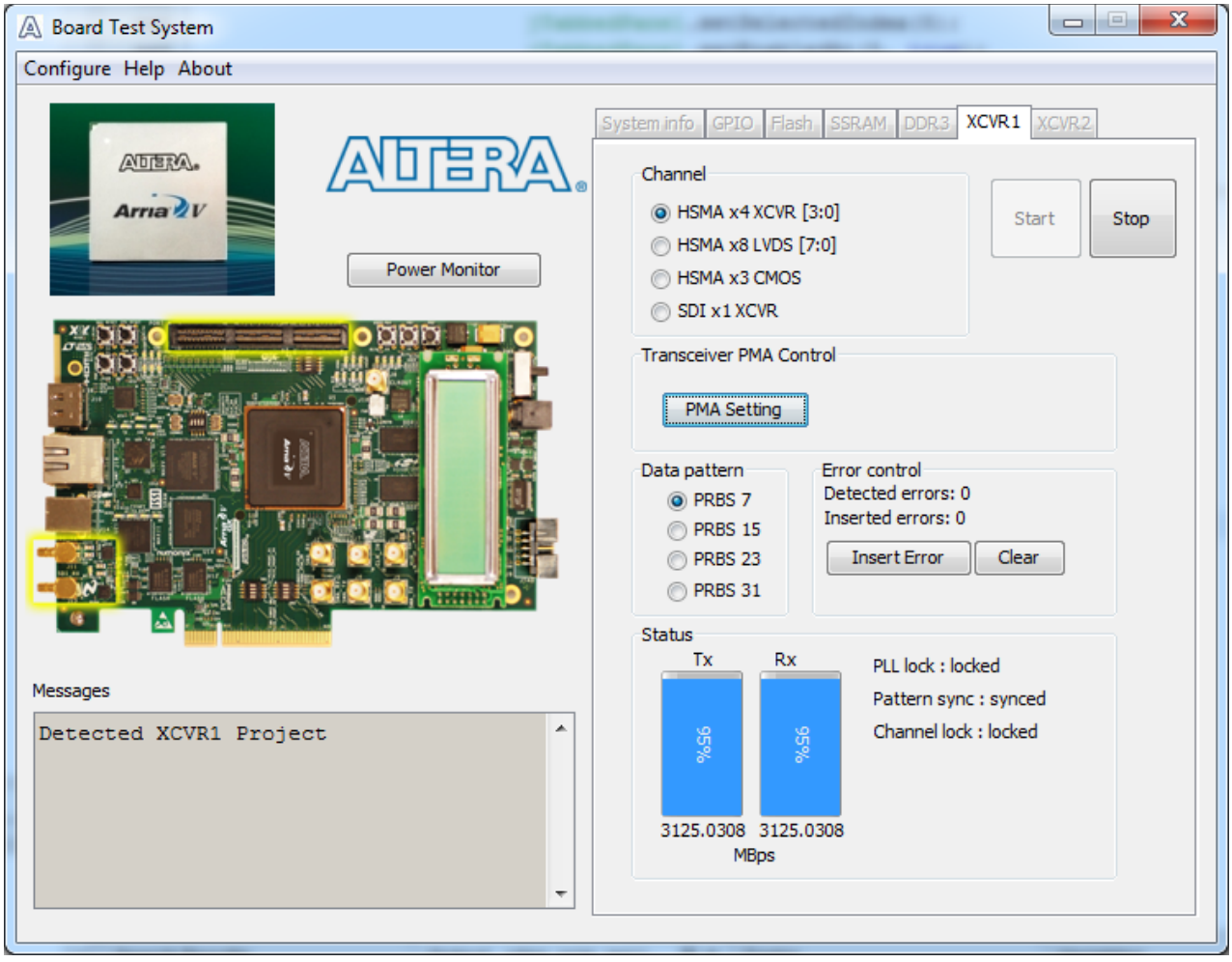
Number of Addresses to Write and Read

The **Number of addresses to write and read** control determines the number of addresses to use in each iteration of reads and writes.

The XCVR1 Tab

The **XCVR1** tab allows you to perform loopback tests on the HSMC and SDI ports. Figure 6–7 shows the **XCVR1** tab.

Figure 6–7. The XCVR1 Tab



You must have the loopback HSMC installed on the HSMC connector Port A and the SDI loopback cable for all tests to function in external loopback mode. Otherwise, set the PMA setting tab to test internal loopback mode (serial loopback = 1).

The following sections describe the controls on the **XCVR1** tab.

Channel

The **Channel** control allows you to specify which interface to test. The following port tests are available:

- **HSMA x4 XCVR [3:0]**
- **HSMA x8 LVDS [7:0]**
- **HSMA x3 CMOS**

- **SDI x1 XCVR**

Start

The **Start** control initiates the active port transaction performance analysis.

☞ Always click **Clear** before **Start.**

Stop

The **Stop** control terminates transaction performance analysis.

PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver to the transmitter. Enter the following values to enable the serial loopbacks:

  0 = High speed serial transceiver signals to loopback on the board
  1 = Serial loopback (internal loopback)
  2 = Reverse serial loopback pre-CDR
  4 = Reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Pattern

The **Data Pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error Control** control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.

- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

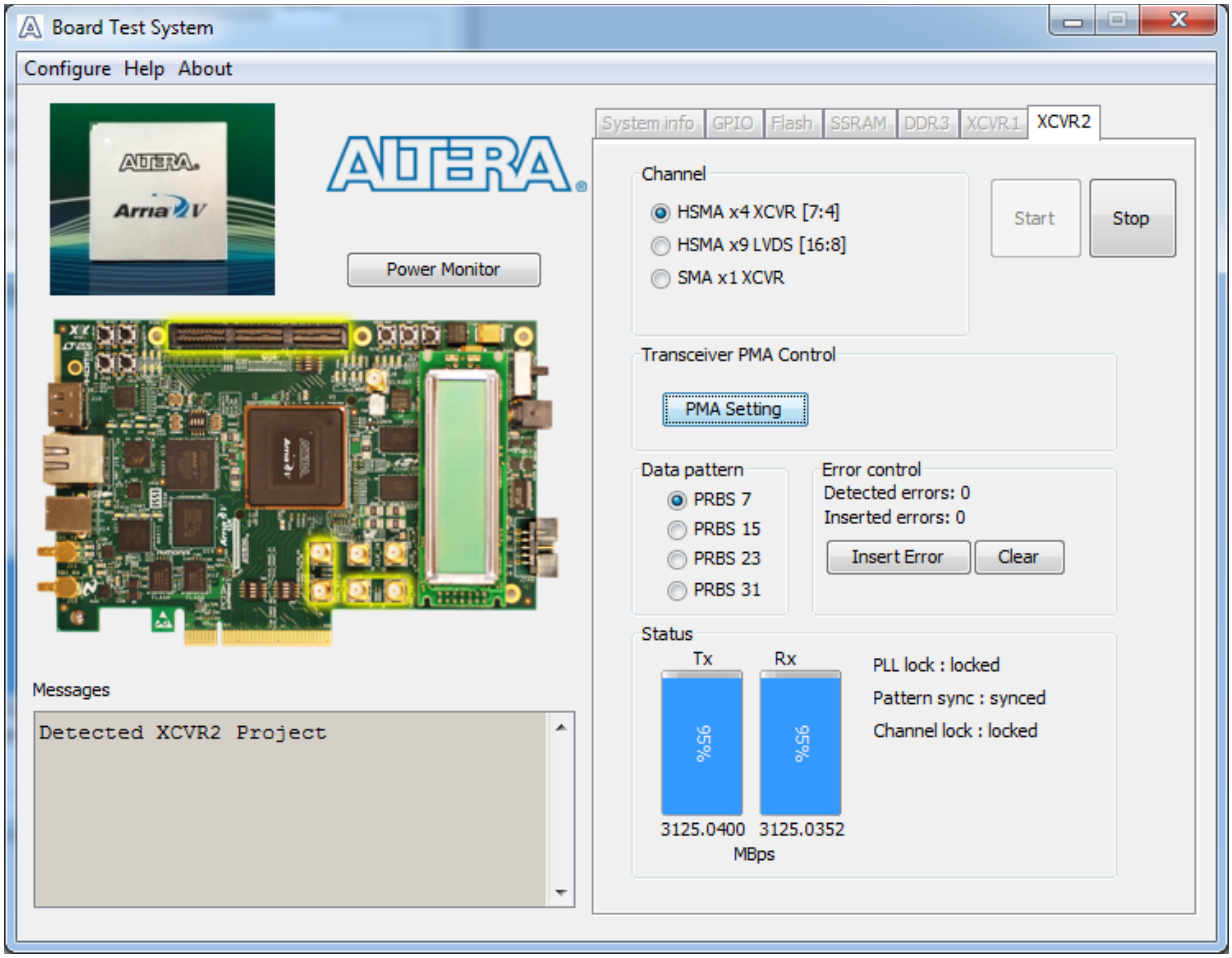
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected after channel lock is acquired.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded, and all TX and RX PLL lanes are phase locked to data; RX lanes are word aligned and deskewed.

The XCVR2 Tab

The **XCVR2** tab allows you to perform loopback tests on the HSMC and SMA ports. Figure 6–8 shows the **XCVR2** tab.

Figure 6–8. The XCVR2 Tab



You must have the loopback HSMC installed on the HSMC connector Port A and the SMA loopback cable for all tests to function in external loopback mode. Otherwise, set the PMA setting tab to test internal loopback mode (serial loopback = 1).

The following sections describe the controls on the **XCVR2** tab.

Channel

The **Channel** control allows you to specify which interface to test. The following port tests are available:

- **HSMA x4 XCVR [7:4]**
- **HSMA x9 LVDS [16:8]**
- **SMA x1 XCVR**

Start

The **Start** control initiates the active port transaction performance analysis.

Always click **Clear** before **Start.**

Stop

The **Stop** control terminates transaction performance analysis.

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver to the transmitter. Enter the following values to enable the serial loopbacks:

  0 = High speed serial transceiver signals to loopback on the board
  1 = Serial loopback (internal loopback)
  2 = Reverse serial loopback pre-CDR
  4 = Reverse serial loopback post-CDR

- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Pattern

The **Data Pattern** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences.
- **PRBS 15**—Selects pseudo-random 15-bit sequences.
- **PRBS 23**—Selects pseudo-random 23-bit sequences.
- **PRBS 31**—Selects pseudo-random 31-bit sequences.

Error Control

The **Error Control** control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Status

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **PLL lock**—Shows the PLL locked or unlocked state.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected after channel lock is acquired.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded, and all TX and RX PLL lanes are phase locked to data; RX lanes are word aligned and deskewed.

The Power Monitor

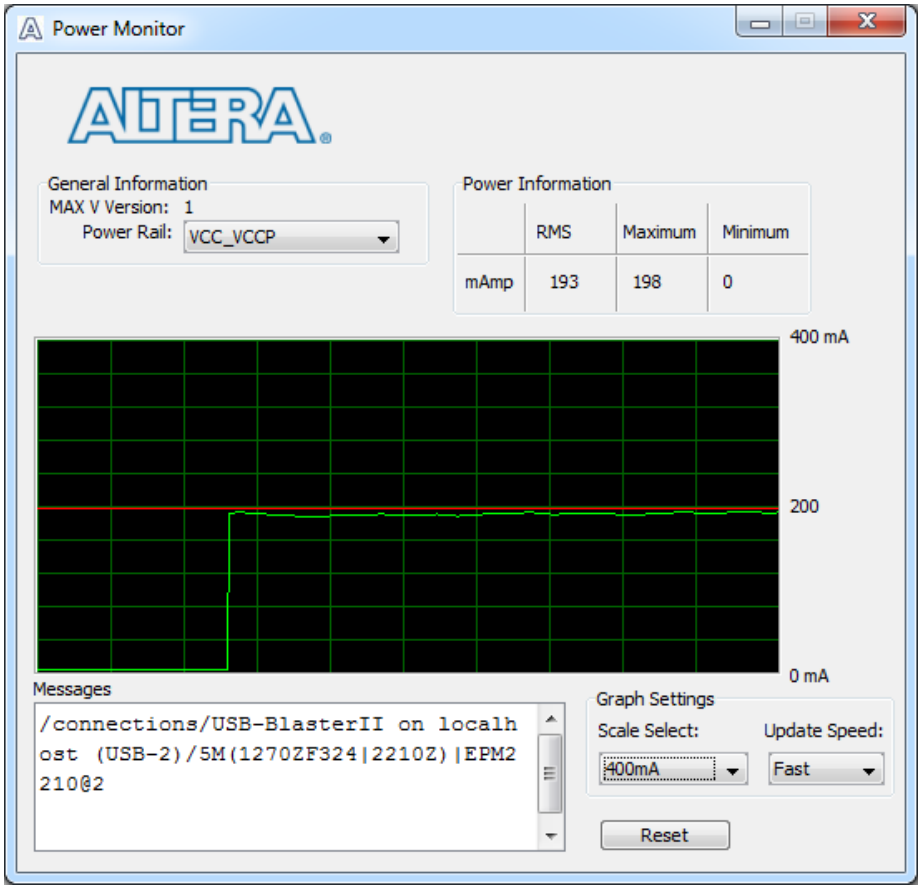
The Power Monitor measures and reports current power information. To start the application, click **Power Monitor** in the Board Test System application.

You can also run the Power Monitor as a stand-alone application. **PowerMonitor.exe** resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GX Starter Kit** <*version*> > **Power Monitor** to start the application.

The Power Monitor communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the Arria V GX FPGA device is consuming.

Figure 6–9 shows the Power Monitor.

Figure 6–9. The Power Monitor



The following sections describe the Power Monitor controls.

General Information

The **General information** controls display the following information about the MAX V device:

- **MAX V version**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery** and <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples\max5** directories. Newer revisions of this code might be available on the Arria V GX Starter Kit page of the Altera website.
- **Power rail**—Selects the power rail to measure. After setting the **Power rail** list to the desired rail, click **Reset** to refresh the screen with new board readings.

A table with the power rail switch positions/information is available in the *Arria V GX Starter Board Reference Manual*.

Power Information

The **Power information** control displays current, maximum, and minimum power readings for the following unit:

- **mAmp**

Power Graph

The power graph displays the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

Graph Settings

The following **Graph settings** controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

Reset

This **Reset** control clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

The Clock Control

The Clock Control application sets the Si571 programmable oscillator to any frequency between 10 MHz and 810 MHz with eight digits of precision to the right of the decimal point.

The Si5338 device has four independently programmable outputs. All four outputs are programmable between 16 KHz and 350 MHz. All four outputs can support the higher frequencies, but they cannot be programmed for multiple frequencies above 350 MHz. If you want multiple outputs above 350 MHz, all outputs above 350 MHz must be the same frequency, and must be frequencies from 367 MHz to 473.33 MHz or from 550 MHz to 710 MHz. Channel 0 of Si5338 drives a 2-to-4 buffer that drives a copy of the clock to all four edges of the FPGA.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\examples\board_test_system** directory. On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GX Starter Kit** <*version*> > **Clock Control** to start the application.

For more information about the Si5338/Si571 and the Arria V GX starter board's clocking circuitry and clock input pins, refer to the *Arria V GX Starter Board Reference Manual*.

The Clock Control communicates with the MAX V device on the board through the JTAG bus. The Si571 programmable oscillator is connected to the MAX V device through a 2-wire serial bus. Clock frequencies will return to the default values after power cycling the board. Figure 6–10 and Figure 6–11 shows both tabs of the Clock Control.

Figure 6–10. The Clock Control - U4 Tab

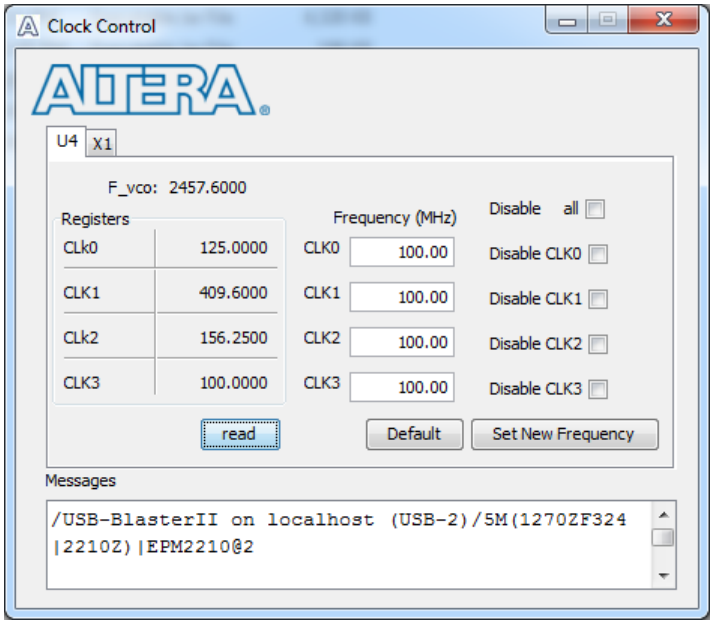
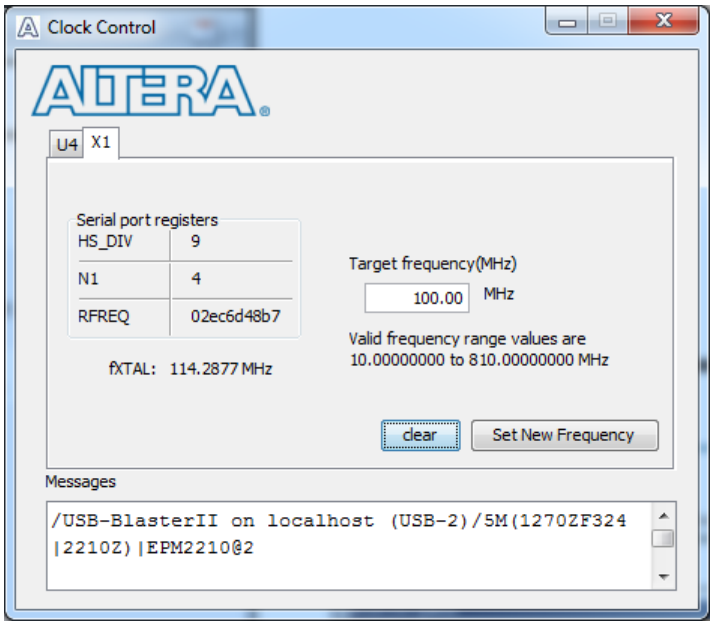


Figure 6–11. The Clock Control - X1 Tab



The following sections describe the Clock Control controls.

Serial Port Registers

The **Serial port registers** control shows the current values from the Si571 registers.

For more information about the Si571 registers, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

fXTAL

The **fXTAL** control shows the calculated internal fixed-frequency crystal, based on the serial port register values.

For more information about the f_{XTAL} value and how it is calculated, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

Target Frequency

The **Target frequency** control allows you to specify the frequency of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

Read

This control reads the current frequency setting for the oscillator associated with the active tab.

Clear/Default

This control sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set New Frequency

This control sets the programmable oscillator frequency for the selected clock to the value in the **Target frequency** control for the Si571 and the **Frequency** controls for the Si5338 (U4). Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with your own **.sof**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster II driver are installed on the host computer, the USB cable is connected to the starter board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Arria V GX FPGA, perform the following steps:

1. Start the Quartus II Programmer.

2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

☞ Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

☞ If the Quartus II programming window is already open, and then you power cycle the board, you may be required to click **Hardware Setup** in the Quartus II Programmer window and reselect USB-Blaster II in order to properly detect the JTAG chain.

A. Programming the Flash Memory Device

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Arria V GX starter board and how to reprogram the user portions of the flash memory device.

The Arria V GX starter board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.

For more information about Altera development tools, refer to the Design Software page of the Altera website.

CFI Flash Memory Map

Table A–1 shows the default memory contents of the 1-Gb CFI flash device (U12). Each flash device has a 16-bit data bus, and the two combined flash devices allow for a 32–bit flash memory interface. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A–1. Byte Address Flash Memory Map of U12

Block Description	Size KB	Address Range
Board Test System scratch	128	0x07FE.0000 - 0x07FF.FFFF
User software	46,464	0x0528.0000 - 0x07FD.FFFF
Factory software	8,192	0x04A8.0000 - 0x0527.FFFF
zipfs (html, web content)	8,192	0x0428.0000 - 0x04A7.FFFF
User hardware 2	22,656	0x02C6.0000 - 0x0427.FFFF
User hardware 1	22,656	0x0164.0000 - 0x02C5.FFFF
Factory hardware	22,656	0x0002.0000 - 0x0163.FFFF
PFL option bits	32	0x0001.8000 - 0x0001.FFFF
Board information	32	0x0001.0000 - 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 - 0x0000.FFFF
User design reset vector	32	0x0000.0000 - 0x0000.7FFF

CAUTION

Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to "Restoring the Flash Device to the Factory Settings" on page A–4.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the Arria V GX Starter Kit page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user hardware 1 and user software locations of the flash memory.

For more information about Nios II EDS software tools and practices, refer to the Embedded Software Development page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:
   - For Quartus II **.sof** files at user hardware 1 location:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x01640000
--pfl --optionbit=0x00018000 --programmingmode=FPP↵
```

   - For Quartus II **.sof** files at user hardware 2 location:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x02C60000
--pfl --optionbit=0x00018000 --programmingmode=FPP↵
```

   - For Nios II **.elf** files:

```
elf2flash --base=0x00000000 --end=0x07FFFFFF --reset=0x05280000
--input=<yourfile>_sw.elf --output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_sources/boot_loader_cfi.sre
c↵
```

The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.

CAUTION

If you have **.elf** files for both user hardware 1 and user hardware 2 design, you need to make sure the user software `--reset` location doesn't occupy a flash location that contains the image of another user software design file.

The Board Update Portal standard **.flash** format conventionally uses either <*filename*>**_hw.flash** for hardware design files or <*filename*>**_sw.flash** for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "Using the Board Update Portal to Update User Designs" on page 5–2 for more information.

If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Set the DIP switch FAC_LOAD (SW4.3) to the factory off (1) position (factory design) to load the Board Update Portal design from flash memory on power up.
2. Attach the USB-Blaster cable and power up the board.
3. If the board has powered up and the LCD displays either *Connecting...* or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the Config Done LED (D12) does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.
4. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–21 for more information.
5. Click **Add File** and select <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery\a5gx_starter_fpga_bup_top.sof**.
6. Turn on the **Program/Configure** option for the added file.
7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D12) illuminates indicating that the flash device is ready for programming.
8. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
9. In the Nios II command shell, navigate to the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery** directory (or to the directory of the **.flash** files you created in "Creating Flash Files Using the Nios II EDS" on page A–2) and type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_hw.flash ↵
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x00000000 <yourfile>_sw.flash ↵
```

11. Set the DIP switch FAC_LOAD (SW4.3) to the user on (0) position position and power cycle the board. The Config Done LED (D12) illuminates indicating that the flash device is ready for programming.

Programming the board is now complete.

For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the starter board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.
2. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–21 for more information.
3. Click **Add File** and select <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery\a5gx_starter_fpga_bup_top.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D12) illuminates indicating that the flash device is ready for programming.
6. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.
7. In the Nios II command shell, navigate to the <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery** directory and type the following command to run the restore script:

   ```
   ./restore.sh ↵
   ```

   Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.
8. After all flash programming completes, cycle the POWER switch (SW5) off then on.
9. Using the Quartus II Programmer, click **Add File** and select <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery\a5gx_starter_fpga_bup_top.sof**.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The Config Done LED (D12) illuminates indicating that the flash device is ready for programming.
12. Cycle the POWER switch (SW5) off then on to load and run the restored factory design.
13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

```
nios2-terminal ↵
```

and follow the instructions in the terminal window to generate a unique MAC address.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Arria V GX Starter Kit page of the Altera website.

Restoring the MAX V CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX V CPLD on the starter board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.
2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select <*install dir*>**\kits\arriaVGX_5agxfb3hf35_start\factory_recovery\max5.pof**.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Arria V GX Starter Kit page of the Altera website.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
November 2014	1.3	Updated SW1 (PCIe) default switch settings.
February 2013	1.2	Updates for CE compliance.
October 2012	1.1	Update for production silicon.
July 2014	1.0	Preliminary release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.

Visual Cue	Meaning
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.

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