THE DATASHEET OF

LMR22007YYZFT

LMR22007 2.7V - 20V, 750mA Step-Down Converter with Adjustable Input Current Limit

Check for Samples: LMR22007

FEATURES

- **High efficiency**
  - **Greater than 90% at 12 V_{IN} to 5 V_{OUT}**
- **Adjustable input current limit from 150mA to 600mA**
- **Input voltage range: 2.7V to 20V**
- **Adjustable output voltage from 0.9V to 5.5V**
- **Up to 750 mA output current**
- **Ultra low quiescent current (18µA typical)**
- **Ultra low shutdown current (300nA typical)**
- **< +/-2% V_{OUT} ripple at no load**
- **< +/-1% V_{OUT} ripple at full load**
- **Internal compensation, Soft-start and Thermal Shutdown**
- **Solution size less than 26mm^2**
  - **Low BOM count with small external components**
- **Wafer Chip Scale Package (WCSP)**
- **Light load power save mode**
- **Set frequency of 2.1 MHz (typical)**

APPLICATIONS

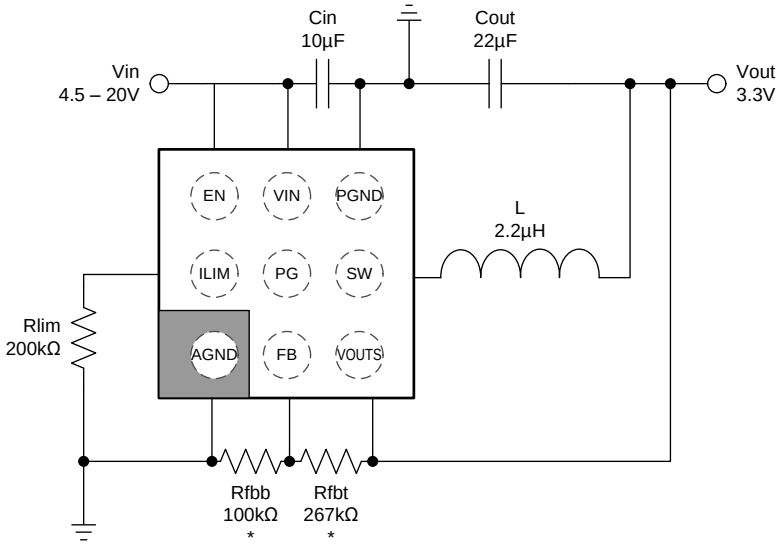
- **3.3V, 5V and 12V Interface**
- **POL Supply from Single or Multiple Li-Ion Battery**
- **Solid-State Disk Drives**
- **LDO Replacement**
- **Mobile PC's, Tablet, Modems, Cameras**

DESCRIPTION

The LMR22007 is a switching regulator designed for the high-efficiency requirement of applications with stand-by and shut-down modes. The device features a low-current mode to maintain efficiency under light-load conditions, and an adaptive on-time control architecture for fast transient response.

The LMR22007 can deliver up to 750mA of continuous load current with an adjustable input current limit. The device has a wide input voltage range of 2.7V to 20V, and supports V_{IN} transients to 24V. Other features include internal compensation, internal soft start, input under-voltage protection, internal bootstrap diode, and thermal shutdown.

TYPICAL APPLICATION



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ABSOLUTE MAXIMUM RATINGS (1)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage range (2)	VIN, SW, PG	-0.3	24	V
	EN	-0.3	24	
	V_{OUT}	-0.3	6	
	FB, ILIM	-0.3	3.3	
Power good sink current	PG		10	mA
Temperature range	Operating junction temperature range, T_J	-40	125	°C
	Storage temperature range, Tstg	-65	150	
ESD rating (1)	HBM Human body model		2	kV
	CDM Charge device model		0.5	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. All voltages are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage range	VIN, EN, PG	2.7	20	V
	V_{OUT}	0.9	5.5	
Power Good sink current	PG		100	µA
Temperature range	Operating junction temperature range, T_J	-40	125	°C

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise

THERMAL METRIC (1)			UNIT
θ_{JA}	Junction-to-ambient thermal resistance	72.3	°C/W
θ_{JB}	Junction-to-board characterization parameter	32.5	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

Min and Max Limits apply over the junction temperature (T_J) range of -40°C to +125°C, typical values at VIN = 12V and TA = 25°C (unless otherwise noted)

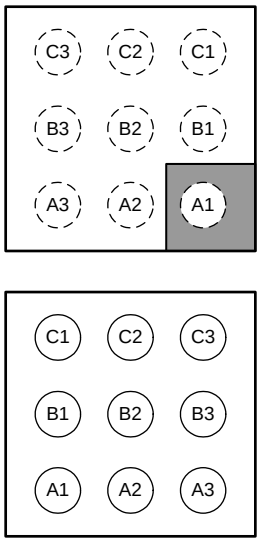
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Regulation and Over-Voltage Comparator						
V_{FB}	In-regulation feedback voltage	I_{OUT} = 0.5A, T_J -40°C to 85°C	0.891	0.9	0.909	V
		I_{OUT} = 0.5A, T_J -40°C to 125°C	0.886	0.9	0.914	
I_{FB}	Feedback input bias current			0.25		nA
Quiescent Current						
I_Q	Non Switching Quiescent Current	Non Switching		18	100	µA
I_{SD}	Shut down	V_{EN} = 0V, T_J = -40°C to 85°C		0.3	2	µA
V_{IN} Under Voltage Lockout (UVLO)						
V_{UVLO}	VIN Under Voltage Lockout	VIN Rising threshold		2.3	2.6	V
$V_{UVLO-HYS}$	VIN UVLO Hysteresis			269		mV

ELECTRICAL CHARACTERISTICS (continued)

Min and Max Limits apply over the junction temperature (T_J) range of -40°C to +125°C, typical values at VIN = 12V and TA = 25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Softstart						
SS	Internal soft-start time	V_{OUT} 10% to 90%, T_J -40°C to 85°C	1.4	3.3	5	ms
Power Good						
RPG	Power Good Pull-Down Resistance	I_{OUT} = 5mA, EN = 2V			70	Ohms
VPG_Rising	Power Good Pin is floating when VFB rises above this voltage			0.855		V
VPG_Falling	Power Good Pin is pulled low when VFB falls below this voltage			0.812		V
Switch Frequency Range						
f_{SW}				2.09		MHz
Ton	Minimum on time of NMOS high-side Switch			77		ns
Toff	Minimum off time of NMOS low-side Switch	T_J = 25°C			157	ns
D-max	The Max Duty Cycle of the high side NMOS FET	I_{OUT} = 750mA		80		%
Switch Characteristics						
$R_{DSON-NMOS-HIGH}$	High Side NMOS switch on-resistance			0.141	0.21	Ω
$R_{DSON-NMOS-LOW}$	Low side NMOS switch on-resistance			0.1	0.144	Ω
Input Current limit						
I_{LIMIN}	Open Loop Input current limit	R_{LIM} = 15kΩ, VIN = 12V, T_J = 25°C	925	1000	1150	mA
I_{LIMIN_HOT}	Open Loop Input current limit	R_{LIM} = 15kΩ, VIN = 12V, T_J = 125°C		907		
I_{LIMIN_COLD}	Open Loop Input current limit	R_{LIM} = 15kΩ, VIN = 12V, T_J = -40°C		1084		
Current limit for NMOS switch devices						
$I_{LIMIT-\ LOWSIDE}$	Current limit for short circuit and faults	T_J = 25°C	900	977		mA
$I_{LIMIT-LOWSIDE\_HOT}$	Current limit for short circuit and faults	T_J = 125°C		858		
$I_{LIMIT-LOWSIDE\_COLD}$	Current limit for short circuit and faults	T_J = -40°C		1008		
Enable Control						
V_{EN}	Enable threshold-Rising	V_{EN} Rising		0.662	0.9	V
	Enable threshold-Falling	V_{EN} Falling	0.4	0.612		V

9 Bump WCSP Package, Bump size 300 µm, 0.5mm pitch
Top View and Bottom View



PIN FUNCTIONS

NO.	NAME	TYPE(1)	DESCRIPTION
A1	AGND	G	Ground reference for all internal circuitry.
A2	ILIM	I	Connect to ground through a resistor to adjust input current limit, see applications information. DO NOT FLOAT.
A3	EN	I	The device is in shutdown mode when voltage to the EN pin is <0.4V and enabled when >0.9V. Do not leave this pin floating. Maximum operating voltage on this pin is 20V.
B1	FB	I	Divide down the output voltage with a resistor divider to 0.9 and connect to this pin.
B2	PG	O	Power good flag. Open drain connection of an internal pull-down MOSFET. Tie a resistor from the desired logic voltage to the PG pin. The pin will float when the FB pin is greater than 0.855V. The pin will be pulled down when VIN > 2.5V and the FB pin is less than 0.812V.
B3	VIN	P	Input voltage to the device. Connect directly to closely placed input bypass capacitor.
C1	VOUT	I	Connect to the regulated output voltage.
C2	SW	O	Connection to the external inductor.
C3	PGND	G	Power ground connection to internal half bridge. Connect directly to closely placed input bypass capacitor.

TYPICAL CHARACTERISTICS

Input Current Limit vs V_{IN}
V_{OUT} = 1.2V

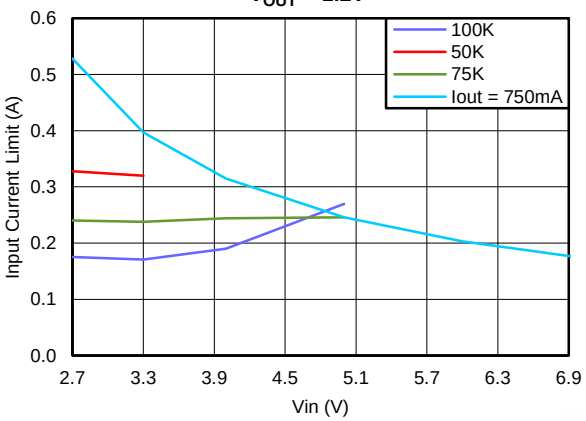


Figure 1.

Input Current Limit vs V_{IN}
V_{OUT} = 2.5V

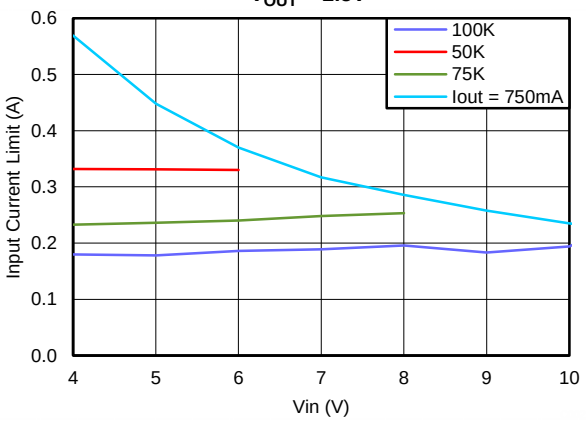


Figure 2.

TYPICAL CHARACTERISTICS (continued)

Input Current Limit vs V_{IN}
V_{OUT} = 3.3V

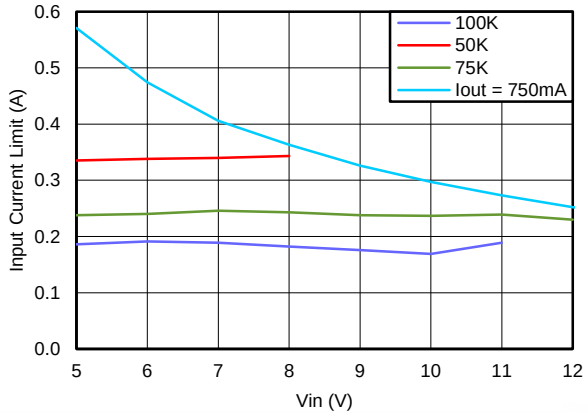


Figure 3.

Input Current Limit vs V_{IN}
V_{OUT} = 5V

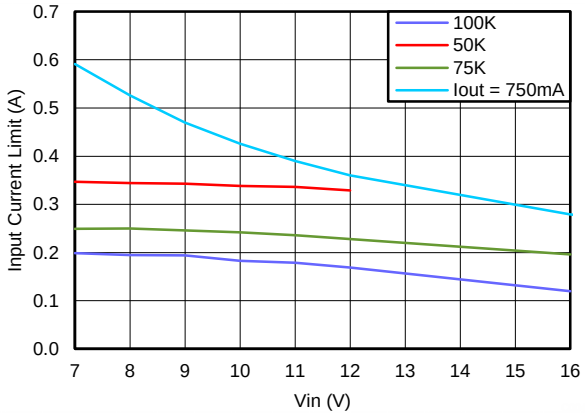


Figure 4.

Power Dissipation 5V

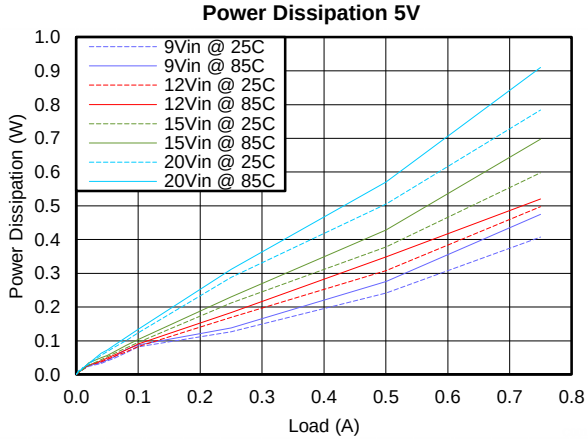


Figure 5.

V_{OUT} Regulation 5V

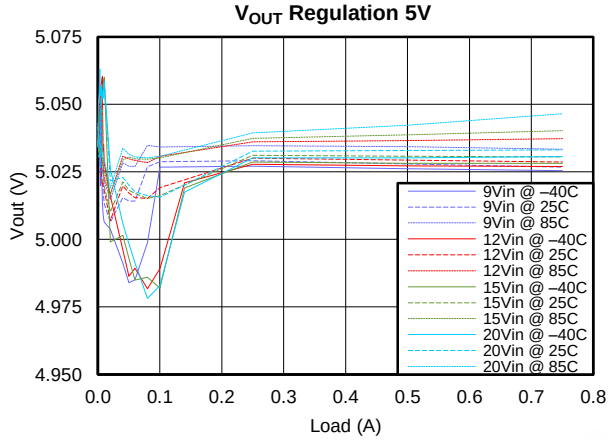


Figure 6.

Efficiency 5V @85°C

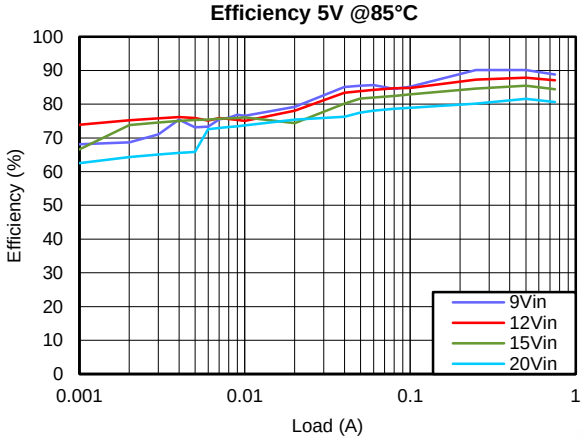


Figure 7.

Efficiency 5V @25°C

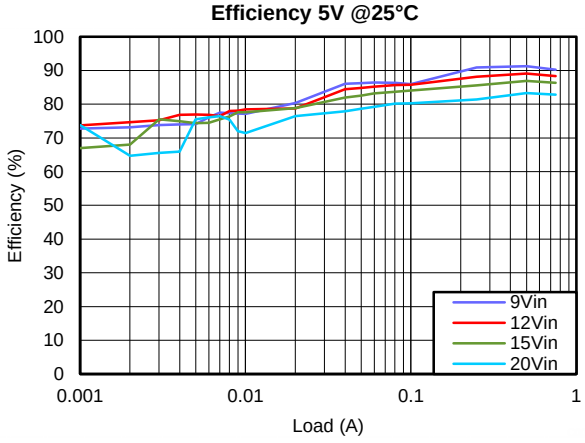


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Efficiency 5V @-40°C

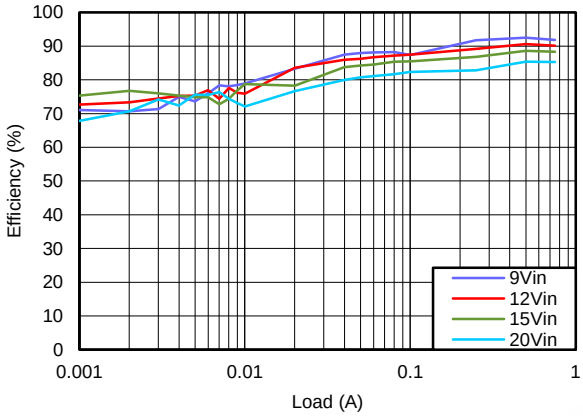


Figure 9.

Power Dissipation 3.3V

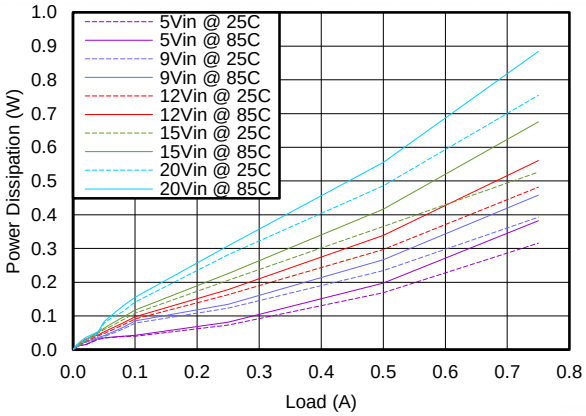


Figure 10.

Efficiency 3.3V @85°C

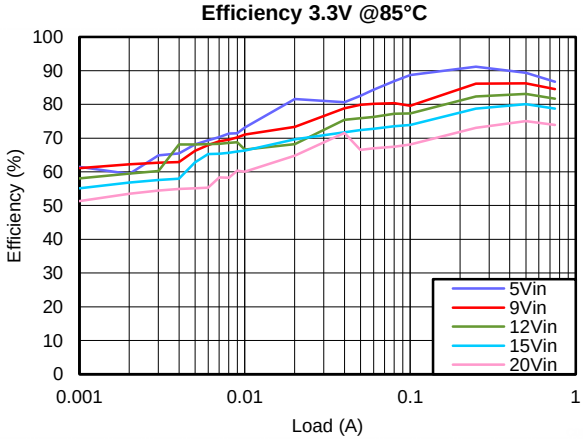


Figure 11.

Efficiency 3.3V @25°C

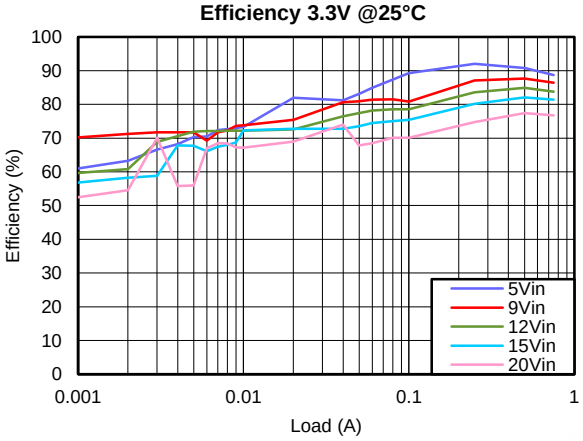


Figure 12.

Power Dissipation 2.5V

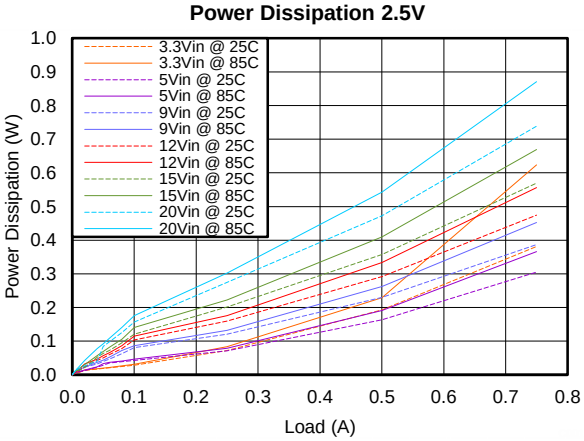


Figure 13.

Efficiency 2.5V @85°C

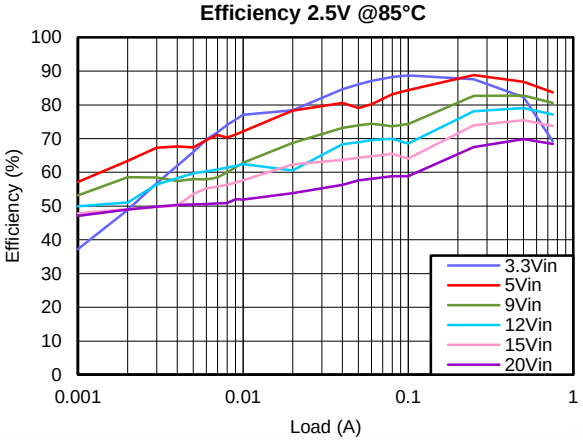


Figure 14.

TYPICAL CHARACTERISTICS (continued)

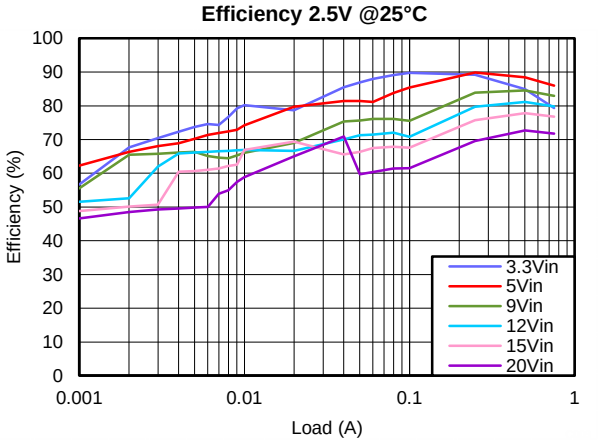


Figure 15.

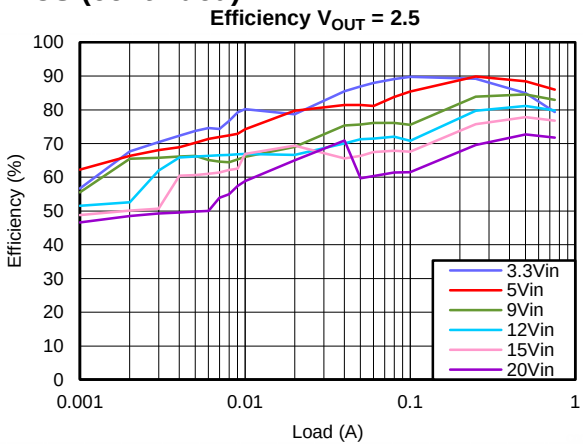


Figure 16.

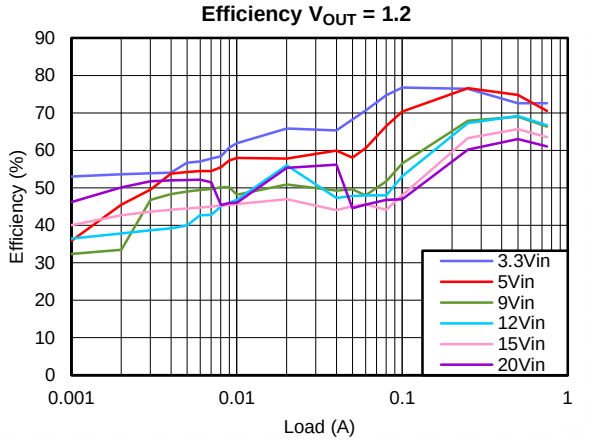


Figure 17.

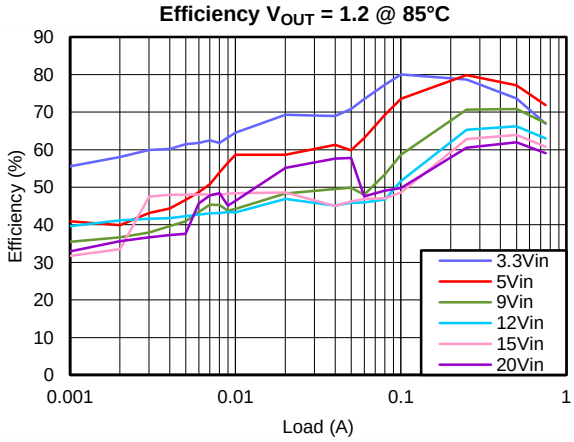


Figure 18.

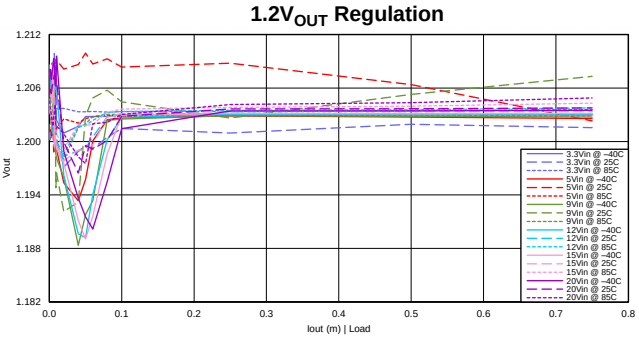


Figure 19.

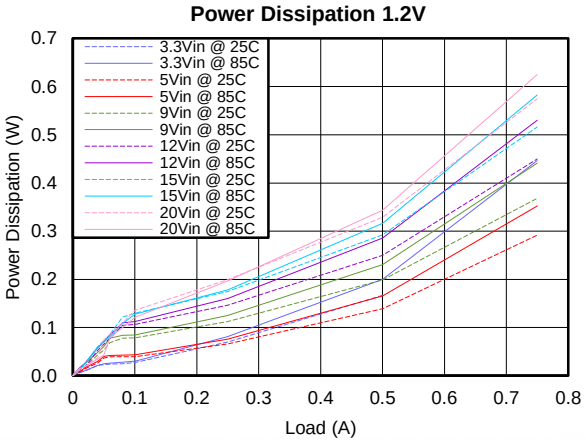


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Startup $5V_{IN}$ Full Load

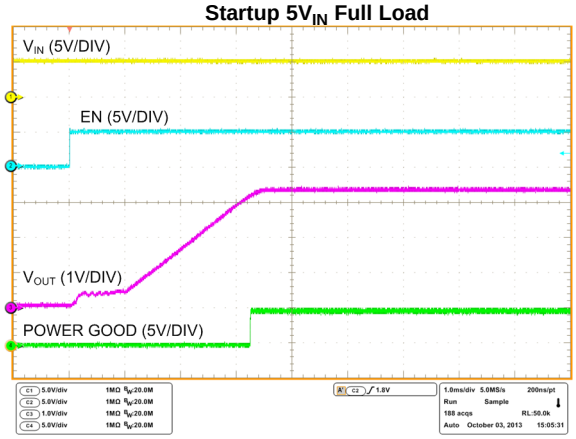


Figure 21.

Load Transient $12V_{IN}$ 50-750mA

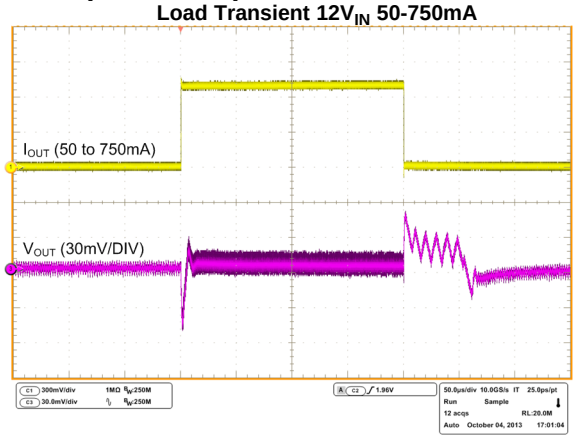


Figure 22.

Shutdown $5V_{IN}$ Full Load

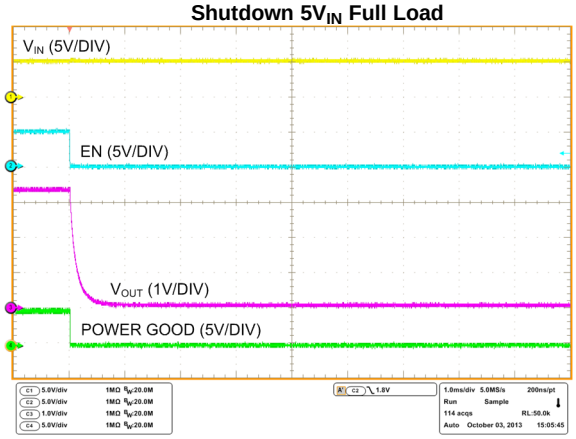


Figure 23.

Line Transient 9-15V 500mA Load

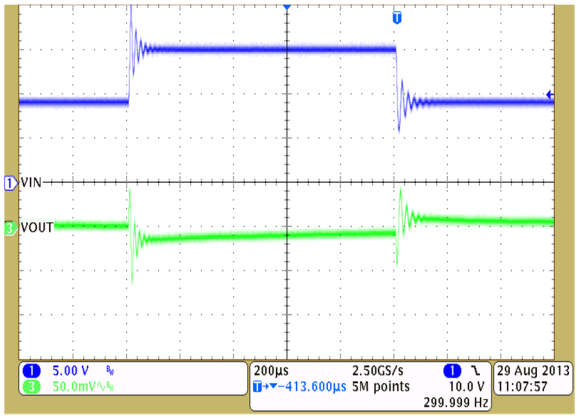


Figure 24.

Switching Light Load

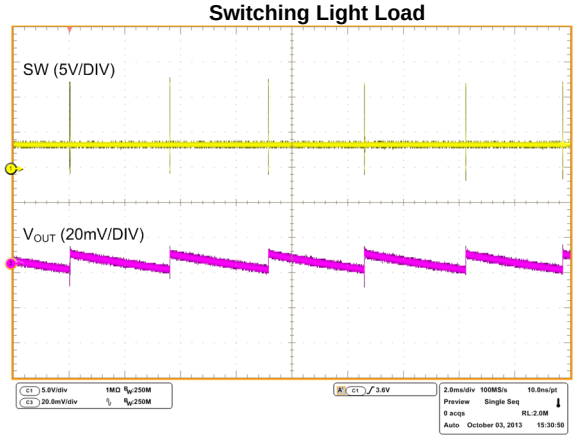


Figure 25.

Switching Loaded

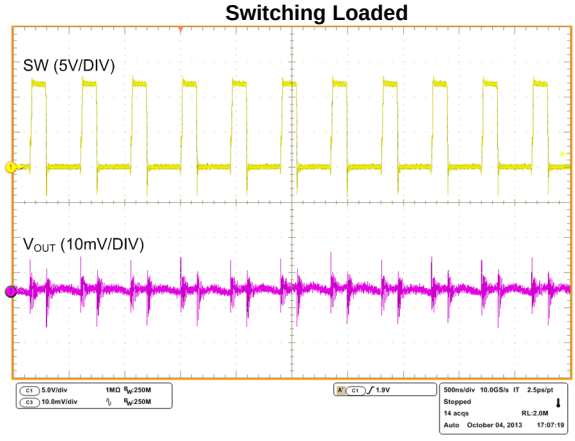


Figure 26.

TYPICAL CHARACTERISTICS (continued)

Short Circuit 12V$_{IN}$

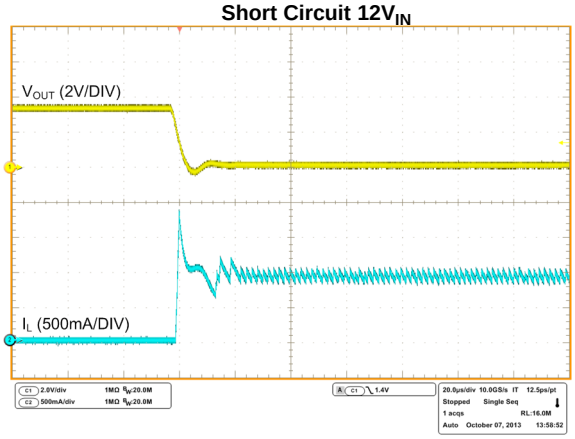


Figure 27.

Short Circuit Recovery 12V$_{IN}$

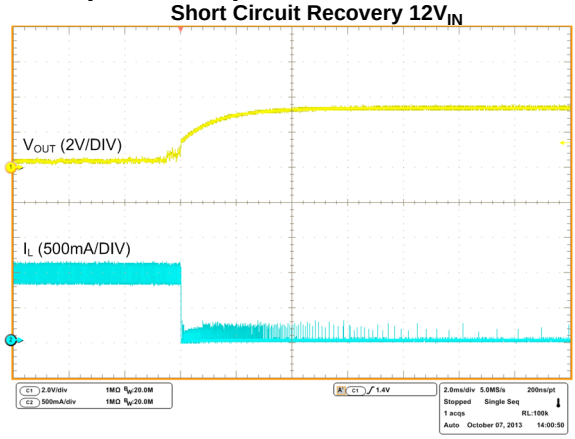


Figure 28.

Thermal Shutdown

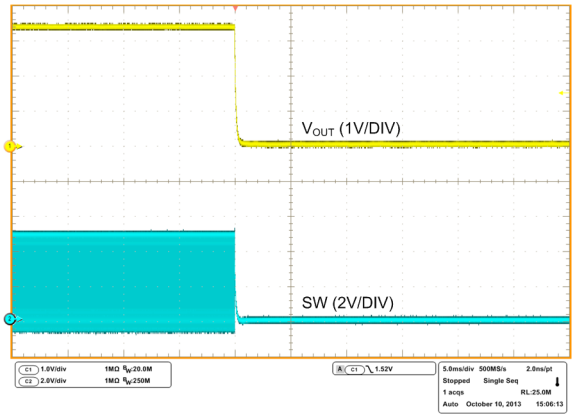


Figure 29.

Thermal Shutdown Recovery

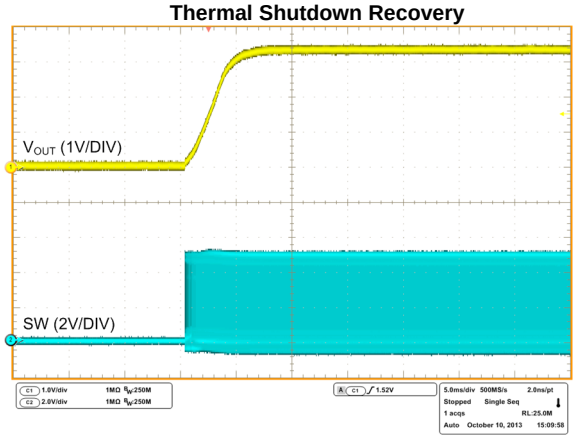
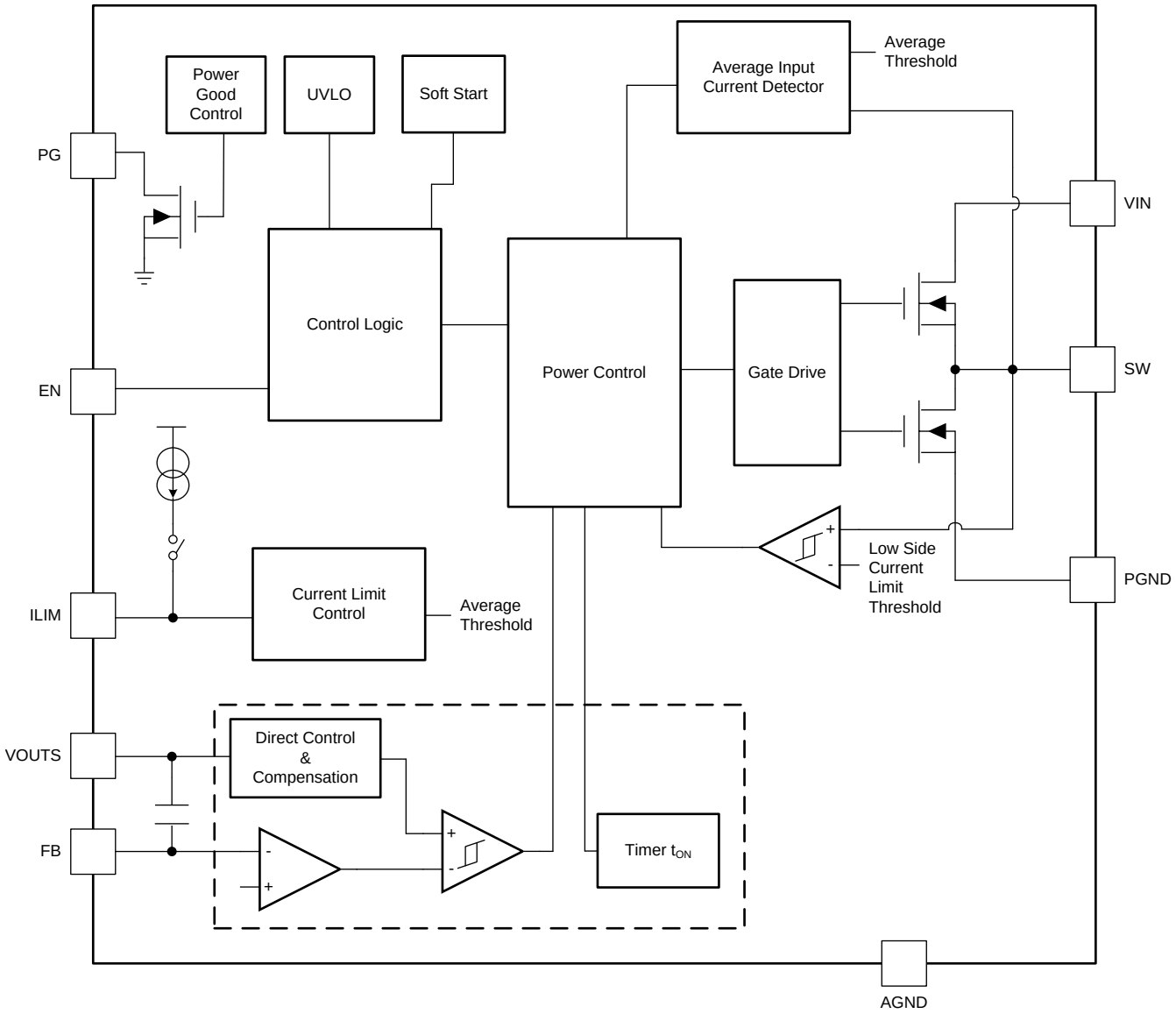


Figure 30.

FUNCTIONAL BLOCK DIAGRAM

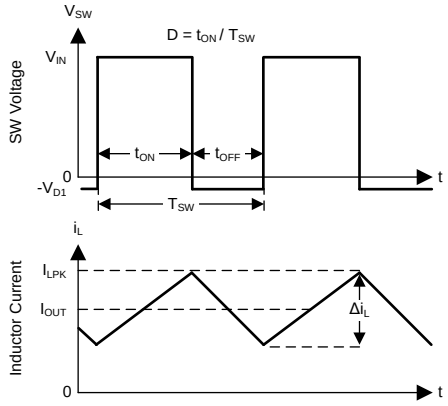


Theory of Operation

The LMR22007 is a buck regulator IC that delivers a 750 mA load current. The regulator has a preset switching frequency of 2.1 MHz. This high frequency allows the LMR22007 to operate with small surface mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LMR22007 is internally compensated, which reduces design time, and requires few external components.

The following operating description of the LMR22007 will refer to the Block Diagram and to the waveforms in the Figure below. The LMR22007 supplies a regulated output voltage by turning on the internal NMOS switch and varying the on-time. During the on-time, the SW pin voltage V_{SW} swings up to approximately V_{IN}, and the inductor current i_L increases with a linear slope. The switch is turned off by the control logic. During the switch off-time t_{OFF}, inductor current discharges through the low side device, which forces the SW pin (V_{SW}) to swing below ground by the voltage drop across the low side device. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

$$D = \frac{V_{OUT}}{V_{IN}}$$



The LMR22007 synchronous switched mode power converters are based on DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.1 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Detailed Description of Pins and Key Functions

POWER SAVE MODE OPERATION

The LMR22007's built in Power Save Mode will be entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

The LMR22007 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 478\text{ns} \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 77ns is kept to limit switching losses. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

$$i_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L} \quad (2)$$

When V_{IN} decreases to typically 15% above V_{OUT}, the LMR22007 won't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

ENABLE (EN)

The simplest way to enable the operation of the LMR22007 is to connect the EN pin to V_{IN} which allows self start-up of the LMR22007 when the input voltage is applied. A resistor value of less than 3kΩ is recomended.

Connect the EN pin to a voltage source greater than 0.9V to enable operation of the LMR22007. Apply a voltage less than 0.4V to put the part into shutdown mode. In shutdown mode the quiescent current drops to typically 300nA. An internal pull-down resistor of about 400kΩ keeps EN logic low, if the pin is floating. The pull-down resistor is disconnected if the pin is held High. During the soft start sequence the part will pull down with 2kΩ from the EN pin to ground. To keep the part from turning itself off when using a pull-up resistor, the resistor should be sized to keep the EN voltage above 0.9V when the UVLO threshold of the LMR22007 is reached. The 2kΩ is disconnected after start up.

When the rise time of V_{IN} is longer than the soft-start time of the LMR22007 this method may result in an overshoot in output voltage. In such applications, the EN pin voltage can be controlled by a separate logic signal, or tied to a resistor divider, which reaches 0.9V after V_{IN} is fully established. Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails. This will minimize the potential for output voltage overshoot during a slow V_{IN} ramp condition. Use the lowest value of V_{IN}, seen in your application when calculating the resistor network, to ensure that the 0.9V minimum EN threshold is reached.

INPUT CURRENT LIMIT and R_{LIM} SECTION

The LMR22007 offers a user adjustable input current limit. Limiting the input current can be very useful when the upstream power supply has a tight current budget. The input current limit can be set over a range of 150mA to 1000mA by connecting a resistor from 100kΩ to 15kΩ from pin B2 and ground. The higher the value of the R_{LIM} resistor, the lower the average input current limit.

When the output current increases, either from increased load current or charging of external capacitors during start-up, the average input current will increase until it exceeds the set point. At this point the off time of the next switching cycle will be lengthened to lower the average input current. This has the effect of lowering the switching frequency and decreasing the duty cycle, thus lowering the output voltage. Although the average input current is limited the peak switch current can still increase, this peak current is limited by the low side current limit. A simplified equation for calculating the input current limit is shown below.

$$\text{Input Current Limit} = \frac{15000 \text{ Volts}}{R_{LIM}} \tag{3}$$

The input current limit is dependent on the delay of the comparator circuit (τ) and the inductor current ripple. When we include these higher order terms into the equation for the current limit set resistor we get the following equation.

$$R_{LIM} = \frac{15000 \text{ Volts}}{\text{Input Current Limit} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT} \times \tau}{V_{IN} \times L \times \eta}} \tag{4}$$

Here, V_{IN} is the input voltage where input current limit is most critical, V_{OUT} is the output voltage set by the feedback resistors, L is the value of the inductor in µH, η is converter efficiency found in the characteristic charts, and the delay τ is a non linear factor with a typical value of 40ns.

The higher the ripple current in the inductor the more the input current limit will vary with input voltage. However, variation of the input current limit is usually only significant when the inductor ripple current is comparable in magnitude to the current limit to be set. Please refer to the characteristic curves for input current limit for more details.

The input current limit also tends to move up as the input voltage increases. This effect becomes much more significant as the device goes below 25% duty cycle.

LOW SIDE CURRENT LIMIT

The LMR22007 uses cycle-by-cycle current limiting to protect the output switches. During each switching cycle, a current limit comparator detects if the low side device current exceeds the low side current limit. If the low side current limit is exceeded the part skips the next on-time pulse until the current falls below the limit. This protects the part from current run-away due to short circuits of the output.

SOFT-START

The LMR22007 has a fixed internal soft-start of 3.3 ms (typ). During soft-start, the error amplifier's reference voltage ramps from 0.0 V to its nominal value of 0.9 V in approximately 3.3 ms. This forces the regulator output to ramp in a controlled fashion, which helps reduce inrush current. Upon soft-start the part will initially be in diode emulation mode to avoid discharging a pre-biased load.

If the device is set to shutdown (EN <0.4V), under voltage lockout or thermal shutdown, an internal resistor pulls the soft start reference down to ensure a proper low level. Returning from those states causes a new startup sequence.

POWER GOOD (PG)

The LMR22007 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor to the appropriate logic voltage (any voltage below 20V). The pin can sink different amounts of current based upon the state of the LMR22007. When V_{IN} is above 1.6V but below the UVLO of the part the PG pink can sink up to 100uA of current and maintain a logic low level. When V_{IN} is above the UVLO threshold the sinking current capability of the PG pin increases to 5mA. A typical pull-up resistor value is 100kΩ.

OUTPUT OVER VOLTAGE PROTECTION

The overvoltage comparator turns off the internal power NFET when the FB pin voltage exceeds the internal reference voltage by 13%. With the power NFET turned off the output voltage will decrease toward the regulation level.

INPUT UNDER VOLTAGE LOCKOUT

Under voltage lockout (UVLO) prevents the LMR22007 from operating until the input voltage exceeds V_{UVLO} . The UVLO threshold has at least 100 mV of hysteresis, so the part will operate until V_{IN} drops below 2.2V (typ). Hysteresis prevents the part from turning off during power up if V_{IN} droops due to input current demands.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 155°C (typ), and the part is switching in constant conduction mode. After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 130°C. When the junction temperature falls below 130°C, the LMR22007 will attempt to soft-start.

DESIGN GUIDE

EXTERNAL COMPONENT SELECTION

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The LMR22007 is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter. Table 1 can be used to simplify the output filter component selection.

Table 1. L-C Output Filter Combinations

	10µF	22µF	47µF	100µF
1.0µH		√	√	√
2.2µH	√	√2)	√	√
3.3µH	√	√	√	
4.7µH	√	√	√	
6.8 µH	√	√		
10 µH	√	√		

The LMR22007 can be run with an inductor as low as 1µH or 2.2µH. The control is similar to that detailed in SLVA463 and similar tradeoffs can be made with the LMR22007.

INDUCTOR SELECTION

A 2.2µH inductor is recommended to optimize the performance of the LMR22007 for stability and performance. Inductor selection is critical to the performance of the LMR22007. The selection of the inductor affects stability, transient response and efficiency. A key factor in inductor selection is determining the ripple current Δi_L

$$\Delta i_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}} \tag{5}$$

The ripple ratio (r) is defined as the ratio of inductor ripple current Δi_L to output current I_{OUT}, evaluated at maximum load.

$$r = \frac{\Delta i_L}{I_{OUT}} \tag{6}$$

The maximum inductor current can then be calculated.

$$I_L(max) = I_{OUT} + \frac{\Delta i_L}{2} \tag{7}$$

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the LMR22007 and are recommended for use:

Table 2. List of Inductors

Type	Inductance [µH]	Saturation Current [A]	Dimensions [L x B x H] [mm]	MANUFACTURER
D1286AS-H-2R2M	2.2 µH, ±20%	1.3	2 x 1.6 x 1.2	TOKO
XFL3012-222MEC	2.2 µH, ±20%	1.6	3 x 3 x 1.2	Coilcraft
VLS252012T-2R2M1R3	2.2 µH, ±20%	1.3	2.5 x 2 x 1.2	TDK
PSI25201B-2R2MS	2.2 µH, ±20%	1.3	2.5 x 2 x 1.2	Cyntec

The inductor value also determines the load current at which Power Save Mode is entered. This mode is entered when the part enters discontinuous conduction:

$$I_{OUT}(PSM) = \frac{\Delta i_L}{2} \tag{8}$$

This current level can be adjusted by changing the inductor value.

OUTPUT CAPACITOR SELECTION

The recommended value for the output capacitor is 22µF. The architecture of the LMR22007 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode.

The final selection of output capacitor is based upon the desired output ripple and transient response. The LMR22007's loop compensation is designed for ceramic capacitors. A minimum of 10µF is required and a maximum value of 200µF is allowed. The output voltage ripple of the converter is:

$$\Delta V_{OUT} = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right) \quad (9)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90 degrees phase shifted from the switching action. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A well placed ceramic capacitor will help to reduce this noise.

INPUT CAPACITOR SELECTION

For most applications, 10µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor (X5R, X7R) is recommended for best filtering and should be placed between V_{IN} and PGND as close as possible to those pins.

An input capacitor is necessary to ensure that V_{IN} does not droop or ring excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage rating, RMS current rating, and Equivalent Series Resistance (ESR). The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating IRMS-INPUT must be greater than:

$$I_{RMS\text{-}IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12} \right)} \quad (10)$$

where r is the ripple ratio defined earlier, I_{OUT} is the output current, and D is the duty cycle. It can be shown from the above equation that the maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESR of an input capacitor is stated in its datasheet. A large leaded aluminum electrolytic capacitor will have high ESR and a 0805 ceramic chip capacitor will have very low ESR. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult the capacitor manufacturer's datasheet to see how rated capacitance varies over operating conditions. If a PI filter is used on the input of the device to meet conducted EMI or other noise constraints, a damping capacitor with twice the value of the ceramic input capacitor and with enough ESR to lower the Q of the input filter should be added to the design.

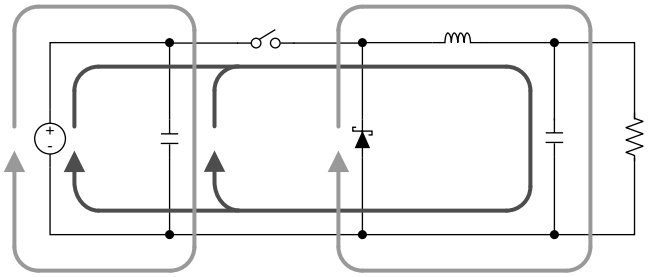
NOTE

DC Bias ffect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore, the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

PCB Layout Considerations

COMPACT LAYOUT

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines will help the user design a circuit with maximum rejection of outside EMI and minimum generation of unwanted EMI. Parasitic inductance can be reduced by keeping the power path components close together and keeping the area of the loops small, on which high currents travel. Short, thick traces or copper pours (shapes) are best. In particular, the switch node to the inductor and the connections from the LMR22007 to the input capacitor should be as short as possible, and just wide enough to carry the load current without excessive heating. The LMR22007 operates in two distinct cycles whose high current paths are shown below.



The dark grey, inner loop represents the high current path during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

GROUND PLANE AND SHAPE ROUTING

The figure above is also useful for analyzing the flow of continuous current vs. the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing should be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just like any other circuit path. The path between the input source and the input capacitor and the path between the inductor and the load are examples of continuous current paths. In contrast, the path between the low-side device and the input capacitor carries a large pulsating current. This path should be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel should be used right at the pad of the input capacitor to connect the component side shapes to the ground plane.

FB RESISTOR SELECTION

The FB pin is a high-impedance input, and the loop created by R_{FBB}, the FB pin and ground should be made as small as possible to maximize noise rejection. R_{FBB} should therefore be placed as close as possible to the FB and GND pins of the IC.

The feedback resistors are connected as a voltage divider from V_{OUT} to ground. The feedback resistors should be chosen to set the output voltage according to the following equation.

$$R_{FBT} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_{FBB} \tag{11}$$

A typical value for R_{FBB} is between 10 and 200kΩ.

THERMAL DESIGN

When calculating regulator dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.75A, and $T_{A\text{-}MAX}$ = 85°C, the part must see a thermal resistance from board to ambient (θ_{BA}) .

$$\theta_{BA} < \frac{T_{J\text{-}MAX} - T_{A\text{-}MAX}}{P_{IC\_LOSS}} - \Psi_{JB} \quad (12)$$

The typical thermal impedance from junction to board is 32.5°C/W. Use the power dissipation curves in the Typical Performance Characteristics section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is around 0.4W

$$\theta_{BA} < \frac{125°C - 85°C}{0.4\ W} - 32.5\frac{°C}{W} < 67.5\frac{°C}{W} \quad (13)$$

To reach θ_{BA} = 67.5°C/W, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2 oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 \geq \frac{500}{\theta_{CA}} \cdot \frac{°C \times cm^2}{W} \quad (14)$$

As a result, approximately 7.4 square cm of 2 oz copper on top and bottom layers is the minimum required area for the example PCB design. This is 2.72 x 2.72 cm (1.07 x 1.07 in). The GND, and V_{IN} pins should be connected to as large a copper plane as possible to remove heat from the device.

For an example of a high thermal performance PCB layout refer to AN-2020 and the evaluation board documentation.

LAYOUT HIGHLIGHTS

1. Minimize area of switched current loops. From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PC board layout as shown in the figure above. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor CIN is placed at a distance away from the LMR22007. Therefore place C_{IN} as close as possible to the LMR22007 V_{IN} and PGND pins. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND pin.
2. Have a single point ground. The ground connections for the feedback, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
3. Minimize trace length to the FB pin. Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB} should be routed away from the body of the LMR22007 to minimize possible noise pickup.
4. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.
5. Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the GND pin to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. For best results use 0.2 to 0.3mm thermal vias spaced at 1mm. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

REVISION HISTORY

Changes from Revision Splat (October 2013) to Revision A	Page

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR22007YYZFR	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	LM22007	Samples
LMR22007YYZFT	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	LM22007	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

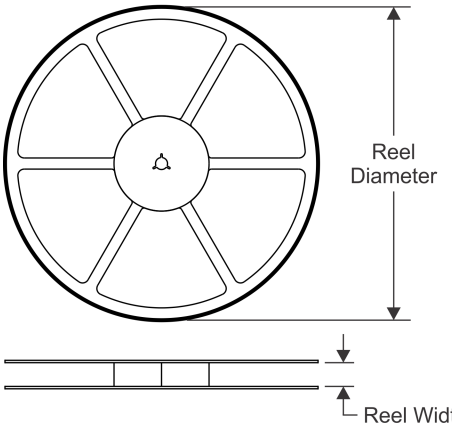
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

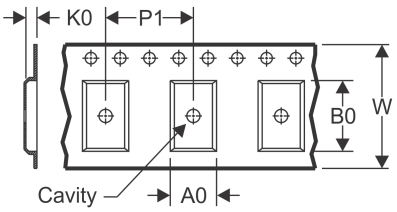
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

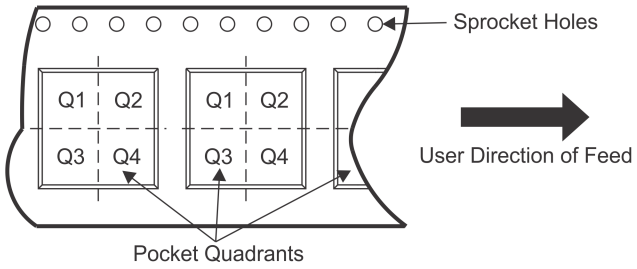


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

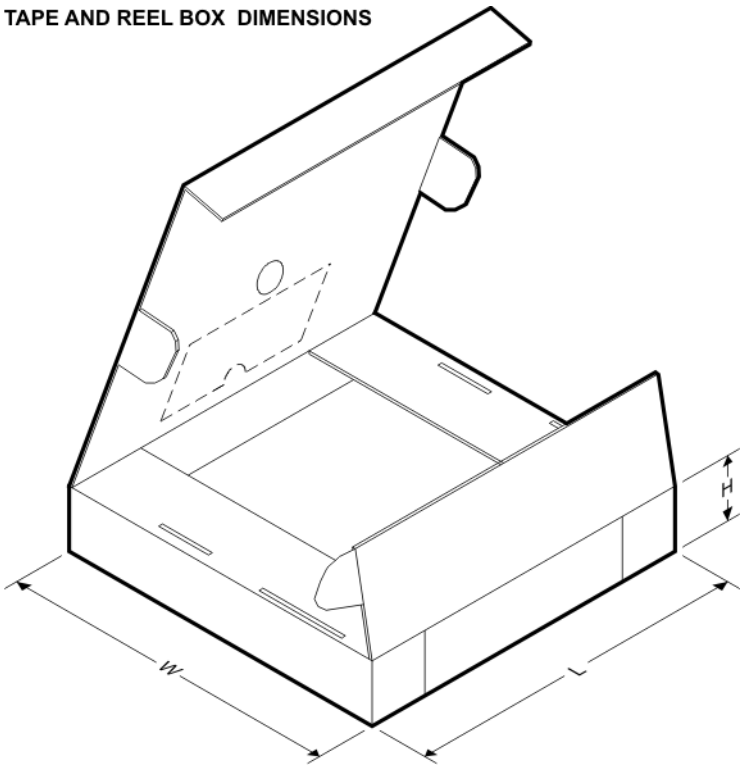
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR22007YYZFR	DSBGA	YZF	9	3000	180.0	8.4	1.71	1.71	0.81	4.0	8.0	Q1
LMR22007YYZFT	DSBGA	YZF	9	250	180.0	8.4	1.71	1.71	0.81	4.0	8.0	Q1

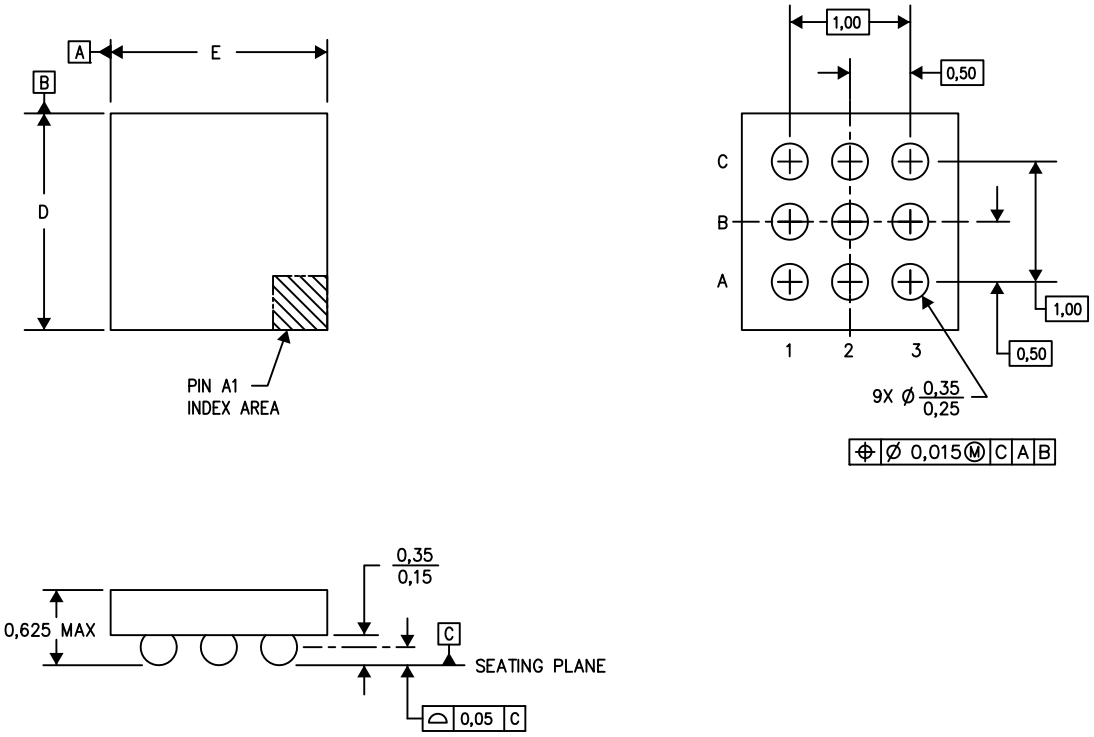
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR22007YYZFR	DSBGA	YZF	9	3000	182.0	182.0	17.0
LMR22007YYZFT	DSBGA	YZF	9	250	182.0	182.0	17.0

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



D: Max = 1.652 mm, Min =1.592 mm

E: Max = 1.652 mm, Min =1.592 mm

4205058–4/P 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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