THE DATASHEET OF

NCV97200MW33R2G

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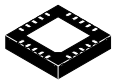
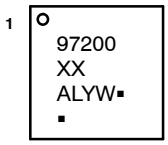
Power Management (PMIC) - Automotive, Multi-Output, Safety Applications

NCV97200



QFNW20
MW SUFFIX
CASE 484AD

MARKING DIAGRAM



97200	= Specific Device Code
XX	= 01 or 33
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 21 of this data sheet.

Description

The NCV97200 is a 2−output monolithic regulator consisting of 1 buck regulator and 1 boost regulator with supervisory functions including window voltage monitoring on all outputs and a window watchdog. This product is ideal for ADAS (Advanced Driver Assistance Systems) applications and utilizes an independent voltage reference and an adjustable independent oscillator to realize the supervisory features.

A 40 V non−synchronous buck regulator converts the battery supply voltage to a 3.3 V output, and delivers up to 3 A (peak). This output rail may be used as the low voltage input voltage for the non−synchronous secondary boost converter. The secondary boost is fixed and is intended to supply a low current 5.0 V rail for In−Vehicle Networking circuits (IVN).

All internal MOSFETs are N−channel devices, and a bootstrap circuit is used to drive the buck high−side MOSFET. Both SMPS outputs use peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the low−voltage gate drivers.

The NCV97200 is a functional safety solution that reduces the time required to develop safety systems that comply with the International Standards Organization (ISO) 26262. The device includes a range of integrated safety features such as dedicated feedback references, output voltage monitoring, and window watchdog.

Features

- 1 Enabled Buck Converter
- 1 Boost Converter for IVN Supply
- Wide Input of 4.1 to 40 V with Undervoltage Lockout (UVLO)
- Fixed Frequency Operation at 2 MHz
- Window Watchdog with Independent References
- Cycle−by−cycle Current Limit Protection
- External Frequency Synchronization
- Pseudo−random Spread Spectrum for Improved EMI
- Option for Switcher Shutdown upon Watchdog Fault (controlled by part number)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and Halide Free

Typical Applications

- Safety Applications
- ADAS (Advanced Driver Assistance Systems)
- Body Electronics
- Telematics

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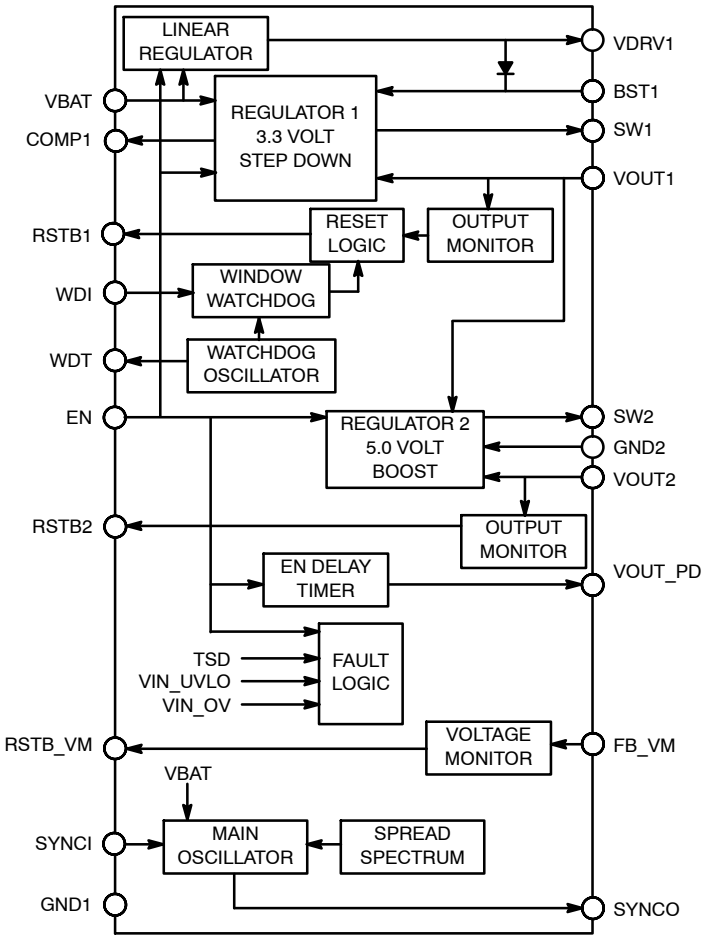


Figure 1. NCV97200 Block Diagram

TYPICAL APPLICATION

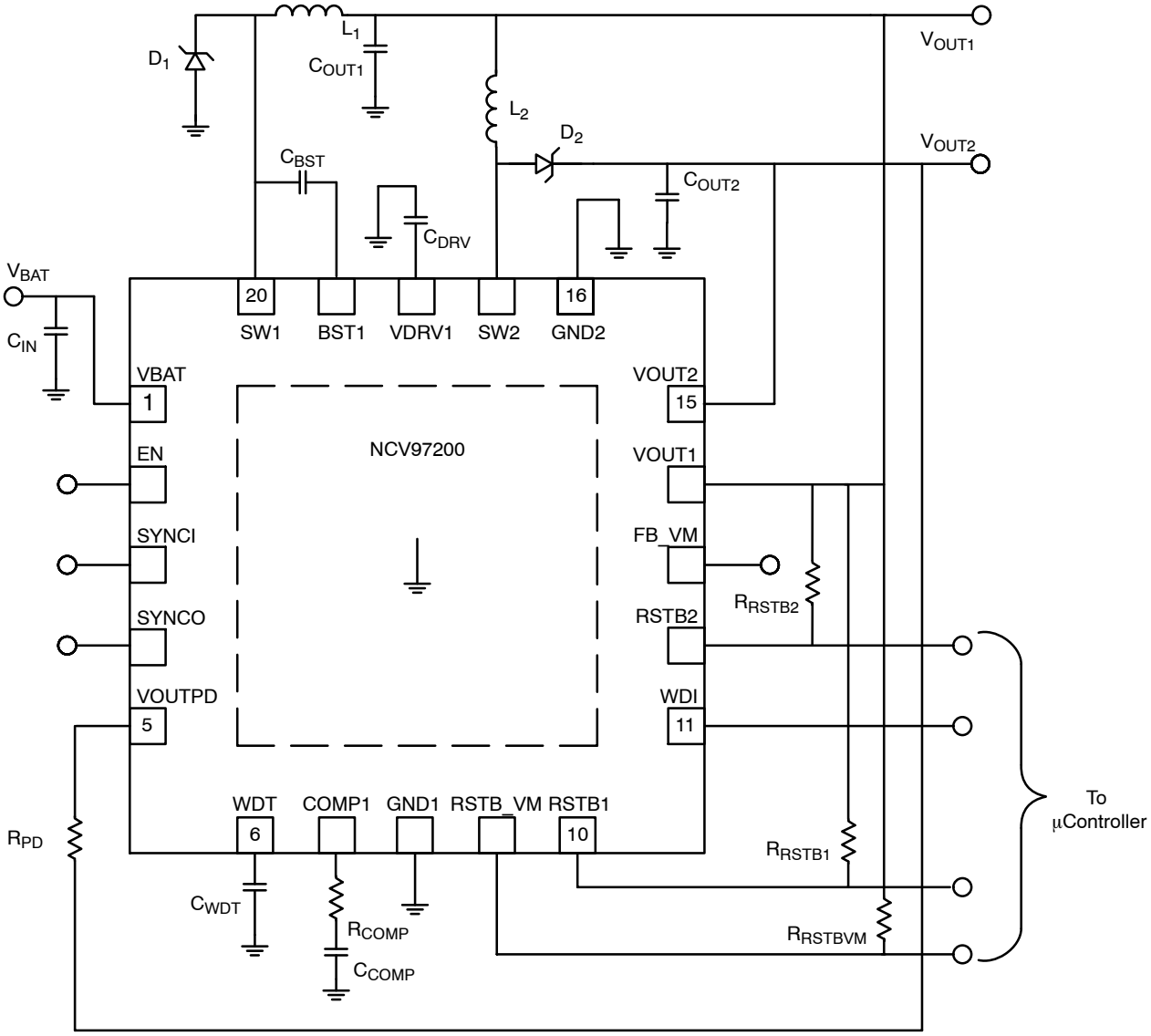


Figure 2. NCV97200 Typical Application

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage VBAT		−0.3 to 40	V
Max Voltage VBAT to SW1 and VBAT to GND − peak voltage during load dump		45	V
Min/Max Voltage SW1		−0.7 to 40	V
Min Voltage SW1, SW2 − 20 ns		−3.0	V
Min/Max Voltage BST1, EN		−0.3 to 40	V
Min/Max Voltage SW2		−0.3 to 7.2	V
Min/Max Voltage on WDI, SYNCI, SYNCO, VOUT2, RSTB1, RSTB2, RSTB_VM, VOUT_PD		−0.3 to 6	V
Max Voltage BST1 to SW1		3.6	V
Min/Max Voltage FB_VM, VDRV1, COMP1, WDT, VOUT1		−0.3 to 3.6	V
Thermal Resistance, 4x4 QFN Junction−to−Ambient (Note 1)	$R_{\theta JA}$	39	°C/W
Storage Temperature range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
ESD withstand Voltage (Human Body Model)	V_{ESD}	2.0	kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 1 sq. in. of a 4−layer PCB with 1 oz. copper thickness.

Table 2. PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	VBAT	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
2	EN	High−voltage (battery), TTL−compatible, master enable signal. Grounding this input stops all outputs and reduces Iq to a minimum (shutdown mode).
3	SYNCI	Synchronization input. Connecting an external clock to the SYNCI pin synchronizes switching to the rising edge of the SYNCI voltage. If unused, the SYNCI pin should be grounded.
4	SYNCO	Synchronization output pin. If unused, the SYNCO pin should have no connection.
5	VOUT_PD	Internal pull−down circuit − active during Enable delay time. Connect to GND when not used.
6	WDT	Watchdog delay programming. Connect a capacitor between this pin and ground to adjust the watchdog window time.
7	COMP1	Output of the error amplifier for switcher 1
8	GND1	Ground reference for the IC.
9	RSTB_VM	External voltage monitor reset output with adjustable delay. Goes low when the FB_VM for the external supply is out of regulation. If unused, the RSTB_VM pin should have no connection.
10	RSTB1	Switcher 1 voltage monitor reset output with adjustable delay. Goes low when the output is out of regulation and when a watchdog pulse is not received from the microcontroller. If unused, the RSTB1 pin should have no connection.
11	WDI	CMOS compatible Watchdog pulse input from a CPU. To be valid, the time between rising edges of this signal must be between the watchdog window time.
12	RSTB2	Switcher 2 voltage monitor reset output with adjustable delay. Goes low when the output is out of regulation. If unused, the RSTB2 pin should have no connection.
13	FB_VM	Input for the external voltage monitor. Connect to external voltage reference through resistor divider. If unused, the FB_VM pin should be grounded.
14	VOUT1	Output voltage sensing for switcher 1.
15	VOUT2	Output voltage sensing for switcher 2.
16	GND2	Ground connection for the source of the low−side switch of switcher 2.
17	SW2	Switching node of the switcher 2 boost regulator. Connect the output inductor to this pin.
18	VDRV1	Internal supply voltage for driving the low−voltage internal switch. Connect a 0.1 μF to 1.0 μF capacitor for noise filtering purposes.
19	BST1	Bootstrap input provides drive voltage higher than VBAT to the N−channel Power Switch for optimum switch $R_{DS(on)}$ and highest efficiency.
20	SW1	Switching node of the switcher 1 buck regulator. Connect the output inductor and cathode of the freewheeling diode to this pin.
Exposed Pad	EP	Must be connected to GND1 (electrical ground) and to a low thermal resistance path to the ambient temperature environment.

Table 3. ELECTRICAL CHARACTERISTICS
(V_{BAT} = 4.5 V to 28 V, EN = 5 V, BSTx = SWx + 3.0 V, C_{DRV1} = 0.1 μF. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, shutdown	I_{qSD}	V_{BAT} = 13.2 V, T_J = 25°C, V_{EN} = 0 V	–	3	10	μA
UNDERVOLTAGE LOCKOUT – VBAT (UVLO)						
VBAT UVLO Start Threshold	V_{UV1ST}	V_{BAT} rising	4.45	–	4.85	V
VBAT UVLO Stop Threshold	V_{UV1SP}	V_{BAT} falling	3.7	–	4.1	V
VBAT UVLO Hysteresis	V_{UV1HY}		–	0.75	–	V
ENABLE						
Delay Time	t_{ENDLY}		13.6	16	18.4	ms
Logic Low	V_{ENLO}		–	–	0.8	V
Logic High	V_{ENHI}		2.0	–	–	V
Enable Pin Input Current	I_{EN}	V_{EN} = 5 V	–	15	20	μA
Disable Response Time	t_{DISABL}	Time EN Voltage must be < V_{ENLO} in order to force restart	–	2	10	μs
OUTPUT VOLTAGE						
Switcher 1 Output	V_{OUT1}		3.23	3.3	3.37	V
Switcher 2 Output	V_{OUT2}		4.9	5.0	5.1	V
ERROR AMPLIFIER – SWITCHER 1						
Transconductance	g_m $g_{m(HV)}$	V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	 0.6 0.35	 1.0 0.55	 1.4 0.75	mmho
Output Resistance	R_{OUT}		–	1.4	–	MΩ
COMP Source Current Limit	I_{SOURCE}	V_{OUT1} = 2.8 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	 50 25	 75 40	 100 55	μA
COMP Sink Current Limit	I_{SINK}	V_{OUT1} = 3.8 V, V_{COMP} = 1.1 V 4.5 V < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	 50 25	 75 40	 100 55	μA
Minimum COMP Voltage	V_{CMPMIN}	V_{OUT1} = 3.8 V	–	0.15	0.3	V
Maximum COMP Voltage	V_{CMPMAX}	V_{OUT1} = 2.8 V	1.3	1.6	–	V
OSCILLATOR						
Base Switching Frequency – Switcher 1	f_{SW1}	4.5 < V_{BAT} < 18 V (see Spread Spectrum Section)	1.8	2.0	2.2	MHz
Switching Frequency – Switcher 1	$f_{SW1(HV)}$	20 V < V_{BAT} < 28 V	0.9	1.0	1.1	MHz
Base Switching Frequency – Switcher 2	f_{SW2}	(see Spread Spectrum Section)	1.8	2.0	2.2	MHz
SYNCHRONIZATION INPUT (SYNCI)						
SYNCI Pin Input Current	I_{SYNCI}	V_{SYNCI} = 5.0 V	30	50	70	μA
SYNCI Input High Input Voltage	V_{SYNCIH}		2.0	–	–	V
SYNCI Input Low Input Voltage	V_{SYNCIL}		–	–	0.8	V
SYNCI High Pulse Width	t_{SYNCIH}	V_{SYNCI} > V_{SYNCIH}	40	–	–	ns
SYNCI Low Pulse Width	t_{SYNCIL}	V_{SYNCI} < V_{SYNCIL}	40	–	–	ns
External Synchronization Frequency	f_{SYNCI}		1.8	–	2.6	MHz
Master Reassertion Time	$t_{SYNCIMR}$	Time between last synchronized SW rising edge and first unsynchronized SW rising edge.	–	650	–	ns
SYNCHRONIZATION OUTPUT (SYNCO)						
SYNCO High Voltage	$V_{SYNCO,H}$	SYNCO load current = −1 mA	VDRV −0.2 V	–	VDRV	V

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{BAT} = 4.5 V to 28 V, EN = 5 V, BSTx = SWx + 3.0 V, C_{DRV1} = 0.1 μF. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYNCHRONIZATION OUTPUT (SYNCO)						
SYNCO Low Voltage	$V_{SYNCO,L}$	SYNCO load current = 1 mA	0	–	0.2	V
SYNCO Duty Cycle	D_{SYNCO}		40	50	60	%
SYNCO Rise Time	$t_{SYNCO,R}$	SYNCO load capacitance = 40 pF	–	8	–	ns
SYNCO Fall Time	$t_{SYNCO,F}$	SYNCO load capacitance = 40 pF	–	5	–	ns
Phase	ϕ_{SO-SW1}	Rising edge lag with respect to SW1 rising edge	–	140	–	°
VBAT OVERVOLTAGE SHUTDOWN MONITOR						
Overvoltage Stop Threshold	V_{OV1SP}	V_{BAT} rising	37	–	40	V
Overvoltage Start Threshold	V_{OV1ST}	V_{BAT} falling	34	–	–	V
Overvoltage Hysteresis	V_{OV1HY}		0.6	–	2.7	V
VBAT FREQUENCY FOLDBACK MONITOR						
Frequency Foldback Threshold	V_{FL1U} V_{FL1D}	V_{BAT} rising V_{BAT} falling	18.4 18	– –	20 19.8	V
Frequency Foldback Hysteresis	V_{FL1HY}		0.2	0.3	0.4	V
SOFT−START						
Soft−Start Completion Time	t_{SS1}		0.8	1.4	2.0	ms
	t_{SS2}		1.6	2.8	4.0	
SLOPE COMPENSATION						
Ramp Slope – Switcher 1 (With respect to switch current)	S_{ramp1} $S_{ramp1(HV)}$	4.5 < V_{BAT} < 18 V 20 V < V_{BAT} < 28 V	1.8 0.8	– –	3.4 1.6	A/μs
Ramp Slope – Switcher 2	S_{ramp2}		0.76	1.1	1.44	A/μs
POWER SWITCH – SWITCHER 1						
ON Resistance	R_{DS1ON}	V_{BST1} = V_{SW1} + 3.0 V, I_{SW1} = 500 mA	–	–	360	mΩ
Leakage current VBAT to SW1	I_{LKSW1}	V_{EN} = 0 V, V_{SW1} = 0 V, V_{BAT} = 18 V	–	–	10	μA
Minimum ON Time	t_{ON1MIN}	Measured at SW1 pin	45	–	70	ns
Minimum OFF Time	$t_{OFF1MIN}$	Measured at SW1 pin	30	50	70	ns
POWER SWITCH – SWITCHER 2						
ON Resistance	R_{DS2ON}	I_{SW2} = 100 mA	–	–	1.0	Ω
Switch Leakage Current	I_{LKSW2}	V_{EN} = 0 V, V_{SW2} = 5.0 V, V_{BAT} = 18 V	–	–	5	μA
Minimum ON Time	t_{ON2MIN}	Measured at SW2 pin	65	85	100	ns
Minimum OFF Time	$t_{OFF2MIN}$	Measured at SW2 pin	35	55	75	ns
PEAK CURRENT LIMITS						
Current Limit Threshold – Switcher 1	I_{LIM1}		3.9	4.4	4.9	A
Current Limit Threshold – Switcher 2	I_{LIM2}		0.96	1.2	1.44	A
SHORT CIRCUIT FREQUENCY FOLDBACK – SWITCHER 1						
Lowest Foldback Frequency Lowest Foldback Frequency – High V_{IN}	f_{SW1AF} $f_{SW1AFHV}$	V_{OUT1} = 0 V, 4.5 V < V_{BAT} < 18 V V_{OUT1} = 0 V, 20 V < V_{BAT} < 28 V	450 225	550 275	650 325	kHz
HICCUP MODE						
Hiccup Frequency	f_{SW1HIC}	V_{OUT1} = 0 V SW1 pin shorted to ground or VOUT1	24	32	40	kHz
	f_{SW2HIC}	SW2 pin connected to +3.3 V through 20 Ω. Zero volts at the VOUT2 pin.	24	32	40	kHz
Switching Reactivation Delay	SW2	SW2 pin shorted to VOUT1	–	1.9	–	ms

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{BAT} = 4.5 V to 28 V, EN = 5 V, BSTx = SWx + 3.0 V, C_{DRV1} = 0.1 μF. Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
WINDOW WATCHDOG						
Watchdog Oscillator Frequency	f_{WD}	C_{WDT} = 1000 pF C_{WDT} = 100 pF	8.2 77	10.6 100	13.0 122	kHz
First Watchdog Timeout	$t_{WD_timeout}$	Watchdog timeout after rising edge at RSTB1 C_{WDT} = 1000 pF 800 pF < C_{WDT} < 1200 pF C_{WDT} = 100 pF 80 pF < C_{WDT} < 120 pF	 2300 2070 240 221	 2840 – 300 –	 3700 4090 385 430	ms
Watchdog Window Time	t_{WD}	C_{WDT} = 1000 pF 800 pF < C_{WDT} < 1200 pF C_{WDT} = 100 pF 80 pF < C_{WDT} < 120 pF	150 138 15.9 14.7	189 – 20 –	250 273 27 28.7	ms
Watchdog Closed Window Time	t_{WD_CLS}		–	t_{WD}/4	–	ms
WDI Pulse Duration	t_{WDImin}	Number of Oscillator periods (WDT pin) the WDI input must remain high or low	3	–	–	WDT cycles
Watchdog Input WDI Threshold Voltage	V_{WDH} V_{WDL} V_{WD_HYS}	V_{WD} increasing V_{WI} decreasing	– 0.8 150	– – –	2.0 – 500	V V mV
Watchdog Input WDI Current	I_{WDI}	V_{WD} = 5 V	30	50	70	μA
RESET						
Low Voltage Reset Threshold – Switcher 1	V_{UV1FAL} V_{UV1RIS}	V_{OUT1} decreasing V_{OUT1} increasing	2.97 3.04	3.05 3.12	3.14 3.20	V
High Voltage Reset Threshold – Switcher 1	V_{OV1FAL} V_{OV1RIS}	V_{OUT1} decreasing V_{OUT1} increasing	3.40 3.47	3.48 3.55	3.56 3.63	V
Low Voltage Reset Threshold – Switcher 2	V_{UV2FAL} V_{UV2RIS}	V_{OUT2} decreasing V_{OUT2} increasing	4.50 4.60	4.63 4.73	4.75 4.85	V
High Voltage Reset Threshold – Switcher 2	V_{OV2FAL} V_{OV2RIS}	V_{OUT2} decreasing V_{OUT2} increasing	5.15 5.25	5.28 5.38	5.40 5.50	V
Low Voltage Reset Threshold – External Supply	$V_{UVextFAL}$ $V_{UVextRIS}$	FB_VM decreasing FB_VM increasing	0.720 0.736	0.740 0.756	0.760 0.776	V
High Voltage Reset Threshold – External Supply	$V_{OVextFAL}$ $V_{OVextRIS}$	FB_VM decreasing FB_VM increasing	0.824 0.840	0.844 0.860	0.864 0.880	V
Reset Hysteresis (ratio of VOUTx)	K_{RES_HYS}		0.5	2	–	%
Noise−Filtering Delay	t_{RES_FILT}		5	–	25	μs
Reset Delay Time Time RSTB1 remains low after output voltage enters the monitor window.	t_{RESET}	I_{RSTBx} = 1 mA I_{RSTBx} = 500 μA I_{RSTBx} = 100 μA	– 4.0 19	1.0 5.0 24	– 6.0 29	μs ms ms
Reset Output Low level	V_{RESL}	I_{RSTBx} = 1 mA	–	–	0.4	V
BOOTSTRAP VOLTAGE SUPPLY						
Output Voltage	V_{DRV1}		3.1	3.3	3.5	V
V_{DRV1} POR Start Threshold	V_{DRV1ST}		2.7	2.875	3.05	V
V_{DRV1} POR Stop Threshold	V_{DRV1SP}		2.55	2.75	2.95	V
THERMAL SHUTDOWN						
Thermal Shutdown Activation Temperature	T_{SD}		150	–	190	°C
Hysteresis	T_{HYS}		5	–	20	°C
VOUT_PD						
Pulldown Resistance	R_{PD}	During Enable Delay Time	5	16	40	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – (DEMOBOARD DATA)

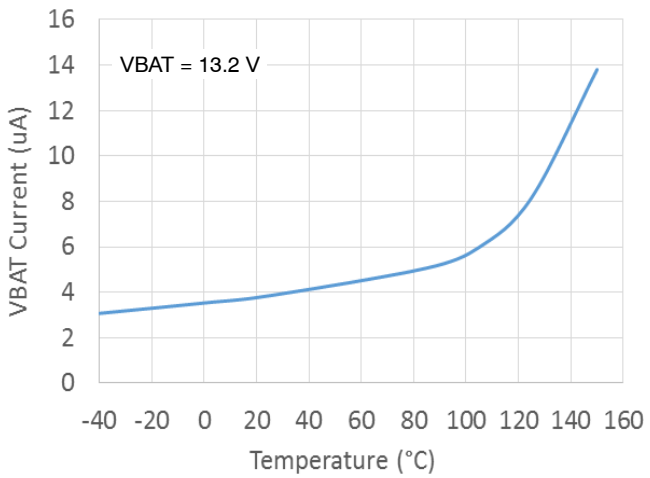


Figure 3. Shutdown VBAT Current vs. Temperature

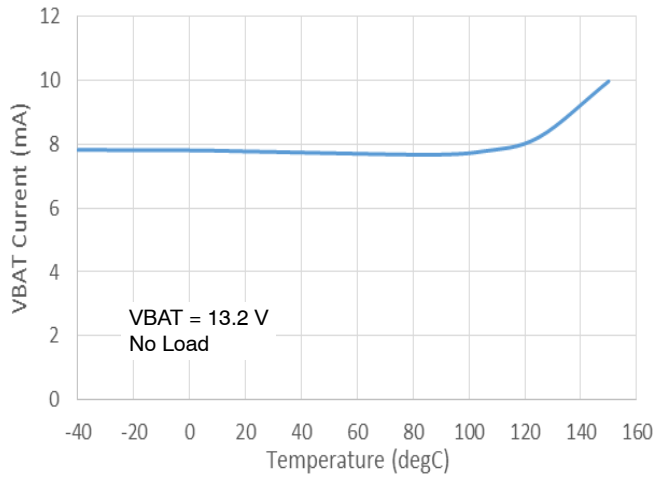


Figure 4. Operating VBAT Current vs. Temperature

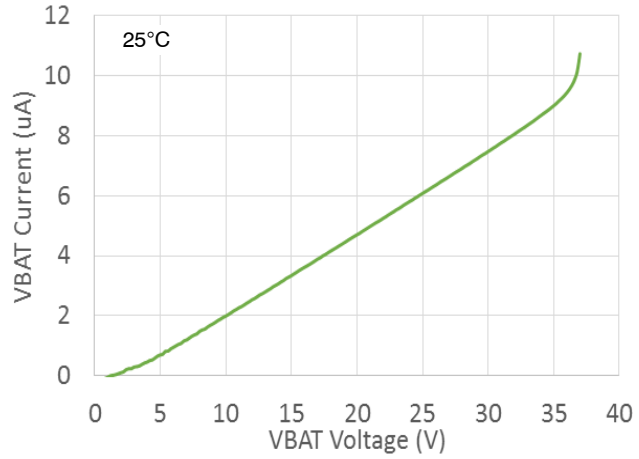


Figure 5. Shutdown VBAT Current vs. VBAT Voltage

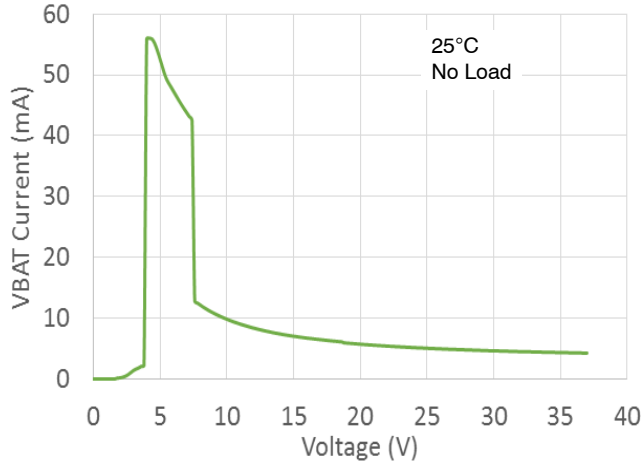


Figure 6. Operating VBAT Current vs. VBAT Voltage

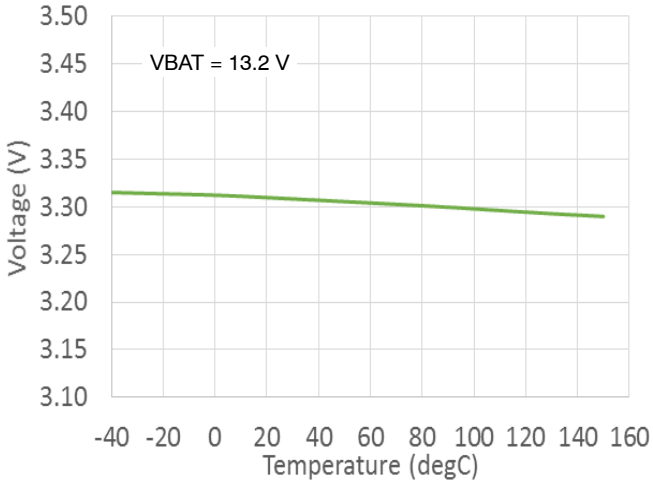


Figure 7. VDRV1 Voltage vs. Temperature

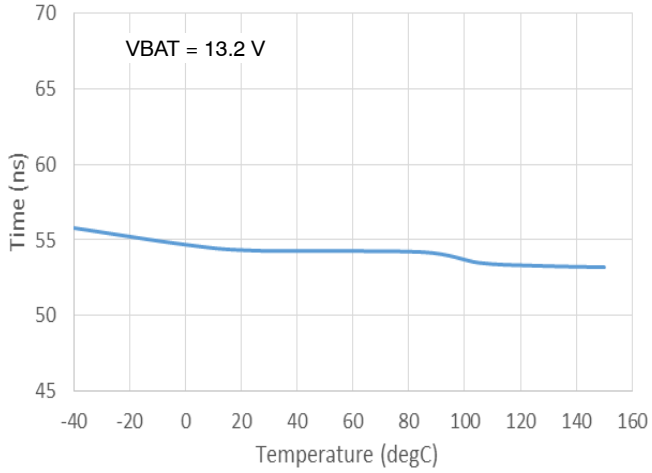


Figure 8. Switcher 1 Minimum ON Time vs. Temperature

TYPICAL CHARACTERISTICS – (DEMOBOARD DATA)

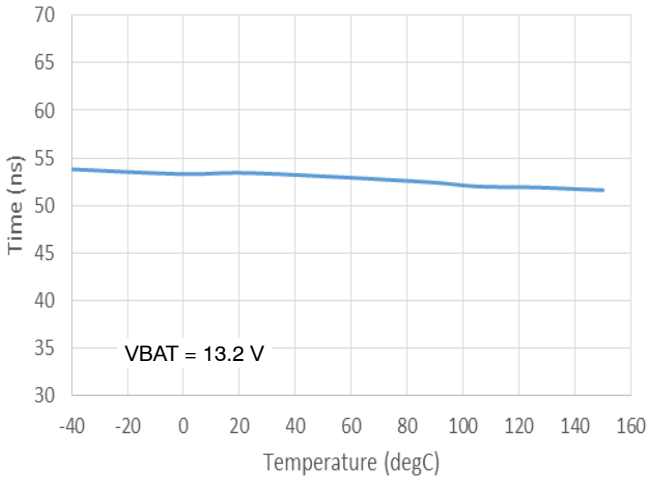


Figure 9. Switcher 1 Minimum OFF Time vs. Temperature

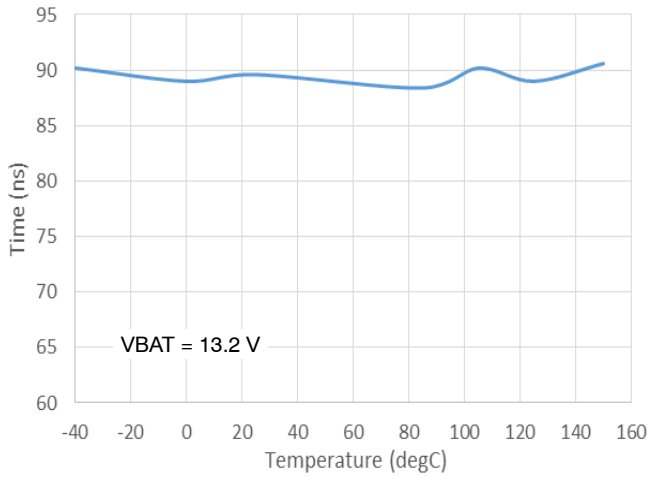


Figure 10. Switcher 2 Minimum ON Time vs. Temperature

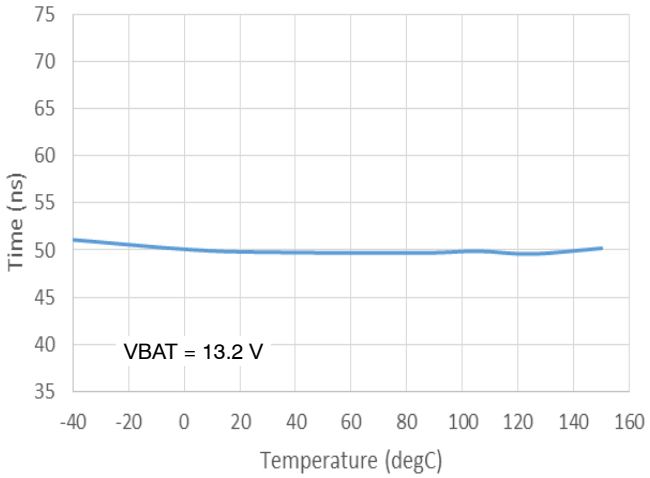


Figure 11. Switcher 2 Minimum OFF Time vs. Temperature

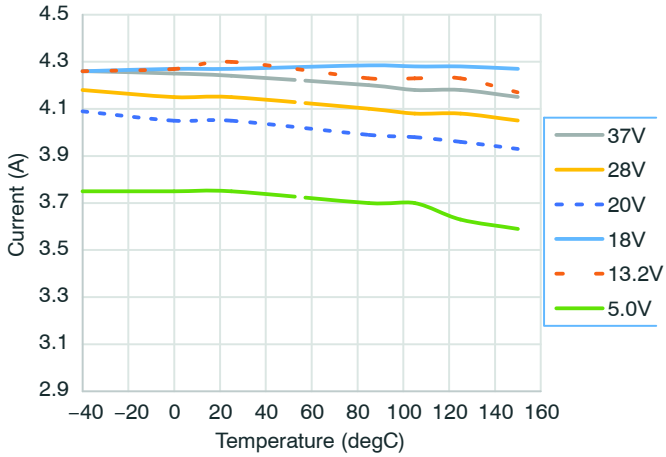


Figure 12. Switcher 1 Load Current Limit vs. Temperature

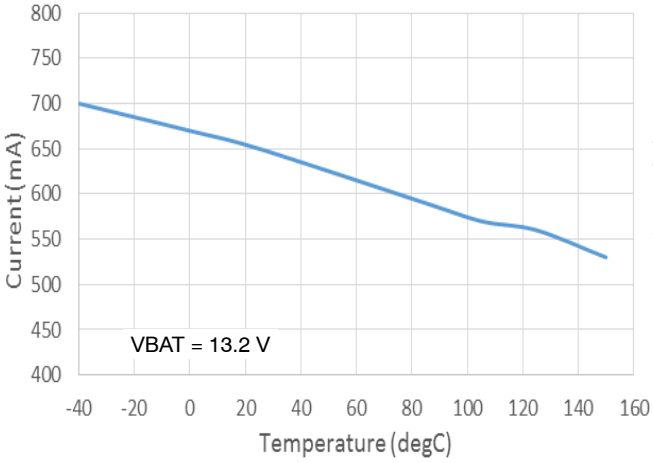


Figure 13. Switcher 2 Load Current Limit vs. Temperature

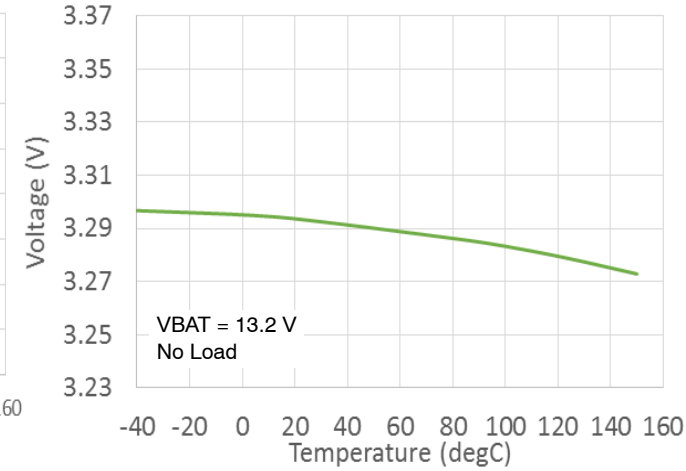


Figure 14. Switcher 1 Output Voltage vs. Temperature

TYPICAL CHARACTERISTICS – (DEMOBOARD DATA)

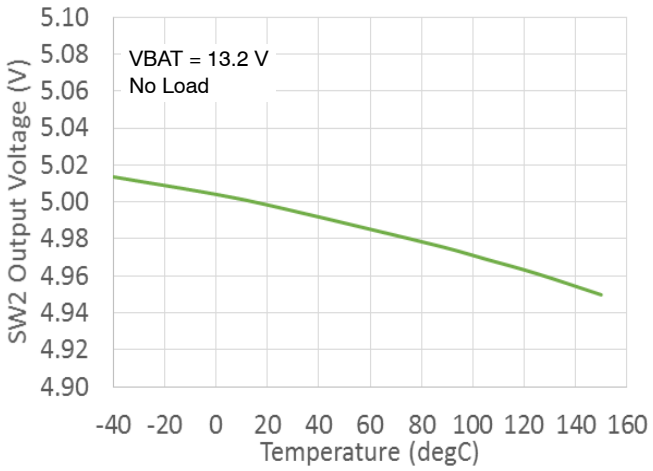


Figure 15. Switcher 2 Output Voltage vs. Temperature

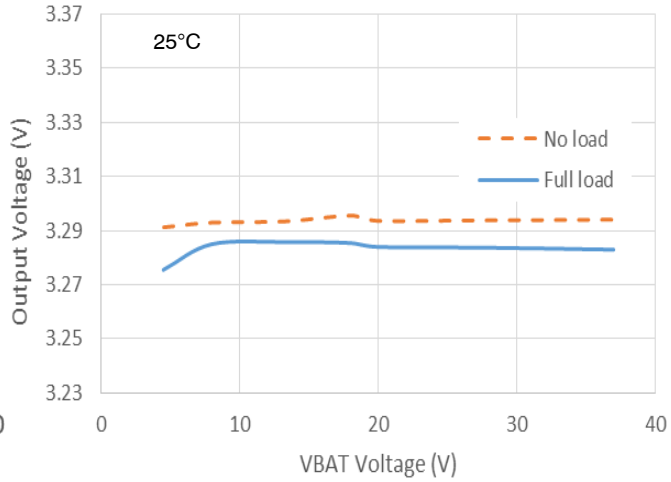


Figure 16. Switcher 1 Output Voltage vs. VBAT Voltage

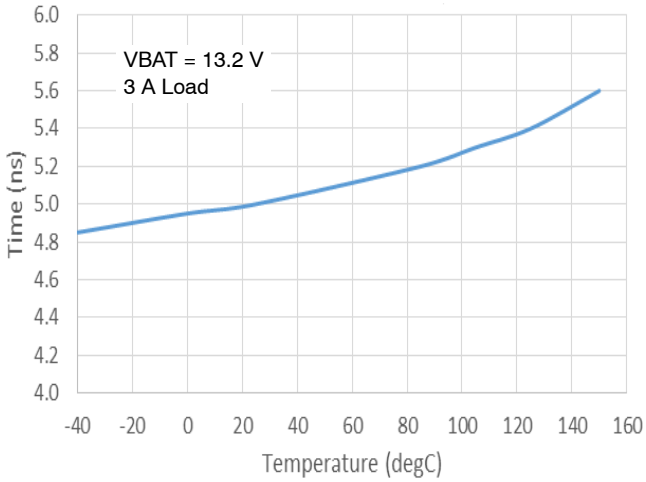


Figure 17. Switcher 1 Risetime vs. Temperature

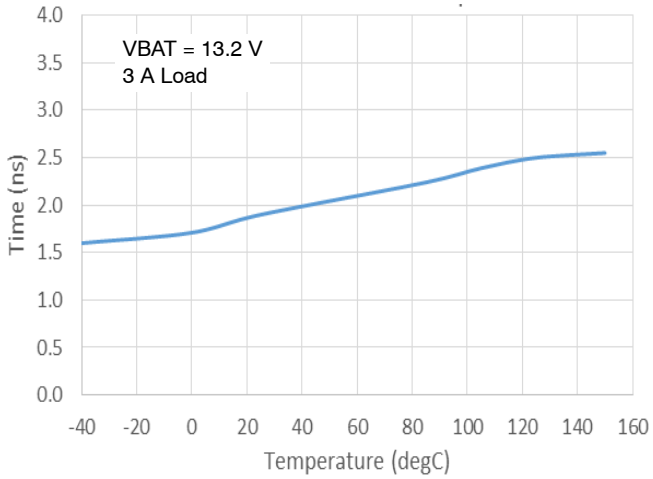


Figure 18. Switcher 1 Falltime vs. Temperature

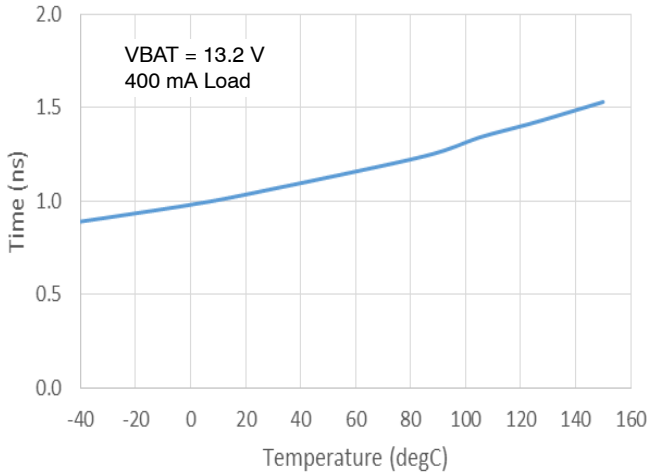


Figure 19. Switcher 2 Risetime vs. Temperature

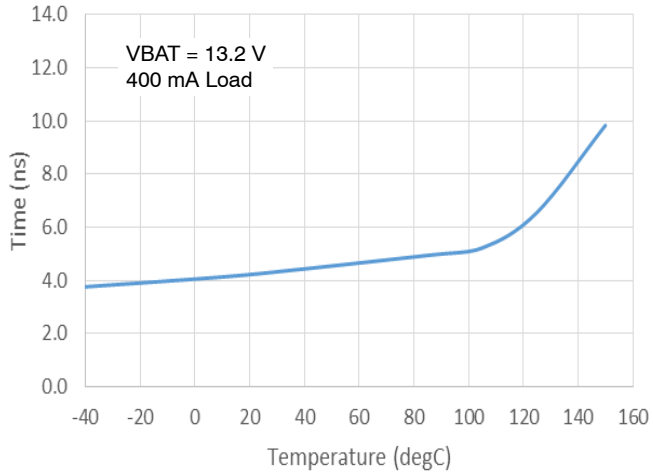


Figure 20. Switcher 2 Falltime vs. Temperature

TYPICAL CHARACTERISTICS – (DEMOBOARD DATA)

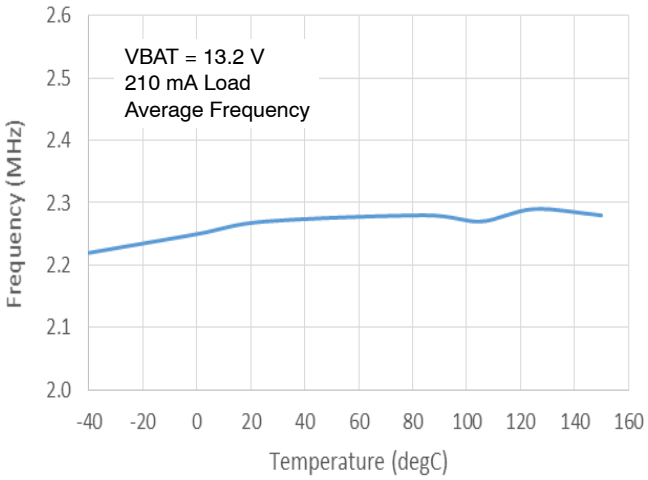


Figure 21. Switcher 1 Frequency vs. Temperature

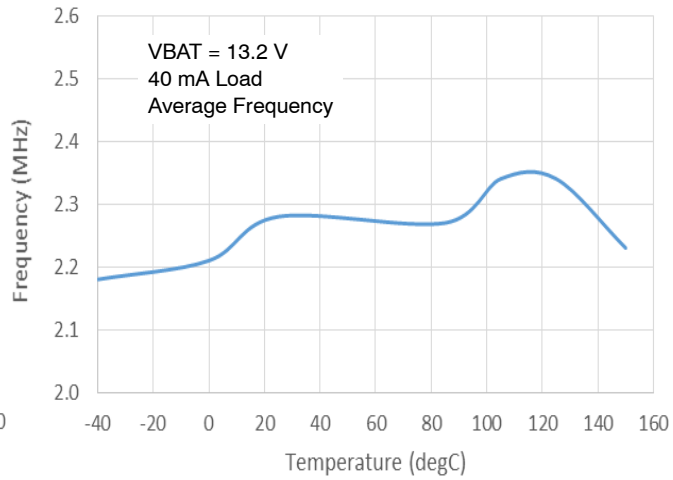


Figure 22. Switcher 2 Frequency vs. Temperature

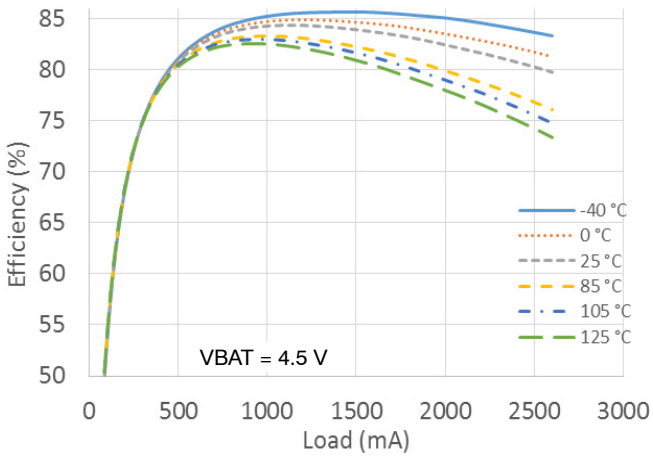


Figure 23. Switcher 1 Efficiency vs. Load, 4.5 V VBAT

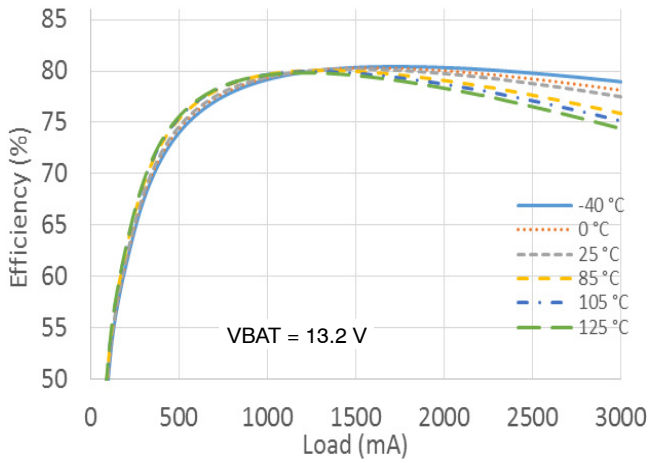


Figure 24. Switcher 1 Efficiency vs. Load, 13.2 V VBAT

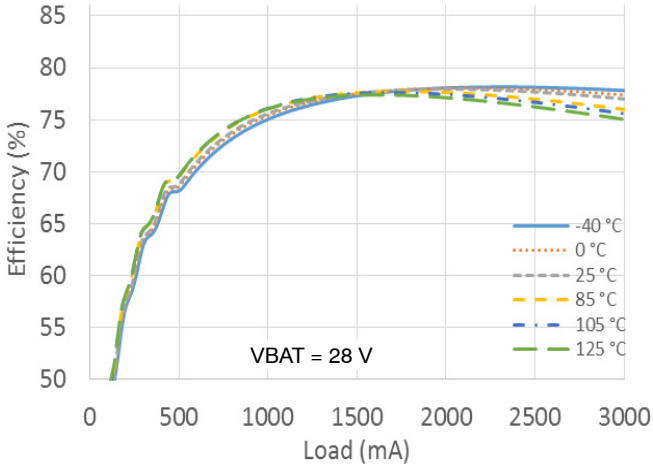


Figure 25. Switcher 1 Efficiency vs. Load, 28 V VBAT

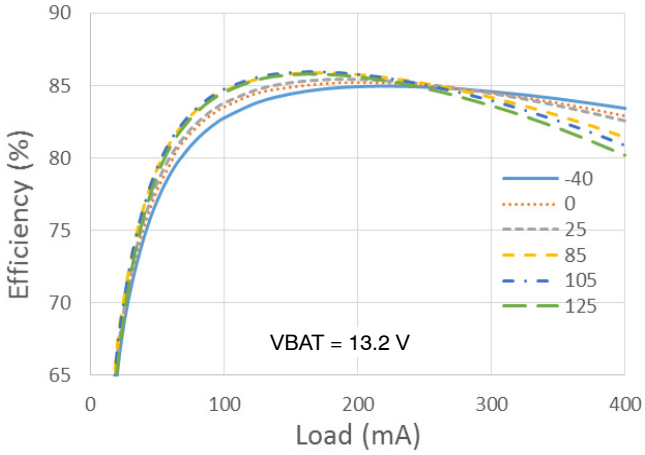


Figure 26. Switcher 2 Efficiency vs. Load

APPLICATION INFORMATION

General Description

The NCV97200 consists of one 2 MHz battery−connected 2.5 A switcher (switcher 1) and a downstream low−current boost converter (switcher 2).

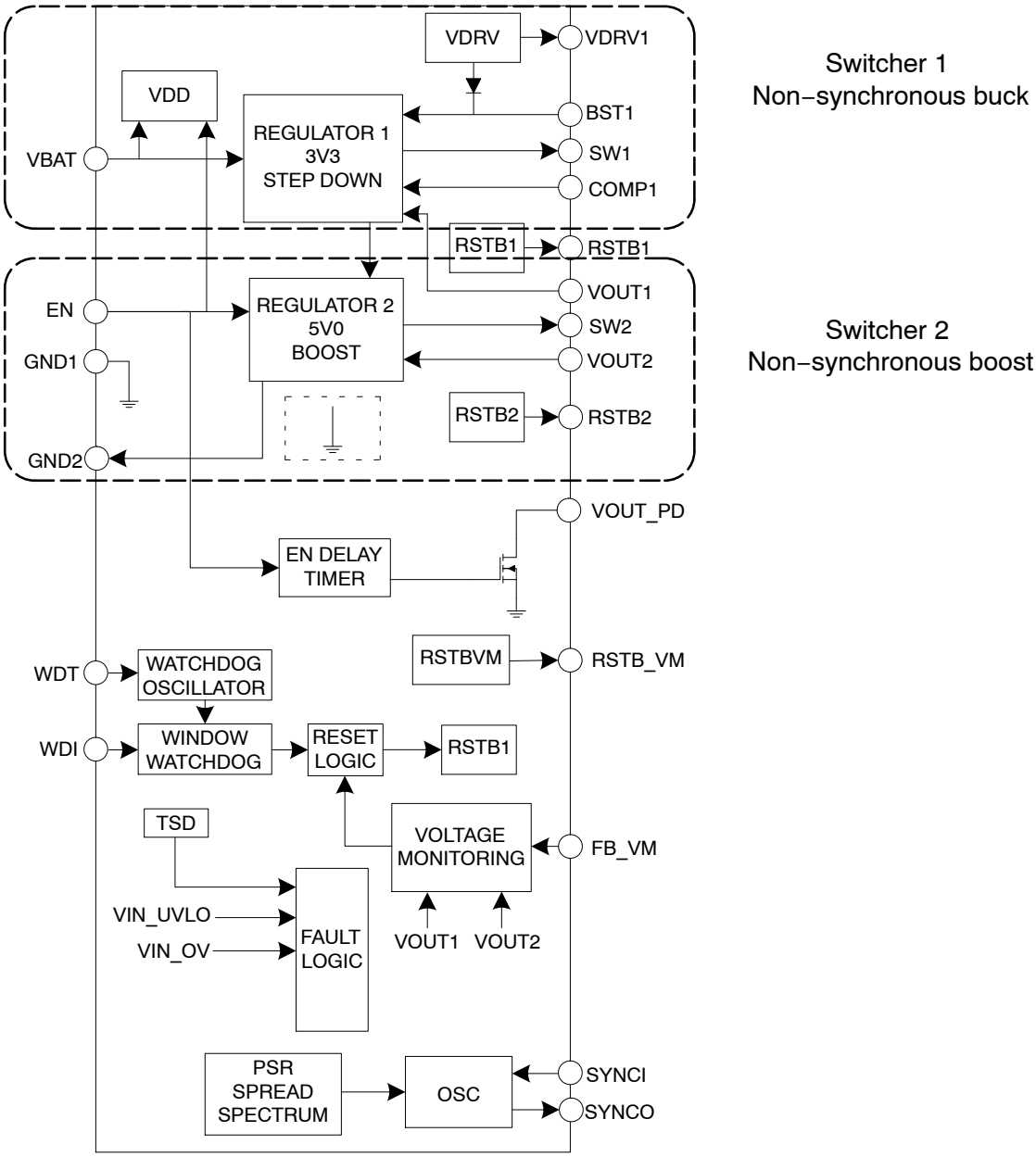


Figure 27. NCV97200 Simplified Block Diagram

Input Voltage

The main supply for the NCV97200 is the VBAT pin, which must always be connected to a voltage source between 4.1 V and 37 V.

- Below 4.1 V (max) an under−voltage lockout (UVLO) circuit inhibits all switching and resets the soft−start circuits.
- Above 40 V (max) an over−voltage shutdown (OVSD) circuit inhibits all switching and allows the NCV97200 to survive a 45 V load dump condition. Normal operation resumes when VBAT decreases below 34 V (min)

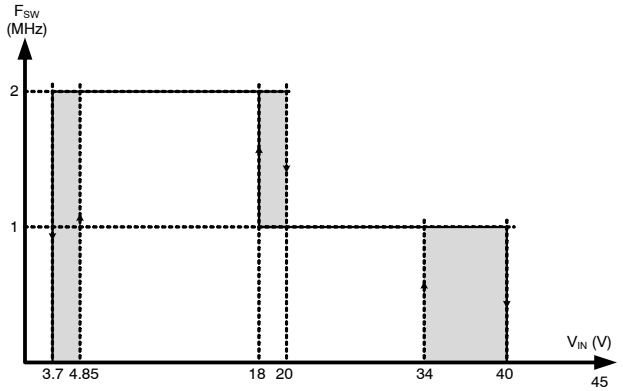


Figure 28. Input Voltage Range

Enable and Soft−Start

The NCV97200 can be completely disabled (shutdown mode) by connecting the enable (EN) pin to GND. As a result, both outputs are stopped and the internal current consumption drops below 10 μA.

The EN pin is designed to accept either a logic−level signal or the battery voltage. If connecting EN to battery, and battery voltage could exceed 40 V, make the connection through a 10 k resistor. Upon receiving an input greater than 2 V, the EN pin allows switcher 1 to begin soft−start and ramp up to 3.3 V (typically in 1.4 ms). After the soft−start of VOUT1 is complete, switcher 2 (the boost regulator) begins its soft−start and ramps up to 5.0 V. Switcher 2 does not have its own enable input pin and is linked to the master enable input.

The diagram below shows the startup sequence when EN is activated:

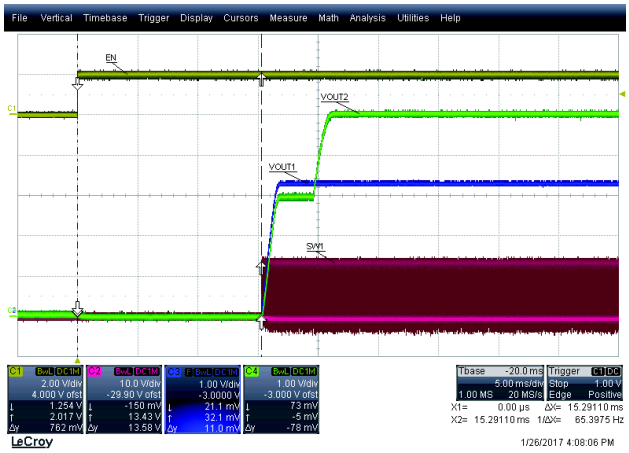


Figure 29. Startup Sequence

Enable Delay Time

The switching outputs of the NCV97200 are delayed for 16 ms after receiving a valid high signal on the EN pin.

When a valid EN signal is received by the IC, the internal rails and circuitry power up. During the enable delay time, switching is inhibited and the outputs do not power up. Once the delay time is complete, switching begins and the regulators power up with a soft start.

Output Discharge Device

In addition to the delay timer on the EN signal, an optional active pull down is available to discharge the outputs during the enable delay time. When not used, the VOUT_PD pin should be connected to GND. Please refer to the following schematic:

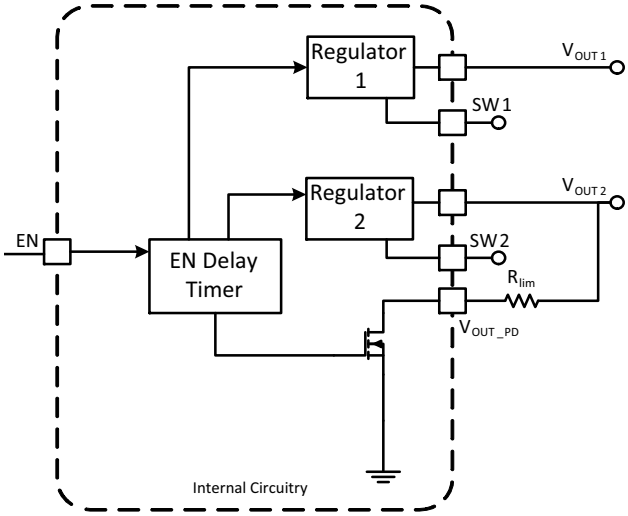


Figure 30. VOUT_PD Internal Circuitry

To use the active discharge, connect VOUT2 through a current limiting resistor to the VOUT_PD pin. The current limiting resistor, Rlim, should be in the range of 10 Ω. Upon enabling and during the enable delay time, the internal discharge device will be activated until the regulators are turned on.

Oscillator

Both switching regulators in the NCV97200 share the same oscillator, which, by default, operates at 2.0 MHz with pseudo−random spread spectrum (spread spectrum described in next section). The switching frequency can be adjusted from 2.0 MHz to 2.6 MHz using the external synchronization input pin, SYNCI. Manually adjusting the switching frequency using the SYNCI pin will adjust the switching frequency for both regulators since they share a common oscillator.

There are 2 types of frequency adjustments that can occur with the NCV97200: maximum duty cycle foldback and high voltage frequency foldback. These frequency foldback mechanisms take place outside the main oscillator in logic and only affect the regulators meeting the criteria. The main oscillator frequency remains unchanged.

Maximum duty cycle foldback takes place at low input voltages where the conversion ratio wants to be larger than the minimum off time allows. Each switch cycle, logic outside the oscillator allows either a maximum duty cycle up to 90% (typical) or 100% duty cycle operation by skipping an off−time. The oscillator is allowed to skip up to three consecutive off−times in this manner. The lowest effective frequency is 500 kHz at typical battery voltages. Once the input voltage increases or the load decreases, 2 MHz operation will resume.

At high input voltages (above 20 V), the oscillator folds back to 1 MHz operation to properly maintain the output voltage when the conversion ratio needs to be lower than the minimum on time allows at 2 MHz operation. If maximum duty cycle foldback also takes place above 20 V input, the lowest effective frequency is still 500 kHz. Once the input voltage drops back below 18 V, 2 MHz operation will resume.

Spread Spectrum

In SMPS devices, switching translates to higher efficiency and switching at high frequency can reduce the size of external components. Unfortunately, switching also leads to a higher EMI profile. We can greatly reduce some of the peak radiated emissions with some spread spectrum techniques. Spread spectrum is a method used to reduce the peak electromagnetic emissions of a switching regulator.

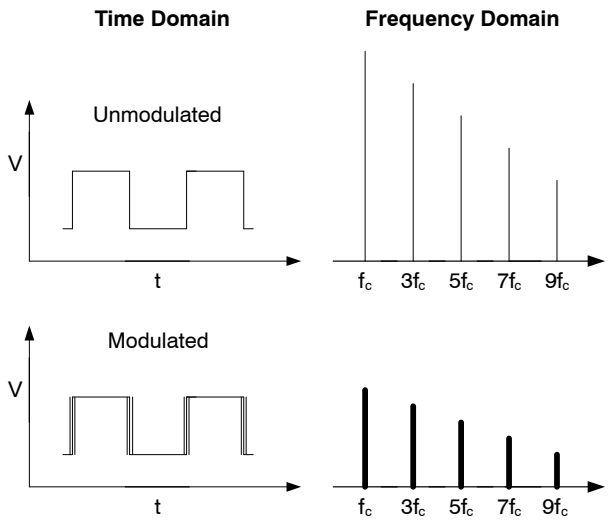


Figure 31. Spread Spectrum Comparison

The NCV97200 includes built−in spread spectrum for reduced peak radiated emissions. This IC uses a pseudo−random generator to set the oscillator frequency to one of 16 discrete frequency bins (shown in the table, below). Each digital bin represents a shift in frequency by 40 kHz over the range 2.0 MHz to 2.6 MHz. Over time, each bin is used an equal number of times to ensure an even spread of the spectrum. This reduces the peak energy at the fundamental frequency, 2.0 MHz, and spreads it into a wider band.

Table 4. PSEUDO−RANDOM FREQUENCY BINS

Pseudo Random Digital Output	Switching Frequency
0000	2.00 MHz
0001	2.04 MHz
0010	2.08 MHz
0011	2.12 MHz
0100	2.16 MHz
0101	2.20 MHz
0110	2.24 MHz
0111	2.28 MHz
1000	2.32 MHz
1001	2.36 MHz
1010	2.40 MHz
1011	2.44 MHz
1100	2.48 MHz
1101	2.52 MHz
1110	2.56 MHz
1111	2.60 MHz

The period of each switch cycle will change inversely to the switching frequency but the duty cycle will remain constant to properly maintain the output.

EMI and Input Filter

In addition to spread spectrum, an input filter is recommended to further reduce emissions due to switching heavy loads.

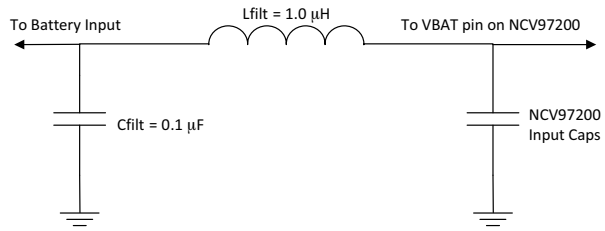


Figure 32. LC Input Filter

When connecting the battery voltage to other circuits on the PCB, be sure to connect them to the battery input side, not the NCV97200 side, of the LC filter. This will give the best possible noise performance.

Current Limit and Short Circuit Frequency Foldback

Each switching regulator has a peak current limit to protect the inductor and downstream components in case of a short circuit or transient event. Due to the ripple current through the inductor, the maximum dc output current of each converter is lower than the peak current limit. If the peak current limit is reached during the switch cycle, the switch turns off for the remainder of the cycle and turns on again at the start of the next cycle.

During severe output overloads or short circuit conditions, the primary regulator (switcher 1) automatically reduces its switching frequency and enters analog foldback.

This creates a duty cycle small enough to limit the power in the output components while maintaining the ability to automatically reestablish the output voltage if the overload is removed. This foldback changes the main oscillator and will apply to both regulators. Once the overload or short circuit is removed, 2 MHz operation will resume.

If the output current is still too high, the regulators, individually, automatically enter an auto−recovery burst mode (hiccup mode) to self−protect and further reduce dissipated power in the output components. When a short−circuit is detected, the switcher disables its output, remains off for the hiccup time, and then goes through the power−on reset procedure. If the short has been removed, the output re−enables and operates normally. If the short is still present, the cycle begins again until the short is removed. Hiccup mode is continuous at a typical rate of 32 kHz until the short is removed.

External Frequency Synchronization

The NCV97200 can be synchronized to an external clock signal. If the IC does not have its switching frequency controlled by the SYNCI input, it operates normally at the default switching frequency, typically 2.0 MHz with spread spectrum.

The signal at the SYNCI pin is used as a synchronization input during normal operation and is ignored during startup, shutdown, overvoltage, and other transient conditions. When the switching frequency is controlled by the SYNCI input, synchronization starts within 2 ms of soft start completion. Please keep in mind that spread spectrum will be disabled when the oscillator is being synchronized with an external clock.

A rising edge on the SYNCI pin causes the current oscillator period to end and a new period to start. The switchnode of switcher 1 goes high 90 ns after a SYNCI rising edge, and the switchnode of switcher 2 goes low 350 ns after a SYNCI rising edge. If another rising edge does not arrive at the SYNCI pin within the Master Reassertion time, the NCV97200 resumes with the default switching frequency. This allows for uninterrupted operation in the event that the external clock is turned off.

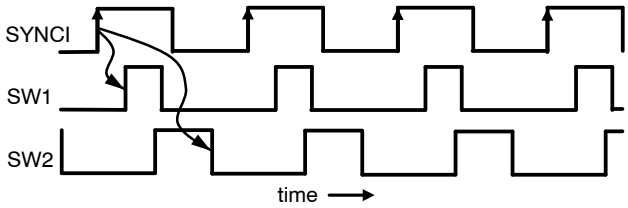


Figure 33. External Synchronization Timing

Output SYNCO

The SYNCO output produces a square wave derived from the VDRV1 output that is suitable for driving the synchronization inputs of other switching converters.

The SYNCO falling edge precedes switchnode 1 rising edge by approximately 100 ns, and SYNCO rises half a switching period later. Connecting the SYNCI pin of another NCV97200 to SYNCO causes both switchers to switch at the same frequency, but out of phase. If a SYNCI signal is present, or under transient conditions such as startup and high VBAT voltage, the SYNCO output is held low. When SYNCO is active, the frequency is modified by the same Spread Spectrum utilized by switchers 1 and 2.

Reset & Delay

When the voltage at the VOUT1 pin is not between the Switcher 1 high−voltage and low−voltage reset thresholds, the open−drain RSTB1 output is asserted (pulled low). Also, if VOUT1 voltage is greater than approximately 2 V, then an EN pin low, or a Thermal Shutdown, VBAT over−or under−voltage, or Watchdog Timer fault will cause the RSTB1 output to be asserted.

When the voltage at the VOUT2 pin is not between the Switcher 2 high−voltage and low−voltage reset thresholds, the open−drain RSTB2 output is asserted. RSTB2 is also asserted in response to VBAT and TSD faults. When the voltage at the FB_VM pin is not between the External Supply high−voltage and low−voltage reset thresholds, the open−drain RSTB_VM output is asserted.

Each of the RSTB signals can either be used as a reset with delay or as a power good (no delay). The delay is determined by the current into the RSTBx pin, set by a resistor, show in Figure 34, below.

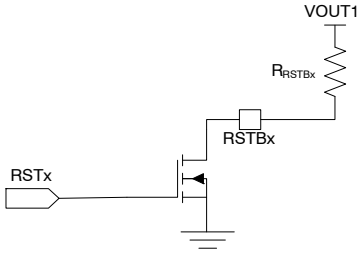


Figure 34. Reset Delay Circuit

Use the following equation to determine the ideal reset delay time using currents less than 500 μA:

$$t_{delay} = \frac{2475}{I_{RSTBx}}$$

where:

t_{delay}: ideal reset delay time [ms]

I_{RSTBx}: current into the RSTBx pin [μA]

Using I_{RSTBx} = 1 mA removes the delay and allows the reset to function as a “power good” pin.

The RSTBx resistor is commonly tied to VOUT1. Typical delay times for a 3.3 V pull−up can be achieved with the following resistor values:

Table 5. RESET DELAY TIMES

R_{RSTBx} (kΩ)	t_{DLY} (ms)
3.3	0
6.6	5
10	7.5
15	11.3
20	15.0
25	18.8
33	24.8

Functional Safety

The NCV97200 has been developed according to ISO−26262 targeting ASIL B/C applications. With this in mind, we've specifically included the following items to make this power supply compatible with your safety application:

1. There are 2 independent bandgaps for the internal reference voltages. The primary bandgap is used for the internal supplies and the regulation of each power supply output. The second bandgap is primarily used as a safety mechanism as a reference to which the RSTBx circuits are compared.
2. Each output voltage has a separate window voltage monitoring circuit that's comparing the output feedback signal to the internal reference generated by the second bandgap. Each output voltage is monitored for overvoltage and undervoltage conditions. Please see "Reset & Delay" for more details.
3. A window watchdog is included to monitor an incoming watchdog signal from a microcontroller. This behavior is detailed in the "Watchdog" section.

Watchdog

The NCV97200 contains a Window Watchdog Timer function, which requires the microcontroller to send a correctly−timed pulse to the WDI pin in order to demonstrate proper functionality. The watchdog oscillator runs independently of the switching oscillator. Window watchdog is active unless RSTB1 is asserted (low) due to VOUT1 out of regulation, or global faults (VBAT under− or over−voltage or thermal shutdown).

Any Watchdog Timer fault (**$t_{WD_timeout}$**, **t_{WD_CLS}**, **t_{WD}**, or WDI always high) causes RSTB1 to be pulled low for the duration of the Reset Delay Time plus 3 WDT cycles (typ). Additionally, depending on the version of NCV97200, Switchers 1 and 2 will be disabled (**see Table 6**).

Watchdog timeout mode with long timing (**$t_{WD_timeout}$**) begins at the rising edge of RSTB1. If a rising edge is not received at the WDI pin during **$t_{WD_timeout}$**, it is a fault.

When a rising edge is received at the WDI pin during **$t_{WD_timeout}$**, both a closed (short) window time (**t_{WD_CLS}**) and an open (longer) window time (**t_{WD}**) are started. If a second rising edge is received during **t_{WD_CLS}**, it is a fault.

To avoid assertion of RSTB1, the second rising edge must appear before the end of **t_{WD}** (but not during **t_{WD_CLS}**). If the second rising edge is not received before the end of **t_{WD}**, it is a fault.

If the WDI pin voltage remains high for the duration of the active timeout or window period (**$t_{WD_timeout}$** or **t_{WD}**), it is a fault. WDI already high when RSTB1 rises is treated as a WDI pulse − immediately starting the closed and open window times (**t_{WD_CLS}** and **t_{WD}**).

Table 6. WATCHDOG FAULTS

Part Number	Type of Watchdog Fault			
	1st timeout (**$t_{WD_timeout}$**)	Closed window (**t_{WD_CLS}**)	Open window (**t_{WD}**)	WDI Stays High
NCV97200MW01	RSTB1 goes low for the Reset Delay Time (**t_{RESET}**), but both switchers remain active			
NCV97200MW33	RSTB1 goes low, and both switchers are disabled for the Enable Delay Time (**t_{DISABL}**) − after which they soft-start. After VOUT1 reaches regulation, RSTB1 remains low for the Reset Delay Time (**t_{RESET}**)			

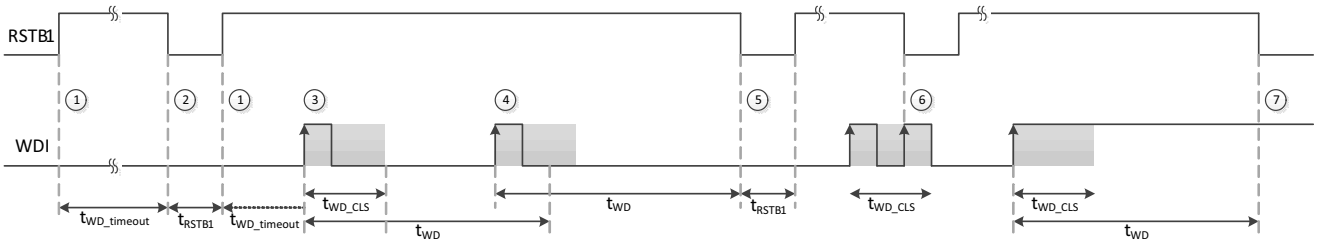


Figure 35. Watchdog Function and Timing

1. Rising edge on RSTB1 triggers the start of watchdog timeout mode.
2. No watchdog trigger within the watchdog timeout time $t_{WD_timeout}$. RSTB1 pulled low.
3. Window trigger mode active after rising edge on the WDI pin.
4. First successful watchdog trigger within the window time t_{WD}.
5. Watchdog trigger failed, no rising edge at WDI pin within window time t_{WD}. RSTB1 pulled low.
6. Watchdog trigger failed, rising edge at WDI pin within boundary time t_{WD_CLS}. RSTB1 pulled low.
7. Watchdog trigger failed, signal at WDI pin permanent high. RSTB1 pulled low.

Choosing the best capacitor for C_{WDT} requires first finding the value that sets the minimum $t_{WD_timeout}$ equal to the maximum processor boot−up time t_{BOOT}:

C_{WDTmin} (pF) ≥ 0.4366 x t_{BOOT} (ms) +7 pF.

Then choose the lowest standard value capacitor C_{WDTstd} satisfying the following equation:

$C_{WDTstd} \geq C_{WDTmin}$ / (100% − tol) [tol = % tolerance & temperature variation of the chosen capacitor]

The resulting typical $t_{WD_timeout}$ interval is:

$t_{WD_timeout}$ (ms, typ) = 2.87 x C_{WDTstd} (pF) + 20

and the resulting $t_{WD_timeout}$ range including NCV97200 temperature & tolerance effects is:

$t_{WD_timeout}$ (ms, min) = 2.29 x (100% − tol) x C_{WDTstd} (pF) + 16

$t_{WD_timeout}$ (ms, max) = 3.63 x (100% + tol) x C_{WDTstd} (pF) + 26

To be valid, the period of the signal the processor applies to the WDI pin (T_{WDI}) must be: min $t_{WD_timeout}$ /15 ≤ T_{WDI} ≤ max $t_{WD_timeout}$ /60.

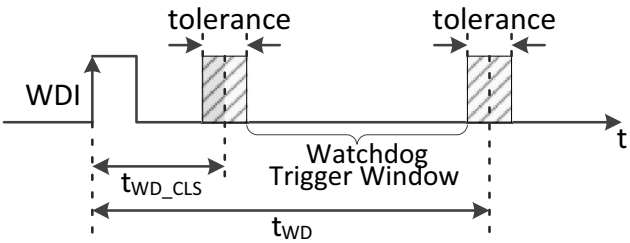


Figure 36. Watchdog Window with Tolerances

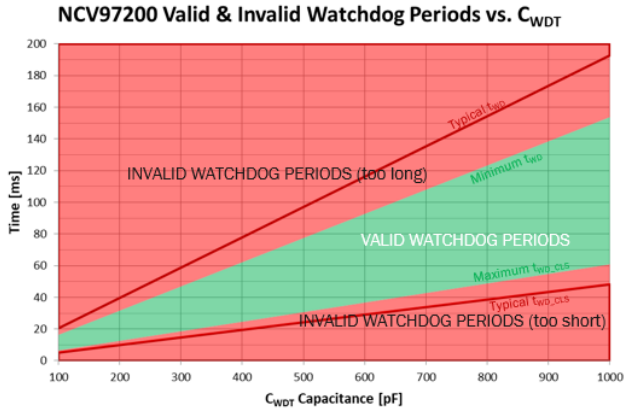


Figure 37. NCV97200 Valid & Invalid Watchdog Periods vs. C_{WDT}

Debug Mode

The NCV97200 includes a user selectable "debug mode" that disables spread spectrum and the watchdog to make it easier to take certain measurements during evaluation. While the watchdog is disabled, it is unable to assert a fault on the RSTB1 signal.

To enter and remain in debug mode, connect the WDT pin to GND and connect the SYNCI pin high (a voltage greater than 2 V). If either of these 2 criteria are not met, the NCV97200 will resume normal operation. Further, if the WDT pin is held low while the SYNCI is not held high, a fault will be reported on RSTB1.

SWITCHER 1

The primary dc−dc output for the NCV97200 is 3.3 V, set by an internal resistor divider. This buck regulator is non−synchronous and requires an external low−side freewheeling diode to operate.

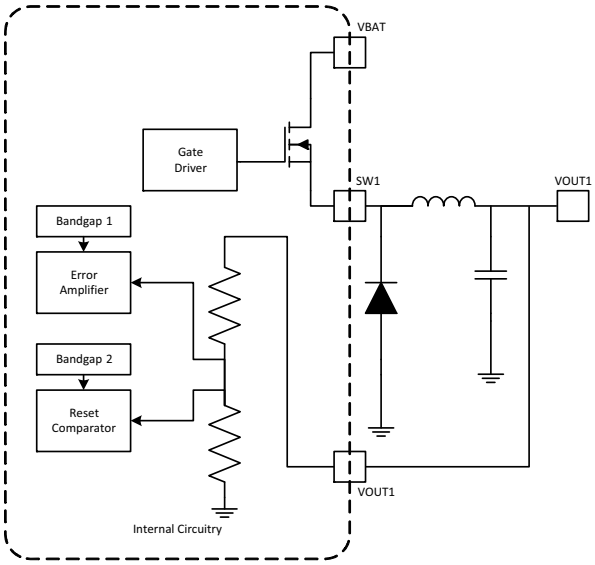


Figure 38. Switcher 1 Block Diagram

Internally, connected to the VOUT1 pin, the primary feedback regulates the output and the secondary path compares to the second reference for the reset circuitry.

The EN pin controls the enable circuitry for the switchers. It can accept a logic−level input and is also capable of high voltages and can be connected directly to VBAT. If EN is connected to VBAT, and VBAT voltage might exceed 40 V, the connection from EN to VBAT should be made with a 10 kΩ resistor.

Error Amplifier

Switcher 1 uses a transconductance type error amplifier. The output voltage of the error amplifier controls the peak inductor current at which the power switch shuts off. The Current Mode control method employed allows the use of a simple, type II compensation to optimize the dynamic response according to system requirements.

The compensation components must be connected between the output of the error amplifier and the electrical ground (between pins COMP1 and GND). For most applications, the following compensation circuitry is recommended:

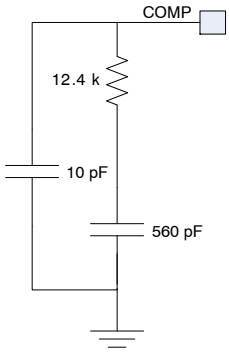


Figure 39. Recommended Compensation for Switcher 1

Slope Compensation

A fixed slope compensation signal is generated internally and added to the sensed current to avoid increased output voltage ripple due to bifurcation of inductor ripple current at duty cycles above 50% (sub−harmonics oscillations). The fixed amplitude of the slope compensation signal requires the inductor to be greater than a minimum value in order to avoid sub−harmonic oscillations. For the 3.3 V output, the recommended inductor value is from 2.2 μH to 4.7 μH.

To determine the minimum inductor required to avoid sub−harmonic oscillations, please refer to the following equation:

$$L_{min} = \frac{V_{OUT}}{2 \cdot S_{ramp}}$$

where:

L_{min}: minimum inductor required to avoid sub−harmonic oscillations [μH]

V_{OUT}: output voltage [V]

S_{ramp}: internal slope compensation [A/μs]

Drive and Bootstrap

At the DRV1 pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV1}), to allow fast recharge of the external bootstrap capacitor (C_{BST1}) used to supply power to the power switch gate driver. If the voltage at the DRV1 pin goes below the DRV1 POR Threshold V_{DRV1SP}, switching is inhibited and the soft−start circuit is reset, until the DRV1 pin voltage goes back up above V_{DRV1ST}.

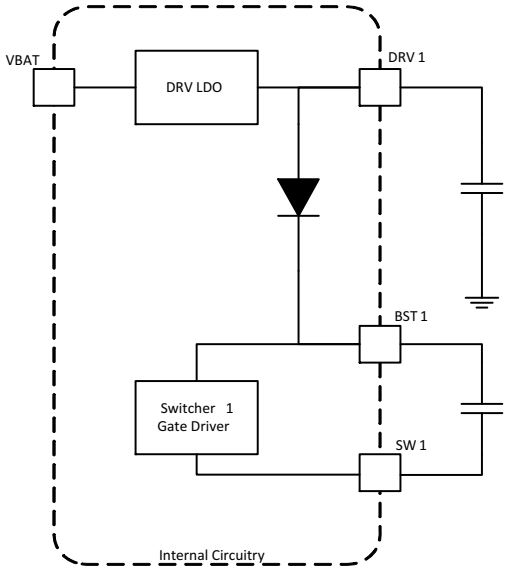


Figure 40. Switcher 1 Drive and Bootstrap Circuitry

In order for the bootstrap capacitor to stay charged, the switch node needs to be pulled down to ground regularly. In very light load condition, when switcher 1 skips switching cycles to keep the output voltage in regulation, the bootstrap voltage could collapse and the regulator stop switching. To prevent this, an approximately 10 mA internal load is connected on VOUT1 to operate correctly in all cases. When the NCV97200 is enabled and VBAT is below approximately 7.5 V, the internal load is increased to approximately 60 mA.

A fast−charge circuit ensures the bootstrap capacitor is always charged prior to starting the switcher after it has been enabled.

Soft Start

Upon being enabled or released from a fault condition, and after the Enable Delay Time, a soft−start circuit ramps the switching regulator error amplifier reference voltage to the target value. During soft−start, the average switching frequency is lower than its normal mode value (typically 2 MHz) until the output voltage approaches regulation.

Current Limit

Due to the ripple on the inductor current, the average output current of a buck converter is lower than the peak

current set point of the regulator. Figure 41 shows – for a 4.7 μH inductor – how the variation of inductor peak current with input voltage affects the maximum DC current switcher 1 can deliver to a load. Figure 42 shows the same for 2.2 μH inductor.

Internal slope compensation Sramp1 also reduces switcher 1 peak current limit proportional to the duty cycle. The amount of this reduction for switcher 1 is the product of Sramp1, switching period, and 3.3 divided by VBAT.

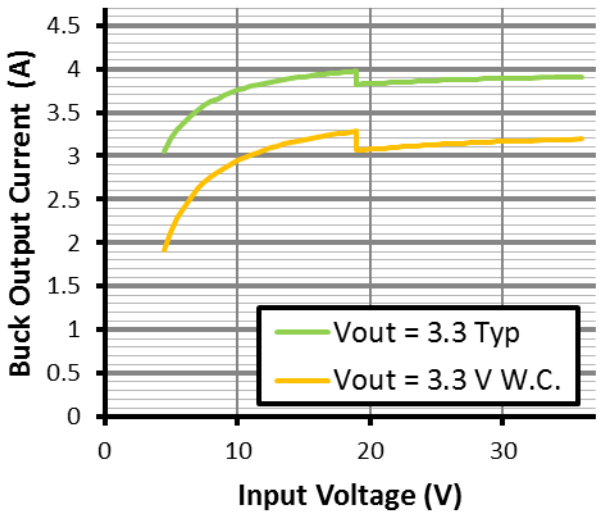


Figure 41. Switcher 1 Dc Output Current vs. VIN with a 4.7 μH Inductor

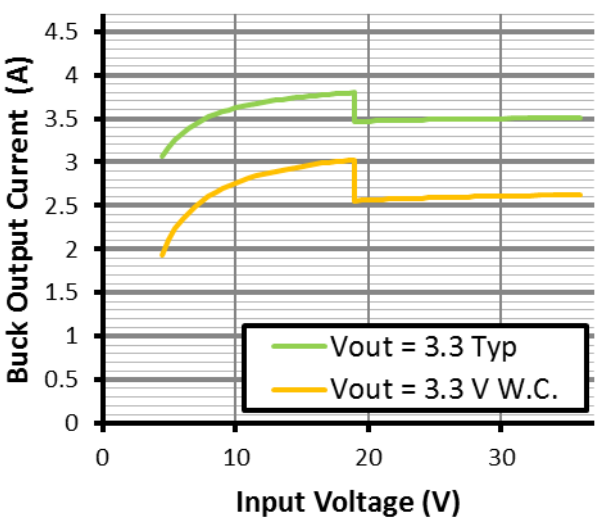


Figure 42. Switcher 1 Dc Output Current vs. VIN with a 2.2 μH Inductor

High Voltage Frequency Foldback

To limit the power lost in generating the drive voltage for the power switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{BAT} Frequency Foldback Threshold V_{FL1U} (see Figure 43) Frequency reduction is automatically terminated when the input voltage drops back below the V_{BAT} Frequency Foldback threshold V_{FL1D}.

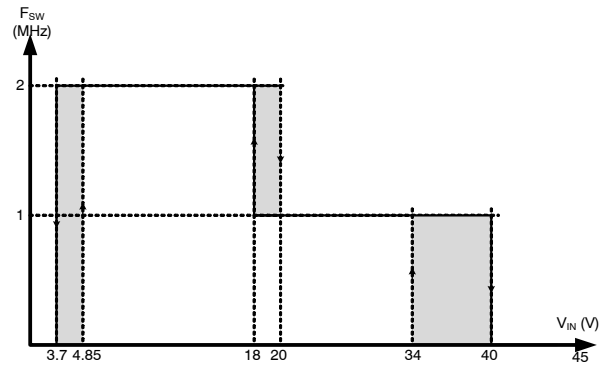


Figure 43. High Voltage Frequency Foldback

Inductor Selection

A 3.3 μH inductor is recommended for Switcher 1, although values between 2.2 μH and 4.7 μH may give more optimized performance in some applications. The relationship between several operating parameters are given by the equation below.

$$L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{\delta I_r \cdot f_{sw} \cdot I_{OUT}}$$

where:

V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
δI_r: inductor current ripple [%]
f_{sw}: switching frequency [Hz]
I_{OUT}: dc output current [A]

Discontinuous Mode

The regulator operates in Continuous Conduction Mode (CCM) when average inductor current exceeds half the peak−to−peak ripple current, and in Discontinuous Conduction Mode (DCM) when it does not. The borderline between these modes can be found using the following equation:

$$I_{BCM} = \frac{1}{2} \cdot \frac{\left(1 - \frac{V_{OUT}}{V_{IN,max}}\right)}{f_{sw}} \cdot \frac{V_{OUT}}{L}$$

where:

I_{BCM}: borderline conduction mode output current [A]
V_{OUT}: dc output voltage [V]
$V_{IN,max}$: maximum dc input voltage [V]
f_{sw}: switching frequency [Hz]
L: inductor value [H]

Average output currents above IBCM will cause operation in CCM while average output currents below IBCM will cause operation in DCM.

SWITCHER 2

The NCV97200 contains a boost regulator, switcher 2, which boosts the 3.3 V from the switcher 1 to 5.0 V. This non−synchronous boost regulator requires an external freewheeling diode. Switcher 2 is intended to be used for in−vehicle networks (e.g. CAN) and can supply up to 400 mA dc.

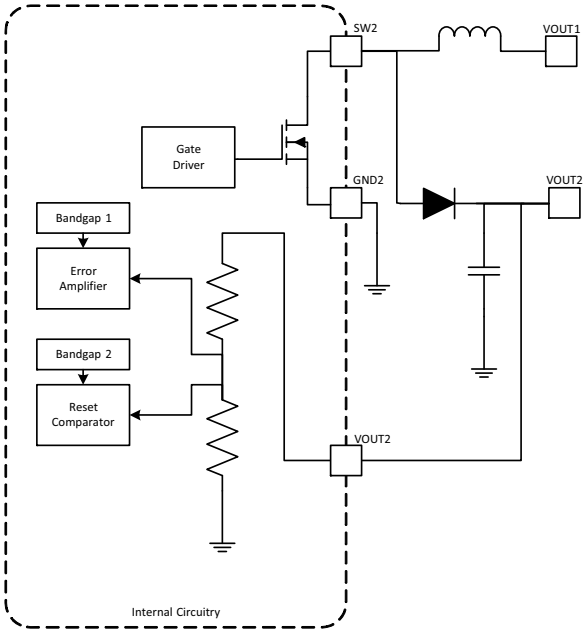


Figure 44. Switcher 2 Block Diagram

Internally, connected to the VOUT2 pin, the primary feedback regulates the output and the secondary path compares to the second reference for the reset circuitry.

The EN pin controls the enable circuitry for the switcher 2 output. Once switcher 1 has completed soft−start and the output is in regulation, switcher 2 is automatically enabled.

Error Amplifier

Switcher 2 uses a voltage type error amplifier. The compensation for this regulator is internal and cannot be adjusted.

Soft Start

Upon being enabled or released from a fault condition, and once switcher 1 has completed soft start, a soft−start circuit ramps the switching regulator error amplifier reference voltage to the final value. The typical soft−start duration is 1.4 ms.

Please note that since this is a boost regulator, the VOUT2 output will be a diode voltage below VOUT1 until it starts switching in regulation. This is normal behavior – please see the scope capture below:

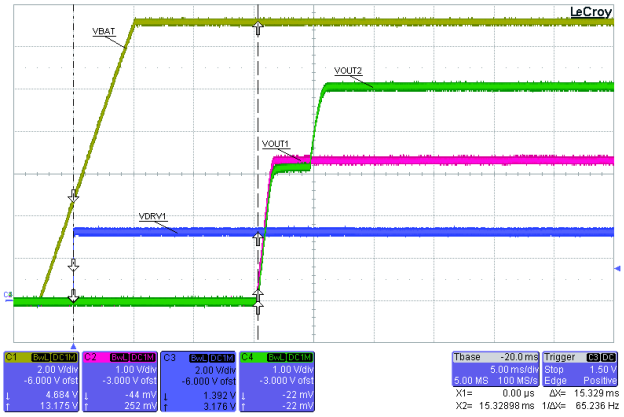


Figure 45. Switcher 2 Soft−start

Current Limit

Due to the ripple on the inductor current, the average output current of the boost converter is lower than the peak current set point of the regulator. Table 7 shows some examples of common setups.

Table 7. SW2 WORST CASE DC OUTPUT CURRENT

Output Voltage (V)	Inductor Value (uH)	Worst Case Max Dc Output (mA)	Typical Max Dc Output (mA)
5.0	4.7	450	530
5.0	2.2	400	480

ORDERING INFORMATION

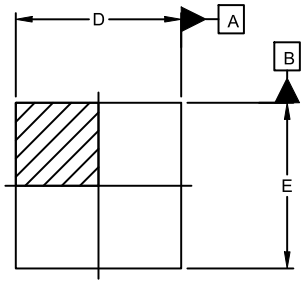
Device	Distinguishing Characteristic	Package	Part Marking	Shipping†
NCV97200MW01R2G	No shutdown upon Watchdog fault	QFNW20 (Pb−Free)	97200 01	4000 / Tape & Reel
NCV97200MW33R2G	Shutdown (auto−restart) upon Watchdog fault	QFNW20 (Pb−Free)	97200 33	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

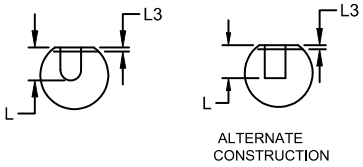
QFNW20 4x4, 0.5P
CASE 484AD
ISSUE C

DATE 03 DEC 2019

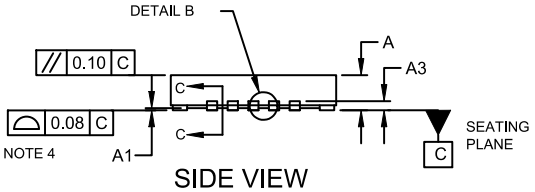
SCALE 2:1



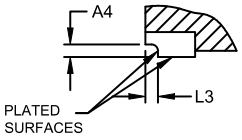
TOP VIEW



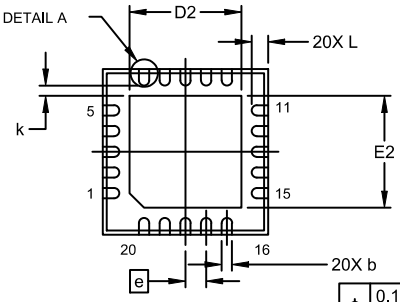
DETAIL A



SIDE VIEW



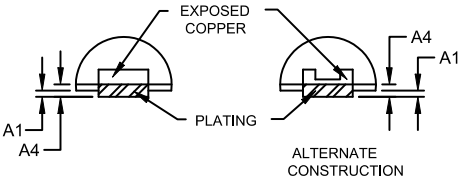
SECTION C-C



	0.10	C	A	B
	0.05	C		

NOTE 3

BOTTOM VIEW



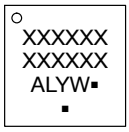
DETAIL B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	0.50 BSC		
k	0.25 REF		
L	0.35	0.40	0.45
L3	---	---	0.09

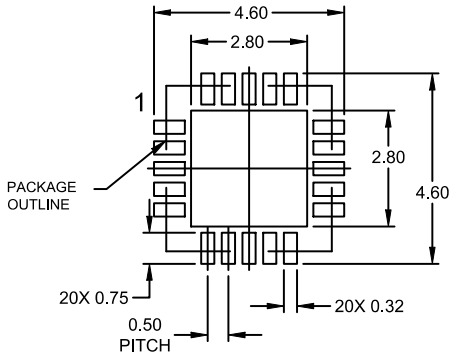
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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