THE DATASHEET OF

MPXR4040VVU264

Freescale Semiconductor
Data Sheet: Technical Data

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RoHS

PXR40

PXR40 Microcontroller Data Sheet

TEPBGA–416
27mm x 27mm

- Dual issue, 32-bit CPU core complex (e200z7)
  - Compliant with the Power Architecture embedded category
  - 16 KB I-Cache and 16 KB D-Cache
  - Includes an instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - Includes signal processing extension (SPE2) instruction support for digital signal processing (DSP) and single-precision floating point operations
- 4 MB on-chip flash
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 256 KB on-chip general-purpose SRAM including 32 KB of standby RAM
- Two direct memory access controller (eDMA2) blocks
  - One supporting 64 channels
  - One supporting 32 channels
- Interrupt controller (INTC)
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External bus interface (EBI) for calibration and application development (not available on all packages)
- System integration unit (SIU)
- Error correction status module (ECSM)
- Boot assist module (BAM) supports serial bootload via CAN or SCI
- Two second-generation enhanced time processor units (eTPU2) that share code and data RAM.
  - 32 standard channels per eTPU2
  - 24 KB code RAM
  - 6 KB parameter (data) RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Four enhanced queued analog-to-digital converters (eQADC)
  - Support for 64 analog channels
  - Includes one absolute reference ADC channel
  - Includes eight decimation filters
- Four deserial serial peripheral interface (SPI) modules
- Three enhanced serial communication interface (UART) modules
- Four controller area network (CAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003/5001-2008 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic

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Table of Contents

1 PXR40 features

Table 1 displays the PXR40 feature set.

Table 1. PXR40 feature set

Feature	PXR40
Core	e200z7
SIMD	Yes
VLE	Yes
Cache	32 KB (16 KB Instruction/16 KB Data)
Non-maskable interrupt (NMI)	NMI & Critical Interrupt
MMU	64 entry
MPU	Yes
XBAR	5 × 5
Windowing software watchdog	Yes
Nexus	3+
SRAM	256 KB
Flash	4 MB
Flash fetch accelerator	4 × 256 bit (first 1 MB of memory is 4 × 128; last 3 MB are 4 × 256)
External bus	Yes
Calibration bus	16 bit non-muxed 32 bit muxed
DMA	96 channel
DMA Nexus	Class 3
Serial	3
UART_A	Yes
UART_B	Yes
UART_C	Yes
Microsecond bus uplink	Yes
CAN	4
CAN_A	64 message buffers
CAN_B	64 message buffers
CAN_C	64 message buffers
CAN_D	64 message buffers
CAN_E	No
SPI	4
SPI_A	Yes
SPI_B	Yes
SPI_C	Yes
SPI_D	Yes
FlexRay	Yes
Ethernet	No
System timers	4 PIT chan 4 SWT 1 Watchdog
eMIOS	32 channel
eTPU	64 channel
eTPU_A	Yes (eTPU2)
eTPU_B	Yes (eTPU2)

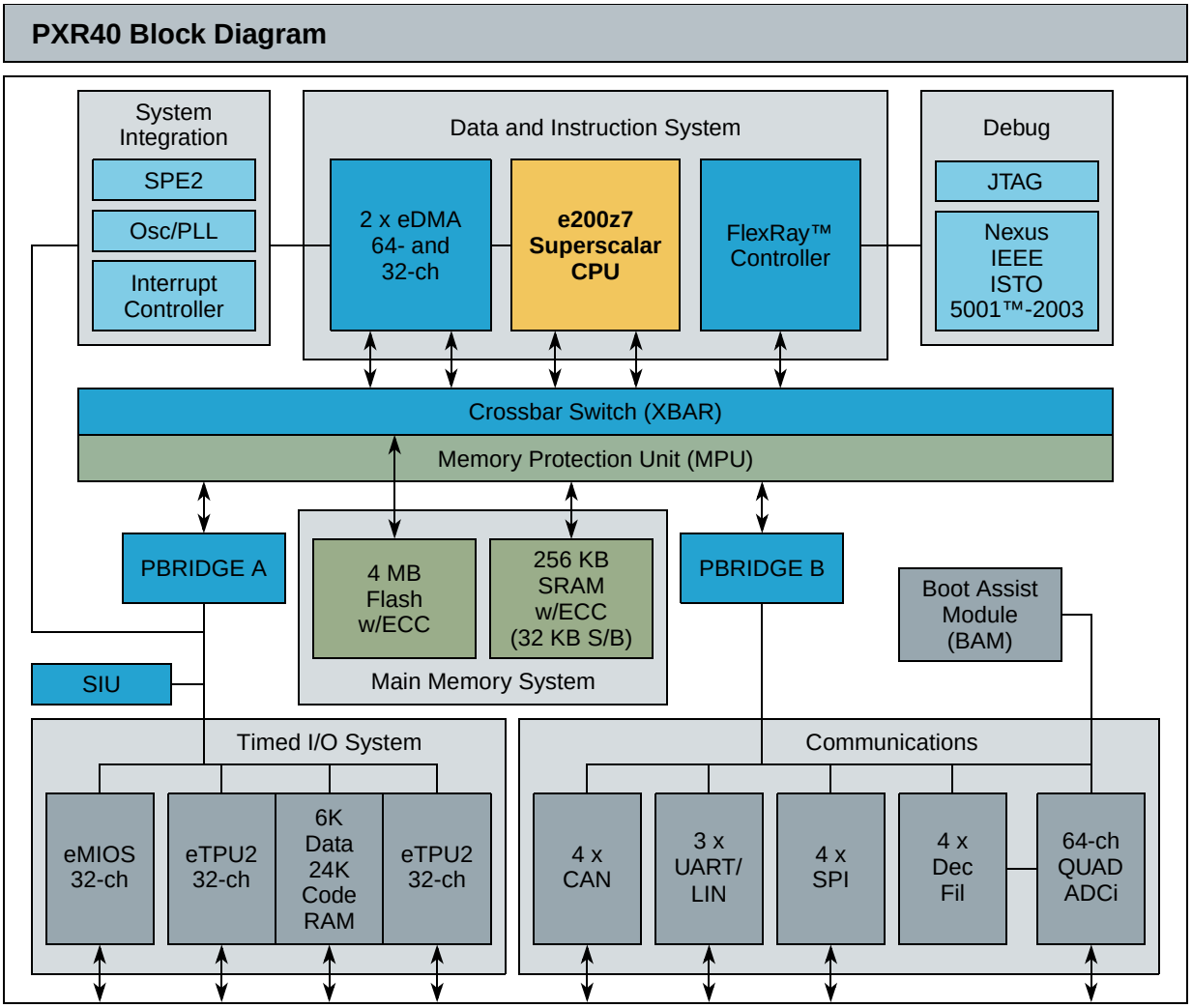
Table 1. PXR40 feature set (continued)

Feature	PXR40
Code memory	24 KB
Data memory	6 KB
Interrupt controller	448
ADC	64 channel
eQADC_A	Yes
eQADC_B	Yes
Temperature sensor	Yes
Variable gain amp.	Yes
Decimation filter	Yes (8 on eQADC_B)
Sensor diagnostics	Yes
PLL	FM
VRC	Yes
Supplies	5V
Low Power Modes	Stop Mode Slow Mode

Note: 3.3 V is required for certain IO segments only during debug/development (e.g., Nexus 3 trace and bus)

2 PXR40 block diagram

Figure 1 shows a top-level block diagram of the PXR40 microcontrollers.



ADC – Analog-to-digital converter
ADCi – ADC interface
AIPS – Peripheral I/O bridge
AMux – Analog multiplexer
CAN – Controller area network
DECFIL – Decimation filter
EBI – External bus interface
ECSM – Error correction status module
eDMA2 – Enhanced direct memory access
eMIOS – Enhanced modular I/O system
eQADC – Enhanced queued A/D converter module
eTPU2 – Enhanced time processing unit 2
MMU – Memory management unit
MPU – Memory protection unit
PBRIDGE – Peripheral I/O bridge
S/B – Stand-by
SIU – System integration unit
SPE2 – Signal processing engine 2
SPI – Serial peripheral interface controller
SRAM – General-purpose static RAM
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
VLE – Variable length instruction encoding

Figure 1. Block diagram

3 Pin assignments

The figures in this section show the primary pin function. For the full signal properties and muxing table, see Table 4.

3.1 416-ball TEPBGA pin assignments

Figure 2 shows the 416-ball TEPBGA pin assignments in one figure. The same information is shown in Figure 3 through Figure 6.

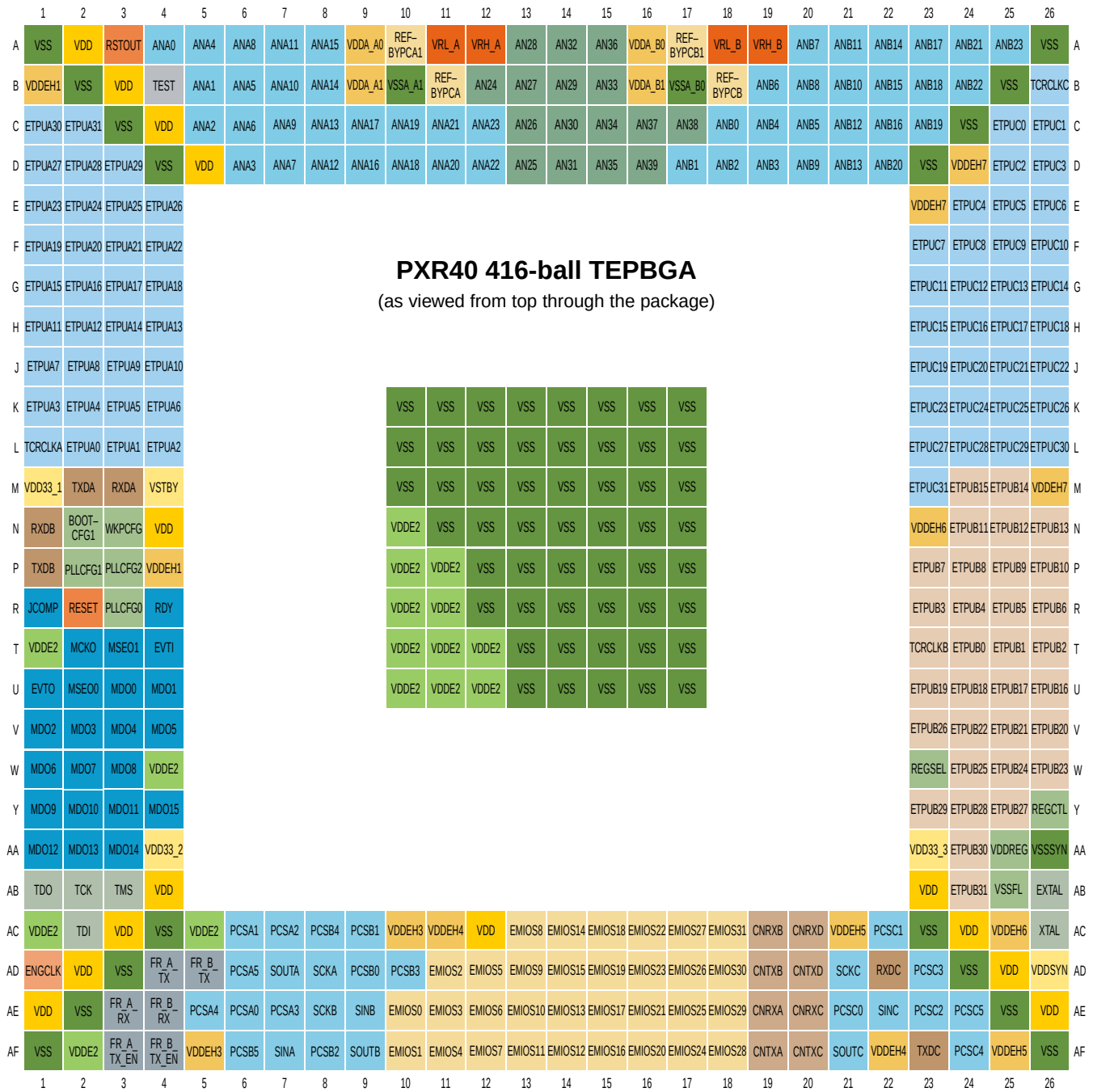


Figure 2. PXR40 416-ball TEPBGA (full diagram)

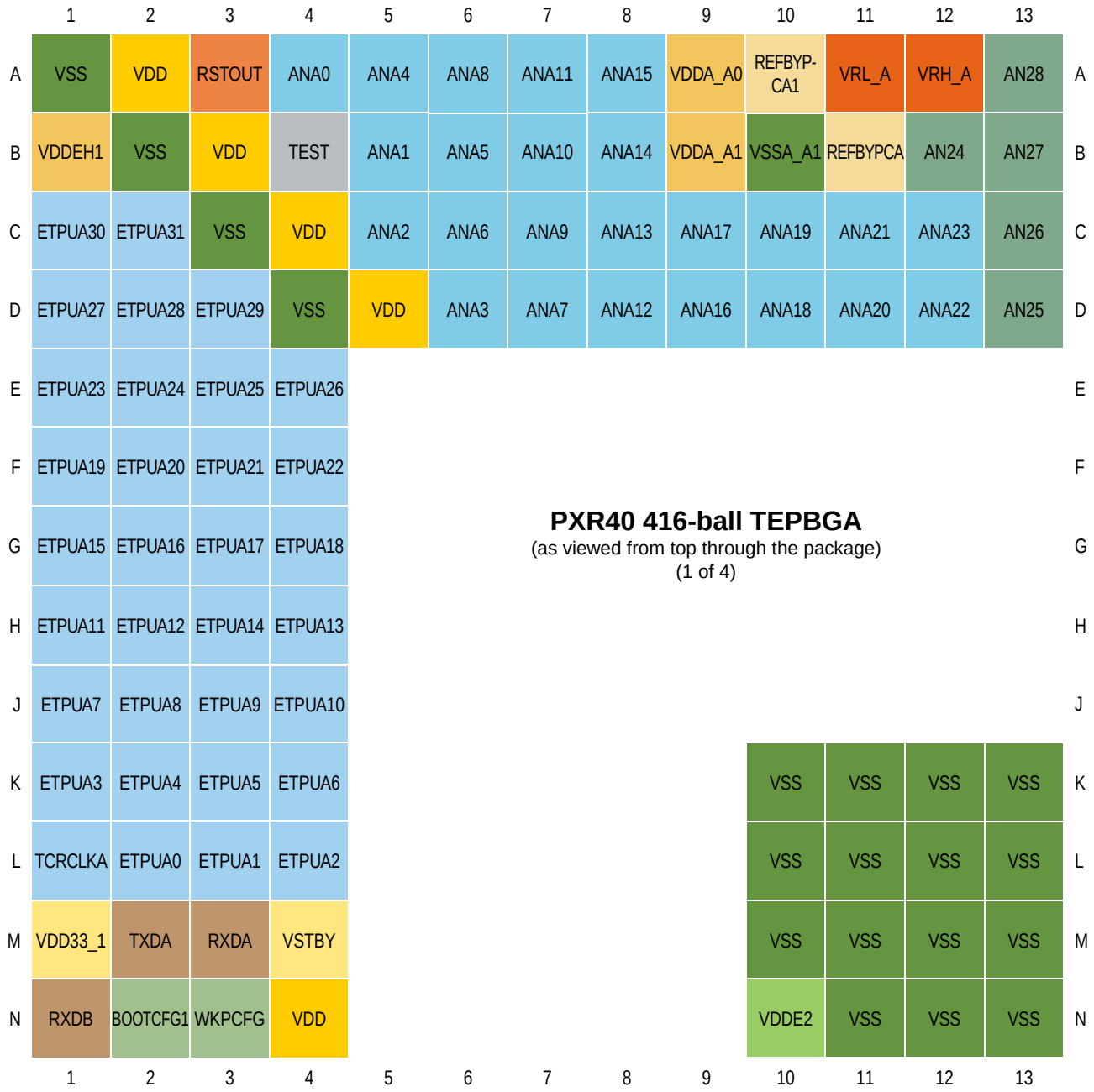


Figure 3. PXR40 416-ball TEPBGA (1 of 4)

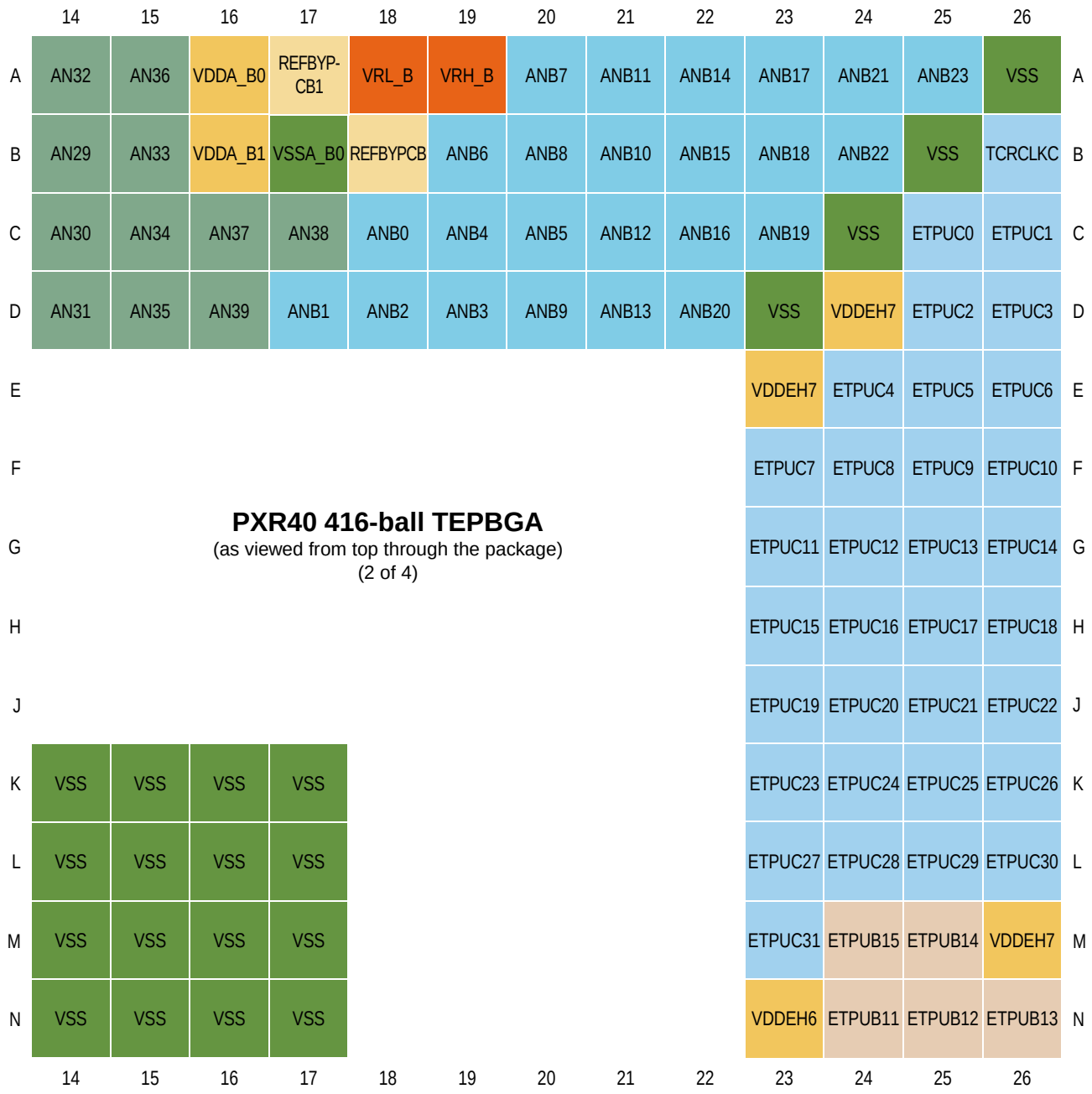


Figure 4. PXR40 416-ball TEPBGA (2 of 4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
P	TXDB	PLLCFG1	PLLCFG2	VDDEH1						VDDE2	VDDE2	VSS	VSS	P
R	JCOMP	RESET	PLLCFG0	RDY						VDDE2	VDDE2	VSS	VSS	R
T	VDDE2	MCKO	MSEO1	EVTI						VDDE2	VDDE2	VDDE2	VSS	T
U	EVTO	MSEO0	MDO0	MDO1						VDDE2	VDDE2	VDDE2	VSS	U
V	MDO2	MDO3	MDO4	MDO5										V
W	MDO6	MDO7	MDO8	VDDE2										W
Y	MDO9	MDO10	MDO11	MDO15										Y
AA	MDO12	MDO13	MDO14	VDD33_2										AA
AB	TDO	TCK	TMS	VDD										AB
AC	VDDE2	TDI	VDD	VSS	VDDE2	PCSA1	PCSA2	PCSB4	PCSB1	VDDEH3	VDDEH4	VDD	EMIOS8	AC
AD	ENGCLK	VDD	VSS	FR_A_TX	FR_B_TX	PCSA5	SOUTA	SCKA	PCSB0	PCSB3	EMIOS2	EMIOS5	EMIOS9	AD
AE	VDD	VSS	FR_A_RX	FR_B_RX	PCSA4	PCSA0	PCSA3	SCKB	SINB	EMIOS0	EMIOS3	EMIOS6	EMIOS10	AE
AF	VSS	VDDE2	FR_A_TX_EN	FR_B_TX_EN	VDDEH3	PCSB5	SINA	PCSB2	SOUTB	EMIOS1	EMIOS4	EMIOS7	EMIOS11	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 5. PXR40 416-ball TEPBGA (3 of 4)

PXR40 416-ball TEPBGA
(as viewed from top through the package)
(4 of 4)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
P	VSS	VSS	VSS	VSS						ETPUB7	ETPUB8	ETPUB9	ETPUB10	P
R	VSS	VSS	VSS	VSS						ETPUB3	ETPUB4	ETPUB5	ETPUB6	R
T	VSS	VSS	VSS	VSS						TCRCLKB	ETPUB0	ETPUB1	ETPUB2	T
U	VSS	VSS	VSS	VSS						ETPUB19	ETPUB18	ETPUB17	ETPUB16	U
V										ETPUB26	ETPUB22	ETPUB21	ETPUB20	V
W										REGSEL	ETPUB25	ETPUB24	ETPUB23	W
Y										ETPUB29	ETPUB28	ETPUB27	REGCTL	Y
AA										VDD33_3	ETPUB30	VDDREG	VSSSYN	AA
AB										VDD	ETPUB31	VSSFL	EXTAL	AB
AC	EMIOS14	EMIOS18	EMIOS22	EMIOS27	EMIOS31	CNRXB	CNRXD	VDDEH5	PCSC1	VSS	VDD	VDDEH6	XTAL	AC
AD	EMIOS15	EMIOS19	EMIOS23	EMIOS26	EMIOS30	CNTXB	CNTXD	SCKC	RXDC	PCSC3	VSS	VDD	VDDSYN	AD
AE	EMIOS13	EMIOS17	EMIOS21	EMIOS25	EMIOS29	CNRXA	CNRXC	PCSC0	SINC	PCSC2	PCSC5	VSS	VDD	AE
AF	EMIOS12	EMIOS16	EMIOS20	EMIOS24	EMIOS28	CNTXA	CNTXC	SOUTC	VDDEH4	TXDC	PCSC4	VDDEH5	VSS	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 6. PXR40 416-ball TEPBGA (4 of 4)

4 Signal properties and muxing

Table 2 shows the signals properties for each pin on the PXR40. For each port pin that has an associated SIU_PCR*n* register to control its pin properties, the supported functions column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit in the order: Primary function (P), Function 2 (F2), Function 3 (F3), and GPIO (G). See Figure 7.

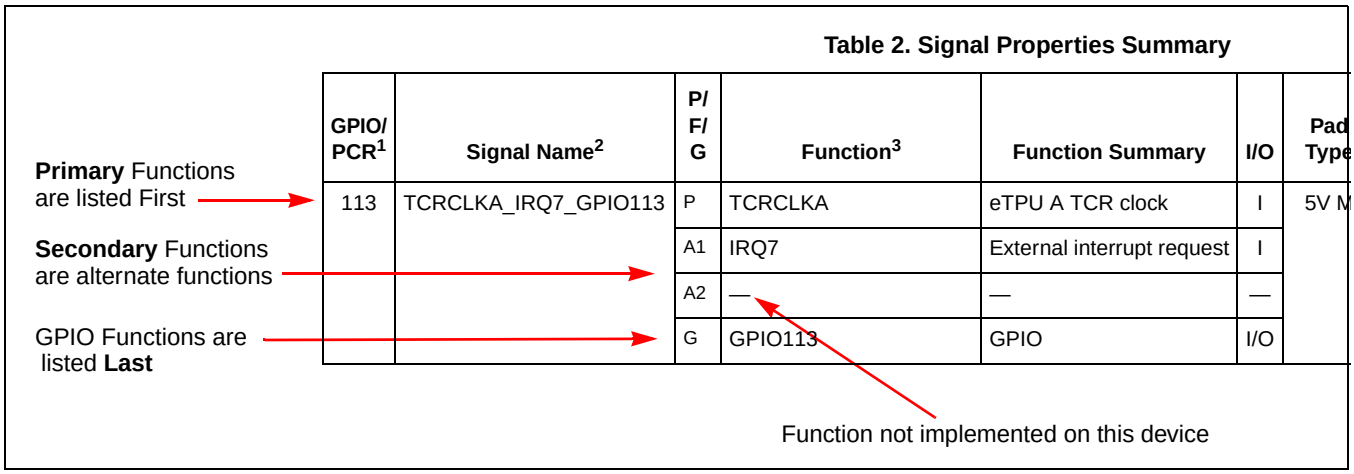


Figure 7. Supported functions example

Table 2. Signal Properties and Muxing Summary

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
eTPU_A								
113	TCRCLKA_IRQ7_ GPIO113	P	TCRCLKA	eTPU A TCR clock	I	MH	V_{DDEH1}	—/Up
		A1	IRQ7	External interrupt request	I			
		A2	—	—	—			
		G	GPIO113	GPIO	I/O			
114	ETPUA0_ETPUA12_ GPIO114	P	ETPUA0	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA12	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO114	GPIO	I/O			
115	ETPUA1_ETPUA13_ GPIO115	P	ETPUA1	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA13	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO115	GPIO	I/O			
116	ETPUA2_ETPUA14_ GPIO116	P	ETPUA2	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA14	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO116	GPIO	I/O			
117	ETPUA3_ETPUA15_ GPIO117	P	ETPUA3	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA15	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO117	GPIO	I/O			
118	ETPUA4_ETPUA16_ GPIO118	P	ETPUA4	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA16	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO118	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
119	ETPUA5_ETPUA17_ GPIO119	P	ETPUA5	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA17	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO119	GPIO	I/O			
120	ETPUA6_ETPUA18_ GPIO120	P	ETPUA6	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA18	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO120	GPIO	I/O			
121	ETPUA7_ETPUA19_ GPIO121	P	ETPUA7	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA19	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO121	GPIO	I/O			
122	ETPUA8_ETPUA20_ GPIO122	P	ETPUA8	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA20	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO122	GPIO	I/O			
123	ETPUA9_ETPUA21_ GPIO123	P	ETPUA9	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA21	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO123	GPIO	I/O			
124	ETPUA10_ETPUA22_ GPIO124	P	ETPUA10	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA22	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO124	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
125	ETPUA11_ETPUA23_ GPIO125	P	ETPUA11	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	ETPUA23	eTPU A channel (output only)	O			
		A2	—	—	—			
		G	GPIO125	GPIO	I/O			
126	ETPUA12_PCSB1_ GPIO126	P	ETPUA12	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSB1	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO126	GPIO	I/O			
127	ETPUA13_PCSB3_ GPIO127	P	ETPUA13	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSB3	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO127	GPIO	I/O			
128	ETPUA14_PCSB4_ GPIO128	P	ETPUA14	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSB4	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO128	GPIO	I/O			
129	ETPUA15_PCSB5_ GPIO129	P	ETPUA15	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSB5	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO129	GPIO	I/O			
130	ETPUA16_PCSD1_ GPIO130	P	ETPUA16	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSD1	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO130	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
131	ETPUA17_PCSD2_ GPIO131	P	ETPUA17	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSD2	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO131	GPIO	I/O			
132	ETPUA18_PCSD3_ GPIO132	P	ETPUA18	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSD3	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO132	GPIO	I/O			
133	ETPUA19_PCSD4_ GPIO133	P	ETPUA19	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSD4	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO133	GPIO	I/O			
134	ETPUA20_IRQ8_ GPIO134	P	ETPUA20	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ8	External interrupt request	I			
		A2	—	—	—			
		G	GPIO134	GPIO	I/O			
135	ETPUA21_IRQ9_ GPIO135	P	ETPUA21	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ9	External interrupt request	I			
		A2	—	—	—			
		G	GPIO135	GPIO	I/O			
136	ETPUA22_IRQ10_ GPIO136	P	ETPUA22	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ10	External interrupt request	I			
		A2	—	—	—			
		G	GPIO136	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
137	ETPUA23_IRQ11_ GPIO137	P	ETPUA23	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ11	External interrupt request	I			
		A2	—	—	—			
		G	GPIO137	GPIO	I/O			
138	ETPUA24_IRQ12_ GPIO138	P	ETPUA24	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ12	External interrupt request	I			
		A2	—	—	—			
		G	GPIO138	GPIO	I/O			
139	ETPUA25_IRQ13_ GPIO139	P	ETPUA25	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ13	External interrupt request	I			
		A2	—	—	—			
		G	GPIO139	GPIO	I/O			
140	ETPUA26_IRQ14_ GPIO140	P	ETPUA26	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ14	External interrupt request	I			
		A2	—	—	—			
		G	GPIO140	GPIO	I/O			
141	ETPUA27_IRQ15_ GPIO141	P	ETPUA27	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	IRQ15	External interrupt request	I			
		A2	—	—	—			
		G	GPIO141	GPIO	I/O			
142	ETPUA28_PCSC1_ GPIO142	P	ETPUA28	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSC1	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO142	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
143	ETPUA29_PCSC2_ GPIO143	P	ETPUA29	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSC2	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO143	GPIO	I/O			
144	ETPUA30_PCSC3_ GPIO144	P	ETPUA30	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSC3	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO144	GPIO	I/O			
145	ETPUA31_PCSC4_ GPIO145	P	ETPUA31	eTPU A channel	I/O	MH	V_{DDEH1}	—/WKPCFG
		A1	PCSC4	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO145	GPIO	I/O			
eTPU_B								
146	TCRCLKB_IRQ6_ GPIO146	P	TCRCLKB	eTPU B TCR clock	I	MH	V_{DDEH6}	—/Up
		A1	IRQ6	External interrupt request	I			
		A2	—	—	—			
		G	GPIO146	GPIO	I/O			
147	ETPUB0_ETPUB16_ GPIO147	P	ETPUB0	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB16	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO147	GPIO	I/O			
148	ETPUB1_ETPUB17_ GPIO148	P	ETPUB1	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB17	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO148	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
149	ETPUB2_ETPUB18_ GPIO149	P	ETPUB2	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB18	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO149	GPIO	I/O			
150	ETPUB3_ETPUB19_ GPIO150	P	ETPUB3	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB19	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO150	GPIO	I/O			
151	ETPUB4_ETPUB20_ GPIO151	P	ETPUB4	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB20	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO151	GPIO	I/O			
152	ETPUB5_ETPUB21_ GPIO152	P	ETPUB5	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB21	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO152	GPIO	I/O			
153	ETPUB6_ETPUB22_ GPIO153	P	ETPUB6	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB22	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO153	GPIO	I/O			
154	ETPUB7_ETPUB23_ GPIO154	P	ETPUB7	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB23	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO154	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
155	ETPUB8_ETPUB24_ GPIO155	P	ETPUB8	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB24	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO155	GPIO	I/O			
156	ETPUB9_ETPUB25_ GPIO156	P	ETPUB9	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB25	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO156	GPIO	I/O			
157	ETPUB10_ETPUB26_ GPIO157	P	ETPUB10	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB26	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO157	GPIO	I/O			
158	ETPUB11_ETPUB27_ GPIO158	P	ETPUB11	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB27	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO158	GPIO	I/O			
159	ETPUB12_ETPUB28_ GPIO159	P	ETPUB12	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB28	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO159	GPIO	I/O			
160	ETPUB13_ETPUB29_ GPIO160	P	ETPUB13	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB29	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO160	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
161	ETPUB14_ETPUB30_ GPIO161	P	ETPUB14	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB30	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO161	GPIO	I/O			
162	ETPUB15_ETPUB31_ GPIO162	P	ETPUB15	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	ETPUB31	eTPU B channel (output only)	O			
		A2	—	—	—			
		G	GPIO162	GPIO	I/O			
163	ETPUB16_PCSA1_ GPIO163	P	ETPUB16	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	PCSA1	DSPI A peripheral chip select	O			
		A2	—	—	—			
		G	GPIO163	GPIO	I/O			
164	ETPUB17_PCSA2_ GPIO164	P	ETPUB17	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	PCSA2	DSPI A peripheral chip select	O			
		A2	—	—	—			
		G	GPIO164	GPIO	I/O			
165	ETPUB18_PCSA3_ GPIO165	P	ETPUB18	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	PCSA3	DSPI A peripheral chip select	O			
		A2	—	—	—			
		G	GPIO165	GPIO	I/O			
166	ETPUB19_PCSA4_ GPIO166	P	ETPUB19	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	PCSA4	DSPI A peripheral chip select	O			
		A2	—	—	—			
		G	GPIO166	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
167	ETPUB20_ GPIO167	P	ETPUB20	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO167	GPIO	I/O			
168	ETPUB21_ GPIO168	P	ETPUB21	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO168	GPIO	I/O			
169	ETPUB22_ GPIO169	P	ETPUB22	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO169	GPIO	I/O			
170	ETPUB23_ GPIO170	P	ETPUB23	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO170	GPIO	I/O			
171	ETPUB24_ GPIO171	P	ETPUB24	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO171	GPIO	I/O			
172	ETPUB25_ GPIO172	P	ETPUB25	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO172	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
173	ETPUB26_ GPIO173	P	ETPUB26	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO173	GPIO	I/O			
174	ETPUB27_ GPIO174	P	ETPUB27	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO174	GPIO	I/O			
175	ETPUB28_ GPIO175	P	ETPUB28	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO175	GPIO	I/O			
176	ETPUB29_ GPIO176	P	ETPUB29	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO176	GPIO	I/O			
177	ETPUB30_ GPIO177	P	ETPUB30	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO177	GPIO	I/O			
178	ETPUB31_ GPIO178	P	ETPUB31	eTPU B channel	I/O	MH	V_{DDEH6}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO178	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
GPIO, IRQ, FlexRay								
440	TCRCLKC_ GPIO440[9]	P	—	—	—	MH	V_{DDEH7}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO440	GPIO	I/O			
441	ETPUC0_ GPIO441[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO441	GPIO	I/O			
442	ETPUC1_ GPIO442[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO442	GPIO	I/O			
443	ETPUC2_ GPIO443[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO443	GPIO	I/O			
444	ETPUC3_ GPIO444[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO444	GPIO	I/O			
445	ETPUC4_ GPIO445[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO445	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
446	ETPUC5_ GPIO446[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO446	GPIO	I/O			
447	ETPUC6_ GPIO447[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO447	GPIO	I/O			
448	ETPUC7_ GPIO448[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO448	GPIO	I/O			
449	ETPUC8_ GPIO449[9]	P	—	—	I/O	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO449	GPIO	I/O			
450	ETPUC9_IRQ0_ GPIO450[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ0	External interrupt request	I			
		A2	—	—	—			
		G	GPIO450	GPIO	I/O			
451	ETPUC10__IRQ1_ GPIO451[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ1	External interrupt request	I			
		A2	—	—	—			
		G	GPIO451	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
452	ETPUC11_IRQ2_ GPIO452[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ2	External interrupt request	I			
		A2	—	—	—			
		G	GPIO452	GPIO	I/O			
453	ETPUC12_IRQ3_ GPIO453[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ3	External interrupt request	I			
		A2	—	—	—			
		G	GPIO453	GPIO	I/O			
454	ETPUC13_3_IRQ4_ GPIO454[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ4	External interrupt request	I			
		A2	—	—	—			
		G	GPIO454	GPIO	I/O			
455	ETPUC14_4_IRQ5_ GPIO455[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	IRQ5	External interrupt request	I			
		A2	—	—	—			
		G	GPIO455	GPIO	I/O			
456	ETPUC15__ GPIO456[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO456	GPIO	I/O			
457	ETPUC16_FR_A_TX_ GPIO457[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	FR_A_TX	FlexRay A transfer	O			
		A2	—	—	—			
		G	GPIO457	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
458	ETPUC17_FR_A_RX_ GPIO458[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	FR_A_RX	FlexRay A receive	I			
		A2	—	—	—			
		G	GPIO458	GPIO	I/O			
459	ETPUC18_FR_A_TX_EN_ GPIO459[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	FR_A_TX_EN	FlexRay A transfer enable	O			
		A2	—	—	—			
		G	GPIO459	GPIO	I/O			
460	ETPUC19_TXDA_ GPIO460[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	TXDA	eSCI A transmit	O			
		A2	—	—	—			
		G	GPIO460	GPIO	I/O			
461	ETPUC20_RXDA _ GPIO461[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	RXDA	eSCI A receive	I			
		A2	—	—	—			
		G	GPIO461	GPIO	I/O			
462	ETPUC21_TXDB_ GPIO462[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	TXDB	eSCI B transmit	O			
		A2	—	—	—			
		G	GPIO462	GPIO	I/O			
463	ETPUC22_RXDB_ GPIO463[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	RXDB	eSCI B receive	I			
		A2	—	—	—			
		G	GPIO463	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
464	ETPUC23_PCSD5_ GPIO464[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD5	DSPI D peripheral chip select	O			
		A2	MAA0	ADC A Mux Address 0	O			
		A3	MAB0	ADC B Mux Address 0	O			
		G	GPIO464	GPIO	I/O			
465	ETPUC24_PCSD4_ GPIO465[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD4	DSPI D peripheral chip select	O			
		A2	MAA1	ADC A Mux Address 1	O			
		A4	MAB1	ADC B Mux Address 1	O			
		G	GPIO465	GPIO	I/O			
466	ETPUC25_PCSD3_ GPIO466[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD3	DSPI D peripheral chip select	O			
		A2	MAA2	ADC A Mux Address 2	O			
		A3	MAB2	ADC B Mux Address 2	O			
		G	GPIO466	GPIO	I/O			
467	ETPUC26_PCSD2_ GPIO467[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD2	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO467	GPIO	I/O			
468	ETPUC27_PCSD1_ GPIO468[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD1	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO468	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
469	ETPUC28_PCSD0_ GPIO469[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	PCSD0	DSPI D peripheral chip select	I/O			
		A2	—	—	—			
		G	GPIO469	GPIO	I/O			
470	ETPUC29_SCKD_ GPIO470[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	SCKD	DSPI D clock	I/O			
		A2	—	—	—			
		G	GPIO470	GPIO	I/O			
471	ETPUC30_SOUTD_ GPIO471[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	SOUTD	DSPI D data output	O			
		A2	—	—	—			
		G	GPIO471	GPIO	I/O			
472	ETPUC31_SIND_ GPIO472[9]	P	—	—	—	MH	V_{DDEH7}	—/WKPCFG
		A1	SIND	DSPI D data input	I			
		A2	—	—	—			
		G	GPIO472	GPIO	I/O			
eMIOS								
179	EMIOS0_ETPUA0_ GPIO179	P	EMIOS0	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA0	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO179	GPIO	I/O			
180	EMIOS1_ETPUA1_ GPIO180	P	EMIOS1	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA1	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO180	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
181	EMIOS2_ETPUA2_ GPIO181	P	EMIOS2	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA2	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO181	GPIO	I/O			
182	EMIOS3_ETPUA3_ GPIO182	P	EMIOS3	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA3	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO182	GPIO	I/O			
183	EMIOS4_ETPUA4_ GPIO183	P	EMIOS4	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA4	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO183	GPIO	I/O			
184	EMIOS5_ETPUA5_ GPIO184	P	EMIOS5	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA5	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO184	GPIO	I/O			
185	EMIOS6_ETPUA6_ GPIO185	P	EMIOS6	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA6	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO185	GPIO	I/O			
186	EMIOS7_ETPUA7_ GPIO186	P	EMIOS7	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA7	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO186	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
187	EMIOS8_ETPUA8_ GPIO187	P	EMIOS8	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA8	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO187	GPIO	I/O			
188	EMIOS9_ETPUA9_ GPIO188	P	EMIOS9	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUA9	eTPU A channel	O			
		A2	—	—	—			
		G	GPIO188	GPIO	I/O			
189	EMIOS10_SCKD_ GPIO189	P	EMIOS10	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	SCKD	DSPI D clock	O			
		A2	—	—	—			
		G	GPIO189	GPIO	I/O			
190	EMIOS11_SIND_ GPIO190	P	EMIOS11	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	SIND	DSPI D data input	I			
		A2	—	—	—			
		G	GPIO190	GPIO	I/O			
191	EMIOS12_SOUTC_ GPIO191	P	EMIOS12	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG
		A1	SOUTC	DSPI C data output	O			
		A2	—	—	—			
		G	GPIO191	GPIO	I/O			
192	EMIOS13_SOUTD_ GPIO192	P	EMIOS13	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG
		A1	SOUTD	DSPI D data output	O			
		A2	—	—	—			
		G	GPIO192	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
193	EMIOS14_IRQ0_ GPIO193	P	EMIOS14	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG
		A1	IRQ0	External interrupt request	I			
		A2	CNTXD	FlexCAN D transmit	O			
		G	GPIO193	GPIO	I/O			
194	EMIOS15_IRQ1_ GPIO194	P	EMIOS15	eMIOS channel	O	MH	V_{DDEH4}	—/WKPCFG
		A1	IRQ1	External interrupt request	I			
		A2	CNRXD	FlexCAN D receive	I			
		G	GPIO194	GPIO	I/O			
195	EMIOS16_ETPUB0_ GPIO195	P	EMIOS16	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB0	eTPU B channel	O			
		A2	FR_DBG[3]	FlexRay debug	O			
		G	GPIO195	GPIO	I/O			
196	EMIOS17_ETPUB1_ GPIO196	P	EMIOS17	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB1	eTPU B channel	O			
		A2	FR_DBG[2]	FlexRay debug	O			
		G	GPIO196	GPIO	I/O			
197	EMIOS18_ETPUB2_ GPIO197	P	EMIOS18	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB2	eTPU B channel	O			
		A2	FR_DBG[1]	FlexRay debug	O			
		G	GPIO197	GPIO	I/O			
198	EMIOS19_ETPUB3_ GPIO198	P	EMIOS19	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB3	eTPU B channel	O			
		A2	FR_DBG[0]	FlexRay debug	O			
		G	GPIO198	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
199	EMIOS20_ETPUB4_ GPIO199	P	EMIOS20	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB4	eTPU B channel	O			
		A2	—	—	—			
		G	GPIO199	GPIO	I/O			
200	EMIOS21_ETPUB5_ GPIO200	P	EMIOS21	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB5	eTPU B channel	O			
		A2	—	—	—			
		G	GPIO200	GPIO	I/O			
201	EMIOS22_ETPUB6_ GPIO201	P	EMIOS22	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB6	eTPU B channel	O			
		A2	—	—	—			
		G	GPIO201	GPIO	I/O			
202	EMIOS23_ETPUB7_ GPIO202	P	EMIOS23	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	ETPUB7	eTPU B channel	O			
		A2	—	—	—			
		G	GPIO202	GPIO	I/O			
203	EMIOS24_PCSB0_ GPIO203	P	EMIOS24	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSB0	DSPI B peripheral chip select	I/O			
		A2	—	—	—			
		G	GPIO203	GPIO	I/O			
204	EMIOS25_PCSB1_ GPIO204	P	EMIOS25	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSB1	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO204	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
432	EMIOS26_PCSB2_ GPIO432	P	EMIOS26	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSB2	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO432	GPIO	I/O			
433	EMIOS27_PCSB3_ GPIO433	P	EMIOS27	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSB3	DSPI B peripheral chip select	O			
		A2	—	—	—			
		G	GPIO433	GPIO	I/O			
434	EMIOS28_PCSC0_ GPIO434	P	EMIOS28	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSC0	DSPI C peripheral chip select	I/O			
		A2	—	—	—			
		G	GPIO434	GPIO	I/O			
435	EMIOS29_PCSC1_ GPIO435	P	EMIOS29	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSC1	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO435	GPIO	I/O			
436	EMIOS30_PCSC2_ GPIO436	P	EMIOS30	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSC2	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO436	GPIO	I/O			
437	EMIOS31_PCSC5_ GPIO437	P	EMIOS31	eMIOS channel	I/O	MH	V_{DDEH4}	—/WKPCFG
		A1	PCSC5	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO437	GPIO	I/O			
eQADC								

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
—	ANA0	P	ANA0[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA0
—	ANA1	P	ANA1[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA1
—	ANA2	P	ANA2[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA2
—	ANA3	P	ANA3[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA3
—	ANA4	P	ANA4[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA4
—	ANA5	P	ANA5[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA5
—	ANA6	P	ANA6[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA6
—	ANA7	P	ANA7[10]	eQADC A analog input	I	AE/up-down	V_{DDA_A1}	ANA7
—	ANA8	P	ANA8	eQADC A analog input	I	AE	V_{DDA_A1}	ANA8
—	ANA9	P	ANA9	eQADC A analog input	I	AE	V_{DDA_A1}	ANA9
—	ANA10	P	ANA10	eQADC A analog input	I	AE	V_{DDA_A1}	ANA10
—	ANA11	P	ANA11	eQADC A analog input	I	AE	V_{DDA_A1}	ANA11
—	ANA12	P	ANA12	eQADC A analog input	I	AE	V_{DDA_A1}	ANA12
—	ANA13	P	ANA13	eQADC A analog input	I	AE	V_{DDA_A1}	ANA13
—	ANA14	P	ANA14	eQADC A analog input	I	AE	V_{DDA_A1}	ANA14
—	ANA15	P	ANA15	eQADC A analog input	I	AE	V_{DDA_A1}	ANA15
—	ANA16	P	ANA16	eQADC A analog input	I	AE	V_{DDA_A1}	ANA16
—	ANA17	P	ANA17	eQADC A analog input	I	AE	V_{DDA_A1}	ANA17
—	ANA18	P	ANA18	eQADC A analog input	I	AE	V_{DDA_A1}	ANA18
—	ANA19	P	ANA19	eQADC A analog input	I	AE	V_{DDA_A1}	ANA19

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
—	ANA20	P	ANA20	eQADC A analog input	I	AE	V_{DDA_A1}	ANA20
—	ANA21	P	ANA21	eQADC A analog input	I	AE	V_{DDA_A1}	ANA21
—	ANA22	P	ANA22	eQADC A analog input	I	AE	V_{DDA_A1}	ANA22
—	ANA23	P	ANA23	eQADC A analog input	I	AE	V_{DDA_A1}	ANA23
—	AN24	P	AN24	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN24
—	AN25	P	AN25	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN25
—	AN26	P	AN26	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN26
—	AN27	P	AN27	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN27
—	AN28	P	AN28	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN28
—	AN29	P	AN29	eQADC A and B shared analog input	I	AE	V_{DDA_A0}	AN29
—	AN30	P	AN30	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN30
—	AN31	P	AN31	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN31
—	AN32	P	AN32	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN32
—	AN33	P	AN33	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN33
—	AN34	P	AN34	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN34
—	AN35	P	AN35	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN35
—	AN36	P	AN36	eQADC A and B shared analog input	I	AE	V_{DDA_B1}	AN36
—	AN37	P	AN37	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN37
—	AN38	P	AN38	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN38
—	AN39	P	AN39	eQADC A and B shared analog input	I	AE	V_{DDA_B0}	AN39
—	ANB0	P	ANB0	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB0
—	ANB1	P	ANB1	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB1
—	ANB2	P	ANB2	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB2

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
—	ANB3	P	ANB3	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB3
—	ANB4	P	ANB4	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB4
—	ANB5	P	ANB5	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB5
—	ANB6	P	ANB6	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB6
—	ANB7	P	ANB7	eQADC B analog input	I	AE/up-down	V_{DDA_B0}	ANB7
—	ANB8	P	ANB8	eQADC B analog input	I	AE	V_{DDA_B0}	ANB8
—	ANB9	P	ANB9	eQADC B analog input	I	AE	V_{DDA_B0}	ANB9
—	ANB10	P	ANB10	eQADC B analog input	I	AE	V_{DDA_B0}	ANB10
—	ANB11	P	ANB11	eQADC B analog input	I	AE	V_{DDA_B0}	ANB11
—	ANB12	P	ANB12	eQADC B analog input	I	AE	V_{DDA_B0}	ANB12
—	ANB13	P	ANB13	eQADC B analog input	I	AE	V_{DDA_B0}	ANB13
—	ANB14	P	ANB14	eQADC B analog input	I	AE	V_{DDA_B0}	ANB14
—	ANB15	P	ANB15	eQADC B analog input	I	AE	V_{DDA_B0}	ANB15
—	ANB16	P	ANB16	eQADC B analog input	I	AE	V_{DDA_B0}	ANB16
—	ANB17	P	ANB17	eQADC B analog input	I	AE	V_{DDA_B0}	ANB17
—	ANB18	P	ANB18	eQADC B analog input	I	AE	V_{DDA_B0}	ANB18
—	ANB19	P	ANB19	eQADC B analog input	I	AE	V_{DDA_B0}	ANB19
—	ANB20	P	ANB20	eQADC B analog input	I	AE	V_{DDA_B0}	ANB20
—	ANB21	P	ANB21	eQADC B analog input	I	AE	V_{DDA_B0}	ANB21
—	ANB22	P	ANB22	eQADC B analog input	I	AE	V_{DDA_B0}	ANB22
—	ANB23	P	ANB23	eQADC B analog input	I	AE	V_{DDA_B0}	ANB23
—	VRH_A	P	VRH_A	ADC A Voltage reference high	I	VDDINT	V_{RH_A}	VRH_A

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
—	VRL_A	P	VRL_A	ADC A Voltage reference low	I	VSSINT	V_{RL_A}	VRL_A
—	VRH_B	P	VRH_B	ADC B Voltage reference high	I	VDDINT	V_{RH_B}	VRH_B
—	VRL_B	P	VRL_B	ADC B Voltage reference low	I	VSSINT	V_{RL_B}	VRL_B
—	REFBYPCB	P	REFBYPCB	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB
—	REFBYPCA	P	REFBYPCA	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA
—	VDDA_A0	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A0}	VDDA_A0
—	VDDA_A1	P	VDDA_A	Internal logic supply input	I	VDDE	V_{DDA_A1}	VDDA_A1
—	REFBYPCA1	P	REFBYPCA1	ADC A Reference bypass capacitor	I	AE	V_{DDA_A1}	REFBYPCA1
—	VSSA_A1	P	VSSA_A	Ground	I	VSSE	V_{SSA_A1}	VSSA_A1
—	VDDA_B0	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B0}	VDDA_B0
—	VDDA_B1	P	VDDA_B	Internal logic supply input	I	VDDE	V_{DDA_B1}	VDDA_B1
—	VSSA_B0	P	VSSA_B	Ground	I	VSSE	V_{SSA_B0}	VSSA_B0
—	REFBYPCB1	P	REFBYPCB1	ADC B Reference bypass capacitor	I	AE	V_{DDA_B0}	REFBYPCB1
FlexRay								
248	FR_A_TX_ GPIO248	P	FR_A_TX	FlexRay A transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO248	GPIO	I/O			
249	FR_A_RX_ GPIO249	P	FR_A_RX	FlexRay A receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO249	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
250	FR_A_TX_EN_ GPIO250	P	FR_A_TX_EN	FlexRay A transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO250	GPIO	I/O			
251	FR_B_TX_ GPIO251	P	FR_B_TX	FlexRay B transfer	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO251	GPIO	I/O			
252	FR_B_RX_ GPIO252	P	FR_B_RX	FlexRay B receive	I	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO252	GPIO	I/O			
253	FR_B_TX_EN_ GPIO253	P	FR_B_TX_EN	FlexRay B transfer enable	O	FS	V_{DDE2}	—/Up (–/– for Rev.1 of the device)
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO253	GPIO	I/O			
FlexCAN								
83	CNTXA_TXDA_ GPIO83	P	CNTXA	FlexCAN A transmit	O	MH	V_{DDEH4}	—/Up
		A1	TXDA	eSCI A transmit	O			
		A2	—	—	—			
		G	GPIO83	GPIO	I/O			
84	CNRXA_RXDA_ GPIO84	P	CNRXA	FlexCAN A receive	I	MH	V_{DDEH4}	—/Up
		A1	RXDA	eSCI A receive	I			
		A2	—	—	—			
		G	GPIO84	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
85	CNTXB_PCSC3_ GPIO85	P	CNTXB	FlexCAN B transmit	O	MH	V_{DDEH4}	—/Up
		A1	PCSC3	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO85	GPIO	I/O			
86	CNRXB_PCSC4_ GPIO86	P	CNRXB	FlexCAN B receive	I	MH	V_{DDEH4}	—/Up
		A1	PCSC4	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO86	GPIO	I/O			
87	CNTXC_PCSD3_ GPIO87	P	CNTXC	FlexCAN C transmit	O	MH	V_{DDEH4}	—/Up
		A1	PCSD3	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO87	GPIO	I/O			
88	CNRXC_PCSD4_ GPIO88	P	CNRXC	FlexCAN C receive	I	MH	V_{DDEH4}	—/Up
		A1	PCSD4	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO88	GPIO	I/O			
246	CNTXD_ GPIO246	P	CNTXD	FlexCAN D transmit	O	MH	V_{DDEH4}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO246	GPIO	I/O			
247	CNRXD_ GPIO247	P	CNRXD	FlexCAN D receive	I	MH	V_{DDEH4}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO247	GPIO	I/O			
eSCI								

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
89	TXDA_ GPIO89	P	TXDA	eSCI A transmit	O	MH	V_{DDEH1}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO89	GPIO	I/O			
90	RXDA _ GPIO90	P	RXDA	eSCI A receive	I	MH	V_{DDEH1}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO90	GPIO	I			
91	TXDB_PCSD1_ GPIO91	P	TXDB	eSCI B transmit	O	MH	V_{DDEH1}	—/Up
		A1	PCSD1	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO91	GPIO	I/O			
92	RXDB_PCSD5_ GPIO92	P	RXDB	eSCI B receive	I	MH	V_{DDEH1}	—/Up
		A1	PCSD5	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO92	GPIO	I/O			
244	TXDC_ETRIG0_ GPIO244	P	TXDC	eSCI C transmit	O	MH	V_{DDEH4}	—/Up
		A1	ETRIG0	eQADC trigger input	I			
		A2	—	—	—			
		G	GPIO244	GPIO	I/O			
245	RXDC_ GPIO245	P	RXDC	eSCI C receive	I	MH	V_{DDEH5}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO245	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
DSPI								
93	SCKA_PCSC1_ GPIO93	P	SCKA	DSPI A clock	I/O	MH	V_{DDEH3}	—/Up
		A1	PCSC1	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO93	GPIO	I/O			
94	SINA_PCSC2_ GPIO94	P	SINA	DSPI A data input	I	MH	V_{DDEH3}	—/Up
		A1	PCSC2	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO94	GPIO	I/O			
95	SOUTA_PCSC5_ GPIO95	P	SOUTA	DSPI A data output	O	MH	V_{DDEH3}	—/Up
		A1	PCSC5	DSPI C peripheral chip select	O			
		A2	—	—	—			
		G	GPIO95	GPIO	I/O			
96	PCSA0_PCSD2_ GPIO96	P	PCSA0	DSPI A peripheral chip select	I/O	MH	V_{DDEH3}	—/Up
		A1	PCSD2	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO96	GPIO	I/O			
97	PCSA1_ GPIO97	P	PCSA1	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO97	GPIO	I/O			
98	PCSA2_ GPIO98	P	PCSA2	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO98	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
99	PCSA3_ GPIO99	P	PCSA3	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO99	GPIO	I/O			
100	PCSA4_ GPIO100	P	PCSA4	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO100	GPIO	I/O			
101	PCSA5_ETRIG1_ GPIO101	P	PCSA5	DSPI A peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	ETRIG1	eQADC trigger input	I			
		A2	—	—	—			
		G	GPIO101	GPIO	I/O			
102	SCKB_ GPIO102	P	SCKB	DSPI B clock	I/O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO102	GPIO	I/O			
103	SINB_ GPIO103	P	SINB	DSPI B data input	I	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO103	GPIO	I/O			
104	SOUTB_ GPIO104	P	SOUTB	DSPI B data output	O	MH	V_{DDEH3}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO104	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
105	PCSB0_PCSD2_ GPIO105	P	PCSB0	DSPI B peripheral chip select	I/O	MH	V_{DDEH3}	—/Up
		A1	PCSD2	DSPI D peripheral chip select	O			
		A2	—	—	—			
		G	GPIO105	GPIO	I/O			
106	PCSB1_PCSD0_ GPIO106	P	PCSB1	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	PCSD0	DSPI D peripheral chip select	I/O			
		A2	—	—	—			
		G	GPIO106	GPIO	I/O			
107	PCSB2_SOUTC_ GPIO107	P	PCSB2	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	SOUTC	DSPI C data output	O			
		A2	—	—	—			
		G	GPIO107	GPIO	I/O			
108	PCSB3_SINC_ GPIO108	P	PCSB3	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	SINC	DSPI C data input	I			
		A2	—	—	—			
		G	GPIO108	GPIO	I/O			
109	PCSB4_SCKC_ GPIO109	P	PCSB4	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	SCKC	DSPI C clock	I/O			
		A2	—	—	—			
		G	GPIO109	GPIO	I/O			
110	PCSB5_PCSC0_ GPIO110	P	PCSB5	DSPI B peripheral chip select	O	MH	V_{DDEH3}	—/Up
		A1	PCSC0	DSPI C peripheral chip select	I/O			
		A2	—	—	—			
		G	GPIO110	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
235	SCKC_SCK_C_LVDSP_ GPIO235	P	SCKC	DSPI C clock	I/O	MH+ LVDS	V_{DDEH4}	—/Up
		A1	SCK_C_LVDSP	LVDS+ downstream signal positive output clock	O			
		A2	—	—	—			
		G	GPIO235	GPIO	I/O			
236	SINC_SCK_C_LVDSM_ GPIO236	P	SINC	DSPI C data input	I	MH+ LVDS	V_{DDEH4}	—/Up
		A1	SCK_C_LVDSM	LVDS– downstream signal negative output clock	O			
		A2	—	—	—			
		G	GPIO236	GPIO	I/O			
237	SOUTC_SOUT_C_LVDSP_ GPIO237	P	SOUTC	DSPI C data output	O	MH+ LVDS	V_{DDEH4}	—/Up
		A1	SOUT_C_LVDSP	LVDS+ downstream signal positive output data	O			
		A2	—	—	—			
		G	GPIO237	GPIO	I/O			
238	PCSC0_SOUT_C_LVDSM_ GPIO238	P	PCSC0	DSPI C peripheral chip select	I/O	MH+ LVDS	V_{DDEH4}	—/Up
		A1	SOUT_C_LVDSM	LVDS– downstream signal negative output data	O			
		A2	—	—	—			
		G	GPIO238	GPIO	I/O			
239	PCSC1_ GPIO239	P	PCSC1	DSPI C peripheral chip select	O	MH	V_{DDEH4}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO239	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
240	PCSC2_GPIO240	P	PCSC2	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO240	GPIO	I/O			
241	PCSC3_GPIO241	P	PCSC3	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO241	GPIO	I/O			
242	PCSC4_GPIO242	P	PCSC4	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO242	GPIO	I/O			
243	PCSC5_GPIO243	P	PCSC5	DSPI C peripheral chip select	O	MH	V_{DDEH5}	—/Up
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO243	GPIO	I/O			
Reset and Clocks								
—	RESET	P	RESET	External reset input	I	MH	V_{DDEH1}	RESET/Up
230	RSTOUT	P	RSTOUT	External reset output	O	MH	V_{DDEH1}	RSTOUT/Low
212	BOOTCFG1_IRQ3_ GPIO212	P	BOOTCFG1	Boot configuration	I	MH	V_{DDEH1}	BOOTCFG/ Down
		A1	IRQ3	External interrupt request	I			
		A2	—	—	—			
		G	GPIO212	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
213	WKPCFG_NMI_ GPIO213	P	WKPCFG	Weak pull configuration input	I	MH	V_{DDEH1}	WKPCFG/Up
		A1	NMI	Critical interrupt to core[11]	I			
		A2	—	—	—			
		G	GPIO213	GPIO	I			
208	PLLCFG0_IRQ4_ GPIO208	P	PLLCFG0	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up
		A1	IRQ4	External interrupt request	I			
		A2	—	—	—			
		G	GPIO208	GPIO	I/O			
209	PLLCFG1_IRQ5_ GPIO209	P	PLLCFG1	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/Up
		A1	IRQ5	External interrupt request	I			
		A2	SOUTD	DSPI D data output	O			
		G	GPIO209	GPIO	I/O			
—	PLLCFG2	P	PLLCFG2	FMPLL mode configuration input	I	MH	V_{DDEH1}	PLLCFG/ Down
—	XTAL	P	XTAL	Crystal oscillator output	O	AE	V_{DD33}	XTAL
—	EXTAL	P	EXTAL	Crystal oscillator input	I	AE	V_{DD33}	EXTAL
214	ENGCLK	P	ENGCLK	EBI engineering clock output Note: EXTCLK (External clock input) selected through SIU register)	O	F	V_{DDE2}	ENGCLK/ Enabled
JTAG and Nexus (see footnote[12] about resets)								
—	$\overline{\text{EVTI}}$	–[13]	EVTI	Nexus event in	I	F	V_{DDE2}	—/Up
227	$\overline{\text{EVTO}}$ (the BAM uses this pin to select if auto baud rate is on or off)	–[13]	EVTO	Nexus event out	O	F	V_{DDE2}	ABS/Up
219	MCKO	–[13]	MCKO	Nexus message clock out	O	F	V_{DDE2}	O/Low

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
220	MDO0_GPIO220 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO0[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO220	GPIO	I/O			
221	MDO1_GPIO221 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO1[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO221	GPIO	I/O			
222	MDO2_GPIO222 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO2[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO222	GPIO	I/O			
223	MDO3_GPIO223 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO3[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO223	GPIO	I/O			
75	MDO4_GPIO75 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO4[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO75	GPIO	I/O			
76	MDO5_GPIO76 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO5[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO76	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
77	MDO6_GPIO77 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO6[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO77	GPIO	I/O			
78	MDO7_GPIO78 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO7[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO78	GPIO	I/O			
79	MDO8_GPIO79 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO8[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO79	GPIO	I/O			
80	MDO9_GPIO80 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO9[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO80	GPIO	I/O			
81	MDO10_GPIO81 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO10[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO81	GPIO	I/O			
82	MDO11_GPIO82 (GPIO function on this pin is only available on Rev.2 of the device)	–[13]	MDO11[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO82	GPIO	I/O			

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
231	MDO12_GPIO231	–[13]	MDO12[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO231	GPIO	I/O			
232	MDO13_GPIO232	–[13]	MDO13[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO232	GPIO	I/O			
233	MDO14_GPIO233	–[13]	MDO14[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO233	GPIO	I/O			
234	MDO15_GPIO234	–[13]	MDO15[15]	Nexus message data out	O	F	V_{DDE2}	O/Low
		A1	—	—	—			
		A2	—	—	—			
		G	GPIO234	GPIO	I/O			
224	$\overline{\text{MSEO0}}$	–[13]	MSEO0[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low
225	$\overline{\text{MSEO1}}$	–[13]	MSEO1[15]	Nexus message start/end out	O	F	V_{DDE2}	O/Low
226	RDY	–[13]	RDY	Nexus ready output	O	F	V_{DDE2}	O/Low
—	TCK	–[13]	TCK	JTAG test clock input	I	F	V_{DDE2}	TCK/Down
—	TDI	–[13]	TDI	JTAG test data input	I	F	V_{DDE2}	TDI/Up
228	TDO	–[13]	TDO	JTAG test data output	O	F	V_{DDE2}	TDO/Up
—	TMS	–[13]	TMS	JTAG test mode select input	I	F	V_{DDE2}	TMS/Up
—	JCOMP	–[13]	JCOMP	JTAG TAP controller enable	I	F	V_{DDE2}	JCOMP/Down

Table 2. Signal Properties and Muxing Summary (continued)

GPIO/PCR[1]	Signal Name[2]	P/A/G[3]	Function[4]	Function Summary	Direction	Pad Type[5]	Voltage[6]	State during RESET[7]
—	TEST	—	TEST	Test mode select (not for customer use)	I	F	V_{DDEH1}	TEST/Down
—	VDDSYN	—	VDDSYN	Clock synthesizer power input	I	VDDE	V_{DDSYN}	VDDSYN
—	VSSSYN	—	VSSSYN	Clock synthesizer ground input	I	VSSE	V_{DDSYN}	VSSSYN
—	VSTBY	—	VSTBY	SRAM standby power input	I	VHV	V_{DDEH1}	VSTBY
—	REGSEL	—	REGSEL	Selects regulator mode (Linear/Switch mode)	I	AE	V_{DDREG}	REGSEL
—	REGCTL	—	REGCTL	Regulator controller output to base/gate of power transistor	O	AE	V_{DDREG}	REGCTL
—	VSSFL	—	VSSFL	Tie to V_{SS}	I	VSS	V_{DDREG}	VSSFL
—	VDDREG	—	VDDREG	Source voltage for on-chip regulators and Low voltage detect circuits	I	VDDINT	V_{DDREG}	VDDREG

1 The GPIO number is the same as the corresponding pad configuration register (SIU_PCRn) number in pins that have GPIO funct have GPIO functionality, this number is the PCR number.

2 The primary signal name is used as the pin label on the BGA map for identification purposes. However, the primary signal function is and is indicated by a dash in the following table columns: Signal Functions, P/F/G, and I/O Type.

3 P/A/G stands for Primary/Alternate/GPIO. This column indicates which function on a pin is Primary, Alternate 1, Alternate 2, (Alte

4 Each line in the Function column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternat are designated in the PA field of the SIU_PCRn registers except where explicitly noted.

5 MH = High voltage, medium speed
F = Fast speed
FS = Fast speed with slew
AE = Analog with ESD protection circuitry (up/down = pull up and pull down circuits included in the pad)
VHV = Very high voltage

6 VDDE (fast I/O) and VDDEH (slow I/O) power supply inputs are grouped into segments. Each segment of VDDEH pins can conn (+5%/–10%) power supply input. Each segment of VDDE pins can connect to a separate 1.8–3.3 V (±10%) power supply.

7 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – Auto Baud Select (during Reset or until JCOMP assertion). A dash on the left side of the slash denotes that both the input and ou off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left o the pin is enabled.

8 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the inpu pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

[9] This signal name includes eTPU_C functionality that this device does not have. This is for forward compatibility with devices that

[10] During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull the system clock propagates through the device.

[11] NMI does not have a PCR PA configuration; it is enabled when NMI is enabled through the SIU_IREER and SIU_IFEER registers

[12] Nexus reset is different than system reset; MDO 1-11 are enabled when trace (RPM or FPM) is enabled, and MDO 12-15 when FI and MCKO are also dependent on trace (RPM or FPM) being enabled.

[13] The Nexus pins don't have a "primary" function as they are not configured by the SIU. The pins are selected by asserting JCOMP SIU values have no effect on the function of these pins once enabled.

[14] MCKO is disabled from reset; it can be enabled from the tool (controlled by Nexus NPC_PCR register).

[15] Do not connect pin directly to a power supply or ground.

5 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the PXR40.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

5.1 Maximum ratings

Table 3. Absolute maximum ratings[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	1.2 V Core Supply Voltage	V_{DD}	–0.3	2.0 [2]	V
2	SRAM Standby Voltage	V_{STBY}	–0.3	6.4 [3,4]	V
3	Clock Synthesizer Voltage	V_{DDSYN}	–0.3	5.3 [4,5]	V
4	I/O Supply Voltage (I/O buffers and predrivers)	V_{DD33}	–0.3	5.3 [4,5]	V
5	Analog Supply Voltage (reference to V_{SSA}[6])	V_{DDA}[7]	–0.3	6.4 [3,4]	V
6	I/O Supply Voltage (fast I/O pads)	V_{DDE}	–0.3	5.3 [4,5]	V
7	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	–0.3	6.4 [3,4]	V
8	Voltage Regulator Input Supply Voltage	V_{DDREG}	–0.3	6.4 [3,4]	V
9	Analog Reference High Voltage (reference to V_{RL}[8])	V_{RH}[9]	–0.3	6.4 [3,4]	V
10	V_{SS} to V_{SSA}[8] Differential Voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
11	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	–0.3	6.4 [3,4]	V
12	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
13	V_{DD33} to V_{DDSYN} Differential Voltage	$V_{DD33} – V_{DDSYN}$	–0.1	0.1	V
14	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
15	Maximum Digital Input Current [10] (per pin, applies to all digital pins)	I_{MAXD}	–3 [11]	3 [11]	mA
16	Maximum Analog Input Current [12] (per pin, applies to all analog pins)	I_{MAXA}	– 3 [7]	3 [7,11]	mA
17	Maximum Operating Temperature Range [13] – Die Junction Temperature	T_J	–40.0	150.0	°C
18	Storage Temperature Range	T_{stg}	–55.0	150.0	°C
19	Maximum Solder Temperature [14] Pb-free package SnPb package	T_{sdr}	 — —	 260.0 245.0	°C
20	Moisture Sensitivity Level [15]	MSL	—	3	—

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 2.0 V for 10 hours cumulative time, 1.32 V +10% for time remaining.

3 6.4 V for 10 hours cumulative time, 5.25 V +10% for time remaining.

4 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

5 5.3 V for 10 hours cumulative time, 3.60 V +10% for time remaining.

6 PXR40 has two analog power supply pins on the pinout: VDDA_A and VDDA_B.

7 PXR40 has two analog ground supply pins on the pinout: VSSA_A and VSSA_B.

8 PXR40 has two analog low reference voltage pins on the pinout: VRL_A and VRL_B.

9 PXR40 has two analog high reference voltage pins on the pinout: VRH_A and VRH_B.

10 Total injection current for all pins must not exceed 25 mA at maximum operating voltage.

11 Injection current of ±5 mA allowed for limited duration for analog (ADC) pads and digital 5 V pads. The maximum accumulated time at this current shall be 60 hours. This includes an assumption of a 5.25 V maximum analog or V_{DDEH} supply when under this stress condition.

12 Total injection current for all analog input pins must not exceed 15 mA.

13 Lifetime operation at these specification limits is not guaranteed.

14 Solder profile per CDF-AEC-Q100.

15 Moisture sensitivity per JEDEC test method A112.

5.2 Thermal characteristics

Table 4. Thermal characteristics, 416-pin TEPBGA package[1]

Characteristic	Symbol	Value	Unit
Junction to Ambient [2,3] Natural Convection (Single layer board)	$R_{\theta JA}$	24	°C/W
Junction to Ambient [2,4] Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	18	°C/W
Junction to Ambient (@200 ft./min., Single layer board)	$R_{\theta JMA}$	19	°C/W
Junction to Ambient (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	14	°C/W
Junction to Board [5]	$R_{\theta JB}$	9	°C/W
Junction to Case [6]	$R_{\theta JC}$	6	°C/W
Junction to Package Top [7] Natural Convection	Ψ_{JT}	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization. This data is PRELIMINARY based on similar package used on other devices.

2 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.2.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the TEPBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction to case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm. of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road

San Jose, CA 95134
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

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- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

5.3 EMI (Electromagnetic Interference) characteristics

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to www.freescale.com and perform a keyword search for “radiated emissions.” The following tables list the values of the device's radiated emissions operating behaviors.

Table 5. EMC radiated emissions operating behaviors: 416 BGA

Symbol	Description	Conditions	f_{OSC} f_{SYS}	Frequency band (MHz)	Level (max.)	Unit	Notes
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK on FM off	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	26	dBμV	1
				50–150	30		
				150–500	34		
				500–1000	30		
				IEC and SAE level	I^2	—	1, 3
V_{RE_TEM}	Radiated emissions, electric field and magnetic field	V_{DD} = 1.2 V V_{DDE} = 3.3 V V_{DDEH} = 5 V T_A = 25 °C 416 BGA EBI off CLK off FM on[4]	40 MHz crystal 264 MHz (f_{EBI_CAL} = 66 MHz)	0.15–50	24	dBμV	1
				50–150	25		
				150–500	25		
				500–1000	21		
				IEC and SAE level	K[5]	—	1,3

1 Determined according to IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

2 I = 36 dBμV

3 Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method, and Appendix D of SAE Standard J1752-3, Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method.

4 “FM on” = FM depth of ±2%

5 K = 30 dBμV

5.4 ESD characteristics

Table 6. ESD ratings[1,2]

Spec	Characteristic	Symbol	Value	Unit
1	ESD for Human Body Model (HBM)	V_{HBM}	2000	V
2	ESD for Charged Device Model (CDM)	V_{CDM}	750 (corners) 500 (other)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.5 PMC/POR/LVI electrical specifications

Note: For ADC internal resource measurements, see Table 18 in Section 5.9.1 ADC internal resource measurements.

Table 7. PMC operating conditions

Name	Parameter	Condition	Min	Typ	Max	Unit	Note
V_{DDREG}	Supply voltage VDDREG 5V nominal	LDO5V / SMPS5V mode	4.5	5	5.5	V	1
V_{DDREG}	Supply voltage VDDREG 3V nominal	LDO3V mode	3.0	3.3	3.6	V	1
V_{DD33}	Supply voltage VDDSYN / V_{DD33} 3.3V nominal	LDO3V mode	3.0	3.3	3.6	V	2
V_{DD}	Supply voltage VDD 1.2V nominal	—	1.14	1.2	1.32	V	3

1 Voltage should be higher than maximum V_{LVDREG} to avoid LVD event

2 Applies to both V_{DD33} (flash supply) and VDDSYN (PLL supply) pads. Voltage should be higher than maximum V_{LVD33} to avoid LVD event

3 Voltage should be higher than maximum V_{LVD12} to avoid LVD event

NOTE

In the following table, “untrimmed” means “at reset” and “trimmed” means “after reset”.

Table 8. PMC electrical specifications

ID	Name	Parameter	Min	Typ	Max	Unit
1	V_{BG}	Nominal bandgap reference voltage	0.608	0.620	0.632	V
1a	—	Untrimmed bandgap reference voltage	V_{BG} – 5%	V_{BG}	V_{BG} + 5%	V
2	$V_{DD12OUT}$	Nominal VRC regulated 1.2V output VDD	—	1.2	—	V

Table 8. PMC electrical specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
2a	—	Untrimmed VRC 1.2V output variation before band gap trim (unloaded) **Note:** Voltage should be higher than maximum V_{LVD12} to avoid LVD event	$V_{DD12OUT}$ – 8%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 17%	V
2b	—	Trimmed VRC 1.2V output variation after band gap trim (REGCTL load max. 20mA, VDD load max. 1A)[1]	$V_{DD12OUT}$ – 5%	$V_{DD12OUT}$	$V_{DD12OUT}$ + 10%	V
2c	$V_{STEPV12}$	Trimming step $V_{DD12OUT}$	—	10	—	mV
3	V_{PORC}	POR rising VDD 1.2V	—	0.7	—	V
3a	—	POR VDD 1.2V variation	V_{PORC} – 30%	V_{PORC}	V_{PORC} + 30%	
3b	—	POR 1.2V hysteresis	—	75	—	mV
4	V_{LVD12}	Nominal rising LVD 1.2V **Note:** ~$V_{DD12OUT}$ × 0.87	—	1.100	—	V
4a	—	Untrimmed LVD 1.2V variation before band gap trim **Note:** Rising VDD	V_{LVD12} – 6%	V_{LVD12}	V_{LVD12} + 6%	V
4b	—	Trimmed LVD 1.2V variation after band gap trim Rising VDD	V_{LVD12} – 3%	V_{LVD12}	V_{LVD12} + 3%	V
4c	—	LVD 1.2V Hysteresis	15	20	25	mV
4d	$V_{LVDSTEP12}$	Trimming step LVD 1.2V	—	10	—	mV
5	I_{REGCTL}	VRC DC current output on REGCTL	—	—	20	mA
6	—	Voltage regulator 1.2V current consumption VDDREG	—	3	—	mA
7	$V_{DD33OUT}$	Nominal V_{REG} 3.3V output	—	3.3	—	V
7a	—	Untrimmed V_{REG} 3.3V output variation before band gap trim (unloaded) **Note:** Rising VDDSYN	$V_{DD33OUT}$ – 6%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7b	—	Trimmed V_{REG} 3.3V output variation after band gap trim (max. load 80mA)	$V_{DD33OUT}$ – 5%	$V_{DD33OUT}$	$V_{DD33OUT}$ + 10%	V
7c	$V_{STEPV33}$	Trimming step VDDSYN	—	30	—	mV
8	V_{LVD33}	Nominal rising LVD 3.3V **Note:** ~$V_{DD33OUT}$ × 0.872	—	2.950	—	V
8a	—	Untrimmed LVD 3.3V variation before band gap trim **Note:** Rising VDDSYN	V_{LVD33} – 5%	V_{LVD33}	V_{LVD33} + 5%	V
8b	—	Trimmed LVD 3.3V variation after bad gap trim **Note:** Rising VDDSYN	V_{LVD33} – 3%	V_{LVD33}	V_{LVD33} + 3%	V
8c	—	LVD 3.3V Hysteresis	—	30	—	mV
8d	$V_{LVDSTEP33}$	Trimming step LVD 3.3V	—	30	—	mV

Table 8. PMC electrical specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
9	I_{DD33}	V_{REG} = 4.5 V, max DC output current V_{REG} = 4.25 V, max DC output current, crank condition **Note:** Max current supplied by VDDSYN that does not cause it to drop below V_{LVD33}	— —	— —	80 40	mA mA
10	—	Voltage regulator 3.3V current consumption VDDREG **Note:** Except I_{DD33}	—	2	—	mA
11	V_{PORREG}	POR rising on VDDREG	—	2.00	—	V
11a	—	POR VDDREG variation	V_{PORREG} – 30%	V_{PORREG}	V_{PORREG} + 30%	V
11b	—	POR VDDREG hysteresis	—	250	—	mV
12	V_{LVDREG}	Nominal rising LVD VDDREG (LDO3V / LDO5V mode)	—	2.950	—	V
12a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
12b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
12c	—	LVD VDDREG Hysteresis (LDO3V / LDO5V mode)	—	30	—	mV
12d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (LDO3V / LDO5V mode)	—	30	—	mV
13	V_{LVDREG}	Nominal rising LVD VDDREG (SMPS5V mode)	—	4.360	—	V
13a	—	Untrimmed LVD VDDREG variation before band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 5%	V_{LVDREG}	V_{LVDREG} + 5%	V
13b	—	Trimmed LVD VDDREG variation after band gap trim **Note:** Rising VDDREG	V_{LVDREG} – 3%	V_{LVDREG}	V_{LVDREG} + 3%	V
13c	—	LVD VDDREG Hysteresis (SMPS5V mode)	—	50	—	mV
13d	$V_{LVDSTEPREG}$	Trimming step LVD VDDREG (SMPS5V mode)	—	50	—	mV
14	V_{LVDA}	Nominal rising LVD VDDA	—	4.60	—	V
14a	—	Untrimmed LVD VDDA variation before band gap trim	V_{LVDA} – 5%	V_{LVDA}	V_{LVDA} + 5%	V
14b	—	Trimmed LVD VDDA variation after band gap trim	V_{LVDA} – 3%	V_{LVDA}	V_{LVDA} + 3%	V
14c	—	LVD VDDA Hysteresis	—	150	—	mV

Table 8. PMC electrical specifications (continued)

ID	Name	Parameter	Min	Typ	Max	Unit
14d	$V_{LVDASTEP}$	Trimming step LVD VDDA	—	20	—	mV
15	—	SMPS regulator output resistance **Note:** Pullup to VDDREG when high, pulldown to VSSREG when low.	—	15	25	Ohm
16	—	SMPS regulator clock frequency (after reset)	1.0	1.5	2.4	MHz
17	—	SMPS regulator overshoot at start-up[2]	—	1.32	1.4	V
18	—	SMPS maximum output current	—	1.0	—	A
19	—	Voltage variation on current step[2] (20% to 80% of maximum current with 4 µsec constant time)	—	—	0.1	V

1 VRC linear regulator is capable of sourcing a current up to 20 mA and sinking a current up to 500 µA. When using the recommended ballast transistor the maximum output current provided by the voltage regulator VRC/ballast to the VDD core voltage is up to 1A.

2 Parameter cannot be tested; this value is based on simulation and characterization.

5.6 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down in order to operate within specification as long as the following two rules are met:

- When VDDREG is tied to a nominal 3.3V supply, VDD33 and VDDSYN must be both shorted to VDDREG.
- When VDDREG is tied to a 5V supply, VDD33 and VDDSYN must be tied together and shall be powered by the internal 3.3V regulator.

The recommended power supply behavior is as follows: Use 25 V/millisecond or slower rise time for all supplies. Power up each V_{DDE}/V_{DDEH} first and then power up V_{DD}. For power down, drop V_{DD} to 0 V first, and then drop all V_{DDE}/V_{DDEH} supplies. There is no limit on the fall time for the power supplies.

Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies according to Table 9 and Table 10.

Table 9. Power sequence pin states for MH and AE pads

VDD	VDD33	VDDE	MH Pad	MH+LVDS Pads[1]	AE/up-down Pads
High	High	High	Normal operation	Normal operation	Normal operation
—	Low	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs driven high	Pull-ups enabled, pull-downs disabled
Low	High	Low	Output low, pin unpowered	Outputs disabled	Output low, pin unpowered
Low	High	High	Pin is tri-stated (output buffer, input buffer, and weak pulls disabled)	Outputs disabled	Pull-ups enabled, pull-downs disabled

1 MH+LVDS pads are output-only.

Table 10. Power sequence pin states for F and FS pads

VDD	VDD33	VDDE	F and FS pads
low	low	high	Outputs drive high
low	high	—	Outputs Disabled
high	low	low	Outputs Disabled
high	low	high	Outputs drive high
high	high	low	Normal operation - except no drive current and input buffer output is unknown.[1]
high	high	high	Normal Operation

[1] The pad pre-drive circuitry will function normally but since VDDE is unpowered the outputs will not drive high even though the output pmos can be enabled.

5.6.1 Power-up

If V_{DDE}/V_{DDEH} is powered up first, then a threshold detector tristates all drivers connected to V_{DDE}/V_{DDEH}. There is no limit to how long after V_{DDE}/V_{DDEH} powers up before V_{DD} must power up. If there are multiple V_{DDE}/V_{DDEH} supplies, they can be powered up in any order. For each V_{DDE}/V_{DDEH} supply not powered up, the drivers in that V_{DDE}/V_{DDEH} segment exhibit the characteristics described in the next paragraph.

If V_{DD} is powered up first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DD} powers up before V_{DDE}/V_{DDEH} must power up.

The rise times on the power supplies are to be no faster than 25 V/millisecond.

5.6.2 Power-down

If V_{DD} is powered down first, then all drivers are tristated. There is no limit to how long after V_{DD} powers down before V_{DDE}/V_{DDEH} must power down.

If V_{DDE}/V_{DDEH} is powered down first, then all pads are loaded through the drain diodes to V_{DDE}/V_{DDEH}. This presents a heavy load that pulls the pad down to a diode above V_{SS}. Current injected by external devices connected to the pads must meet the current injection specification. There is no limit to how long after V_{DDE}/V_{DDEH} powers down before V_{DD} must power down.

There are no limits on the fall times for the power supplies.

5.6.3 Power sequencing and POR dependent on V_{DDA}

During power up or down, V_{DDA} can lag other supplies (of magnitude greater than $V_{DDEH}/2$) within 1 V to prevent any forward-biasing of device diodes that causes leakage current and/or POR. If the voltage difference between V_{DDA} and V_{DDEH} is more than 1 V, the following will result:

- Triggers POR (ADC monitors on V_{DDEH1} segment which powers the RESET pin) if the leakage current path created, when V_{DDA} is sufficiently low, causes sufficient voltage drop on V_{DDEH1} node monitored crosses low-voltage detect level.
- If V_{DDA} is between 0–2 V, powering all the other segments (especially V_{DDEH1}) will not be sufficient to get the part out of reset.
- Each V_{DDEH} will have a leakage current to V_{DDA} of a magnitude of (($V_{DDEH} - V_{DDA} - 1$ V(diode drop)/200 KOhms) up to ($V_{DDEH}/2 = V_{DDA} + 1$ V).

- Each V_{DD} has the same behavior; however, the leakage will be small even though there is no current limiting resistor since V_{DD} = 1.32 V max.

5.7 DC electrical specifications

Table 11. DC electrical specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Core Supply Voltage (External Regulation)	V_{DD}	1.14	1.32[1,2]	V
1a	Core Supply Voltage (Internal Regulation)[3]	V_{DD}	1.08	1.32	V
2	I/O Supply Voltage (fast I/O pads)	V_{DDE}	3.0	3.6[1,4]	V
3	I/O Supply Voltage (medium I/O pads)	V_{DDEH}	3.0	5.25[1,5]	V
4	3.3 V I/O Buffer Voltage	V_{DD33}	3.0	3.6[1,4]	V
5	Analog Supply Voltage	V_{DDA}	4.75	5.25[1,5]	V
6a	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_LOW}	0.95[6]	1.2	V
6b	SRAM Standby Voltage Keep-out Range: 1.2V–2V	V_{STBY_HIGH}	2	6	V
7	Voltage Regulator Control Input Voltage[7]	V_{DDREG}	2.7[8]	5.5[1,5]	V
8	Clock Synthesizer Operating Voltage[9]	V_{DDSYN}	3.0	3.6[1,4]	V
9	Fast I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_F}	 0.65 × V_{DDE} 0.55 × V_{DDE}	V_{DDE} + 0.3	V
10	Fast I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_F}	V_{SS} – 0.3	 0.35 × V_{DDE} 0.40 × V_{DDE}	V
11	Medium I/O Input High Voltage Hysteresis enabled Hysteresis disabled	V_{IH_S}	 0.65 × V_{DDEH} 0.55 × V_{DDEH}	V_{DDEH} + 0.3	V
12	Medium I/O Input Low Voltage Hysteresis enabled Hysteresis disabled	V_{IL_S}	V_{SS} – 0.3	 0.35 × V_{DDEH} 0.40 × V_{DDEH}	V
13	Fast I/O Input Hysteresis	V_{HYS_F}	0.1 × V_{DDE}	—	V
14	Medium I/O Input Hysteresis	V_{HYS_S}	0.1 × V_{DDEH}	—	V
15	Analog Input Voltage	V_{INDC}	V_{SSA} – 0.1	V_{DDA} + 0.1	V
16	Fast I/O Output High Voltage[10]	V_{OH_F}	0.8 × V_{DDE}	—	V
17	Medium I/O Output High Voltage[11]	V_{OH_S}	0.8 × V_{DDEH}	—	V
18	Fast I/O Output Low Voltage[10]	V_{OL_F}	—	0.2 × V_{DDE}	V
19	Medium I/O Output Low Voltage[11]	V_{OL_S}	—	0.2 × V_{DDEH}	V
20	Load Capacitance (Fast I/O)[12] DSC(PCR[8:9]) = 0b00 DSC(PCR[8:9]) = 0b01 DSC(PCR[8:9]) = 0b10 DSC(PCR[8:9]) = 0b11	C_L	 — — — —	 10 20 30 50	 pF pF pF pF

Table 11. DC electrical specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
21	Input Capacitance (Digital Pins)	C_{IN}	—	7	pF
22	Input Capacitance (Analog Pins)	C_{IN_A}	—	10	pF
24	Operating Current 1.2 V Supplies @ f_{sys} = 264 MHz V_{DD} @1.32 V V_{STBY}[13] @1.2 V and 85°C V_{STBY} @6.0 V and 85°C	 I_{DD} I_{DDSTBY} $I_{DDSTBY6}$	 — — —	 1.0[14] 0.10 0.15	 A mA mA
25	Operating Current 3.3 V Supplies @ f_{sys} = 264 MHz V_{DD33}[15] V_{DDSYN}	 I_{DD33} I_{DDSYN}	 — —	 note[15] 7[16]	 mA mA
26	Operating Current 5.0 V Supplies @ f_{sys} = 264 MHz V_{DDA} Analog Reference Supply Current (Transient) V_{DDREG}	 I_{DDA} I_{REF} I_{REG}	 — — —	 50[17] 1.0 22	 mA mA mA
27	Operating Current V_{DDE}/V_{DDEH}[18] Supplies V_{DDE2} V_{DDEH1} V_{DDEH3} V_{DDEH4} V_{DDEH5} V_{DDEH6} V_{DDEH7}	 I_{DD2} I_{DD1} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7}	 — — — — — — —	 note[18]	 mA mA mA mA mA mA mA
28	Fast I/O Weak Pull Up/Down Current[19] 3.0 V–3.6 V	 I_{ACT_F}	 42	 158	 µA
29	Medium I/O Weak Pull Up/Down Current[20] 3.0 V–3.6 V 4.5 V–5.5 V	I_{ACT_S}	 15 35	 95 200	 µA µA
30	I/O Input Leakage Current[21]	I_{INACT_D}	–2.5	2.5	µA
31	DC Injection Current (per pin)	I_{IC}	–1.0	1.0	mA
32	Analog Input Current, Channel Off[22], AN[0:7], AN38, AN39 Analog Input Current, Channel Off, all other analog inputs AN[x]	I_{INACT_A}	–250 –150	250 150	nA nA
33	V_{SS} Differential Voltage	$V_{SS} – V_{SSA}$	–100	100	mV
34	Analog Reference Low Voltage	V_{RL}	V_{SSA}	V_{SSA} + 100	mV
35	V_{RL} Differential Voltage	$V_{RL} – V_{SSA}$	–100	100	mV
36	Analog Reference High Voltage	V_{RH}	V_{DDA} – 100	V_{DDA}	mV
37	V_{REF} Differential Voltage	$V_{RH} – V_{RL}$	4.75	5.25	V
38	V_{SSSYN} to V_{SS} Differential Voltage	$V_{SSSYN} – V_{SS}$	–100	100	mV
39	Operating Temperature Range—Ambient (Packaged)	T_A (T_L to T_H)	–40.0	125.0	°C
40	Slew rate on power supply pins	—	—	25	V/ms

Table 11. DC electrical specifications (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
41	Weak Pull-Up/Down Resistance[23], 200 K Option	$R_{PUPD200K}$	130	280	kΩ
42	Weak Pull-Up/Down Resistance[23], 100 K Option	$R_{PUPD100K}$	65	140	kΩ
43	Weak Pull-Up/Down Resistance[23], 5 K Option	R_{PUPD5K}	1.4	7.5	kΩ
44	Pull-Up/Down Resistance Matching Ratios[24] (100K/200K)	$R_{PUPDMTCH}$	–2.5	+2.5	%

1 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

2 2.0 V for 10 hours cumulative time, 1.2 V +10% for time remaining.

3 Assumed with DC load.

4 5.3 V for 10 hours cumulative time, 3.3 V +10% for time remaining.

5 6.4 V for 10 hours cumulative time, 5.0 V +10% for time remaining.

6 V_{STBY} below 0.95 V the RAM will not retain states, but will be operational. V_{STBY} can be 0 V when bypass standby mode.

7 Regulator is functional with derated performance, with supply voltage down to 4.0 V for system with V_{DDREG} = 4.5 V (min).

8 2.7 V minimum operating voltage allowed during vehicle crank for system with V_{DDREG} = 3.0 V (min). Normal operating voltage should be either V_{DDREG} = 3.0 V (min) or 4.5 V (min) depending on the user regulation voltage system selected.

9 Required to be supplied when 3.3 V regulator is disabled. See Section 5.5 PMC/POR/LVI electrical specifications.

10 I_{OH_F} = {16,32,47,77} mA and I_{OL_F} = {24,48,71,115} mA for {00,01,10,11} drive mode with V_{DDE} = 3.0 V. This spec is for characterization only.

11 I_{OH_S} = {11.6} mA and IOL_S = {17.7} mA for {medium} I/O with V_{DDE} = 4.5 V;
I_{OH_S} = {5.4} mA and IOL_S = {8.1} mA for {medium} I/O with V_{DDE} = 3.0 V. These specs are for characterization only.

12 Applies to D_CLKOUT, external bus pins, and Nexus pins.

13 V_{STBY} current specified at 1.0 V at a junction temperature of 85 ^{o}C. V_{STBY} current is 700 µA maximum at a junction temperature of 150 ^{o}C.

14 Preliminary. Specification pending typical and/or high-use Runidd pattern simulation as well as final silicon characterization. 900 mA based on transistor count estimate at Worst Case (wcs) process and temperature condition.

15 Power requirements for the V_{DD33} supply depend on the frequency of operation and load of all I/O pins, and the voltages on the I/O segments. See Section 5.7.2 I/O pad V_{DD33} current specifications, for information on both fast (F, FS) and medium (MH) pads. Also refer to Table 13 for values to calculate power dissipation for specific operation.

16 This value is a target that is subject to change.

17 This value allows a 5 V reference to supply ADC + REF.

18 Power requirements for each I/O segment depend on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Section 5.7.1 I/O pad current specifications, for information on I/O pad power. Also refer to Table 12 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

19 Absolute value of current, measured at V_{IL} and V_{IH}.

20 Absolute value of current, measured at V_{IL} and V_{IH}.

21 Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to pad types F and MH.

22 Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to pad types AE and AE/up-down. See Section 4 Signal properties and muxing.

23 This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics

24 Pull-up and pull-down resistances are both enabled and settings are equal.

5.7.1 I/O pad current specifications

The power consumption of an I/O segment is dependent on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 12 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 12.

The AC timing of these pads are described in the Section 5.11.2 Pad AC specifications.

Table 12. V_{DDE}/V_{DDEH} I/O Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	Voltage (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{DRV_MH}	50	50	5.25	11	16.0
2			20	50	5.25	01	6.3
3			3.0	50	5.25	00	1.1
4			2.0	200	5.25	00	2.4
5	Fast	I_{DRV_FC}	66	10	3.6	00	6.5
6			66	20	3.6	01	9.4
7			66	30	3.6	10	10.8
8			66	50	3.6	11	33.3
9	Fast w/ Slew Control	I_{DRV_FSR}	66	50	3.6	11	12.0
10			50	50	3.6	10	6.2
11			33.33	50	3.6	01	4.0
12			20	50	3.6	00	2.4
13			20	200	3.6	00	8.9

1 These are average IDDE numbers for worst case PVT from simulation. Currents apply to output pins only.

2 All loads are lumped.

5.7.2 I/O pad V_{DD33} current specifications

The power consumption of the V_{DD33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The V_{DD33} current draw on fast speed pads can be calculated from Table 13 dependent on the voltage, frequency, and load on all F type pins. The V_{DD33} current draw on medium pads can be calculated from Table 13 dependent on voltage and independent on the frequency and load on all MH type pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 13.

The AC timing of these pads are described in the Section 5.11.2 Pad AC specifications.

Table 13. V_{DD33} Pad Average DC Current[1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load[2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive/Slew Rate Select	Current (mA)
1	Medium	I_{33_MH}	—	—	3.6	5.5	—	0.0007
2	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.92
3			66	20	3.6	3.6	01	1.14
4			66	30	3.6	3.6	10	1.50
5			66	50	3.6	3.6	11	2.19
6	Fast w/ Slew Control	I_{33_FSR}	66	50	3.6	3.6	11	0.74
7			50	50	3.6	3.6	10	0.52
8			33.33	50	3.6	3.6	00	0.19
9			20	50	3.6	3.6	00	0.19
10			20	200	3.6	3.6	00	0.19

1 These are average IDDE for worst case PVT from simulation. Currents apply to output pins only for the fast pads and to input pins only for the medium pads.

2 All loads are lumped.

5.7.3 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol, which is an enhanced feature of the DSPI module.

Table 14. DSPI LVDS pad specification

#	Characteristic	Symbol	Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate							
1	Data Frequency	$f_{LVDSCLK}$	—	—	50	—	MHz
Driver Specs							
2	Differential output voltage	V_{OD}	SRC=0b00 or 0b11	150	—	400	mV
			SRC=0b01	90	—	320	
			SRC=0b10	160	—	480	
3	Common mode voltage (LVDS), VOS	V_{OS}	—	1.06	1.2	1.39	V
4	Rise/Fall time	T_R/T_F	—	—	2	—	ns
5	Propagation delay (Low to High)	T_{PLH}	—	—	4	—	ns
6	Propagation delay (High to Low)	T_{PHL}	—	—	4	—	ns
7	Delay (H/L), sync Mode	t_{PDSYNC}	—	—	4	—	ns
8	Delay, Z to Normal (High/Low)	T_{DZ}	—	—	500	—	ns

Table 14. DSPI LVDS pad specification (continued)

9	Diff Skew Itphla-tplhbI or Itplhb-tphlaI	T_{SKEW}	—	—	—	0.5	ns
Termination							
10	Trans. Line (differential Zo)	—	—	95	100	105	ohms
11	Temperature	—	—	–40	—	150	°C

5.8 Oscillator and FMPLL electrical characteristics

Table 15. FMPLL Electrical Specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range[2] (Normal Mode) Crystal Reference (PLLCFG2 = 0b0) Crystal Reference (PLLCFG2 = 0b1) External Reference (PLLCFG2 = 0b0) External Reference (PLLCFG2 = 0b1)	 $f_{ref\_crystal}$ $f_{ref\_crystal}$ f_{ref_ext} f_{ref_ext}	 8 16 8 16	 20 40[3] 20 40	MHz
2	Loss of Reference Frequency[4]	f_{LOR}	100	1000	kHz
3	Self Clocked Mode Frequency[5]	f_{SCM}	4	16	MHz
4	PLL Lock Time[6]	t_{LPLL}	—	< 400	µs
5	Duty Cycle of Reference [7]	t_{DC}	40	60	%
6	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
7	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
8	D_CLKOUT Period Jitter[8, 9] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{clkout}
9	Peak-to-Peak Frequency Modulation Range Limit [10,11] (f_{sys} Max must not be exceeded)	C_{mod}	0	4	%f_{sys}
10	FM Depth Tolerance[12]	C_{mod_err}	–0.25	0.25	%f_{sys}
11	VCO Frequency	f_{VCO}	192	600	MHz
12	Modulation Rate Limits[13]	f_{mod}	0.400	1	MHz
13	Predivider output frequency range[14]	f_{prediv}	4	10	MHz

1 All values given are initial design targets and subject to change.

2 Crystal and External reference frequency limits depend on device relying on PLL to lock prior to release of reset, default PREDIV/EPREDIV, MFD/EMFD default settings, and VCO frequency range. Absolute minimum loop frequency is 4 MHz.

3 Upper tolerance of less than 1% is allowed on 40MHz crystal.

4 “Loss of Reference Frequency” is the reference frequency detected internally, which transitions the PLL into self clocked mode.

5 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR}. This frequency is measured at D_CLKOUT. A default RFD value of (0x05) is used in SCM mode, and the programmed MFD and RFD values have no effect

6 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

7 For Flexray operation, duty cycle requirements are higher.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval. D_CLKOUT divider set to divide-by-2.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

10 Modulation depth selected must not result in f_{pll} value greater than the f_{pll} maximum specified value.

11 Maximum and minimum variation from programmed modulation depth is pending characterization. Depth settings available in control register are: 2%, 3%, and 4% peak-to-peak.

12 Depth tolerance is the programmed modulation depth ±0.25% of F_{sys}. Violating the VCO min/max range may prevent the system from exiting reset.

13 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

14 Violating this range will cause the VCO max/min range to be violated with the default MFD settings out of reset.

Table 16. Oscillator electrical specifications[1]

(V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Crystal Mode Differential Amplitude[2] (Min differential voltage between EXTAL and XTAL)	$V_{crystal\_diff\_amp}$	$\lvert V_{extal} - V_{xtal} \rvert > 0.4$ V	—	V
2	Crystal Mode: Internal Differential Amplifier Noise Rejection	$V_{crystal\_diff\_amp\_nr}$	—	$\lvert V_{extal} - V_{xtal} \rvert < 0.2$ V	V
3	EXTAL Input High Voltage Bypass mode, External Reference	V_{IHEXT}	$((V_{DD33}/2) + 0.4$ V)	—	V
4	EXTAL Input Low Voltage Bypass mode, External Reference	V_{ILEXT}	—	$(V_{DD33}/2) - 0.4$ V	V
5	XTAL Current[3]	I_{XTAL}	1	3	mA
6	Total On-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
7	Total On-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
8	Crystal manufacturer's recommended capacitive load	C_L	See crystal spec	See crystal spec	pF
9	Discrete load capacitance to be connected to EXTAL	C_{L_EXTAL}	—	$(2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[4]$)$	pF
10	Discrete load capacitance to be connected to XTAL	C_{L_XTAL}	—	$(2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[4]$)$	pF

1 All values given are initial design targets and subject to change.

2 This parameter is meant for those who do not use quartz crystals or resonators, but instead use CAN oscillators in crystal mode. In that case, $V_{extal} - V_{xtal} \geq 400$ mV criterion has to be met for oscillator's comparator to produce output clock.

3 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

4 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

5.9 eQADC electrical characteristics

Table 17. eQADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	ADC Clock (ADCLK) Frequency	f_{ADCLK}	2	16	MHz
2	Conversion Cycles Single Ended Conversion Cycles 12 bit resolution Single Ended Conversion Cycles 10 bit resolution Single Ended Conversion Cycles 8 bit resolution **Note:** Differential conversion (min) is one clock cycle less than the single-ended conversion values listed here.	CC	 2 + 14 2 + 12 2 + 10	 128 + 14 128 + 12 128 + 10	ADCLK cycles
3	Stop Mode Recovery Time[1]	T_{SR}	10	—	µs
4	Resolution[2]	—	1.25	—	mV
5	INL: 8 MHz ADC Clock[3]	INL8	–4[4]	4[4]	LSB[5]
6	INL: 16 MHz ADC Clock[3]	INL16	–8[4]	8[4]	LSB
7	DNL: 8 MHz ADC Clock[3]	DNL8	–3[4]	3[4]	LSB
8	DNL: 16 MHz ADC Clock[3]	DNL16	–3[4]	3[4]	LSB
9	Offset Error without Calibration	OFFNC	0[4]	100[4]	LSB
10	Offset Error with Calibration	OFFWC	–4[4]	4[4]	LSB
11	Full Scale Gain Error without Calibration	GAINNC	–120[4]	0[4]	LSB
12	Full Scale Gain Error with Calibration	GAINWC	–4[4,6]	4[4,6]	LSB
13	Non-Disruptive Input Injection Current [7, 8, 9, 10]	I_{INJ}	–3	3	mA
14	Incremental Error due to injection current[11, 12]	E_{INJ}	–4[4]	4[4]	Counts
15	TUE value at 8 MHz [13, 14] (with calibration)	TUE8	–4[4,6]	4[4,6]	Counts
16	TUE value at 16 MHz [13, 14] (with calibration)	TUE16	–8	8	Counts
17	Maximum differential voltage[15] (DANx+ - DANx-) or (DANx- - DANx+) PREGAIN set to 1X setting PREGAIN set to 2X setting PREGAIN set to 4X setting	 $DIFF_{max}$ $DIFF_{max2}$ $DIFF_{max4}$	 — — —	 $(V_{RH} – V_{RL})/2$ $(V_{RH} – V_{RL})/4$ $(V_{RH} - V_{RL})/8$	 V V V
18	Differential input Common mode voltage[15] (DANx- + DANx+)/2	$DIFF_{cmv}$	$(V_{RH} – V_{RL})/2$ – 5%	$(V_{RH} – V_{RL})/2$ + 5%	V

1 Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.

2 At $V_{RH} – V_{RL}$ = 5.12 V, one count = 1.25 mV without using pregain.

3 INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB. The eQADC is guaranteed to be monotonic at 10 bit accuracy (12 bit resolution selected).

4 New design target. Actual specification will change following characterization. Margin for manufacturing has not been fully included.

5 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

6 The value is valid at 8 MHz, it is ±8 counts at 16 Mhz.

7 Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.

[8] Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

[9] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = –0.3$ V, then use the larger of the calculated values.

[10] Condition applies to two adjacent pins at injection limits.

[11] Performance expected with production silicon.

[12] All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.

[13] The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.

[14] TUE does not apply to differential conversions.

[15] Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

5.9.1 ADC internal resource measurements

Table 18. Power Management Control (PMC) specification

Spec	Characteristic	Symbol	Min	Typical	Max	Unit
PMC Normal Mode						
1	Bandgap 0.62 V ADC0 channel 145	V_{ADC145}	—	0.62	—	V
2	Bandgap 1.2 V ADC0 channel 146	V_{ADC146}	—	1.22	—	V
3	Vreg1p2 Feedback ADC0 channel 147	V_{ADC147}	—	V_{DD} / 2.045	—	V
4	LVD 1.2 V ADC0 channel 180	V_{ADC180}	—	V_{DD} / 1.774	—	V
5	Vreg3p3 Feedback ADC0 channel 181	V_{ADC181}	—	Vreg3p3 / 5.460	—	V
6	LVD 3.3 V ADC0 channel 182	V_{ADC182}	—	Vreg3p3 / 4.758	—	V
7	LVD 5.0 V ADC0 channel 183 — LDO mode — SMPS mode	V_{ADC183}	—	 V_{DDREG} / 4.758 V_{DDREG}/7.032	—	V

Table 19. Standby RAM regulator electrical specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode						
1	Standby Regulator Output ADC1 channel 194	V_{ADC194}	—	1.2	—	V
2	Standby Source Bias 150 mV to 360 mV (30mV Increment @ vref_sel) ADC1 channel 195 Default Value 150 mV (@vref_sel = 1 1 1)	V_{ADC195}	150	—	360	mV
3	Standby Brownout Reference ADC1 channel 195	V_{ADC195}	500	—	850	mV

Table 20. ADC band gap reference / LVI electrical specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	4.75 LVD (from V_{DDA}) ADC1 channel 196	V_{ADC196}	—	4.75	—	V
2	ADC Bandgap ADC0 channel 45 ADC1 channel 45	V_{ADC45}	1.171	1.220	1.269	V

Table 21. Temperature sensor electrical specifications

Spec	Characteristic	Symbol	Min	Typ	Max	Unit
1	Slope –40 °C to 100 °C ±1.0 °C 100 °C to 150 °C ±1.6 °C ADC0 channel 128 ADC1 channel 128	$V_{SADC128}$[1]	—	5.8	—	mV/ °C
2	Accuracy –40 °C to 150 °C ADC0 channel 128 ADC1 channel 128	—	—	±10.0	—	°C

1 Slope is the measured voltage change per °C.

5.10 C90 flash memory electrical characteristics

Table 22. Flash program and erase specifications

Spec	Characteristic	Symbol	Min	Typ[1]	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	38	—	500	µs
2	Page Program Time[4,5]	$t_{pprogram}$	—	45	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	270	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	800	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	1500	2600	7500	ms
6	256 KB Block Pre-program and Erase Time	$t_{256kpperase}$	—	3000	5200	15000	ms

1 Typical program and erase times assume nominal supply values and operation at 25 ^{o}C.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, typical supply voltage, 80 MHz minimum system frequency.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Program times are actual hardware programming times and do not include software overhead.

5 Page size is 128 bits (4 words).

Table 23. Flash EEPROM module life

Spec	Characteristic	Symbol	Min	Typical[1]	Unit
1	Number of program/erase cycles per block for 16 KB and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
2	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range (T_J)	P/E	1,000	100,000	cycles
3	Minimum Data Retention at 85 °C ambient temperature[2] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	Retention	 20 10 5	 — — —	years

1 Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 24 shows the Platform Flash Configuration Register 1 (PFCPR1) settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 24. PFCPR1 settings vs. frequency of operation[1]

Spec	Clock Mode	Maximum Frequency[2] (MHz)		APC = RWSC	WWSC	DPFEN[3]	IPFEN[3]	PFLIM[4]	BFEN[5]
		Core f_{sys}	Platform f_{platf}						
1	Enhanced	264 MHz[6]	132 MHz[6]	0b011	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
2	Enhanced/ Full	200 MHz	100 MHz	0b010	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
3	Legacy	132 MHz	132 MHz	0b100	0b01	0b0 0b1	0b0 0b1	0b00 0b01 0b1x	0b0 0b1
Default setting after reset:				0b111	0b11	0b00	0b00	0b00	0b0

1 Illegal combinations exist. Use entries from the same row in this table.

2 This is the nominal maximum frequency of operation: platform runs at $f_{sys}/2$ in Enhanced Mode .

3 For maximum flash performance, set to 0b1.

4 For maximum flash performance, set to 0b10.

5 For maximum flash performance, set to 0b1.

6 This is the nominal maximum frequency of operation in Enhanced Mode. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system core clock(f_{sys}) + 2% FM and 132 Mhz platform clock (f_{platf})+ 2% FM.

5.11 AC specifications

5.11.1 Clocking

Figure 8 shows the operating frequency domains of various blocks on PXR40.

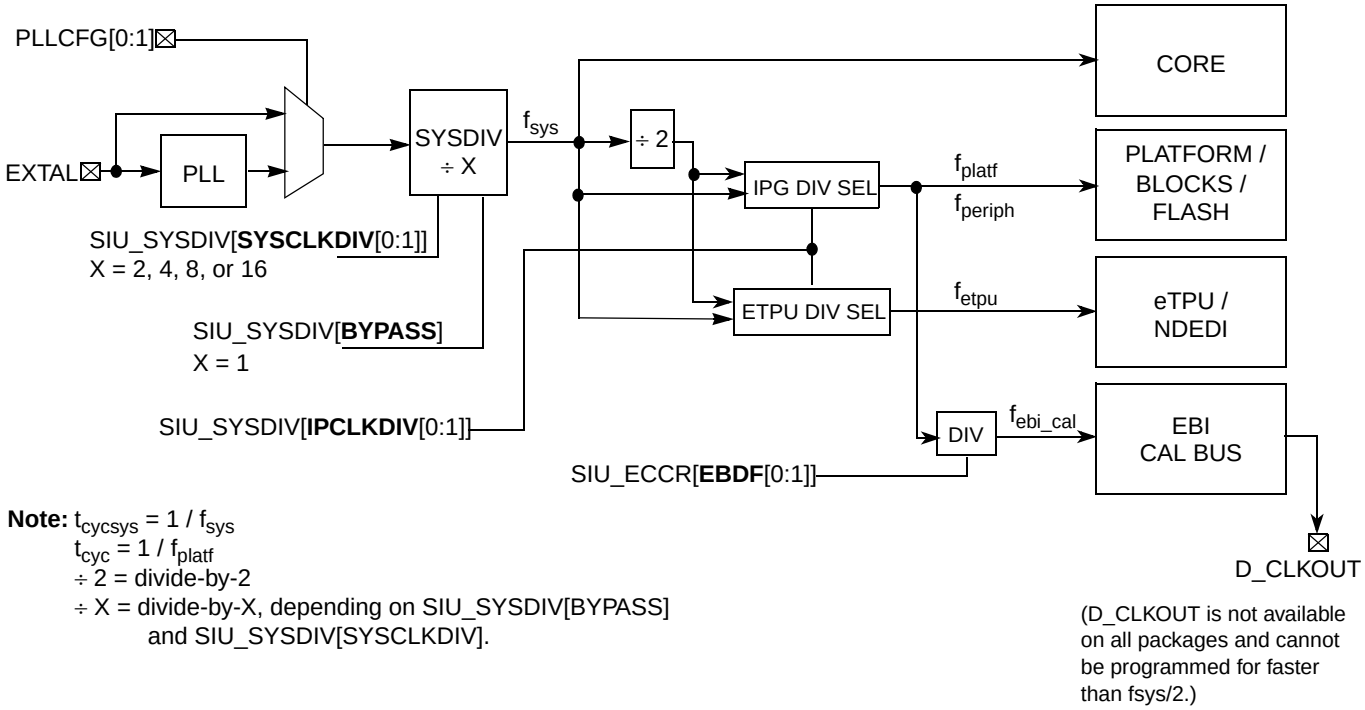


Figure 8. PXR40 block operating frequency domain diagram

Table 25 shows the operating frequencies of various blocks depending on the device's clocking mode configuration settings (see Table 26 and Table 27 for descriptions of bit settings).

Table 25. PXR40 operating frequencies[1, 2]

Mode	SIU_ECCR [EBDF[0:1]][3]	f_{sys} (core)	f_{platf} (platform and all blocks except eTPU)	f_{etpu} (eTPU, eTPU RAM, and NDEDI)	f_{ebi_cal}[4,5]	Unit
Enhanced	01 11	264 264	132 132	132 132	66 33	MHz
Full	01 11	200 200	100 100	200 200	50 25	MHz
Legacy	01 11	132 132	132 132	132 132	66 33	MHz

1 The values in the table are specified at:
V_{DD} = 1.02 V to 1.32 V
V_{DDE} = 3.0 V to 3.6 V
V_{DDEH} = 4.5 V to 5.5 V
V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V
$T_A = T_L$ to T_H.

2 Up to the maximum frequency rating of the device (refer to Table 39). The f_{sys} speed is the nominal maximum frequency. 270 Mhz parts allow for 264 Mhz system clock + 2% FM.

3 See the *PXR40 Reference Manual* for full description as not all bit combinations are valid.

4 EBI/Calibration bus is not available in all packages.

5 The EBI/Calibration Bus operating frequency, f_{ebi_cal} , depends on clock divider settings of block's max allowed frequency of operation. Normally $f_{ebi\_cal} = f_{platf}/2$, but can be limited to < $f_{platf}/2$ in Full Mode.

Table 26. IPCLKDIV settings

SIU_SYSDIV [IPCLKDIV[0:1]]	Mode	Description
00	Enhanced	CPU frequency is doubled (Max 264Mhz). Platform, peripheral, and eTPU clocks are 1/2 of CPU frequency
01	Full	CPU and eTPU frequency is doubled (Max 200Mhz). Platform and peripheral clocks are 1/2 of CPU frequency.
10	—	Reserved
11	Legacy	CPU, eTPU, platform, and peripheral's clocks all run at same speed (Max 132Mhz).

Table 27. SYSCLKDIV settings

SIU_SYSDIV [SYSCLKDIV[0:1]]	Description
00	Divide by 2.
01	Divide by 4.
10	Divide by 8.
11	Divide by 16.

5.11.2 Pad AC specifications

Table 28. Pad AC specifications (v_{ddeh} = 5.0 V, V_{DDE} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
1	Medium[5]	00	152/165	70/74	50
2			205/220	96/96	200
3		01	28/34	12/15	50
4			52/59	28/31	200
5		11	12/12	5.3/5.9	50
6			32/32	22/22	200

Table 28. Pad AC specifications (v_{ddeh} = 5.0 V, V_{DDE} = 3.3 V)[1] (continued)

Spec	Pad	SRC/DSC	Out Delay[2,4] L → H/H → L (ns)	Rise/Fall[3,4] (ns)	Load Drive (pF)
7	Fast[6]	00	2.5	1.2	10
8		01			20
9		10			30
10		11			50
11	Fast with Slew Rate	00	40/40	16/16	50
12			50/50	21/21	200
13		01	13/13	5/5	50
14			19/19	8/8	200
15		10	8/8	2.4/2.4	50
16			12/12	5/5	200
17		11	5/5	1.1/1/1	50
18			8/8	2.6	2.6
19	Pull Up/Down (3.6 V max)	—	—	7500	50
20	Pull Up/Down (5.25 V max)	—	6000	5000/5000	50

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.02 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 4.75 V to 5.25 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested.

4 Delay and rise/fall are measured to 20% or 80% of the respective signal.

5 Out delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

6 Out delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

Table 29. Derated pad AC specifications (V_{DDEH} = 3.3 V)[1]

Spec	Pad	SRC/DSC	Out Delay[2,3] L → H/H → L (ns)	Rise/Fall[4,3] (ns)	Load Drive (pF)
1	Medium[5]	00	200/210	86/86	50
2			270/285	120/120	200
3		01	37/45	15.5/19	50
4			69/82	38/43	200
5		11	18/17	7.6/8.5	50
6			46/49	30/34	200

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DDEH} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 Out delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

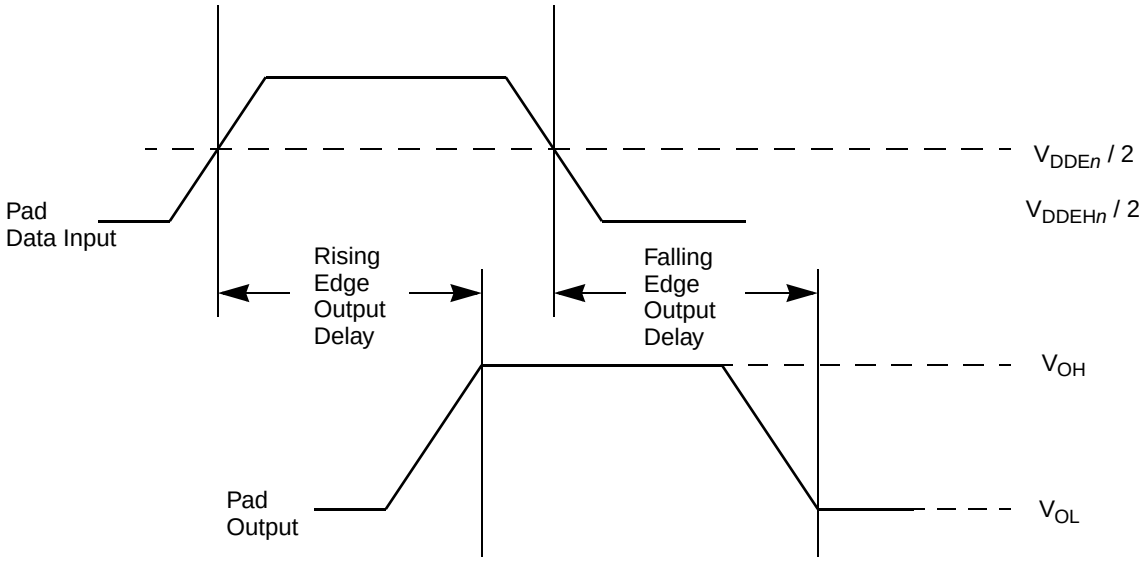


Figure 9. Pad output delay

5.12 AC timing

5.12.1 Generic timing diagrams

The generic timing diagrams in Figure 10 and Figure 11 apply to all I/O pins with pad types F and MH. See 4, Signal properties and muxing, for the pad type for each pin.

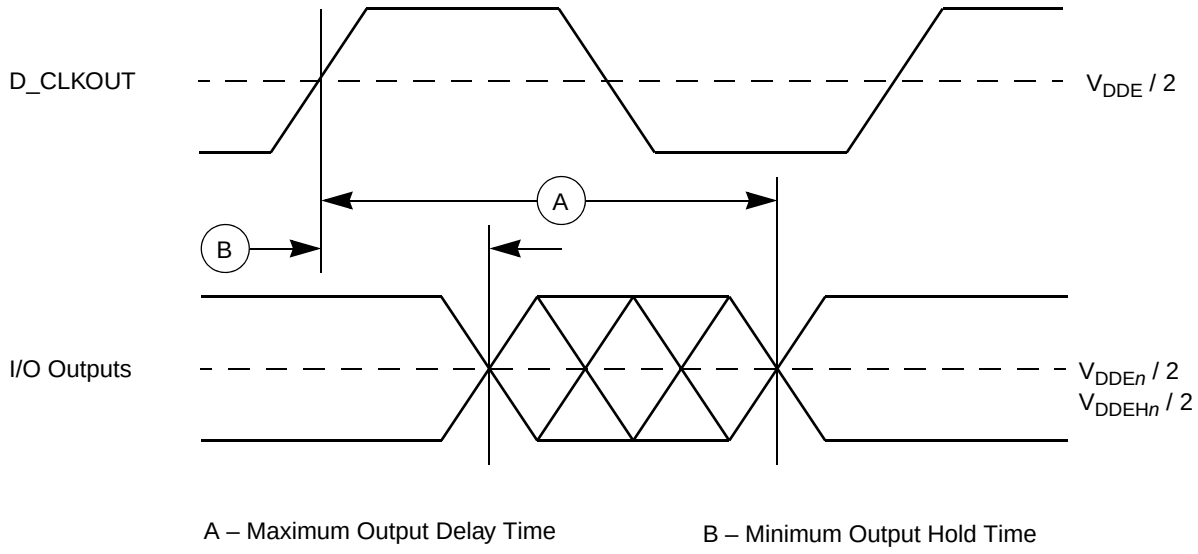


Figure 10. Generic output delay/hold timing

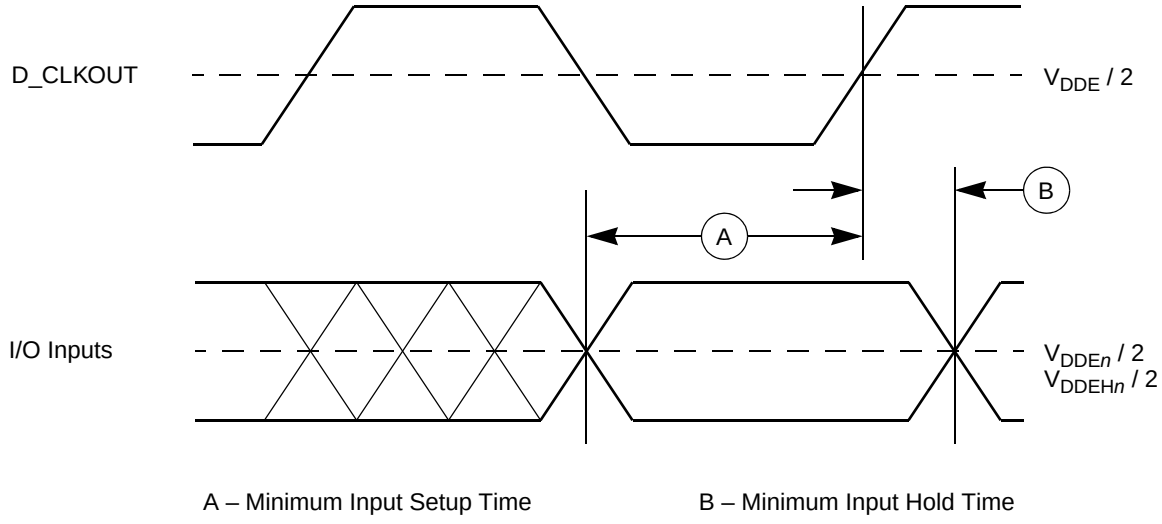


Figure 11. Generic input setup/hold timing

5.12.2 Reset and configuration pin timing

Table 30. Reset and configuration pin timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	10	—	t_{cyc}[2]
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}[2]
3	PLLCFG, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}[2]
4	PLLCFG, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}[2]

1 Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.08 V to 1.32 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 8 and Table 25 in Section 5.11.1 Clocking.

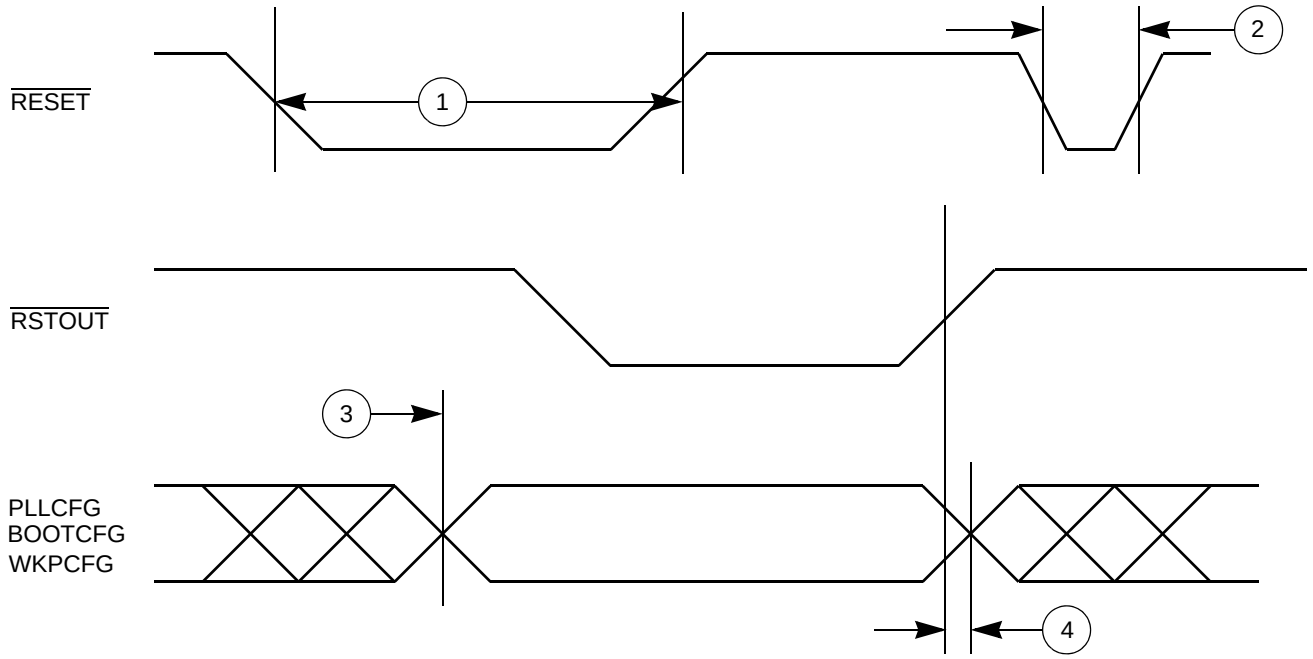


Figure 12. Reset and configuration pin timing

5.12.3 IEEE 1149.1 interface timing

Table 31. JTAG pin AC electrical characteristics[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at V_{DDE} / 2)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40%–70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	10	ns

Table 31. JTAG pin AC electrical characteristics[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

1 JTAG timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b00. These specifications apply to JTAG boundary scan only. See Table 32 for functional specifications.

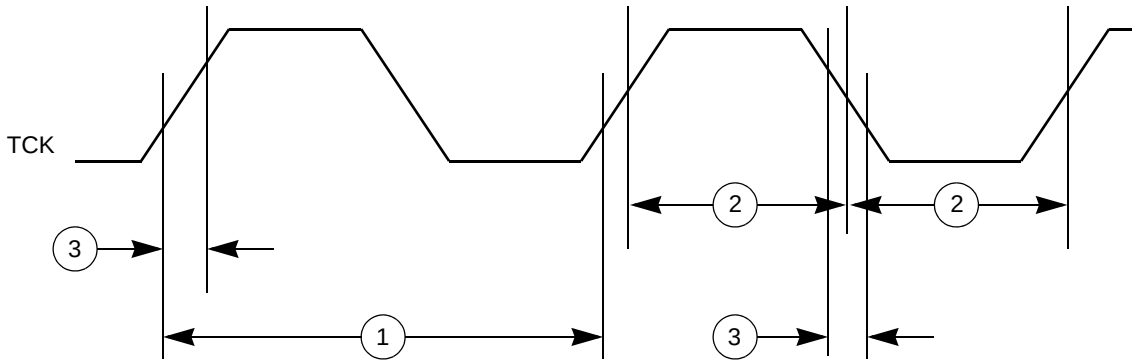


Figure 13. JTAG test clock input timing

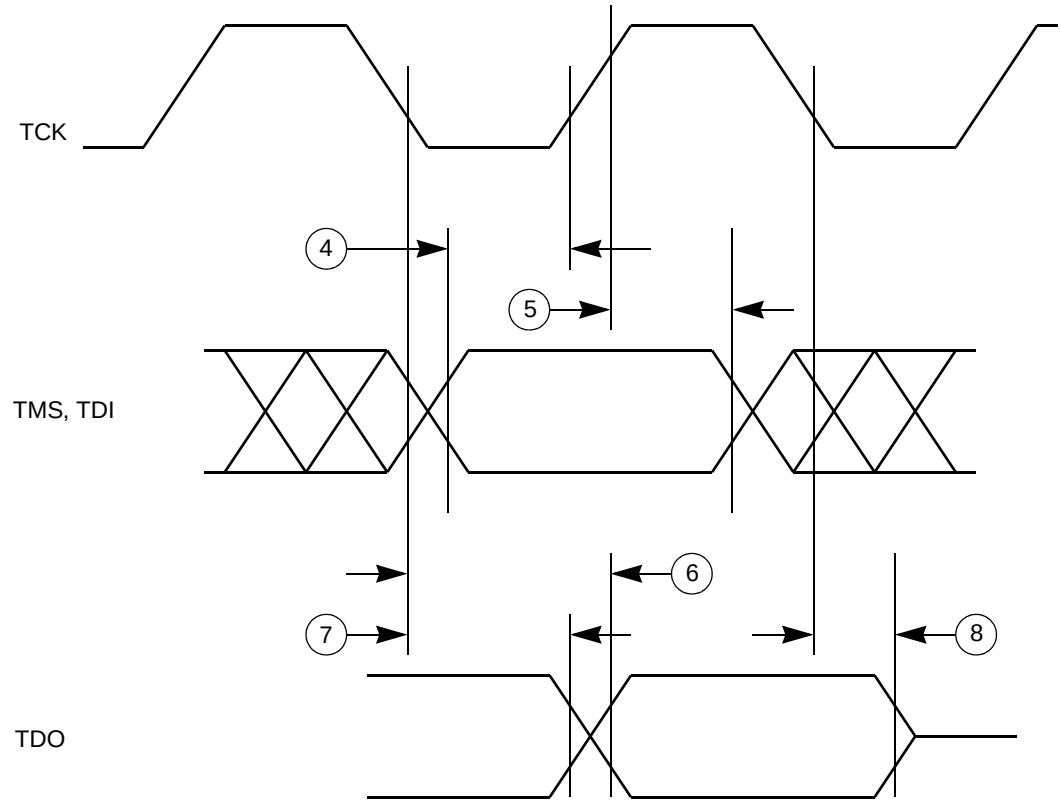


Figure 14. JTAG Test Access Port (TAP) timing

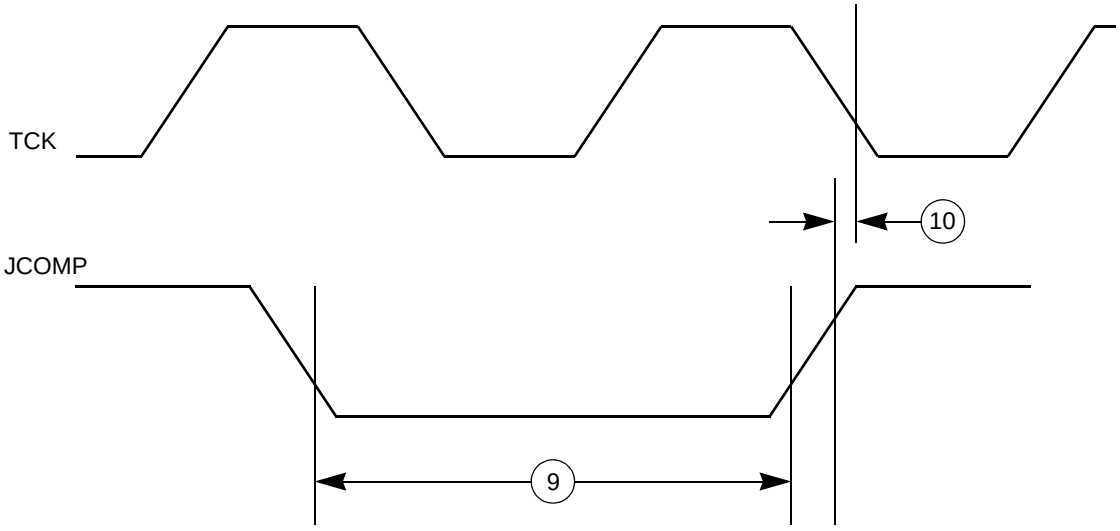


Figure 15. JTAG JCOMP timing

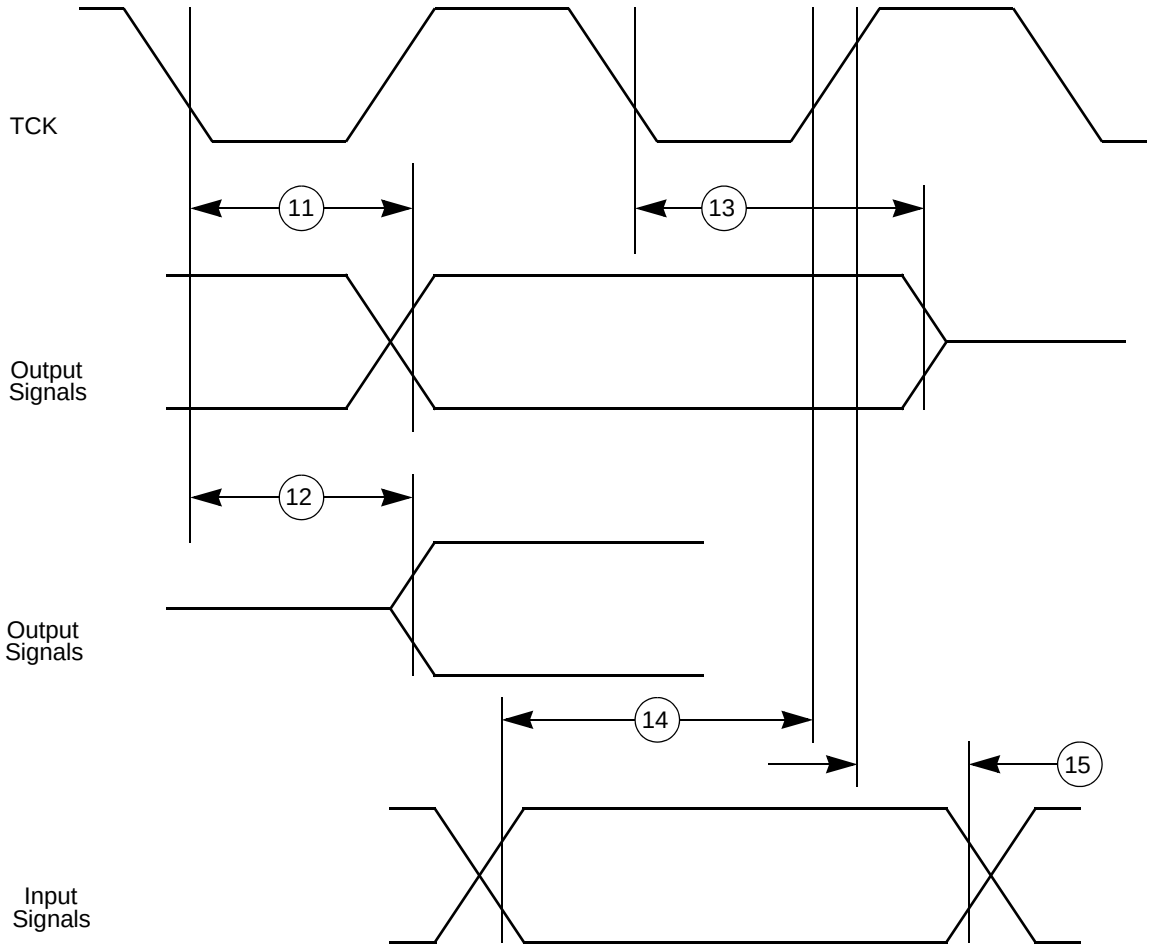


Figure 16. JTAG boundary scan timing

5.12.4 Nexus timing

Table 32. Nexus debug port timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	MCKO Cycle Time	t_{MCYC}	2[2]	8	t_{CYC}[3]
2	MCKO Duty Cycle	t_{MDC}	40	60	%
3	MCKO Low to MDO Data Valid[4]	t_{MDOV}	–0.1	0.2	t_{MCYC}
4	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[4]	t_{MSEOV}	–0.1	0.2	t_{MCYC}
5	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[4]	t_{EVTOV}	–0.1	0.2	t_{MCYC}
6	$\overline{\text{EVTI}}$ Pulse Width	t_{EVTIPW}	4.0	—	t_{TCYC}[3]
7	$\overline{\text{EVTO}}$ Pulse Width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK Cycle Time	t_{TCYC}	4[5]	—	t_{CYC}[3]
9	TCK Duty Cycle	t_{TDC}	40	60	%

Table 32. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
10	TDI, TMS Data Setup Time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid	t_{NTDOV}	0	10	ns
13	$\overline{RDY}$ Valid to MCKO[6]	—	—	—	—

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz (pending characterization). Set NPC_PCR[MKCO_DIV] to correct division depending on the system frequency, not to exceed maximum Nexus AUX port frequency.

3 See Notes on t_{cyc} on Figure 13 and Table 25 in Section Section 5.11.1 Clocking.

4 MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.

5 Lower frequency is required to be fully compliant to standard.

6 The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

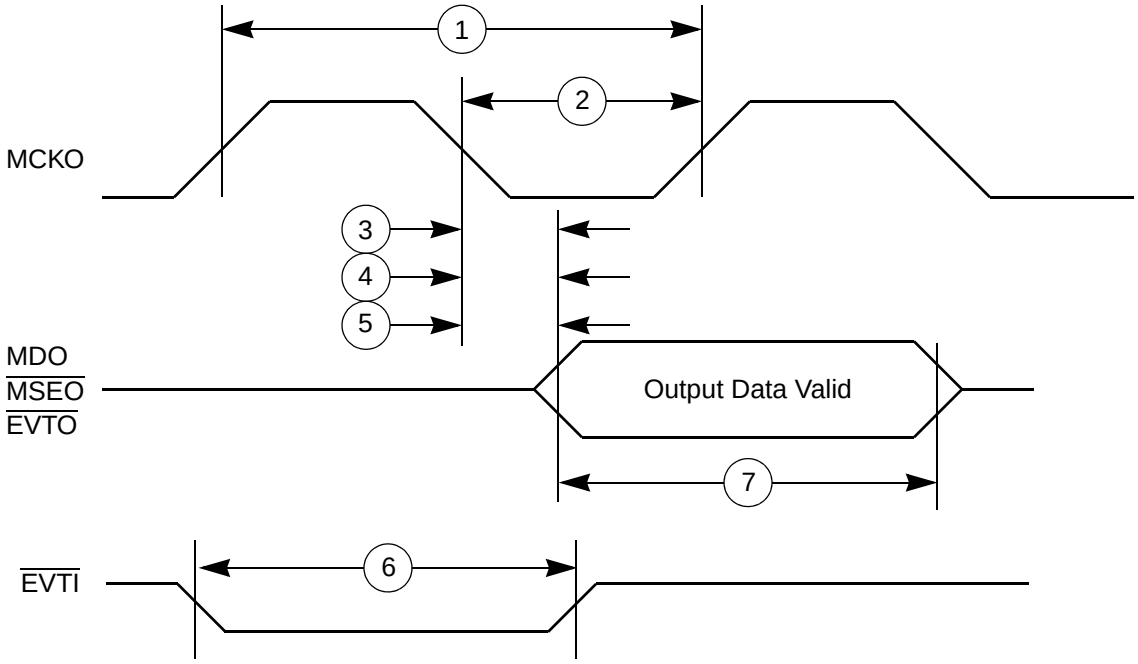


Figure 17. Nexus timings

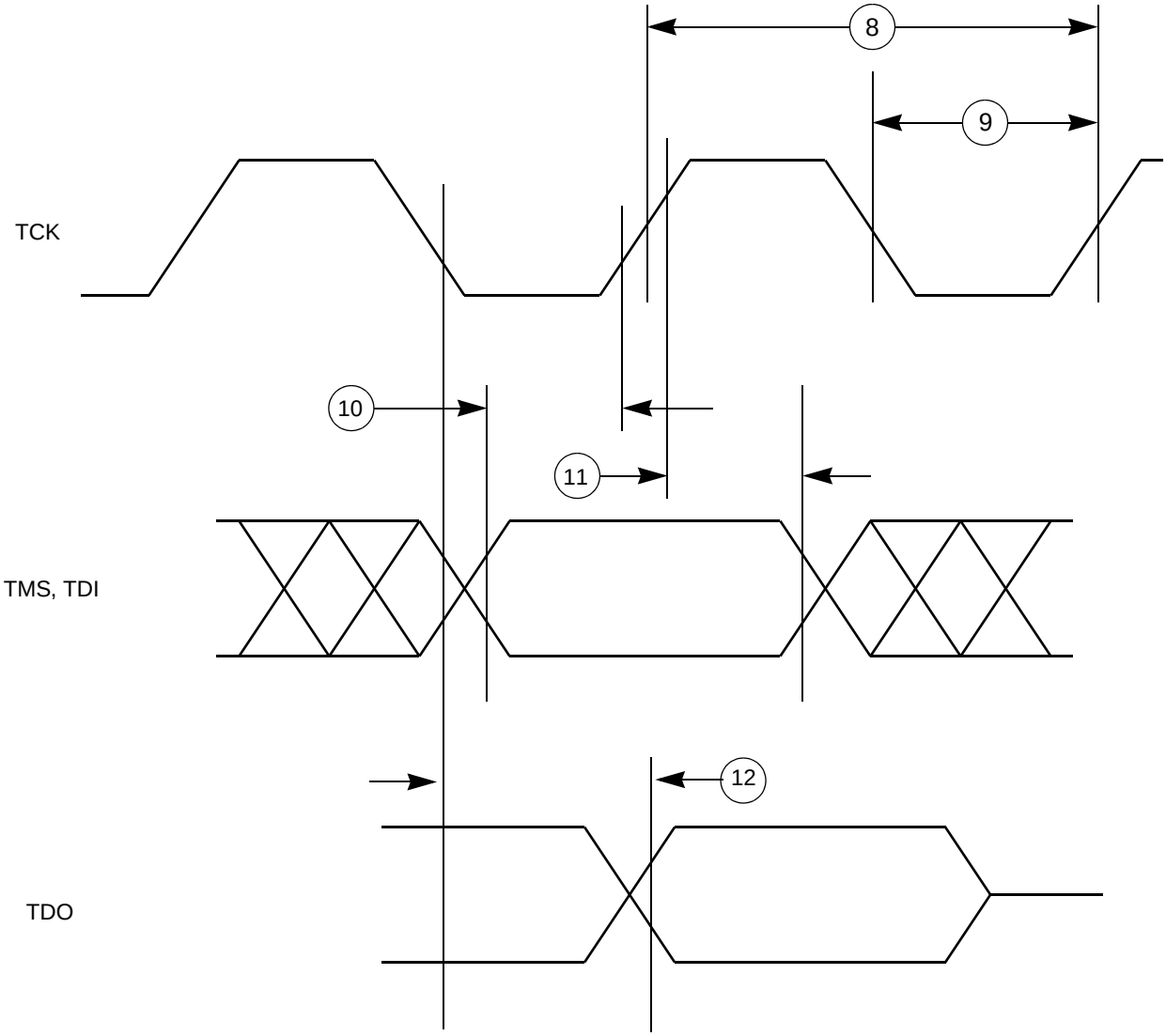


Figure 18. Nexus TCK, TDI, TMS, TDO timing

5.12.5 External Bus Interface (EBI) timing

Table 33. Bus operation timing [1]

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2] [3]		Unit	Notes
			Min	Max		
1	D_CLKOUT Period	t_C	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	D_CLKOUT Duty Cycle	t_{CDC}	45%	55%	t_C	
3	D_CLKOUT Rise Time	t_{CRT}	—	—[4]	ns	
4	D_CLKOUT Fall Time	t_{CFT}	—	—[4]	ns	
5	D_CLKOUT Posedge to Output Signal Invalid or High Z (Hold Time) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COH}	1.0/1.5	—	ns	Hold time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 1.0 ns EBTS = 1: 1.5 ns
6	D_CLKOUT Posedge to Output Signal Valid (Output Delay) D_ADD[9:30] D_BDIP D_CS[0:3] D_DAT[0:15] D_OE D_RD_WR D_TA D_TS D_WE[0:3]/D_BE[0:3]	t_{COV}	—	7.0/7.5	ns	Output valid time selectable via SIU_ECCR[EBTS] bit: EBTS = 0: 7.0 ns EBTS = 1: 7.5 ns

Table 33. Bus operation timing [1] (continued)

Spec	Characteristic	Symbol	66 MHz (Ext. Bus Freq)[2 3]		Unit	Notes
			Min	Max		
7	Input Signal Valid to D_CLKOUT Posedge (Setup Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIS}	5.0/4.5	—	ns	Input setup time selectable via SIU_ECCR[EBTS] bit: EBTS = 0; 5.0ns EBTS = 1; 4.5ns
8	D_CLKOUT Posedge to Input Signal Invalid (Hold Time) D_ADD[9:30] D_DAT[0:15] D_RD_WR D_TA D_TS	t_{CIH}	1.0	—	ns	
9	D_ALE Pulse Width	t_{APW}	6.5	—	ns	The timing is for Asynchronous external memory system.
10	D_ALE Negated to Address Invalid	t_{AAI}	2.0/1.0 [5]	—	ns	The timing is for Asynchronous external memory system. ALE is measured at 50% of VDDE.

1 EBI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 MHz system clock + 2% FM.

3 Depending on the internal bus speed, set the SIU_ECCR[EBDF] bits correctly not to exceed maximum external bus frequency. The maximum external bus frequency is 66 MHz.

4 Refer to Fast pad timing in Table 28 and Table 29.

5 ALE hold time spec is temperature dependant. 1.0 ns spec applies for temperature range -40 to 0 °C. 2.0 ns spec applies to temperatures > 0 °C. This spec has no dependency on SIU_ECCR[EBTS] bit.

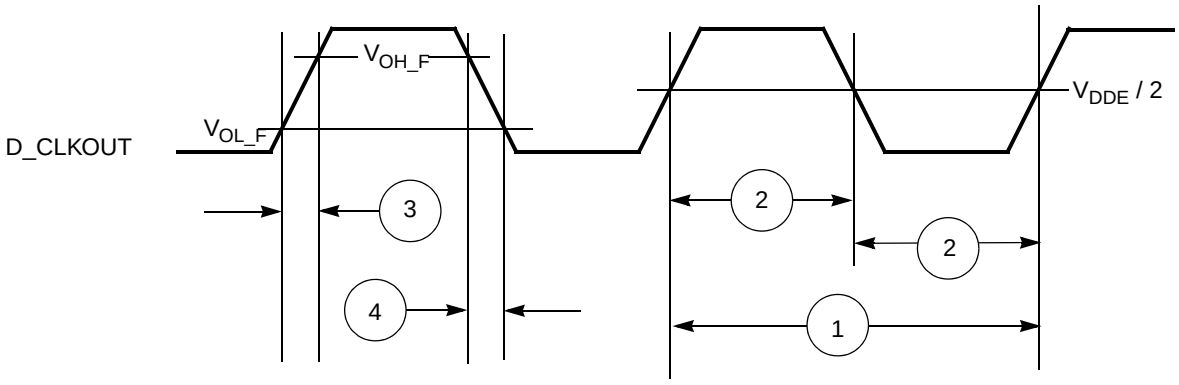


Figure 19. D_CLKOUT timing

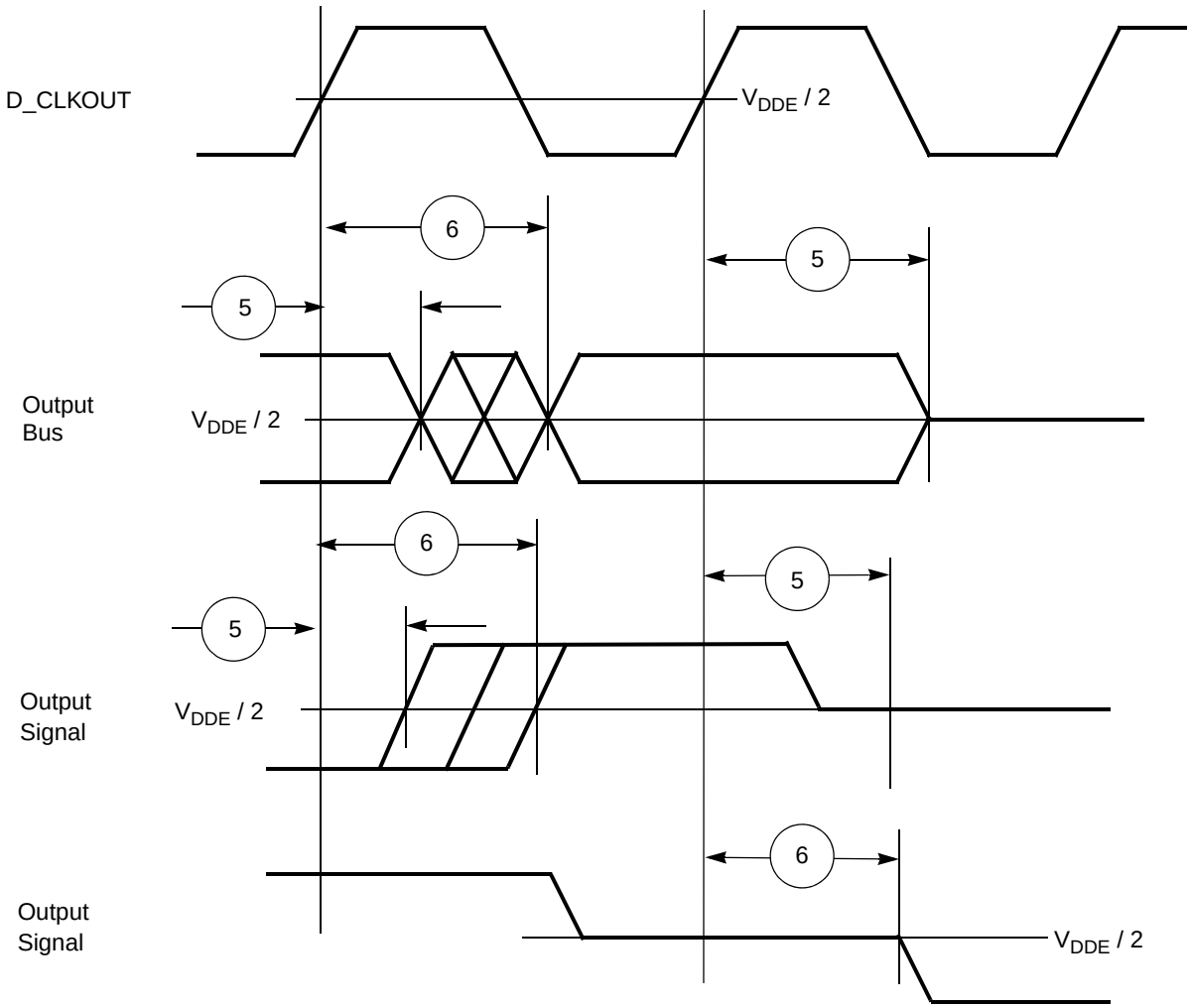


Figure 20. Synchronous output timing

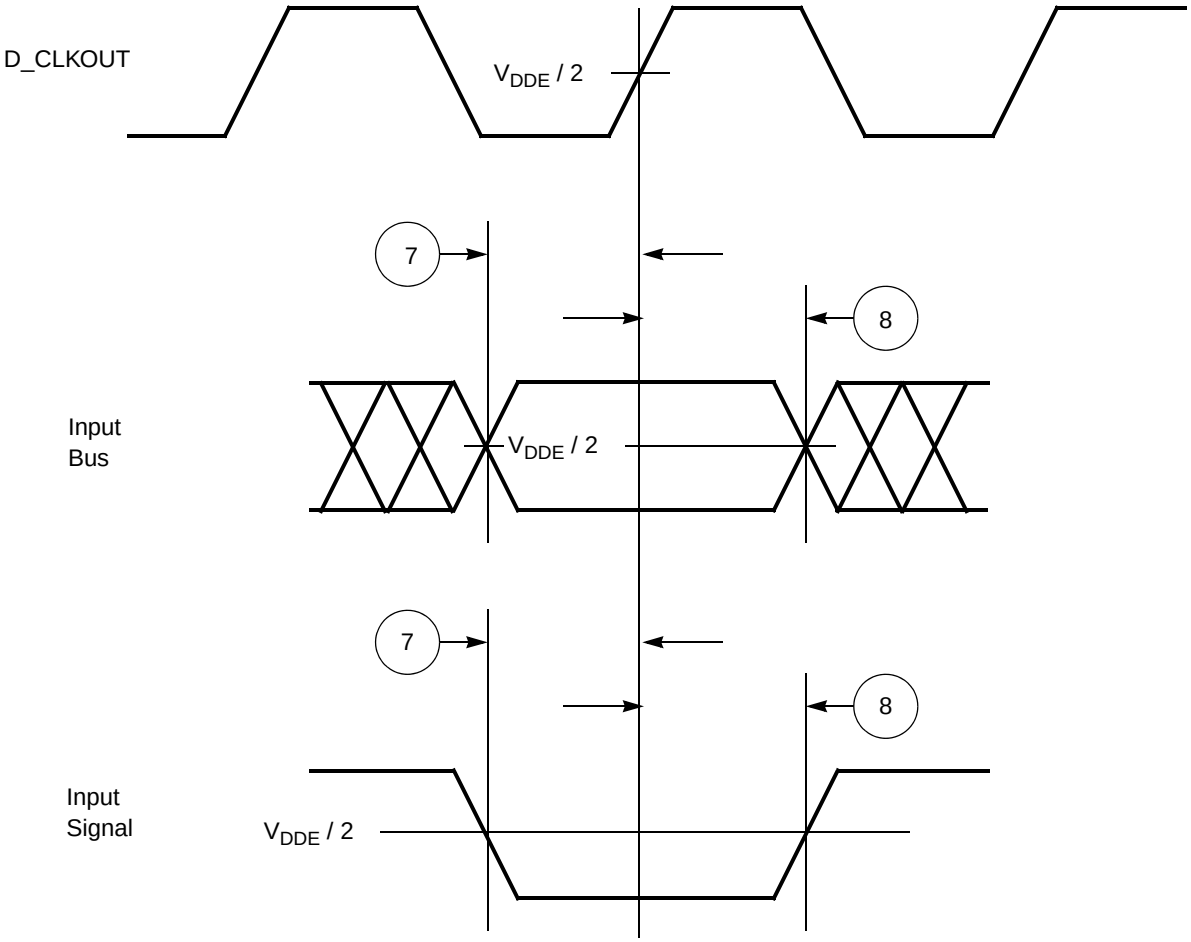


Figure 21. Synchronous input timing

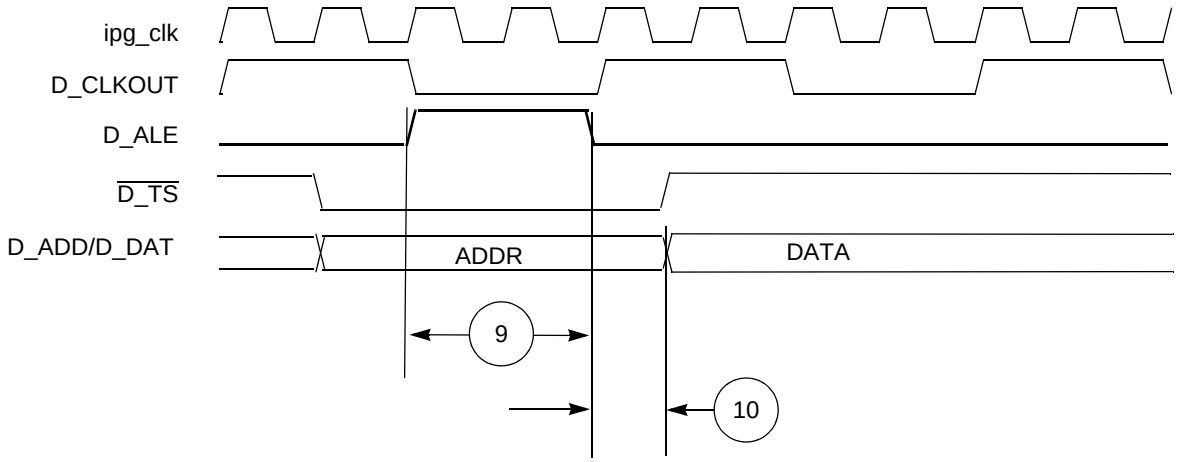


Figure 22. ALE signal timing

5.12.6 External interrupt timing (IRQ pin)

Table 34. External interrupt timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1 IRQ timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 See Notes on t_{cyc} on Figure 8 and Table 25 in Section 5.11.1 Clocking.

3 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

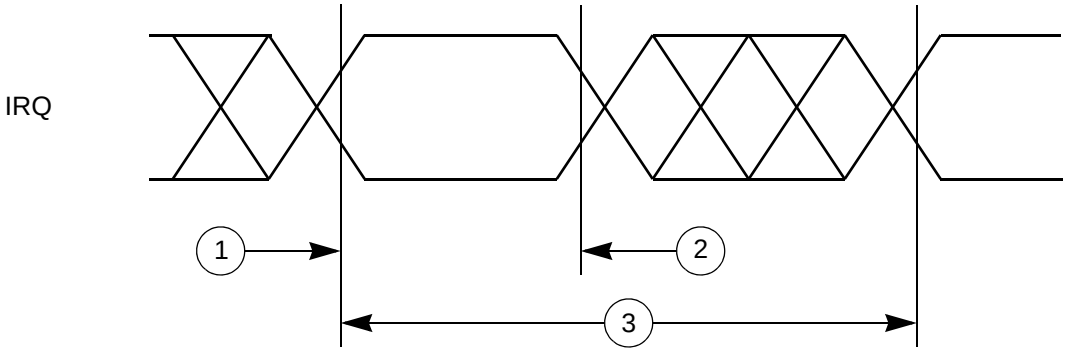


Figure 23. External interrupt timing

5.12.7 eTPU timing

Table 35. eTPU timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{cyc}[2]

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 8 and Table 25 in Section 5.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

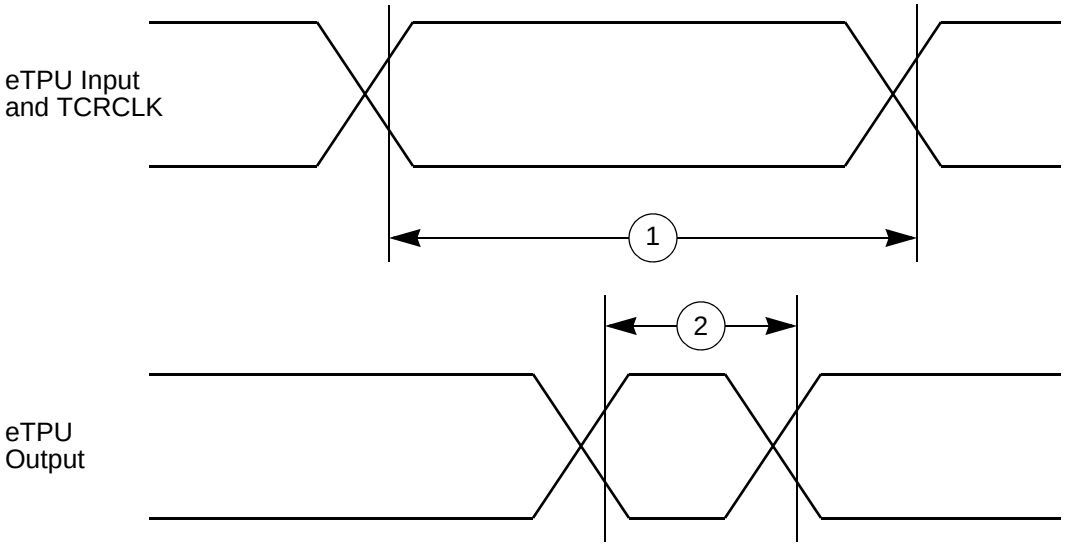


Figure 24. eTPU timing

5.12.8 eMIOS timing

Table 36. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{cyc}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{cyc}[2]

1 eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

2 See Notes on t_{cyc} on Figure 8 and Table 25 in Section 5.11.1 Clocking.

3 This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

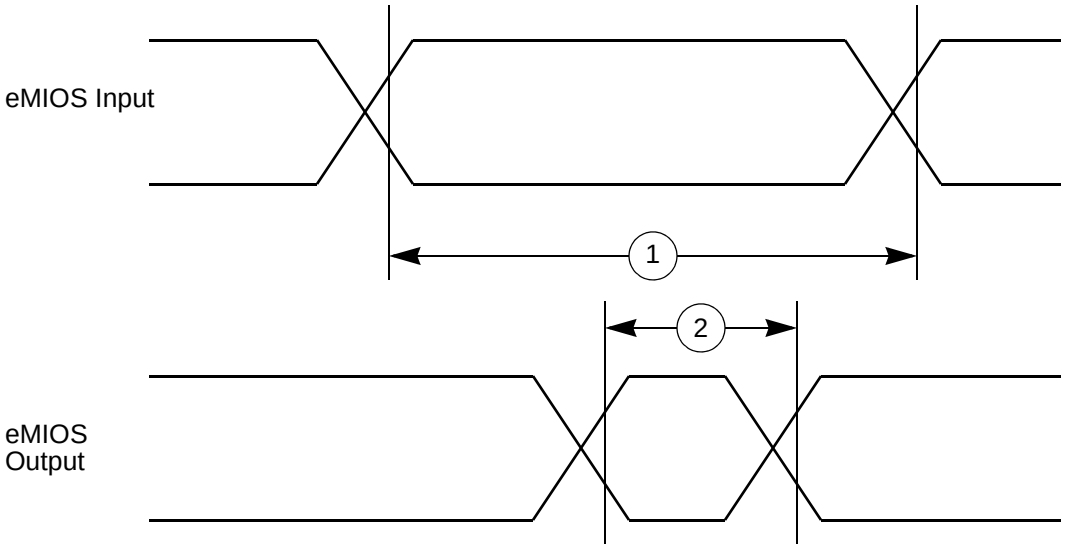


Figure 25. eMIOS timing

5.12.9 DSPI timing

Table 37. DSPI timing[1] [2]

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
1	DSPI Cycle Time[3, 4] Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	t_{SYS} * 2	t_{SYS}*32768*7	ns
2	PCS to SCK Delay[5]	t_{CSC}	12	—	ns
3	After SCK Delay[6] Master mode Slave mode	t_{ASC}	t_{SYS} * 2 t_{SYS} *3 – constraints [7]	—	ns
4	SCK Duty Cycle	t_{SDC}	0.33 * t_{SCK}	0.66 * t_{SCK}	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCS*x* to $\overline{PCSS}$ time	t_{PCSC}	t_{SYS} * 2	t_{SYS} * 7	ns
8	$\overline{PCSS}$ to PCS*x* time	t_{PASC}	t_{SYS} * 2	t_{SYS} * 7	ns

Table 37. DSPI timing[1] [2] (continued)

Spec	Characteristic	Symbol	Peripheral Bus Freq: 132 MHz		Unit
			Min	Max	
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 20 4 6 20	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[8] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –3 7 12 –3	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 5 25 13 5	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –5 2.5 3 –5	 — — — —	 ns ns ns ns

1 DSPI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, and $T_A = T_L$ to T_H

2 Speed is the nominal maximum frequency of platform clock (f_{platf}). Max speed is the maximum speed allowed including frequency modulation (FM). 270 MHz parts allow for 264 Mhz for system core clock (f_{sys}) + 2% FM.

3 The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

6 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

7 For example, external master should start SCK clock not earlier than 3 system clock periods after assertion SS

8 This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

The DSPI in this device can be configured to serialize data to an external device that implements the Microsecond Bus protocol. DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) for data and clock signals to improve high speed operation.

Table 38. DSPI LVDS timing[1, 2]

Characteristic	Symbol	Min	Max	Unit
LVDS Clock to Data/Chip Select Outputs	$t_{LVDSDATA}$	–0.25 × t_{SCYC}	+0.25 × t_{SCYC}	ns

1 These are typical values that are estimated from simulation.

2 See DSPI LVDS Pad related data in Table 14.

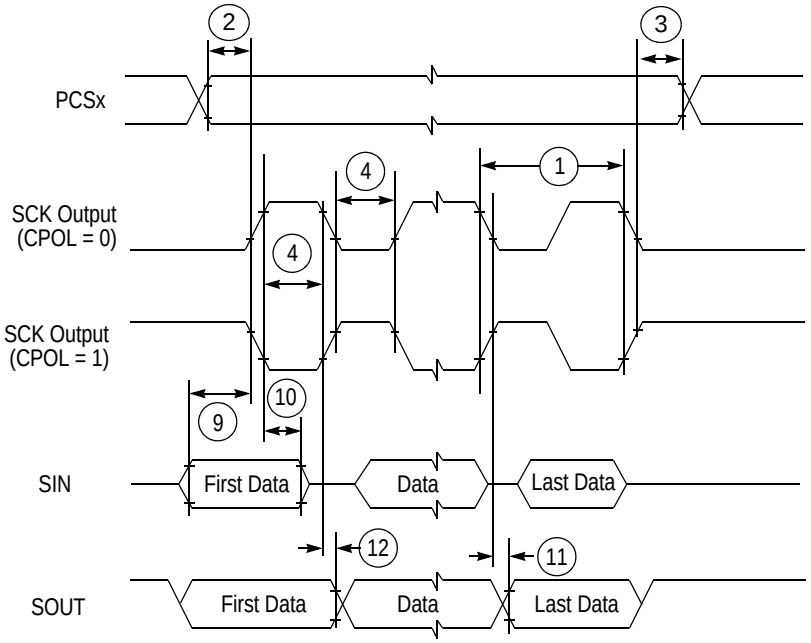


Figure 26. DSPI classic SPI timing — Master, CPHA = 0

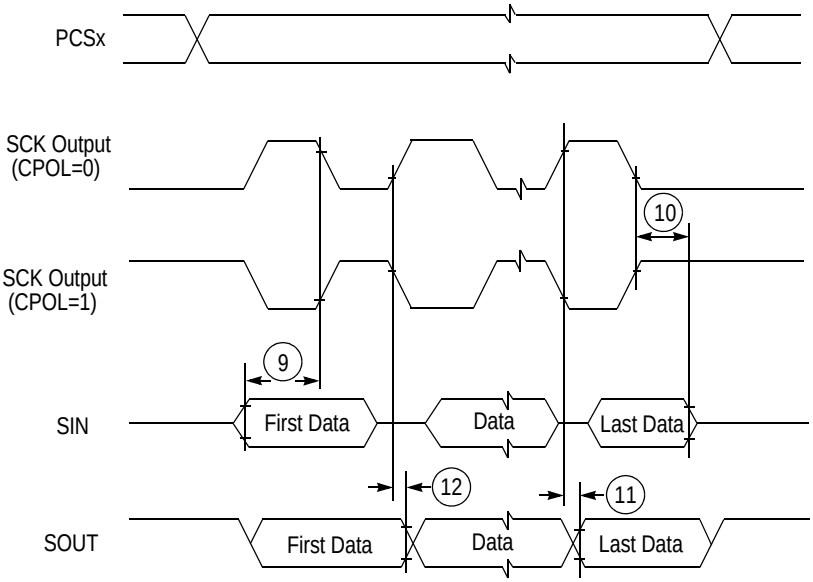


Figure 27. DSPI classic SPI timing — Master, CPHA = 1

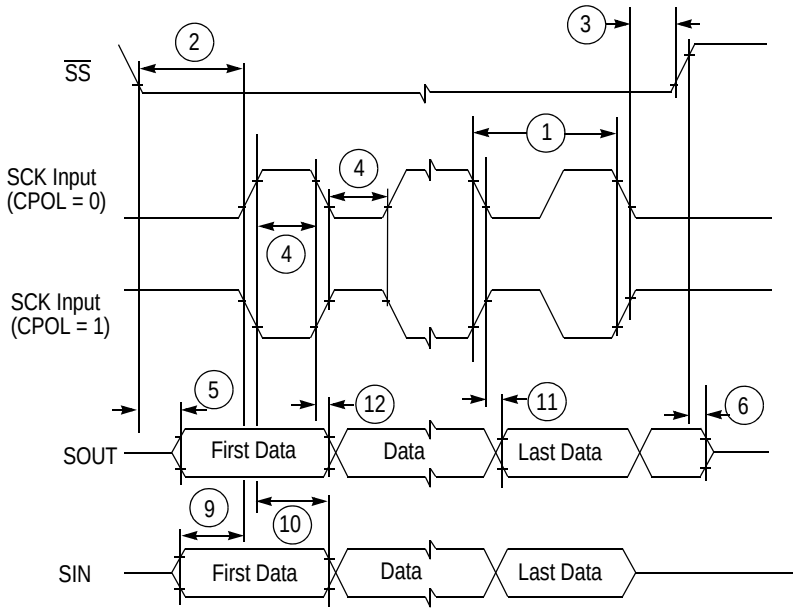


Figure 28. DSPI classic SPI timing — Slave, CPHA = 0

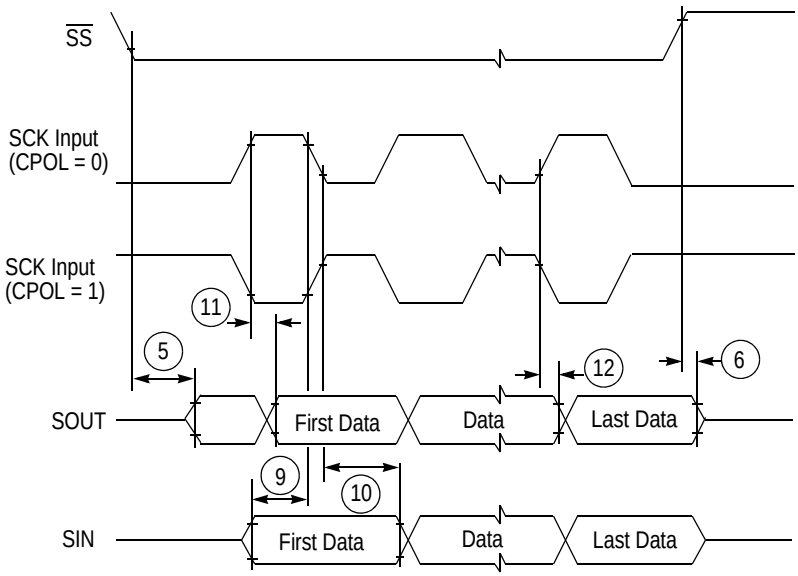


Figure 29. DSPI classic SPI timing — Slave, CPHA = 1

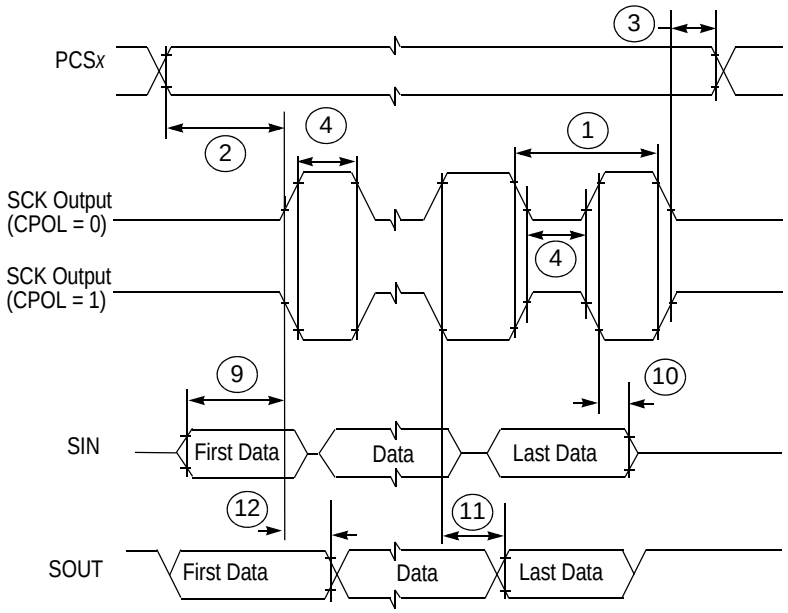


Figure 30. DSPI modified transfer format timing — Master, CPHA = 0

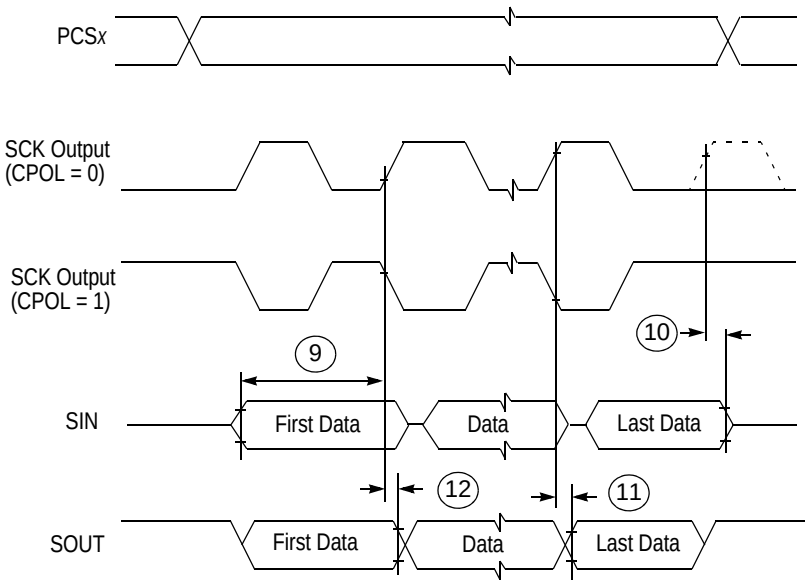


Figure 31. DSPI modified transfer format timing — Master, CPHA = 1

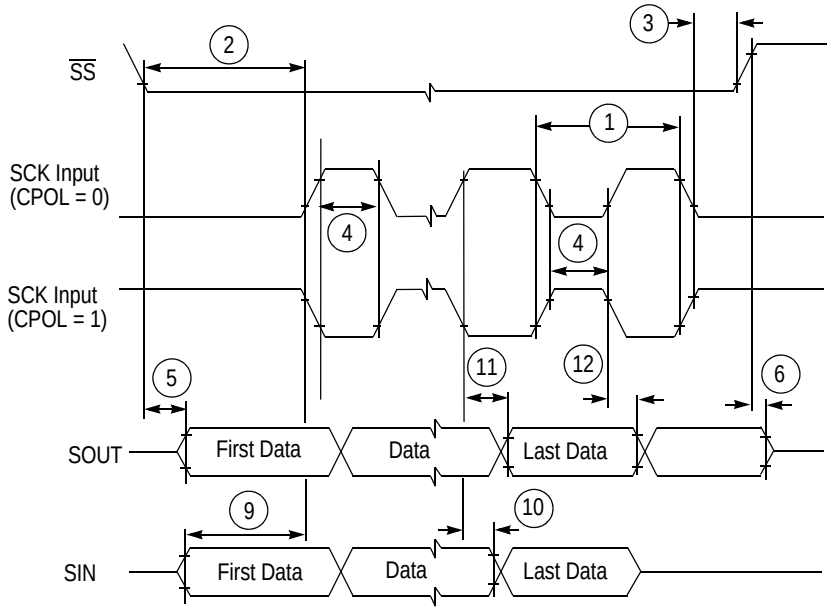


Figure 32. DSPI modified transfer format timing — Slave, CPHA = 0

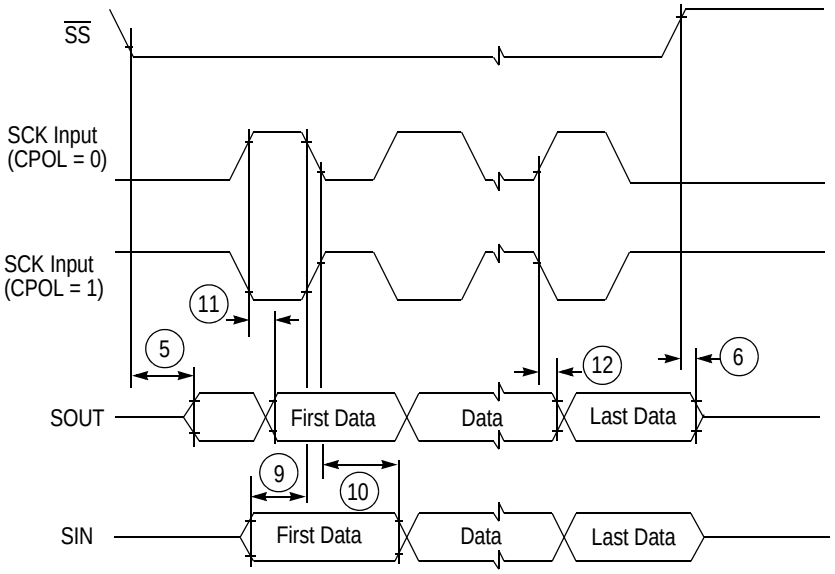


Figure 33. DSPI modified transfer format timing — Slave, CPHA = 1

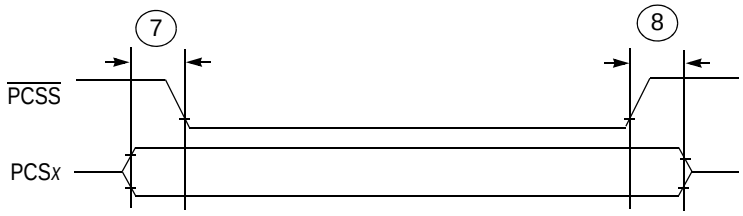
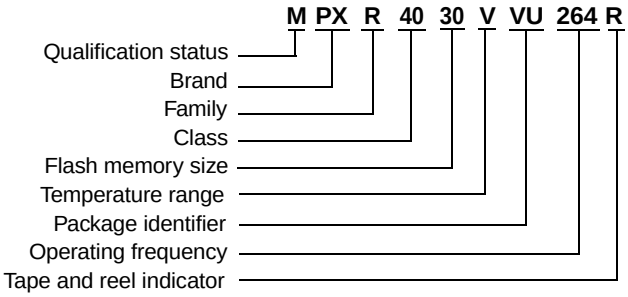


Figure 34. DSPI PCS strobe (PCSS) timing

6 Ordering information

6.1 Orderable parts

Figure 35 and Table 39 describe and list the orderable part numbers for the PXR40.



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Time Control
S = Safety

Flash Memory Size
30 = 3 MB
40 = 4 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
VU = 416 PBGA

Operating frequency
1 = 150 MHz
2 = 180 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 39 for more information.

Figure 35. PXR40 orderable part number description

Table 39. PXR40 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXR4030VVU264	3 MB / 192 KB	416 PBGA (27 mm x 27 mm)	264
MPXR4040VVU264	4 MB / 256 KB	416 PBGA (27 mm x 27 mm)	264

7 Package information

7.1 416-pin package

The package drawings of the 416-pin TEPBGA package are shown in Figure 36 and Figure 37.

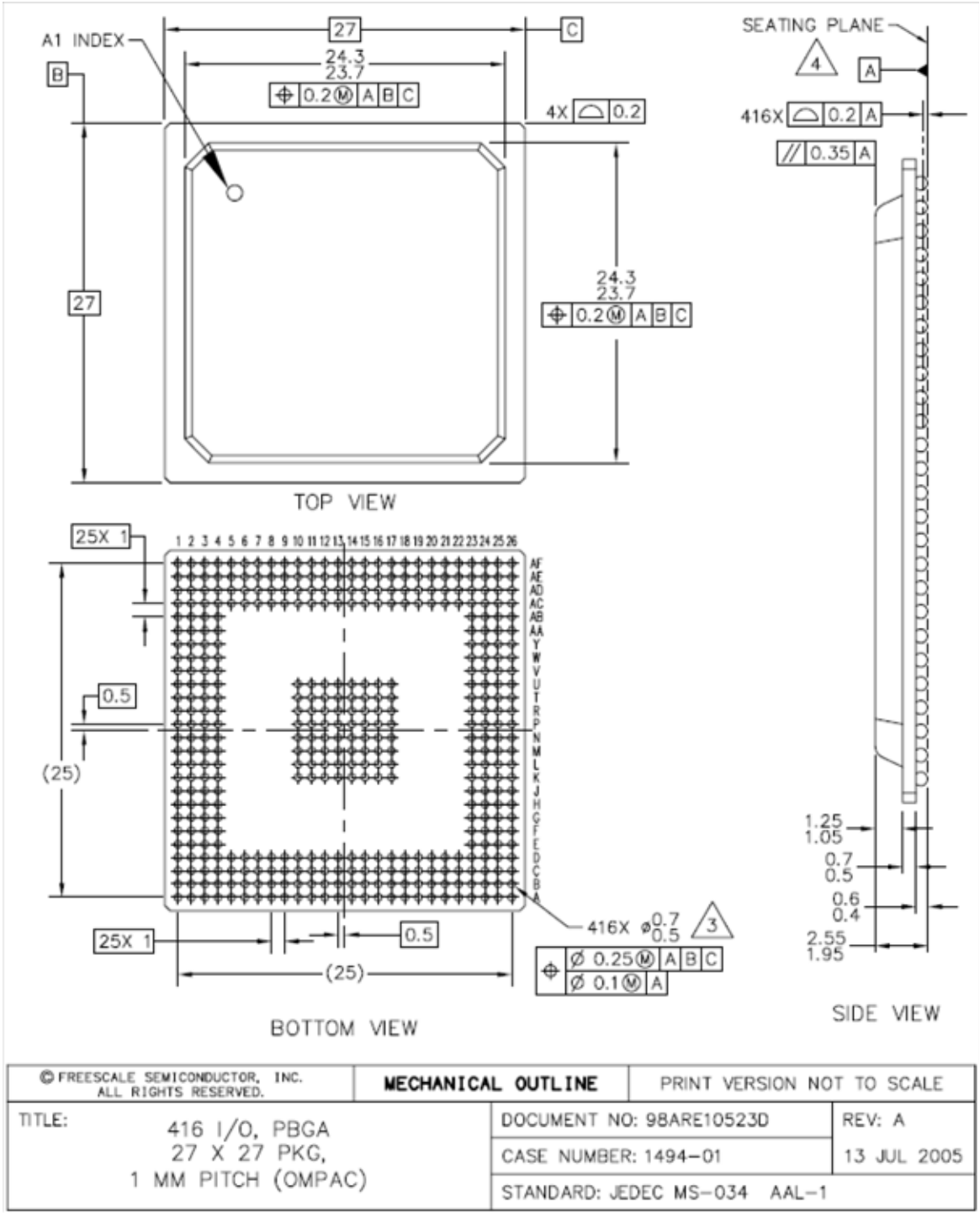


Figure 36. 416 TEPBGA package (1 of 2)

Figure 37. 416 TEPBGA package (2 of 2)

8 Product documentation

This data sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

The following documents are required for a complete description of the device and are necessary to design properly with the parts:

- *PXR40 Microprocessor Reference Manual* (document number PXR40RM).

9 Revision history

Table 40 describes the changes made to this document between revisions.

Table 40. Revision history

Revision	Date	Description of Changes
1	September 2011	Initial release: Technical Data

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