



**THE DATASHEET OF
A19530LUCC-FOOOOEJ-A**





High-Feature Three-Wire Hall-Effect Transmission Speed and Direction Sensor IC

FEATURES AND BENEFITS

- Integrated diagnostics and certified safety design process for ASIL B (pending assessment) compliance
- Three-wire output pulse-width protocol supporting speed, direction, and ASIL
- Advanced algorithms supporting vibration detection and sudden air gap changes
- Ring-magnet and ferrous-target sensing
- Air-gap-independent switch points
- True zero-speed operation
- Integrated electromagnetic-compatible (EMC) capacitor in a single overmolded miniature package
- Robust test coverage capability with scan path and quiescent power-supply current (IDDQ) measurement

DESCRIPTION

The A19530 is an optimized Hall-effect integrated circuit (IC) that provides a user-friendly solution for direction detection and true zero-speed digital magnetic-wheel or gear-tooth sensing. The small package can be easily assembled and used in conjunction with a wide variety of magnetic wheels or back-biased with a magnet for gear-tooth sensing applications.

The IC employs patented algorithms for the special operational requirements of automotive transmission applications. The speed and direction of the target are communicated through a variable pulse-width output protocol. The A19530 high vibration-immunity option prevents direction pulses from occurring under angular vibration without sacrificing maximum air-gap capability, whereas the option that does not have vibration immunity allows for continuous direction pulse emission under vibration. The advanced vibration-detection algorithm systematically calibrates the sensor IC based on the initial teeth of true target rotation, not based on the vibration, thereby always providing an accurate signal in running mode.

More-classic output options—such as speed-only protocol, representation of the target profile, or recognition of fast direction change, with reduced vibration immunity—also complete the programming panel of the A19530.

Advanced signal processing, innovative algorithms, short/open detection capability, and ASIL B-compliant (pending assessment) design make the A19530 an ideal solution for a wide range of speed and direction sensing needs with diagnostic requirements.

This device is available in a lead (Pb) free 3-pin SIP package with tin-plated leadframe.

PACKAGE:



3-pin SIP (suffix UC)

Not to scale

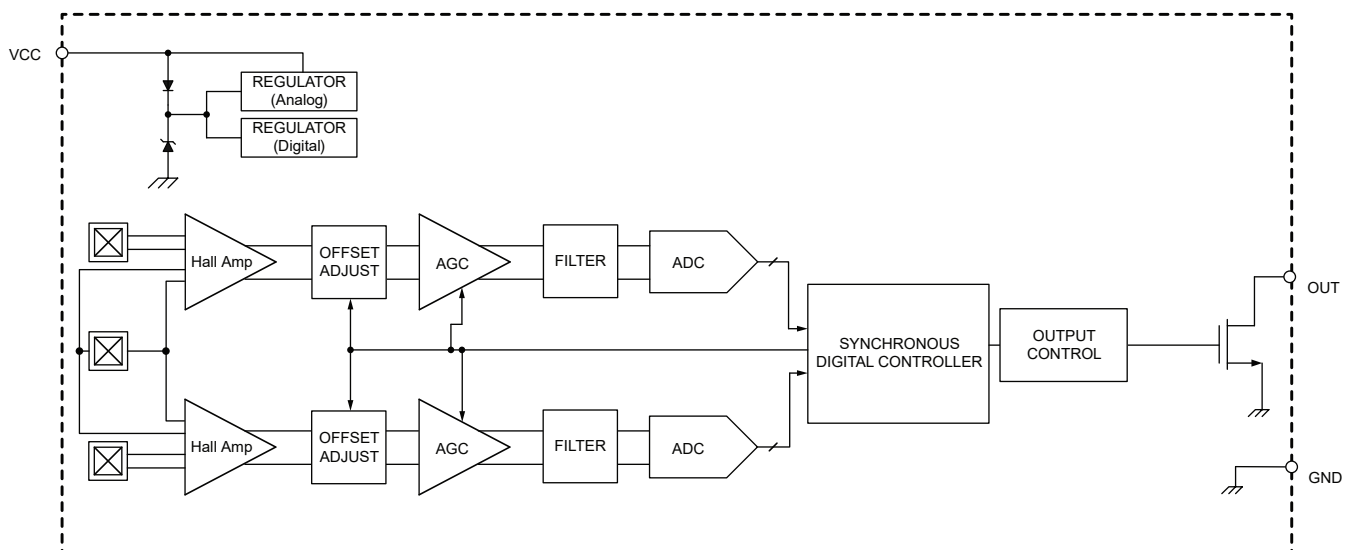


Figure 1: Functional Block Diagram

A19530

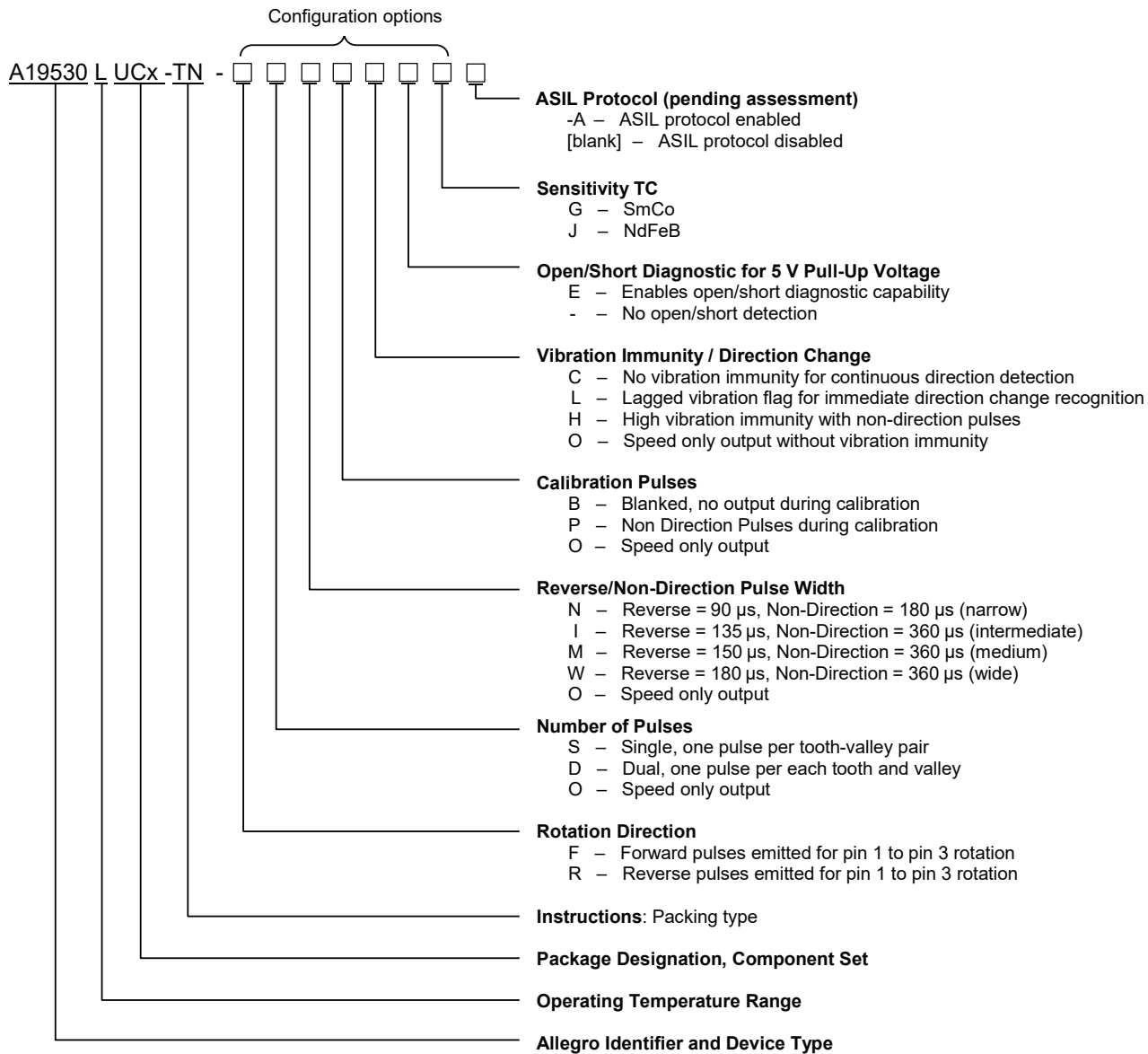
High-Feature Three-Wire Hall-Effect Transmission Speed and Direction Sensor IC

SELECTION GUIDE [1]

Part Number	Packing
A19530LUCCTN-FOOOOJ	Tape and reel, 13-in. reel, 4000 pieces per reel
A19530LUCCTN-RSIBCEJ	Tape and reel, 13-in. reel, 4000 pieces per reel



[1] Not all combinations are available. For availability and pricing of custom programming options, contact Allegro sales.



For example: A19530LUCCTN-RSNPHEJ

Where a configuration character is unspecified, "x" is used. For example, xSNPLEJ applies to both rotation-direction configuration variants.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to the Power Derating section	27	V
Reverse Supply Voltage	V_{RCC}		-18	V
Reverse Supply Current	I_{RCC}		50	mA
Reverse Output Voltage	V_{ROUT}		-0.5	V
Output Sink Current	I_{OUT}	Open/Short detection disabled	25	mA
Operating Ambient Temperature	T_A		-40 to 150	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		-65 to 170	°C

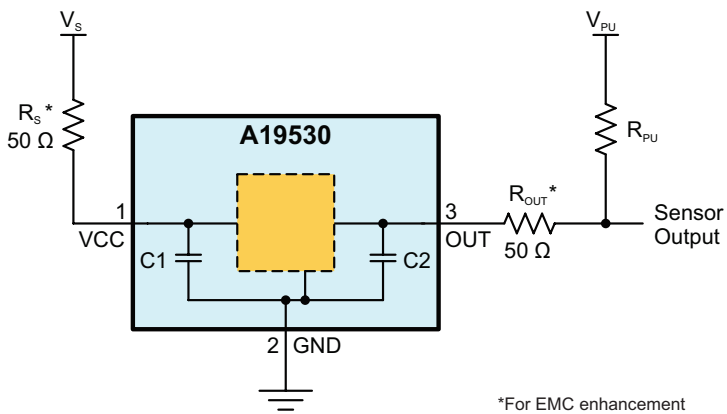
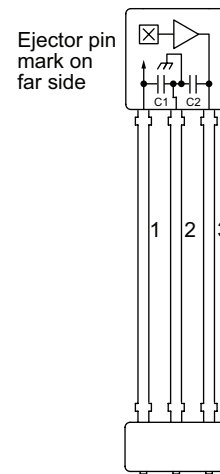


Figure 2: Typical Application Circuit

NOTE: For -xxxxxEx- option (open/short detection enabled), the pull-up resistor value is as noted in the Operating Characteristics table.

Pinout Diagram



INTERNAL DISCRETE COMPONENT RATINGS

Symbol	Characteristic	Rating	Unit
C1 (C_{SUPPLY})	Nominal Capacitance	220	nF
C2 (C_{OUT})	Nominal Capacitance	4.7	nF

Terminal List

Number	Name	Function
1	VCC	Supply voltage
2	GND	Ground
3	OUT	Open drain output

OPERATING CHARACTERISTICS: Valid through full operating and temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit	
ELECTRICAL CHARACTERISTICS							
Supply Voltage [2]	V_{CC}	Operating; $T_J < T_{J(max)}$, $R_{SUPPLY} = 0 \Omega$	4	–	24	V	
Undervoltage Lockout	$V_{CC(UV)}$	$V_{CC} 0 \rightarrow 5 V$ or $5 \rightarrow 0 V$, $R_{SUPPLY} = 0 \Omega$	–	–	3.95	V	
Reverse Supply Current	I_{RCC}	$V_{CC} = V_{RCC(MAX)}$	–10	–	0	mA	
Supply Zener Clamp Voltage	$V_{Zsupply}$	$I_{CC} = I_{CC(MAX)} + 3 mA$, $T_A = 25^\circ C$, $R_{SUPPLY} = 0 \Omega$	27	–	–	V	
Supply Zener Current	I_Z	$T_J < T_{J(max)}$, $V_{CC} = 27 V$	–	–	13	mA	
Supply Current	I_{CC}		–	8	10	mA	
OUTPUT STAGE							
Power-On State	POS	Connected as in Figure 2		High		–	
Low Output Voltage	$V_{diag-Low}$	4.75 V < V_{PU} < 5.25 V, Output = Low, 1.45 k Ω \leq R_{PU} \leq 3.4 k Ω at sensor output in Figure 2	-xxxxxEx variants, $R_{OUT} = 0 \Omega$	435	875	1115	mV
			-xxxxxEx variants, $R_{OUT} = 50 \Omega$	500	875	1250	mV
Low Output Voltage Impedance	$Z_{Sat-Low}$	$I_{SINK} = 10 mA$, Output transistor ON, $R_{OUT} = 0 \Omega$	Open/short disabled	–	–	50	Ω
High Output Voltage	$V_{diag-High}$	4.75 V < V_{PU} < 5.25 V, Output = High, 1.45 k Ω \leq R_{PU} \leq 3.4 k Ω at sensor output in Figure 2	-xxxxxEx variants, $R_{OUT} = 0 \Omega$	3735	4125	4475	mV
			-xxxxxEx variants, $R_{OUT} = 50 \Omega$	3750	4125	4500	mV
Output Leakage Current	I_{OFF}	Output transistor OFF, $V_{OUT} = 24 V$	Open/Short disabled	–	–	10	μA
Output Zener Clamp Voltage	V_{ZOUT}	$I_{OUT} = 3 mA$, $T_A = 25^\circ C$	27	–	–	V	
Output Current Limit	I_{LIM}	$V_{OUT} = 12 V$, $T_J < T_{J(max)}$	25	45	70	mA	
Output Rise Time	$t_{r(out-diag-ON)}$	$R_{PU} = 1.5 k\Omega$, $V_{PU} = 5 V$, from 10% to 90%, $R_{OUT} = 0 \Omega$	-xxxxxEx variants	–	15	–	μs
		$R_{PU} = 3.3 k\Omega$, $V_{PU} = 5 V$, from 10% to 90%, $R_{OUT} = 0 \Omega$	-xxxxxEx variants	–	35	–	μs
Output Fall Time	t_f	$R_{PU} = 1.5 k\Omega$, $V_{PU} = 5 V$, from 90% to 10%, $R_{OUT} = 0 \Omega$	-xxxxxEx variants	1.5	–	4.5	μs
			Open/short disabled	0.5	–	2.5	μs
		$R_{PU} = 3.3 k\Omega$, $V_{PU} = 5 V$, from 90% to 10%, $R_{OUT} = 0 \Omega$	-xxxxxEx variants	–	2.5	–	μs
			Open/short disabled	–	1.5	–	μs
OUTPUT PULSE CHARACTERISTICS [3]							
Pulse Width, Forward Rotation	$t_{w(FWD)}$			38	45	52	μs
Pulse Width, Reverse Rotation	$t_{w(REV)}$	Timing from start of falling output transition to start of rising output transition.	-xxNxxxx variants	76	90	104	μs
			-xxLxxxx variants	114	135	156	μs
			-xxMxxxx variants	127	150	173	μs
Pulse Width, Non-Direction	$t_{w(ND)}$	Measured pulse width depends on circuit configuration and thresholds.	-xxWxxxx variants	153	180	207	μs
			-xxNPxxx variants	153	180	207	μs
			-xxIPxxx variants, -xxMPxxx variants, -xxWPxxx variants	306	360	414	μs

[1] Typical values are at $T_A = 25^\circ C$ and $V_{CC} = 12 V$. Performance may vary for individual units, within the specified maximum and minimum limits.

[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see the Power Derating section.

[3] Only applicable to direction detection options, S (single) and D (dual).

OPERATING CHARACTERISTICS (continued): Valid through full operating and temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit	
PERFORMANCE CHARACTERISTICS							
Operate Point	B _{OP}	% peak to peak	–	69	–	%	
Release Point	B _{RP}	% peak to peak	–	31	–	%	
Switch Point Separation	B _{DIFF(SP-SEP)}	Minimum separation between channels as a percentage of signal amplitude at each switching point; refer to Figure 5	20	–	–	%	
Differential Input Signal Frequency, Forward Rotation [4]	f _{FWD}	-xSxxxx and -xOxxxx variants	0	–	12	kHz	
		-xDxxxx variants	0	–	6	kHz	
Differential Input Signal Frequency, Reverse Rotation [4]	f _{REV}	-xSNxxxx variants	0	–	7	kHz	
		-xDNxxxx variants	0	–	3.5	kHz	
		-xSWxxxx variants	0	–	4	kHz	
		-xDWxxxx variants	0	–	2	kHz	
Differential Input Signal Frequency, Non-Direction [4]	f _{ND}	-xSxPHxx and -xSxPLxx variants	0	–	2.2	kHz	
		-xDxPHxx and -xDxPLxx variants	0	–	1.1	kHz	
TEMPERATURE COEFFICIENT							
Sensitivity Temperature Coefficient (TC)	T _C	-xxxxxG variants	–	0.04	–	%/°C	
		-xxxxxJ variants	–	0.13	–	%/°C	
POWER-ON AND CALIBRATION							
Power-On Time	t _{PO}	f _{OP} < 100 Hz	–	–	2	ms	
First Direction Output Pulse [6]		Amount of target rotation (constant direction) following power-on until first electrical output pulse of either t _{w(FWD)} or t _{w(REV)} ; Refer to Figure 3	-xxxxCxx variants	–	1.5	< 2.5	T _{CYCLE}
			-xxxxLxx variants, -xxxxHxx variants; B _{DIFF(pk-pk)} > 60 G, B _{DIFF(pk-pk)} ≤ 1500 G	–	2	< 3.1	T _{CYCLE}
			-xxxxLxx variants, -xxxxHxx variants; 30 G ≤ B _{DIFF(pk-pk)} , B _{DIFF(pk-pk)} ≤ 60 G	–	2.5	< 4	T _{CYCLE}
First Direction Pulse Output Following Direction Change	N _{CD}	Amount of target rotation (constant direction) following event until first electrical output pulse of either t _{w(FWD)} or t _{w(REV)} ; refer to Figure 3	-xxxxCxx variants, -xxxxLxx variants	–	1	< 1.5	T _{CYCLE}
			-xxxxHxx variants	1	2	< 3	T _{CYCLE}
First Direction Pulse Output Following Running Mode Vibration		Amount of target rotation (constant direction) following event until first electrical output pulse of either t _{w(FWD)} or t _{w(REV)} ; refer to Figure 3	-xxxxCxx variants	–	1	< 2.5	T _{CYCLE}
			-xxxxLxx variants, -xxxxHxx variants	1	2	< 3.5	T _{CYCLE}

[4] Maximum operating frequency specified for output rise time t_r < 17 μs. Parameter determined by satisfactory separation of output pulses t_w. If end-user can resolve smaller time between pulses with faster rise time, maximum frequency may be increased up to 12 kHz.

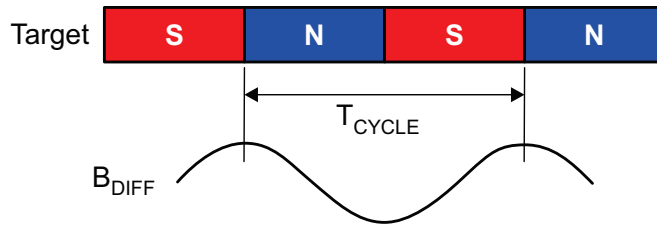
[5] Power-on time includes the time required to complete the internal automatic offset adjust. The part is then ready for peak acquisition.

[6] Power-on frequency < 200 Hz. Higher power-on frequencies may require more input magnetic cycles until directional output pulses are achieved.

OPERATING CHARACTERISTICS (continued): Valid through full operating and temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit	
MAGNETIC CHARACTERISTICS							
Differential Input Signal Range [7]	$B_{DIFF(pk-pk)}$	Differential magnetic signal	30	–	1500	G	
Allowable User-Induced Offset		Magnitude valid on differential magnetic channels	-xxxxCxx variants, -xxxxLxx variants, -xxxxHxx variants	–200	–	200	G
			-xOOOOxx variants	–300	–	300	G
Allowable Differential Sequential Signal Variation	$B_{SEQ(n+1)} / B_{SEQ(n)}$	Single cycle-to-cycle variation, $B_{SEQ(n+1)} / B_{SEQ(n)}$; no missed pulses (pulse variants), nor missed edges (-xOOOOxx variants); refer to Figure 4	0.6	–	–	–	
Allowable Differential Sequential Signal Variation		Single cycle-to-cycle variation, $B_{SEQ(n+1)} / B_{SEQ(n)}$; pulses count error but device can recover (pulse variants) and possible missed edges but no flatline (-xOOOOxx variants); refer to Figure 4	0.35	–	–	–	
VIBRATION IMMUNITY							
Vibration Immunity (Calibration)	$Err_{Vib(SU)}$	-xxxxCxx variants	0.5	1.0	–	T_{CYCLE}	
		-xxxxLxx and -xxxxHxx variants	1	–	–	T_{CYCLE}	
Vibration Immunity (Running Mode)	$Err_{Vib(RM)}$	-xxxxCxx variants	–	none	–	T_{CYCLE}	
		-xxxxLxx and -xxxxHxx variants	1	–	–	T_{CYCLE}	
ASIL OUTPUT							
ASIL Output Safe State	$V_{ASIL_safe_low}$	Internal failure detected for $4.75\text{ V} < V_{PU} < 5.25\text{ V}$, $R_{OUT} = 0\ \Omega$, $1.45\text{ k}\Omega \leq R_{PU} \leq 3.4\text{ k}\Omega$, at sensor output in Figure 2	-xxxxEx variants	–	–	180	mV
Time In Safe State Before Self-Reset	$t_w(ASIL_safe)$	Connected as in Figure 2	-xxxxEx variants	–	5	–	ms

[7] Differential magnetic field is measured for Channel A (F1-F2) and Channel B (F2-F3) for pulse-width variants and for Channel A' (F1-F3) for speed-only variants (-xOOOOxx variants). Magnetic field is measured orthogonally to the front of the package. Refer to Figure 7 and the Package Outline Drawing section.



B_{DIFF} = Differential Input Signal; the differential magnetic flux sensed by the sensor

T_{CYCLE} = Target Cycle; the amount of rotation that moves one tooth (or north pole) and one valley (or south pole) across the sensor

Figure 3: Definition of T_{CYCLE}

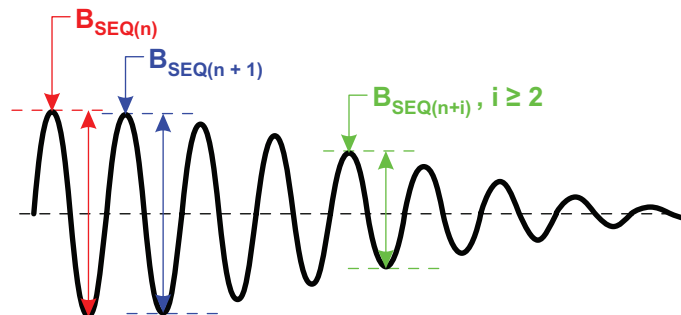


Figure 4: Differential Signal Variation

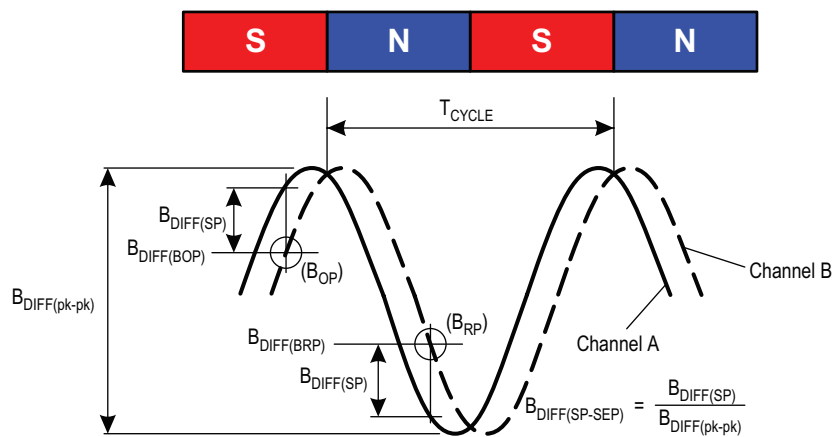


Figure 5: Definition of Switch-Point Separation

FUNCTIONAL DESCRIPTION

Sensing Technology

The sensor IC contains a single-chip Hall-effect circuit that supports a trio of Hall elements. These are used in differential pairs to provide electrical signals containing data regarding edge position and direction of target rotation. The A19530 is intended for use with magnetic trigger wheels or ferromagnetic targets if back-biased with a magnet.

After proper power is applied to the sensor IC, it is capable of providing digital data that is representative of the magnetic features of a rotating target. The waveform diagrams in Figure 7 present the automatic translation of the target profiles, through their induced magnetic profiles, to the digital output signal of the sensor IC.

Direction Detection

The sensor IC compares the relative phase of its two differential channels to determine in which direction the target is moving. The relative switching order is used to determine the direction, which is communicated through the output protocol.

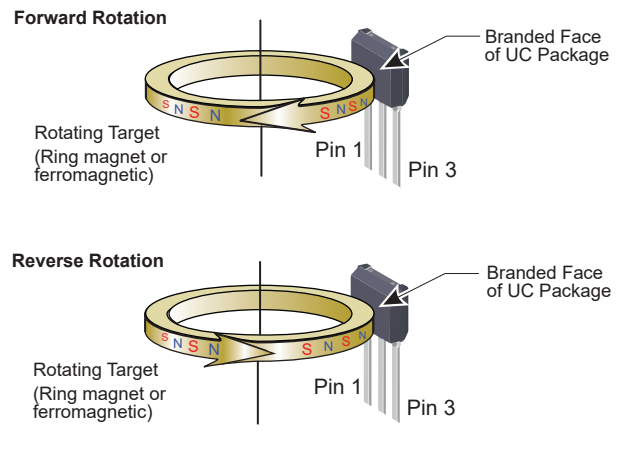
Data Protocol Description

When a target passes in front of the device (opposite the branded face of the package case), the A19530 generates an output pulse for each pole-pair of the target (-xSxxxxx variants). Speed data is provided by the output pulse rate, while direction of target rotation is provided by the duration of the output pulses. The sensor IC can sense target movement in both the forward and reverse directions.

Forward Rotation (see top panel in Figure 6): When the target is rotating such that a tooth near the sensor IC (of -Fxxxxxx variants) passes from pin 1 to pin 3, this is referred to as forward rotation. This direction is the opposite for the -Rxxxxxx variants. Forward rotation is indicated by output pulse widths of $t_{w(FWD)}$ (45 μ s typical).

Reverse Rotation (see bottom Figure 6): When the target is rotating such that a tooth passes from pin 3 to pin 1, it is referred to as reverse rotation for the -Fxxxxxx variants. Reverse rotation is indicated by output pulse widths of $t_{w(REV)}$ (90 μ s typical for -xxNxxxx variants, or 180 μ s typical for -xxWxxxx variants).

Speed-Only Protocol: When the A19530 is configured with a -xOOOOxx variant, the device directly outputs the digital representation of the target from the master differential channel (Channel A' in Figure 7). Changing magnetic polarity (north versus south) inverts the output polarity in the same way as it would if an -FOOOOxx variant were used instead of an -ROOOOxx variant.



**Figure 6: Target Rotation for -Fxxxxxx Variants;
-Rxxxxxx Variants Invert Detected Direction of Rotation**

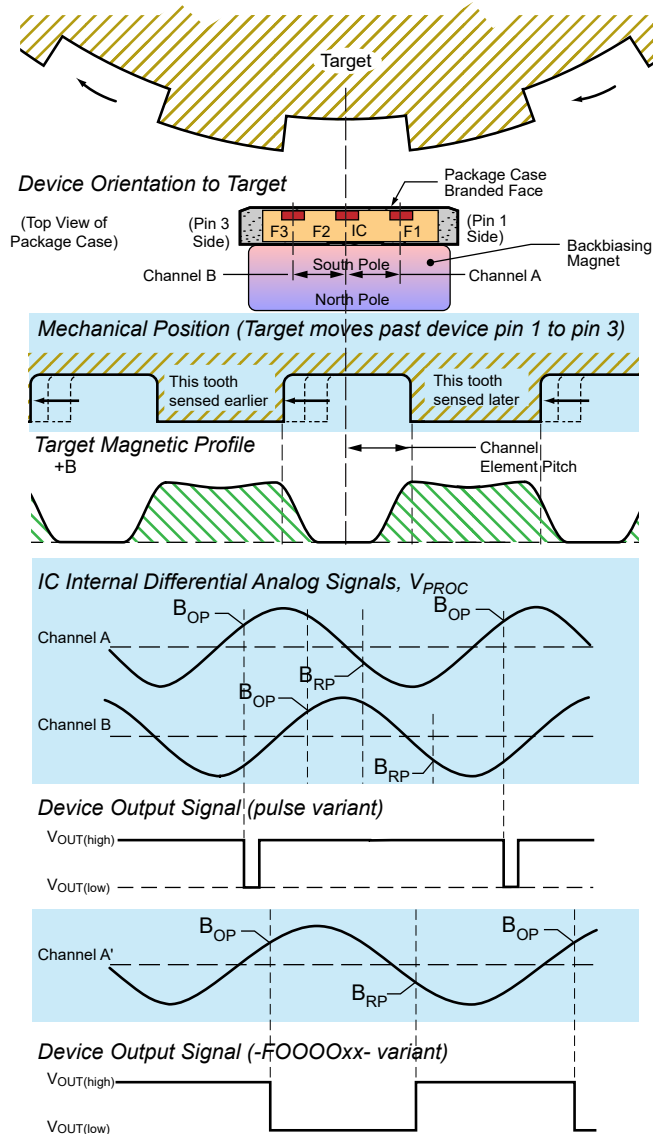
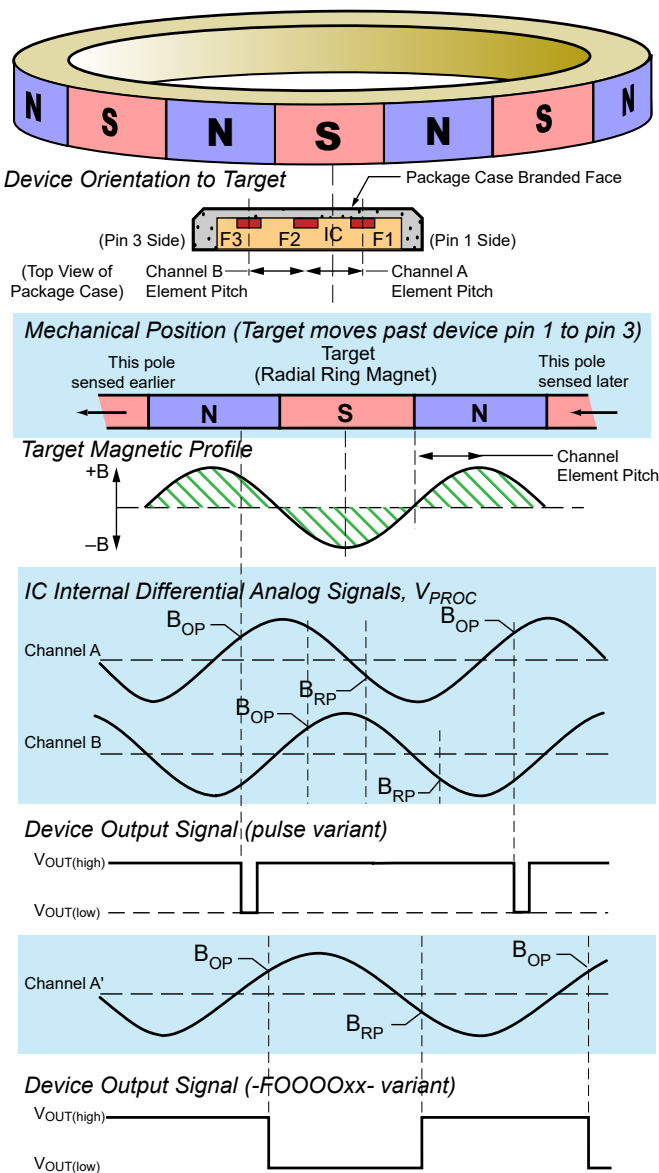


Figure 7: Magnetic Profile Reflects Target Features, Allowing Sensor IC to Present an Accurate Digital Output

Timing

In speed-only mode with forward direction (-FOOOOxx option), the rising electrical edge occurs slightly before the sensed magnetic edge traverses the package branded face (Figure 8).

In pulse output protocol with forward direction (-FSxxLxx and -FSxxHxx variants), the pulse appears at the output slightly before the sensed magnetic edge traverses the package branded face. This is true in both forward and reverse target rotation direction, but it must be noted that the magnetic edge is opposite in reverse direction (Figure 9).

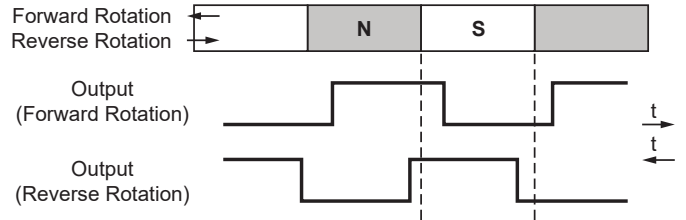
With the -xxxxCxx variants, the sensed mechanical edge that stimulates output pulses is kept the same for both forward and reverse rotation, resulting in the pulse being on same pole in forward and reverse rotation (Figure 10). It must also be noted that, in this mode, the pulse location may be different depending on the power-up cycle conditions.

Direction Validation

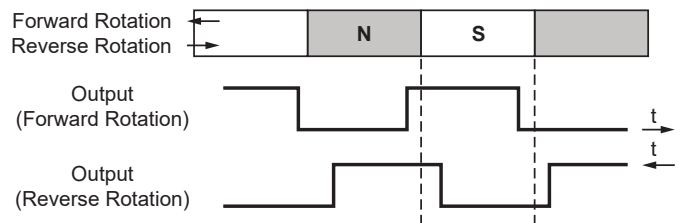
For the -xxxxLxx and -xxxxCxx variants, following a direction change in running mode, direction changes are immediately transmitted to the output (Figure 11 and Figure 12).

For the -xxxxHxx variants, following a direction change in running mode, output pulses have a width of $t_{w(ND)}$ until direction data is validated (Figure 13).

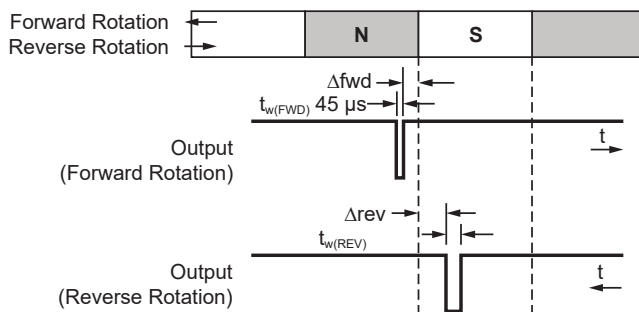
For the -xOOOOxx option, output transitions are emitted directly after a direction-change event.



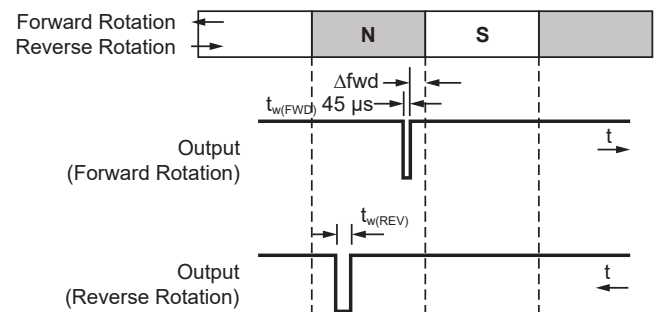
**Figure 8a: Output Protocol
(-FOOOOxx Variants)**



**Figure 8b: Output Protocol
(-ROOOOxx Variants)**



**Figure 9: Output Protocol
(-FSxxLxx and -FSxxHxx Variants)**



**Figure 10: Output Protocol
(-FSxxCxx Variants)**

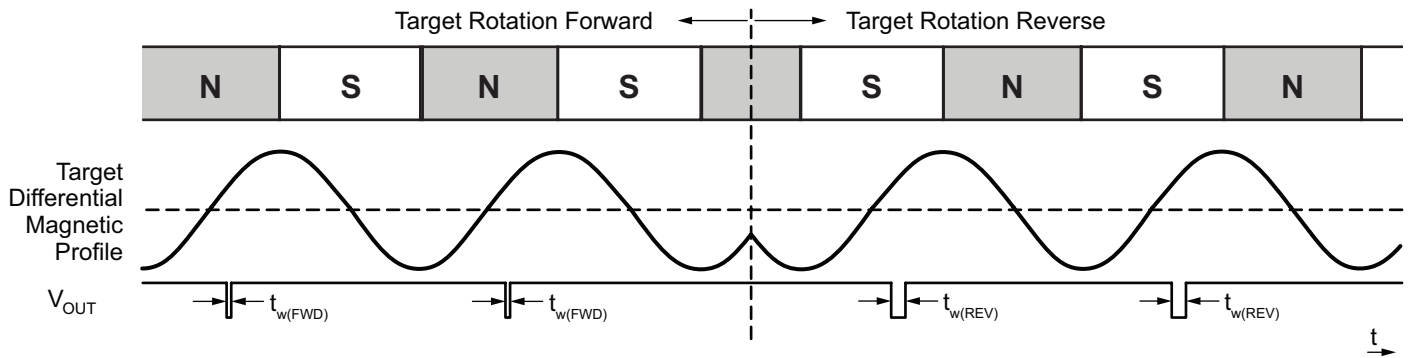


Figure 11: Example of Running Mode Direction Change
(-FSxxLxx Variants)

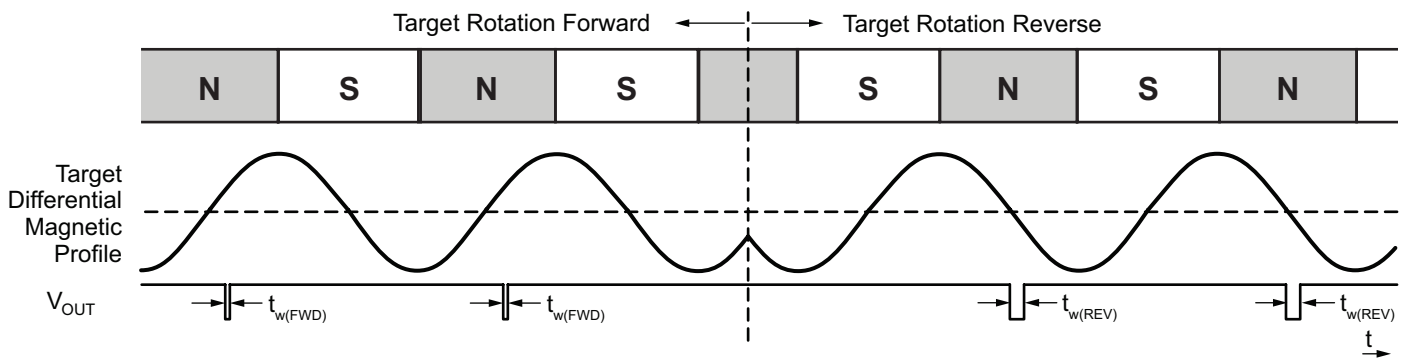


Figure 12: Example of Running Mode Direction Change
(-FSxxCxx Variants)

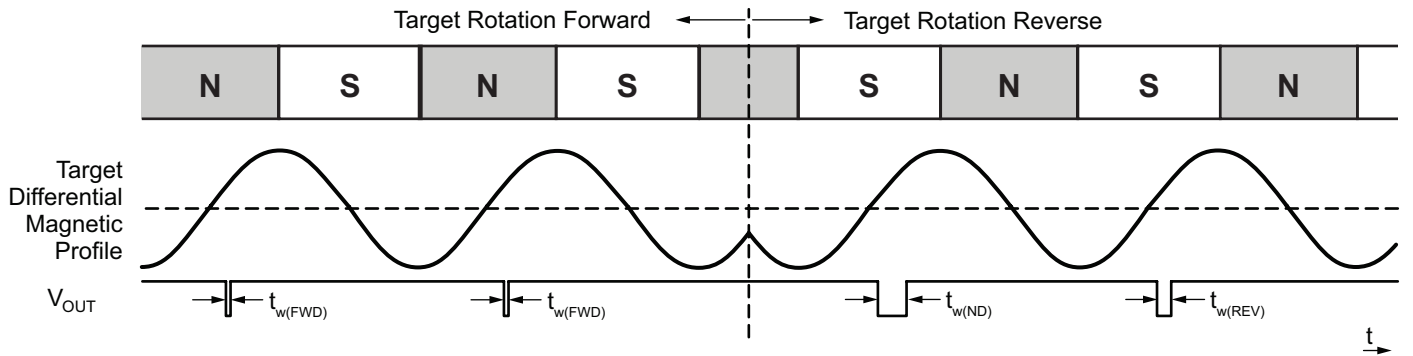


Figure 13: Example of Running Mode Direction Change
(-FSxxHxx Variants)

Start-Up Detection/Calibration

When power is applied to the A19530, the sensor IC internally detects the profile of the target. The gain and offset of the detected signals are adjusted during the calibration period, normalizing the internal signal amplitude for the air-gap range of the device.

The automatic gain control (AGC) feature ensures that operational characteristics are isolated from the effects of installation air-gap variation.

Automatic offset adjustment (AOA) is circuitry that compensates for the effects of chip, magnet, and installation offsets. This cir-

cuitry works with the AGC during calibration to adjust the signal to the analog-to-digital input range and allow for acquisition of signal peaks. AOA and AGC function separately on the two differential signal channels.

Direction data is available after calibration is complete.

For the -xxxBxxx variants, the output becomes active at the end of calibration. For the -xxxPxxx variants, output pulses of $t_w(ND)$ are supplied during calibration.

Figure 14 through Figure 16 show where the first output edge may occur for various starting target phases.

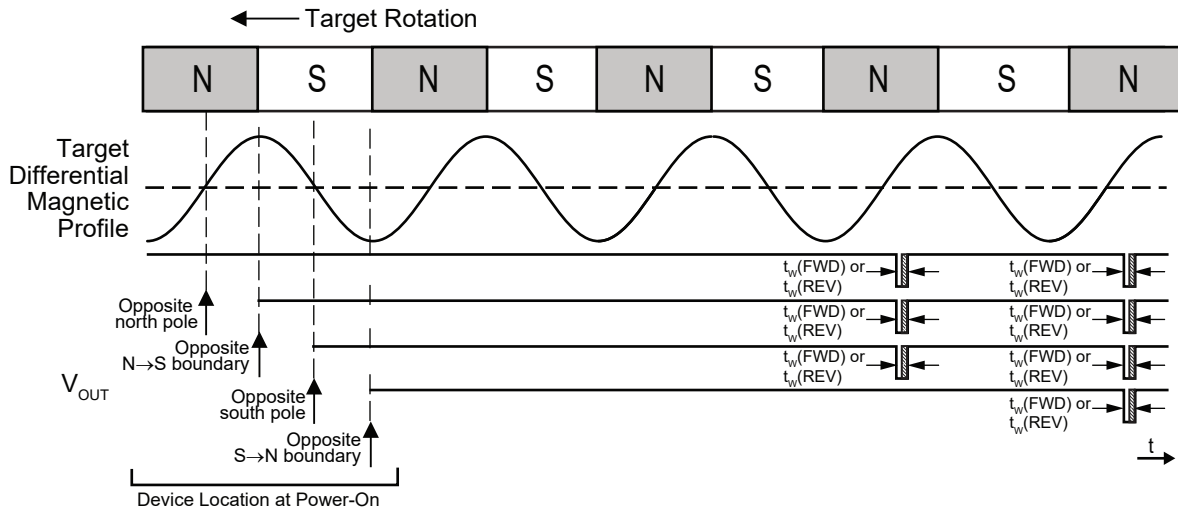


Figure 14: Start-Up Position Effect on First Device Output Switching (-xxxBHxx or -xxxBLxx Variants)

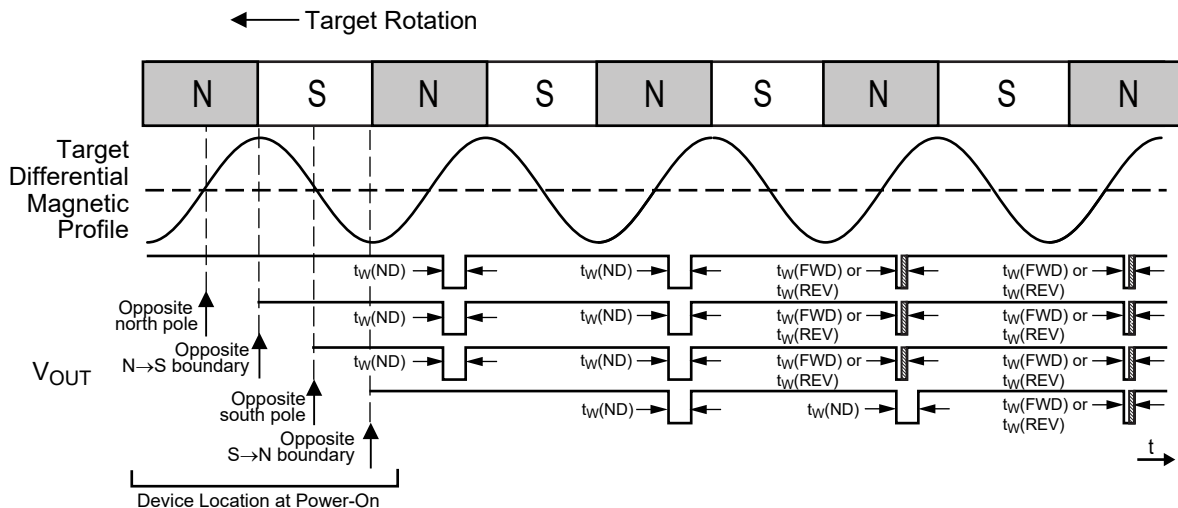


Figure 15: Start-Up Position Effect on First Device Output Switching (-xxxPHxx or -xxxPLxx Variants)

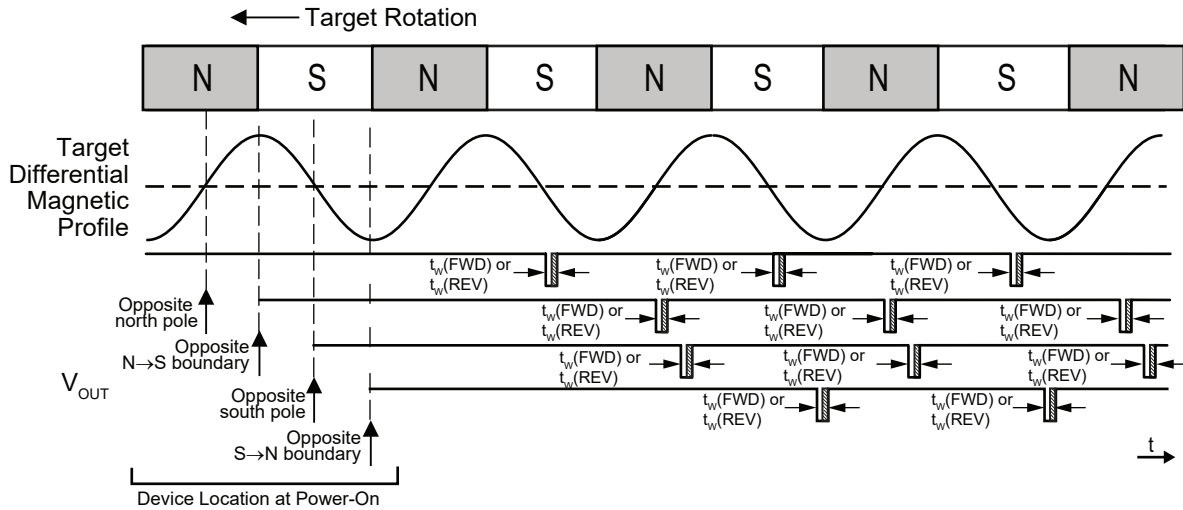


Figure 16: Start-Up Position Effect on First Device Output Switching (-xxxBCxx Variants)

Vibration Detection

Algorithms embedded in the IC's digital controller detect the presence of target vibration through analysis of the two magnetic input channels.

For the -xxxxCxx variants, vibration-detection algorithms are activated in calibration only. Once the device exits calibration, vibration-detection algorithms are deactivated, and any direction change or vibration event is transmitted through the output with continuous direction data.

For the -xxxxLxx variants, any direction change post-calibration is immediately transmitted to the output; and, if any subsequent

vibration occurs, the output is blanked and output pulses are not emitted for vibrations less than the specified vibration immunity. Output pulses containing the proper direction data resume once the direction data has been validated, upon constant target rotation.

For the -xxxxHxx variants, in the presence of vibration, output pulses of $t_{w(ND)}$ may occur or pulses may not occur, depending on the amplitude and phase of the vibration. Output pulses have a width of $t_{w(ND)}$ until direction data is validated, upon constant target rotation.

For the -xOOOOxx variants, in the presence of vibration, output transitions representing the target vibration profile may occur.

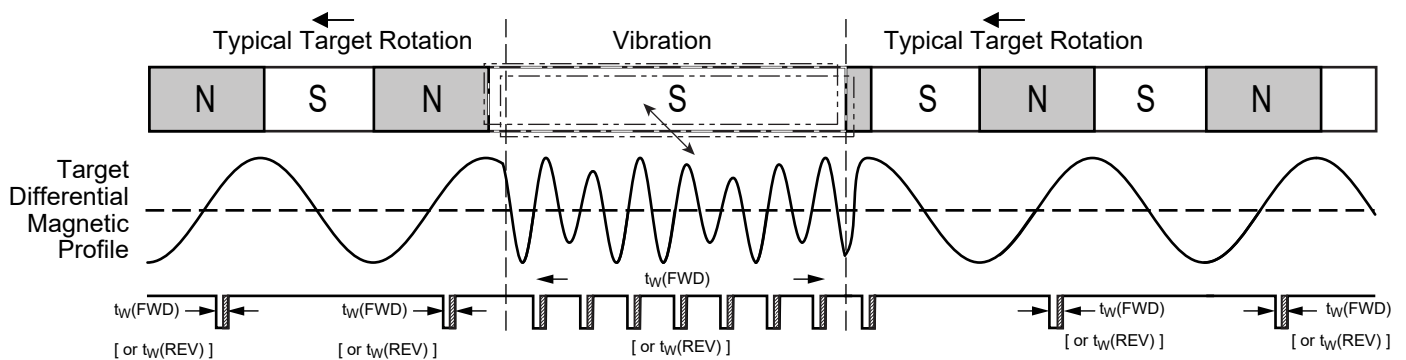


Figure 17: Output Functionality in Presence of Running Mode Target Vibration (-xxxBCxx Variants)

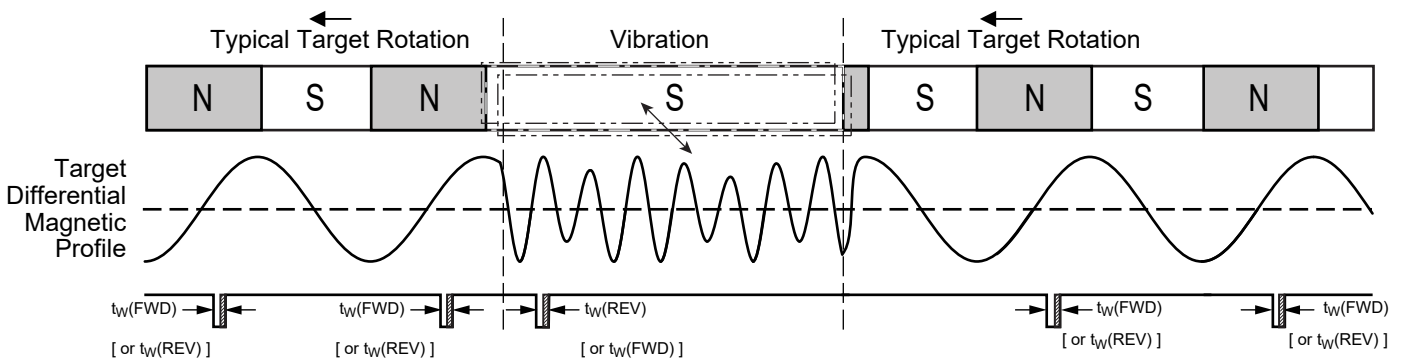


Figure 18: Output Functionality in Presence of Running Mode Target Vibration (-xxxBLxx Variants)

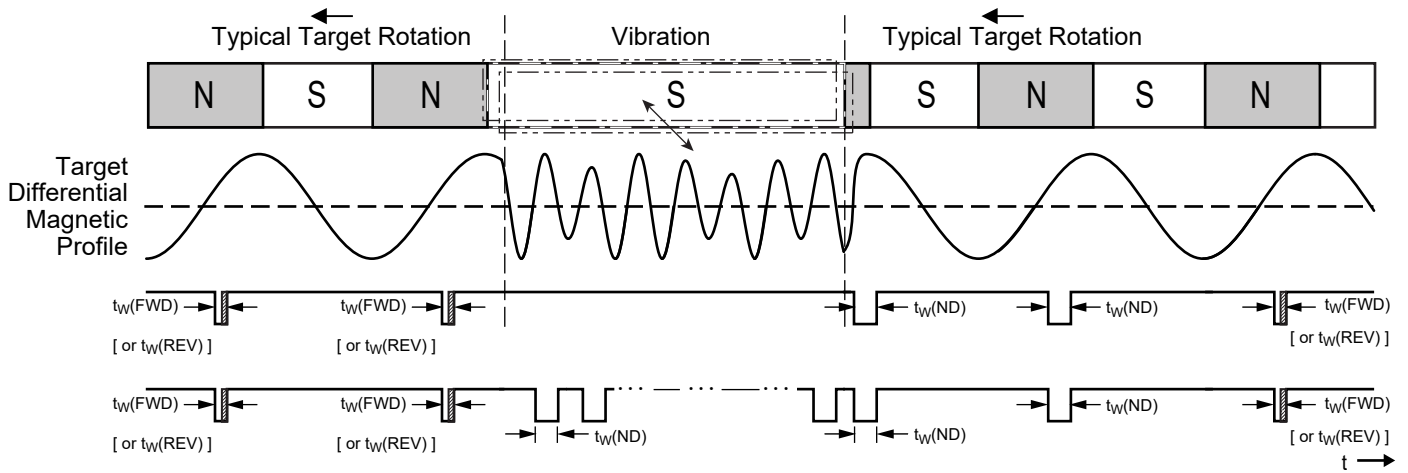


Figure 19: Output Functionality in Presence of Running Mode Target Vibration (-xxxPHxx Variants)

Diagnostic Capability

When diagnostic functionality is activated, the device continuously monitors itself, from the signal chain to output levels, and reports a fault by driving the output to the safe state (low level) for a period of time defined by $t_{w(ASIL_safe)}$. After this period of time, the device attempts to recover by self-reset. In case of permanent detectable failure, the sequence is repeated indefinitely (see Figure 20).

The diagnostic option of A19530 allows for system failure detection, such as a short circuit or open wire. In such case, the output transitions to a voltage less than or greater than the typical operating voltage range ($V_{diag-Low}$ to $V_{diag-High}$) depending on the failure mode.

The possible output states corresponding to each short or open-wire event are summarized in Table 1.

Table 1: Output Open-Short Diagnostic

External Event Type	Output Level
Hard short between VCC and GND	V_{PU}
Hard short between VCC and OUT	V_{CC}
Hard short between OUT and GND	GND
Open VCC	V_{PU}
Open OUT	V_{PU}
Open GND	V_{PU}

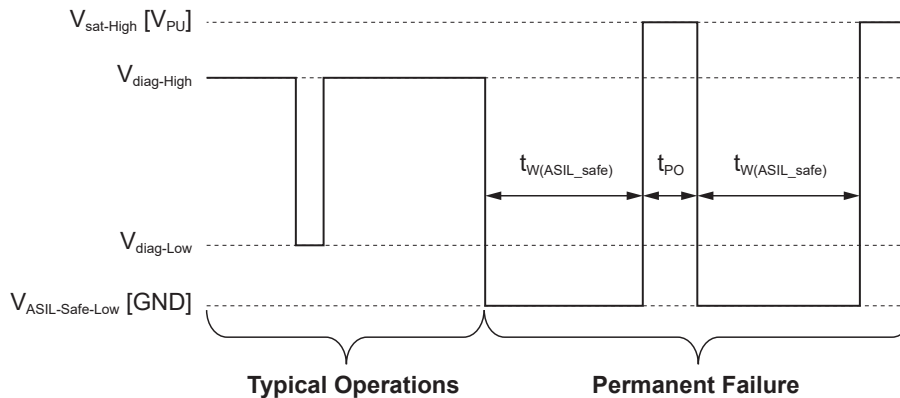


Figure 20: ASIL Output Behavior (-xxxxEx-A Variants)

POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_J(\max)$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J . (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths, to the ambient air. Its primary component is the effective thermal conductivity, K , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (power dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J , at P_D .

$$\text{Equation 1: } P_D = V_{IN} \times I_{IN}$$

$$\text{Equation 2: } \Delta T = P_D \times R_{\theta JA}$$

$$\text{Equation 3: } T_J = T_A + \Delta T$$

For example, given common conditions such as: $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $I_{CC} = 8\text{ mA}$, and $R_{\theta JA} = 270^\circ\text{C/W}$, then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 8\text{ mA} = 96\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 96\text{ mW} \times 270^\circ\text{C/W} = 25.9^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 25.9^\circ\text{C} = 50.9^\circ\text{C}$$

A worst-case estimate, $P_D(\max)$, represents the maximum allowable power level [$V_{CC}(\max)$, $I_{CC}(\max)$], without exceeding $T_J(\max)$, at a selected $R_{\theta JA}$ and T_A .

For example:

Consider the reliability for V_{CC} at $T_A = 150^\circ\text{C}$, using values estimated based on the UC package and a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 270^\circ\text{C/W}$, $T_J(\max) = 165^\circ\text{C}$, $V_{CC(\max)} = 24\text{ V}$, and $I_{CC} = 10\text{ mA}$.

Calculate the maximum allowable power level, $P_D(\max)$. First, invert Equation 3:

$$\Delta T(\max) = T_J(\max) - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert Equation 2:

$$P_D(\max) = \Delta T(\max) \div R_{\theta JA} = 15^\circ\text{C} \div 270^\circ\text{C/W} = 55.5\text{ mW}$$

Finally, invert Equation 1 with respect to voltage:

$$V_{CC(\text{est})} = P_D(\max) \div I_{CC} = 55.5\text{ mW} \div 10\text{ mA} = 5.55\text{ V}$$

The result indicates that, at T_A , the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(\text{est})}$.

Compare $V_{CC(\text{est})}$ to $V_{CC(\max)}$:

- If $V_{CC(\text{est})} \leq V_{CC(\max)}$, reliable operation between $V_{CC(\text{est})}$ and $V_{CC(\max)}$ requires enhanced $R_{\theta JA}$.
- If $V_{CC(\text{est})} \geq V_{CC(\max)}$, operation between $V_{CC(\text{est})}$ and $V_{CC(\max)}$ is reliable under these conditions.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	270	$^\circ\text{C/W}$

[1] Additional thermal information available on the Allegro website.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000409, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

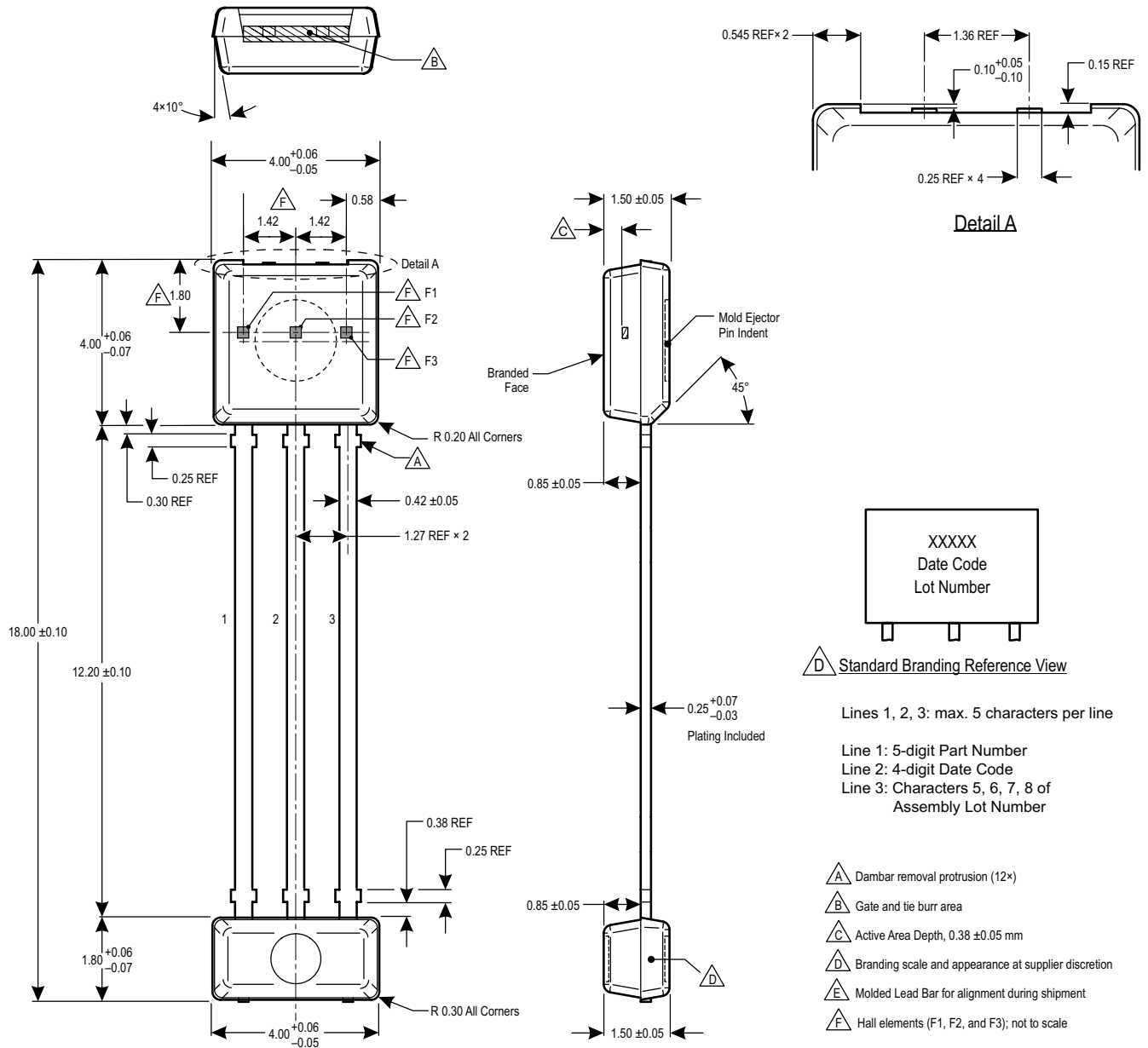


Figure 21: Package UC, 3-Pin SIP

XXXXX
Date Code
Lot Number

D Standard Branding Reference View

Lines 1, 2, 3: max. 5 characters per line
Line 1: 5-digit Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

- A** Dambar removal protrusion (12x)
- B** Gate and tie burr area
- C** Active Area Depth, 0.38 ±0.05 mm
- D** Branding scale and appearance at supplier discretion
- E** Molded Lead Bar for alignment during shipment
- F** Hall elements (F1, F2, and F3); not to scale

Revision History

Number	Date	Description
–	September 13, 2018	Initial release
1	October 7, 2019	Added “Detail A” to package outline drawing (page 17), and other minor editorial updates
2	May 18, 2021	Updated Speed Only Protocol section (page 8), inverted output polarity of -FOOOOxx variant (page 9), updated Figure 8 (page 10).
3	April 15, 2024	Updated ASIL status (pages 1 and 2), updated part numbers in selection guide (page 2), clarified part numbering in Figure 20 (page 15), and made minor editorial corrections throughout, including changing the future tense (“will”) to the present tense where appropriate, updating archaic language (“normal” changed to “typical”), removing trailing dashes in part numbers of variants, adding missing hyperlinks to cross-references, and minimizing use of capitalization (exceptions: register address are in all capitals; and figures, tables, and headings are in sentence case).

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