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ELECTRONICS

# THE DATASHEET OF

# APS12400LLHALT-1H1A

# APS12400

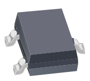
# Two-Wire Hall-Effect Latch

## FEATURES AND BENEFITS

- ASIL A functional safety
  - Developed in accordance with ISO 26262
  - Internal diagnostics and a defined Safe State
  - A$^{2}$-SIL™ documentation available
- Multiple product options
  - Magnetic polarity, switch points, and hysteresis
  - Temperature coefficient (supports SmCo, NdFeB, and ferrite magnets)
  - Output polarity and current levels
- Reduces module bill of materials (BOM) and assembly cost
  - Integrated overvoltage clamp (40 V load dump) and reverse-battery diode
  - Integrated series resistor and bypass capacitor (UC package)
  - Enables PCB-less sensor modules
- Automotive-grade ruggedness and fault tolerance
  - Extended AEC-Q100 Grade 0 qualification
  - Operation at –40°C to 175°C junction temperature
  - 3 to 24 V operating voltage range
  - High EMC/ESD immunity
  - Overtemperature indication

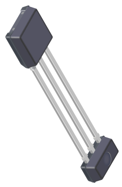
## PACKAGES

3-pin SOT23-W (LH)



3-pin ultramini SIP (UA)

3-pin SIP (UC)



*Not to scale*

## DESCRIPTION

APS12400 devices are two-wire planar Hall-effect sensor integrated circuits (ICs) developed in accordance with ISO 26262. They include internal diagnostics and support a functional safety level of ASIL A. The enhanced two-wire current-mode interface provides interconnect open/short diagnostics and adds a Safe State to communicate diagnostic information while maintaining compatibility with legacy two-wire systems. Two-wire sensors are well-suited to safety applications, especially those involving long wire harnesses.

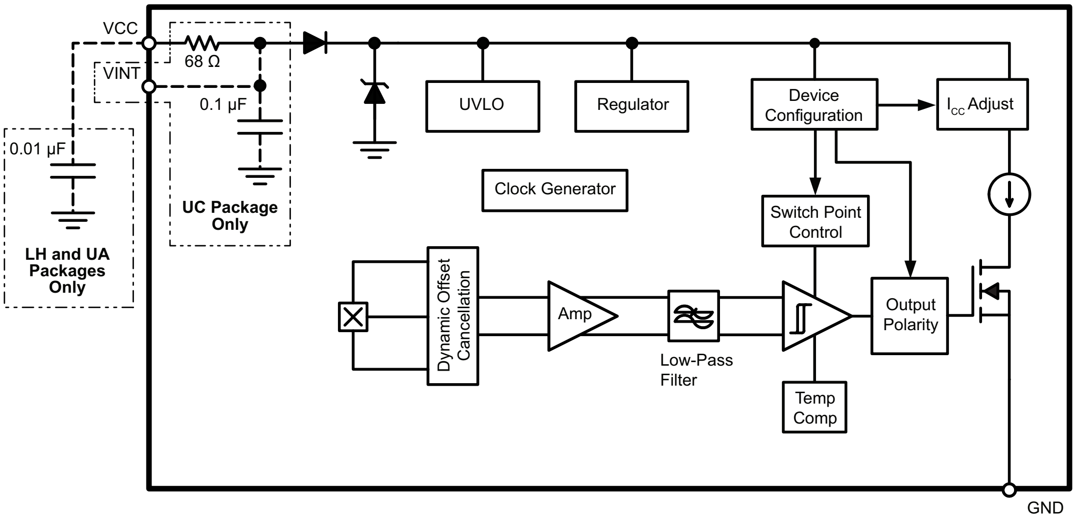
The APS12400 is a factory-calibrated latch (bipolar switch) available in several product options including magnetic switch points, temperature coefficient, and output polarity. The response can be matched to SmCo, NdFeB, or low-cost ferrite magnets. There is a choice of two output current levels and either output polarity.

APS12400 sensors are engineered to operate in the harshest environments with minimal external components. They are qualified beyond the requirements of AEC-Q100 Grade 0 and will survive extended operation at 175°C junction temperature. These monolithic ICs include on-chip reverse-

*Continued on the next page…*

## TYPICAL APPLICATIONS

- Automotive and industrial safety systems
- Sunroof/convertible top/tailgate/liftgate actuation
- Clutch-by-wire
- Electric power steering (EPS)
- Transmissions actuators
- Wiper motors



**Functional Block Diagram**

APS12400-DS, Rev. 5
MCO-0000402

July 21, 2022

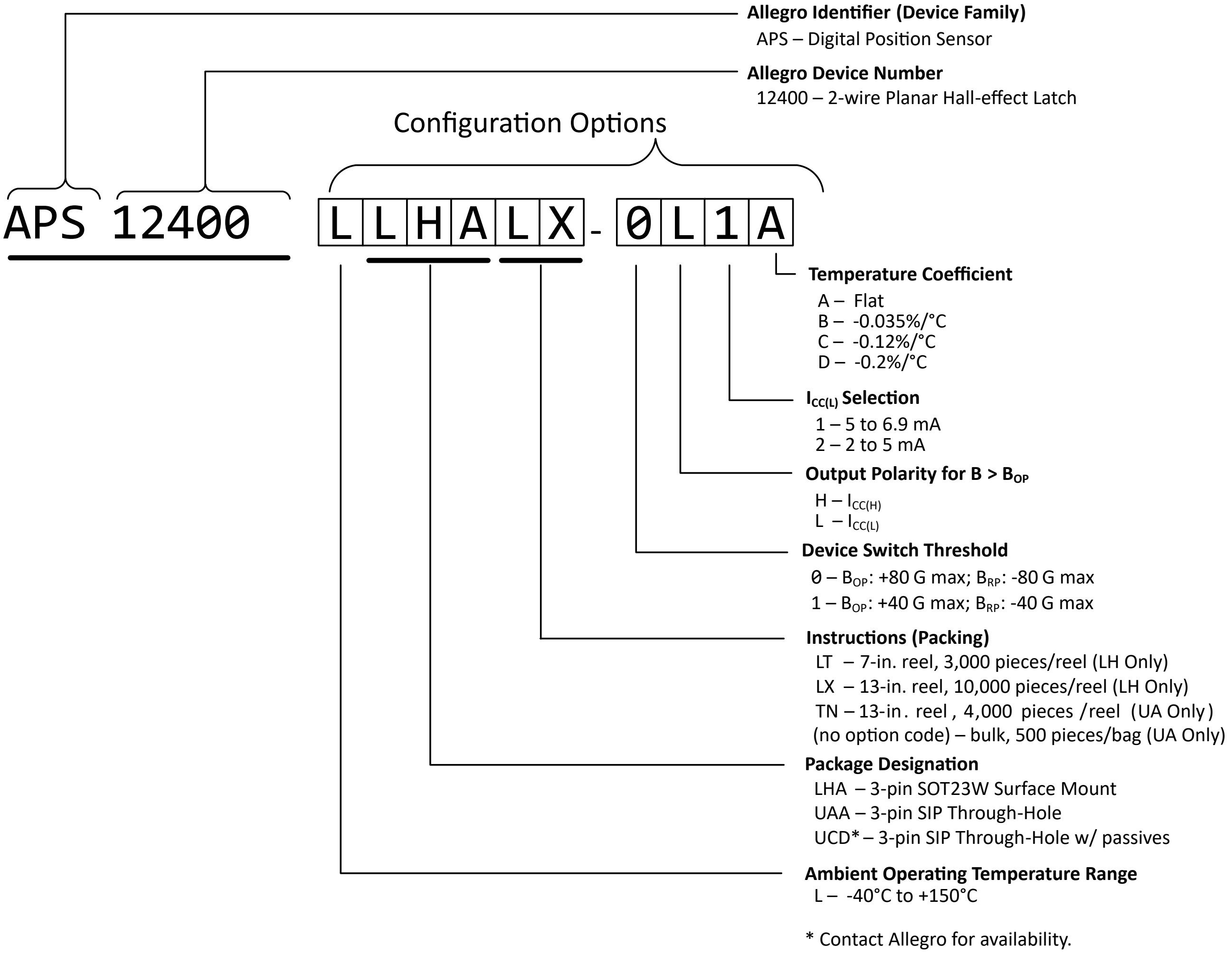
## DESCRIPTION (continued)

battery protection, overvoltage protection (40 V load dump), ESD protection, overtemperature detection, and an internal voltage regulator for operation directly from an automotive battery bus. These integrated features reduce the end-product bill of materials (BOM) and assembly cost.

The available SIP package with integrated discrete components (UC) enables PCB-less applications by incorporating all of the EMC protection components into the IC package. Other package options include industry-standard surface-mount SOT (LH) and through-hole SIP (UA) packages. All three packages are RoHS-compliant and lead (Pb) free with 100% matte-tin-plated leadframes.

For situations where a functionally equivalent but factory-programmed two-wire latch or end-of-line programmable device is preferred, refer to the APS12400 and APS11900 device families, respectively.

### Complete Part Number Format



* Contact Allegro for availability.

## SELECTION GUIDE

| Part Number [1] | Package | Packing | Magnetic Temperature Coefficient | Output Polarity for B > $B_{OP}$ | Device Switch Threshold (G) | $I_{CC(L)}$ Selection (mA) |
|---|---|---|---|---|---|---|
| APS12400LLHALT-0H1A | 3-pin SOT23-W surface mount | 7-inch reel, 3000 pieces/reel | Flat | $I_{CC(H)}$ | $B_{OP}$: +80 max<br>$B_{RP}$: –80 max | 5 to 6.9 |
| APS12400LLHALX-0H1A | 3-pin SOT23-W surface mount | 13-inch reel, 10000 pieces/reel | | | | |
| APS12400LUAA-0H1A | 3-pin SIP through-hole | Bulk, 500 pieces/bag | Flat | $I_{CC(H)}$ | $B_{OP}$: +80 max<br>$B_{RP}$: –80 max | 5 to 6.9 |
| APS12400LUAATN-0H1A | 3-pin SIP through-hole | 13-inch reel, 4000 pieces/reel | | | | |
| APS12400LUAA-0H2A | 3-pin SIP through-hole | Bulk, 500 pieces/bag | Flat | $I_{CC(H)}$ | $B_{OP}$: +80 max<br>$B_{RP}$: –80 max | 2 to 5 |
| APS12400LUAATN-0H2A | 3-pin SIP through-hole | 13-inch reel, 4000 pieces/reel | | | | |
| APS12400LUCD-0H1A [2] | 3-pin SIP through-hole | Bulk, 500 pieces/bag | Flat | $I_{CC(H)}$ | $B_{OP}$: +80 max<br>$B_{RP}$: –80 max | 5 to 6.9 |
| APS12400LUCDTN-0H1A [2] | 3-pin SIP through-hole | 13-inch reel, 4000 pieces/reel | | | | |

[1] Contact Allegro MicroSystems for options not listed in the selection guide.
[2] Contact Allegro MicroSystems for availability.

## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Supply Voltage [1] | $V_{CC}$ | | 40 | V |
| Reverse Supply Voltage | $V_{RCC}$ | | –23 | V |
| Magnetic Flux Density | B | | Unlimited | G |
| Maximum Junction Temperature | $T_J$(max) | | 165 | °C |
| | | For 500 hours | 175 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | °C |

[1] This rating does not apply to extremely short voltage transients such as load dump and/or ESD. Those events have individual ratings specific to the respective transient voltage event. Contact your local field applications engineer for information on EMC test results.

### INTERNAL DISCRETE COMPONENT RATINGS (UC Package Only)

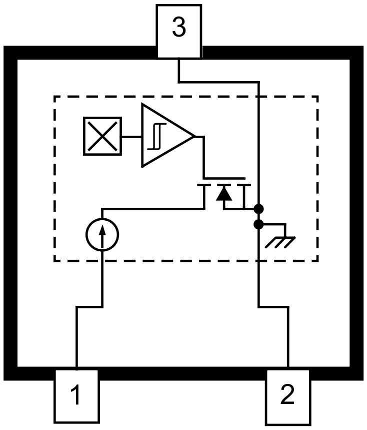
| Component | Symbol | Test Conditions | Characteristics | | | | |
|---|---|---|---|---|---|---|---|
| | | | Rated Nominal Resistance/Capacitance | Rated Voltage | Rated Tolerance | Rated Temp. Range | Rated Power Handling |
| Resistor | $R_{SERIES}$ | In series with VCC | 68 Ω | 50 V | ±15% | – | 1/8 W |
| Capacitor | $C_{SUPPLY}$ | Connected between VCC and GND | 100 nF | 50 V | ±10% | X7R | – |

## PINOUT DIAGRAMS AND TERMINAL LIST TABLE

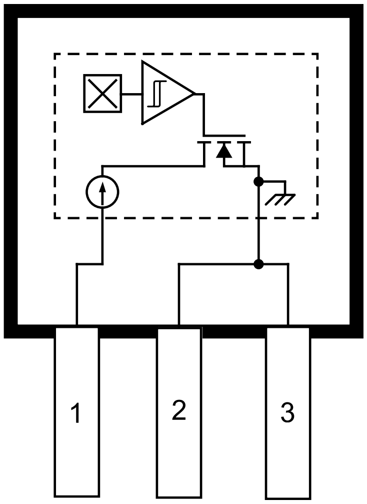
### Terminal List Table (LH, UA Packages)

| Number | Package Name | | Function |
|---|---|---|---|
| | LH | UA | |
| 1 | VCC | VCC | Supply voltage |
| 2 | GND | GND | Ground terminal |
| 3 | GND | GND | Ground terminal |

Note: For best performance, tie Pins 2 and 3 together close to the IC.



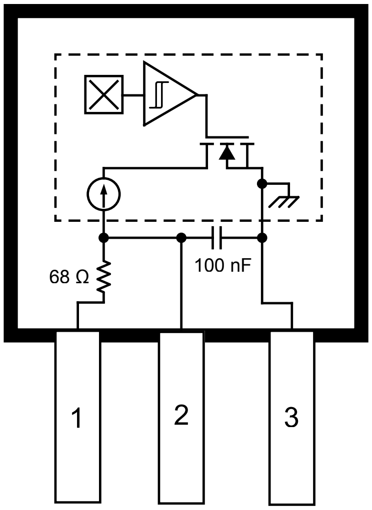
LH Package, 3-Pin SOT23W Pinout



UA Package, 3-Pin SIP Pinout

### Terminal List Table (UC Package)

| Number | Package Name | Function |
|---|---|---|
| | UC | |
| 1 | VCC | Supply voltage |
| 2 | VINT | This pin reflects the internal voltage, $V_{INT}$, after the internal series resistor. This pin should be kept floating. |
| 3 | GND | Ground terminal |



UC Package, 3-Pin SIP Pinout

**ELECTRICAL CHARACTERISTICS:** Valid over full operating voltage and ambient temperature ranges for $T_J < T_J$(max) and $C_{BYP}$ = 0.01 µF, unless otherwise specified

| Characteristics | Symbol | Test Conditions | | Min. | Typ. [3] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **SUPPLY AND STARTUP** | | | | | | | |
| Supply Voltage | $V_{CC}$ | Operating, $T_J$ < 165°C | LH and UA packages | 3.0 | – | 24 | V |
| | | Operating, $T_J$ < 165°C | UC package | 4.33 | – | 24 | V |
| Undervoltage Lockout [4] | $V_{CC(UV)DIS}$ | After power-on, as $V_{CC}$ increases, output is forced to POS until this voltage is reached | LH and UA packages | – | 2.6 | – | V |
| | | | UC package | – | 3.5 | – | V |
| | $V_{CC(UV)EN}$ | After POK, when $V_{CC}$ drops below this voltage, output is forced to POS | LH and UA packages | – | 2.3 | – | V |
| | | | UC package | – | 3.2 | – | V |
| Supply Current | $I_{CC(L1)}$ | | | 5 | – | 6.9 | mA |
| | $I_{CC(L2)}$ | | | 2 | – | 5 | mA |
| | $I_{CC(H)}$ | | | 12 | – | 17 | mA |
| | $I_{SAFE}$ | Safe current state. Indicates overtemperature or device configuration error. | | – | – | 2 | mA |
| Output Slew Rate | dI/dt | No bypass capacitor; $C_L$ [5] = 20 pF | LH and UA packages | – | 50 | – | mA/µs |
| | | $C_{BYP}$ = 100 nF; $C_L$ [5] = 20 pF | | – | 0.22 | – | mA/µs |
| | | Internal bypass capacitor; $C_L$ [5] = 20 pF | UC package | – | 0.22 | – | mA/µs |
| Power-On Time [6] | $t_{PO}$ | $V_{CC} \geq V_{CC}$(min), $B > B_{OP}$(max), $B < B_{RP}$(min) | | – | – | 70 | µs |
| Power-On State [7] | POS | $t < t_{PO}$, $V_{CC} \geq V_{CC(UV)EN}$ | | $I_{CC(H)}$ | | | mA |
| Chopping Frequency | $f_C$ | | | – | 800 | – | kHz |
| Output Jitter (p-p) | | 1 kHz square wave signal | | – | 5 | – | µs |
| **ON-BOARD PROTECTION** | | | | | | | |
| Supply Zener Clamp Voltage | $V_Z$ | $I_{CC} = I_{CC(H)}$ + 1 mA, $T_A$ = 25°C | | 40 | – | – | V |
| Reverse Supply Zener Clamp Voltage | $V_{RZ}$ | $I_{CC}$ = –1 mA | | – | – | –23 | V |
| Overtemperature Shutdown | $T_{SD}$ | Temperature increasing | | – | 205 | – | °C |
| Overtemperature Hysteresis | $T_{JHYS}$ | | | – | 25 | – | °C |

[3] Typical data is at $T_A$ = 25°C and $V_{CC}$ = 12 V unless otherwise noted; for design information only.

[4] UC minimum $V_{CC}$ is higher to accommodate voltage drop in the internal series resistor. UC package minimum $V_{CC}$ is higher to accommodate voltage drop in the internal series resistor. This also affects the $V_{CC(UV)}$.

[5] $C_L$ – scope capacitance.

[6] Measured from $V_{CC} \geq V_{CC(MIN)}$ to valid output.

[7] Power-on state is defined only when $V_{CC}$ slew rate is 1 V/s or greater.

**MAGNETIC CHARACTERISTICS:** Valid over full operating voltage and ambient temperature ranges for $T_J < T_J$(max) and $C_{BYP}$ = 0.01 µF, unless otherwise specified

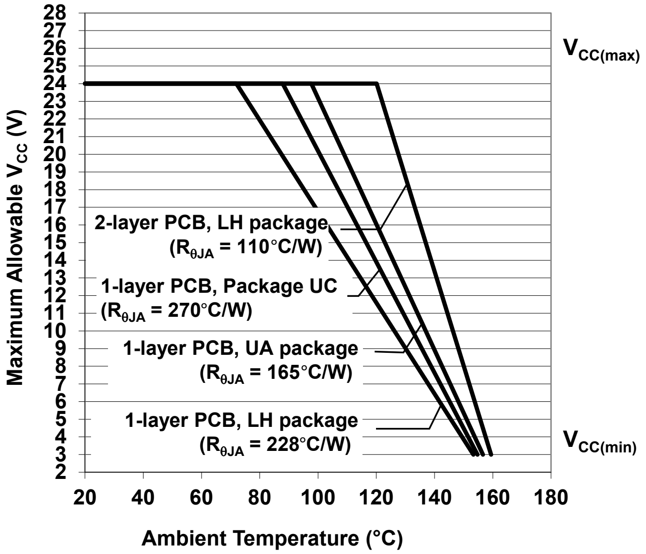
| Characteristics | Symbol | Magnetic Switch Point Option | Temperature Coefficient | Test Conditions | Min. | Typ. [8] | Max. | Unit [9] |
|---|---|---|---|---|---|---|---|---|
| Operate Point | $B_{OP}$ | -0 | A – Flat | $T_A$ = –40°C to 150°C | 5 | – | 80 | G |
| | | -1 | A – Flat | $T_A$ = –40°C to 150°C | 5 | – | 40 | G |
| Release Point | $B_{RP}$ | -0 | A – Flat | $T_A$ = –40°C to 150°C | –80 | – | –5 | G |
| | | -1 | A – Flat | $T_A$ = –40°C to 150°C | –40 | – | –5 | G |
| Hysteresis | $B_{HYS}$ | -0 | A – Flat | $T_A$ = –40°C to 150°C | 40 | – | 110 | G |
| | | -1 | A – Flat | $T_A$ = –40°C to 150°C | 15 | 40 | 65 | G |
| Switch Point Temperature Coefficient | | All | A – Flat | $T_A$ = –40°C to 150°C | – | 0 | – | %/°C |

[8] Typical data is at $T_A$ = 25°C and $V_{CC}$ = 12 V, unless otherwise noted; for design information only.
[9] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields.

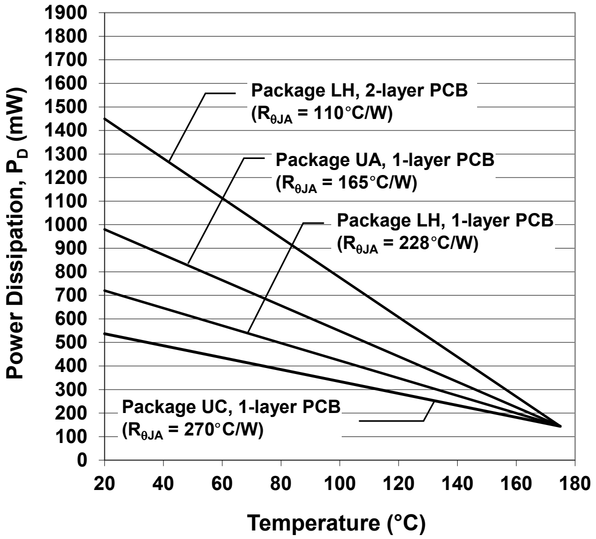
**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | Package LH, on 1-layer PCB based on JEDEC standard | 228 | °C/W |
| | | Package LH, on 2-layer PCB with 0.463 in.$^2$ of copper area each side | 110 | °C/W |
| | | Package UA, on 1-layer PCB with copper limited to solder pads | 165 | °C/W |
| | | Package UC, on 1-layer PCB with copper limited to solder pads | 270 | °C/W |

*Additional thermal information is available on the Allegro website.

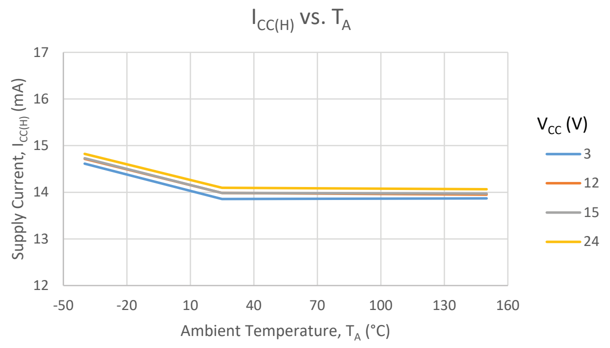


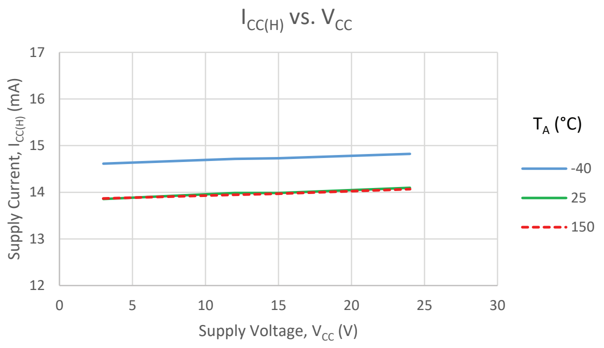
**Power Derating Curve**

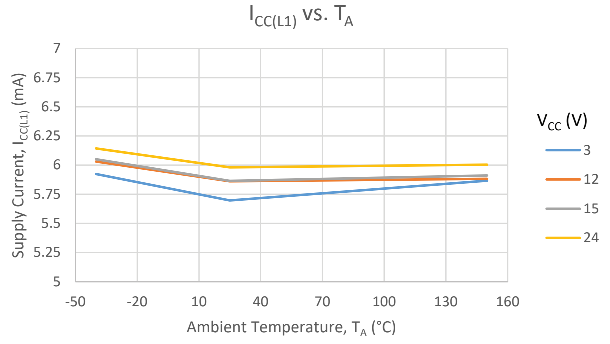


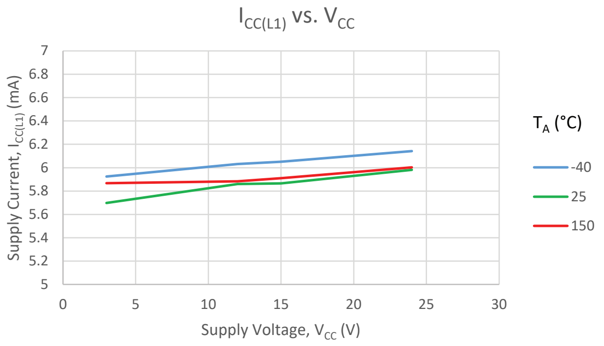
**Power Dissipation versus Ambient Temperature**

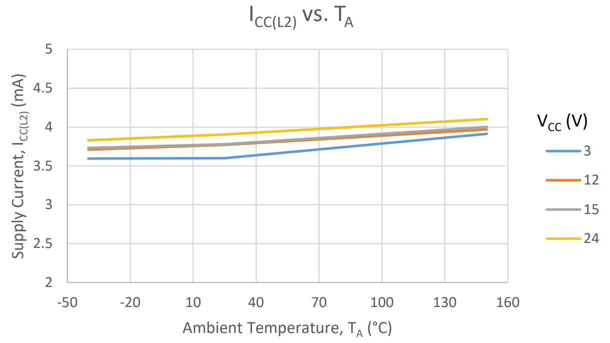
## CHARACTERISTIC PERFORMANCE DATA

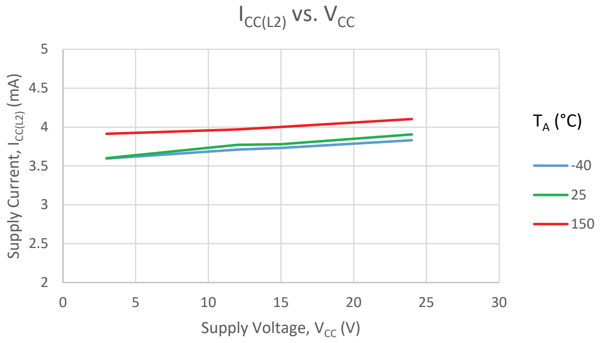

$I_{CC(H)}$ vs. $T_A$

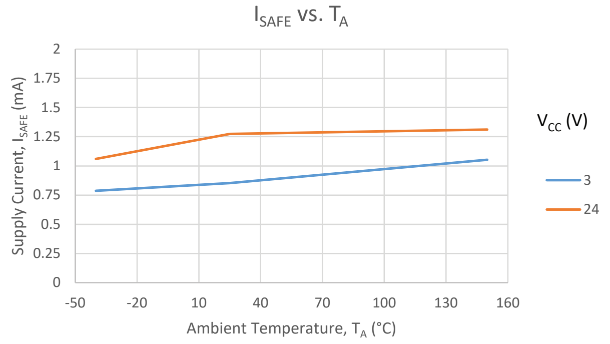

$I_{CC(H)}$ vs. $V_{CC}$

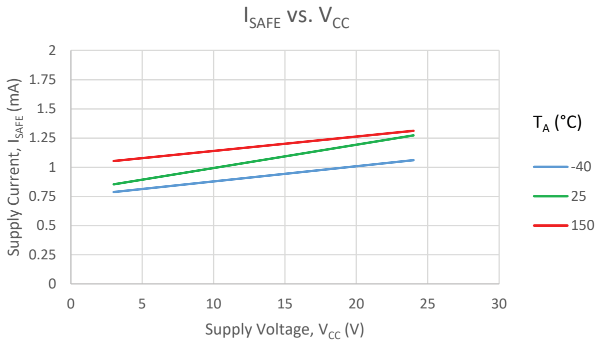

$I_{CC(L1)}$ vs. $T_A$


$I_{CC(L1)}$ vs. $V_{CC}$


$I_{CC(L2)}$ vs. $T_A$


$I_{CC(L2)}$ vs. $V_{CC}$


$I_{SAFE}$ vs. $T_A$


$I_{SAFE}$ vs. $V_{CC}$

## FUNCTIONAL DESCRIPTION

### Functional Safety

The APS12400 was designed in accordance with the international standard for automotive functional safety, ISO 26262. This product achieves an ASIL (Automotive Safety Integrity Level) rating of ASIL A according to the standard. The APS12400 is classified as a SEooC (Safety Element out of Context) and can be easily integrated into safety-critical systems requiring higher ASIL ratings that incorporate external diagnostics or use measures such as redundancy. Safety documentation will be provided to support and guide the integration process. Contact your local FAE for A$^2$-SIL™ documentation: www.allegromicro.com/ASIL.

The APS12400 has internal diagnostics to check the voltage supply (an undervoltage lockout regulator) and to detect overtemperature conditions. See the Diagnostics section for more information.

### Operation

The APS12400 devices are two-wire unipolar planar Hall-effect latches. The user can select a device that respond to a north or south magnetic field. There is a choice of two output current levels, $I_{CC(L1)}$ and $I_{CC(L2)}$, and the user can determine which current state is applied, $I_{CC(L)}$ or $I_{CC(H)}$, when the magnetic field is greater than $B_{OP}$ or less than $B_{RP}$.

The difference between the magnetic operate and release points is called the hysteresis of the device, $B_{HYS}$. Hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Figure 1 shows the potential configuration options for the APS12400. The direction of the applied magnetic field is perpendicular to the branded face of the APS12400. See Figure 2 for an illustration.

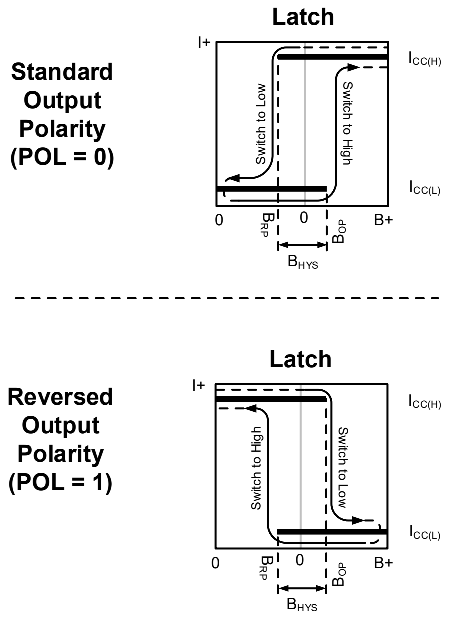


**Figure 1: Unipolar Hall Latch Magnetic and Output Current Polarity Options**

**B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.**

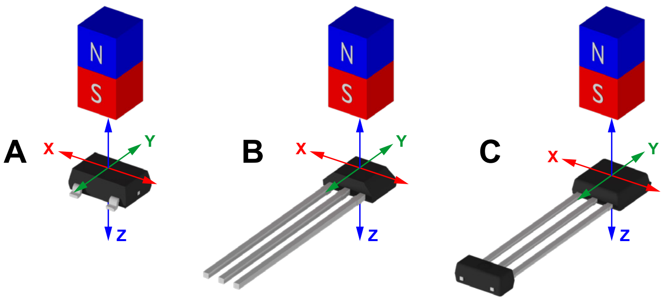


**Figure 2: Magnetic Sensing Orientations**

**APS12400 LH (Panel A), UA (Panel B), and UC (Panel C)**

## Power-On Behavior

The APS12400 has an internal voltage regulator with undervoltage lockout. As the device powers up, it stays in the power-on state (POS) of $I_{CC(H)}$ until the supply voltage exceeds $V_{CC(UV)DIS}$. After $t_{PO}$, the current consumption is $I_{CC(L)}$ or $I_{CC(H)}$, according to the magnetic field and the device configuration, as shown in Figure 1.

Similarly, when the supply voltage decreases, the device returns to the power-on state (POS) when the supply voltage drops below $V_{CC(UV)EN}$, as shown in Figure 3.

When the device powers on in the hysteresis range (less than $B_{OP}$ and higher than $B_{RP}$), the output corresponds to the power-on state. In this case, the correct state is attained after the first excursion beyond $B_{OP}$ or $B_{RP}$.

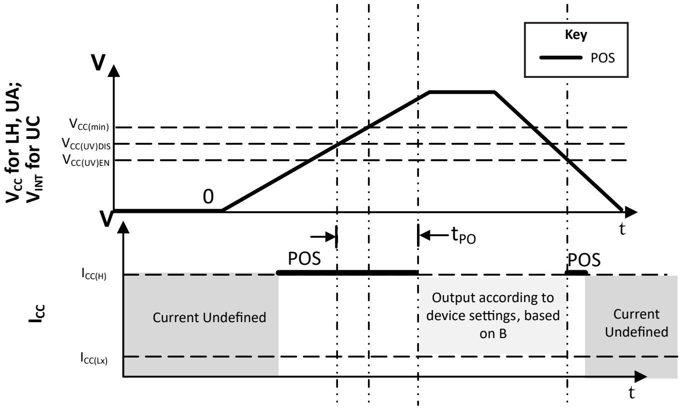


Figure 3: Power-On/UVLO Behavior

## Diagnostic Features

When properly supplied, APS12400 always has current flowing at a specified level: either $I_{CC(H)}$, $I_{CC(L)}$, or $I_{SAFE}$. Any current outside of these narrow ranges is a fault condition. If there is a short, current increases so that $I_{CC} > I_{CC(H)}$ (max), outside the valid $I_{CC(H)}$ range. If there is an open, the current lowers below the $I_{CC(L)}$ (min), outside the valid output current range. In this way, connectivity issues between the ECU and the sensor can easily be detected.

Additionally, the APS12400 has an overtemperature feature: if the junction temperature increases beyond $T_{SD}$, the current is reduced to $I_{SAFE}$. The device current also changes to $I_{SAFE}$ if there is an error in the device configuration which is checked at power-on and after an overtemperature event.

Any value of $I_{CC}$ between the allowed ranges for $I_{CC(H)}$ and $I_{CC(L)}$ indicates a general fault condition.

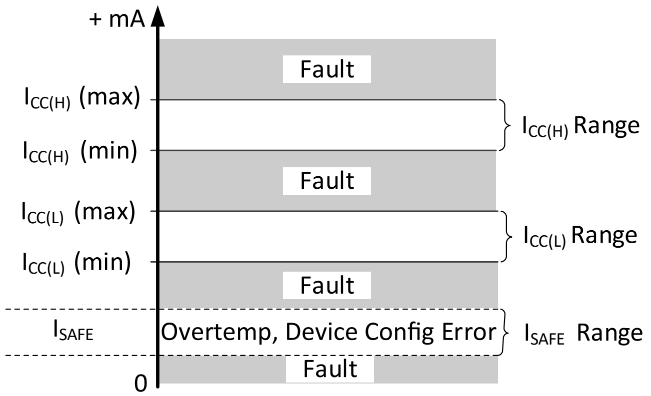


Figure 4: Interpreting $I_{CC}$ for System-Level Diagnostics

## Temperature Coefficient and Magnet Selection

The APS12400 allows the user to select the magnetic temperature coefficient to compensate for drifts of SmCo, NdFeB, and ferrite magnets over temperature—as indicated in the specifications table on page 5. This compensation improves the magnetic system performance over the entire temperature range. For example, the magnetic field strength from ferrite decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as –40°C, due to the higher magnetic field strength from the ferrite magnet. The APS12400 compensates the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

For example, the typical ferrite compensation is –0.2%/°C. With a 25°C temperature $B_{OP}$ switch point of 80 G, the switch point changes nominally by –0.2%/°C × 80 × (150°C – 25°C) = –20 G to 80 G – 20 G = 60 G at 150°C. And at –40°C, the switch point changes by –0.2%/°C × 80 × (–40°C – 25°C) = 10 G to 80 G + 10 G = 90 G.

## Applications

For the LH and UA packages, an external bypass capacitor (from 0.01 µF to 0.1 µF) should be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization. Some applications may require additional EMC immunity, which is achieved with an enhanced protection circuit. For example, increasing the bypass capacitor from 0.01 µF to 0.1 µF improves immunity to Powered ESD (ISO 10605) and Direct Capacitive Coupling.

A series resistor and a 0.1 µF bypass capacitor are integrated into the UC package, making it easy to achieve an EMC-robust design with no external components or PCB required.

Note that the bypass capacitor selection directly affects the slew rate. See the Electrical Characteristics table for the typical slew rate with 0.1 µF bypass capacitor. A 0.01 µF bypass capacitor slew rate is ten times faster.

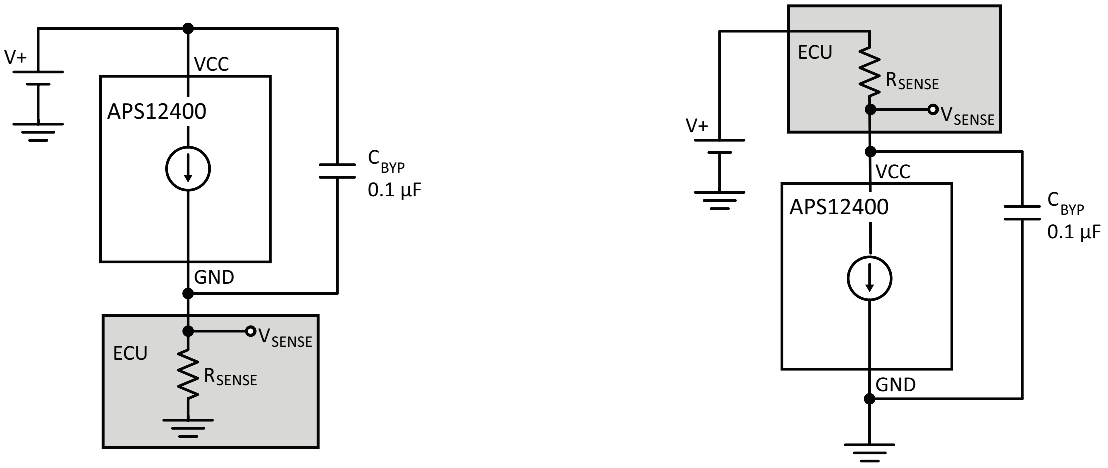
Typical application circuits are shown in “Figure 5: Typical Application Circuits” on page 13.

Extensive applications information for Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide*, AN27701
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices*, AN27703.1
- *Soldering Methods for Allegro’s Products – SMT and Through-Hole*, AN26009
- www.allegromicro.com/ASIL

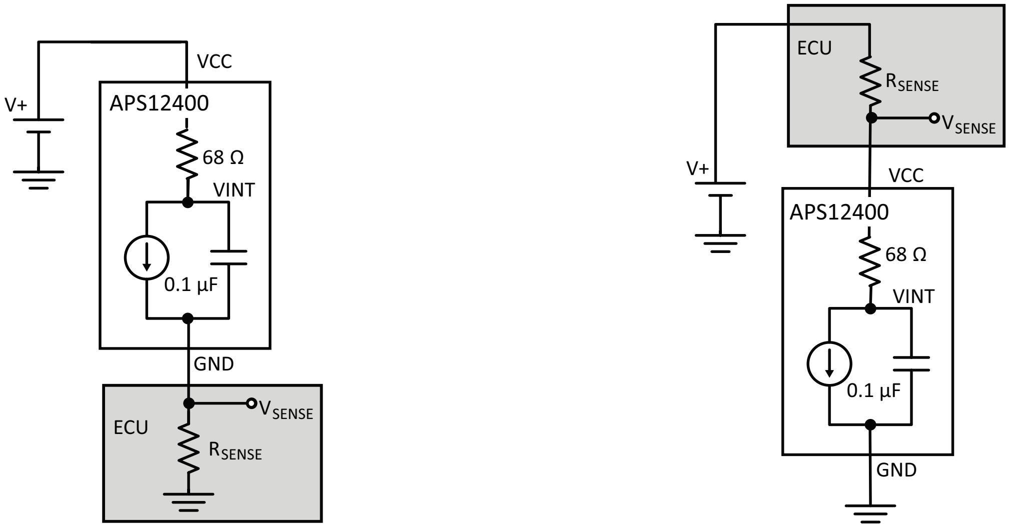
All are provided on the Allegro Web site:

**www.allegromicro.com**



(A) Low-Side Sensing (LH, UA package)

(B) High-Side Sensing (LH, UA package)



(C) Low-Side Sensing (UC package)

(D) High-Side Sensing (UC package)

**Figure 5: Typical Application Circuits**

### Chopper Stabilization Technique

A limiting factor for switch point accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. “Figure 6: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)” illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro’s innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12400 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process that allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

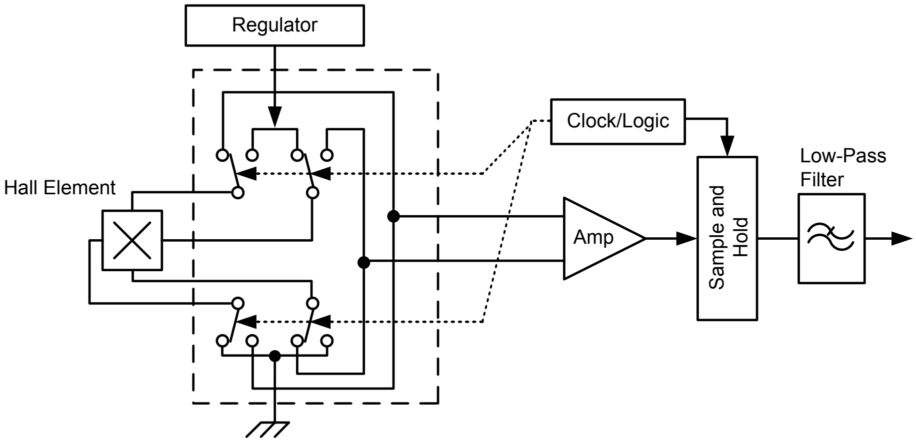


**Figure 6: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)**

## POWER DERATING

The device must be operated below the maximum junction temperature, $T_J$ (max). Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance (junction to ambient), $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K, of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, $T_A$, and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions.

$$P_D = V_{IN} \times I_{IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For example, given common conditions: $T_A$ = 25°C, $V_{CC}$ = 12 V, $I_{CC}$ = 6 mA, and $R_{\theta JA}$ = 110°C/W for the LH package, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6\ mA = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 110°C/W = 7.92°C$$

$$T_J = T_A + \Delta T = 25°C + 7.92°C = 32.92°C$$

### Determining Maximum $V_{CC}$

For a given ambient temperature, $T_A$, the maximum allowable power dissipation as a function of $V_{CC}$ can be calculated. $P_D$ (max) represents the maximum allowable power level without exceeding $T_J$ (max) at a selected $R_{\theta JA}$ and $T_A$.

Example: $V_{CC}$ at $T_A$ = 150°C, package UA, using low-K PCB. Using the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 165°C/W, $T_J$ (max) = 165°C, $V_{CC}$ (max) = 24 V, and $I_{CC}$ (max) = 17 mA, calculate the maximum allowable power level, $P_D$ (max). First, using equation 3:

$$\Delta T\ (max) = T_J\ (max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to $T_J$ resulting from internal power dissipation. Then, from equation 2:

$$P_D\ (max) = \Delta T\ (max) \div R_{\theta JA} = 15°C \div 165°C/W = 91\ mW$$

Finally, using equation 1, solve for maximum allowable $V_{CC}$ for the given conditions:

$$V_{CC}\ (est) = P_D\ (max) \div I_{CC}\ (max) = 91\ mW \div 17\ mA = 5.4\ V$$

The result indicates that, at $T_A$, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC}$ (est).

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must by improved. This can be accomplished by adjusting the layout or the PCB materials, or by controlling the ambient temperature.

### Determining Maximum $T_A$

In cases where the $V_{CC}$ (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature $T_A$ (max), for example, in a worst-case scenario with conditions $V_{CC}$ (max) = 24 V, $I_{CC}$ (max) = 17 mA, and $R_{\theta JA}$ = 228°C/W for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 17\ mA = 408\ mW$$

Then, by rearranging equation 3 and substituting with equation 2:

$$T_A\ (max) = T_J\ (max) - \Delta T$$

$$T_A\ (max) = 165°C - (408\ mW \times 228°C/W)$$

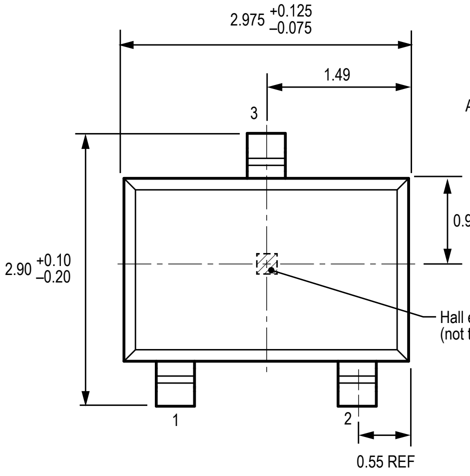
$$T_A\ (max) = 165°C - 93°C = 72°C$$

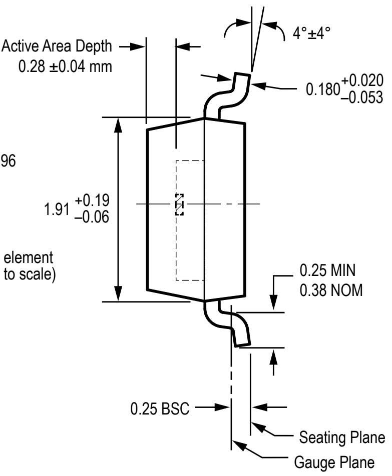
Finally, note that the $T_A$ (max) rating of the device is 150°C and performance is not guaranteed above this temperature for any power level.

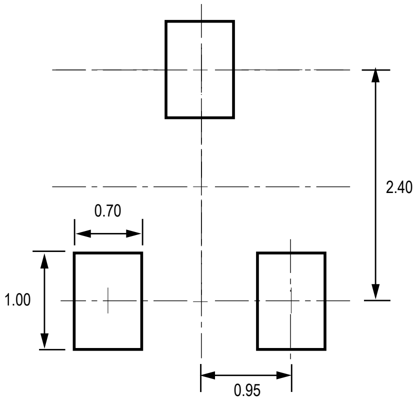
## Package LH, 3-Pin SOT23W

## For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

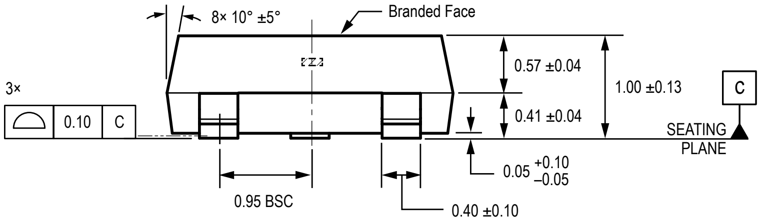


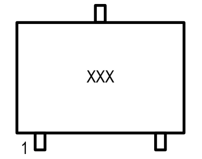




PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances





Standard Branding Reference View 1

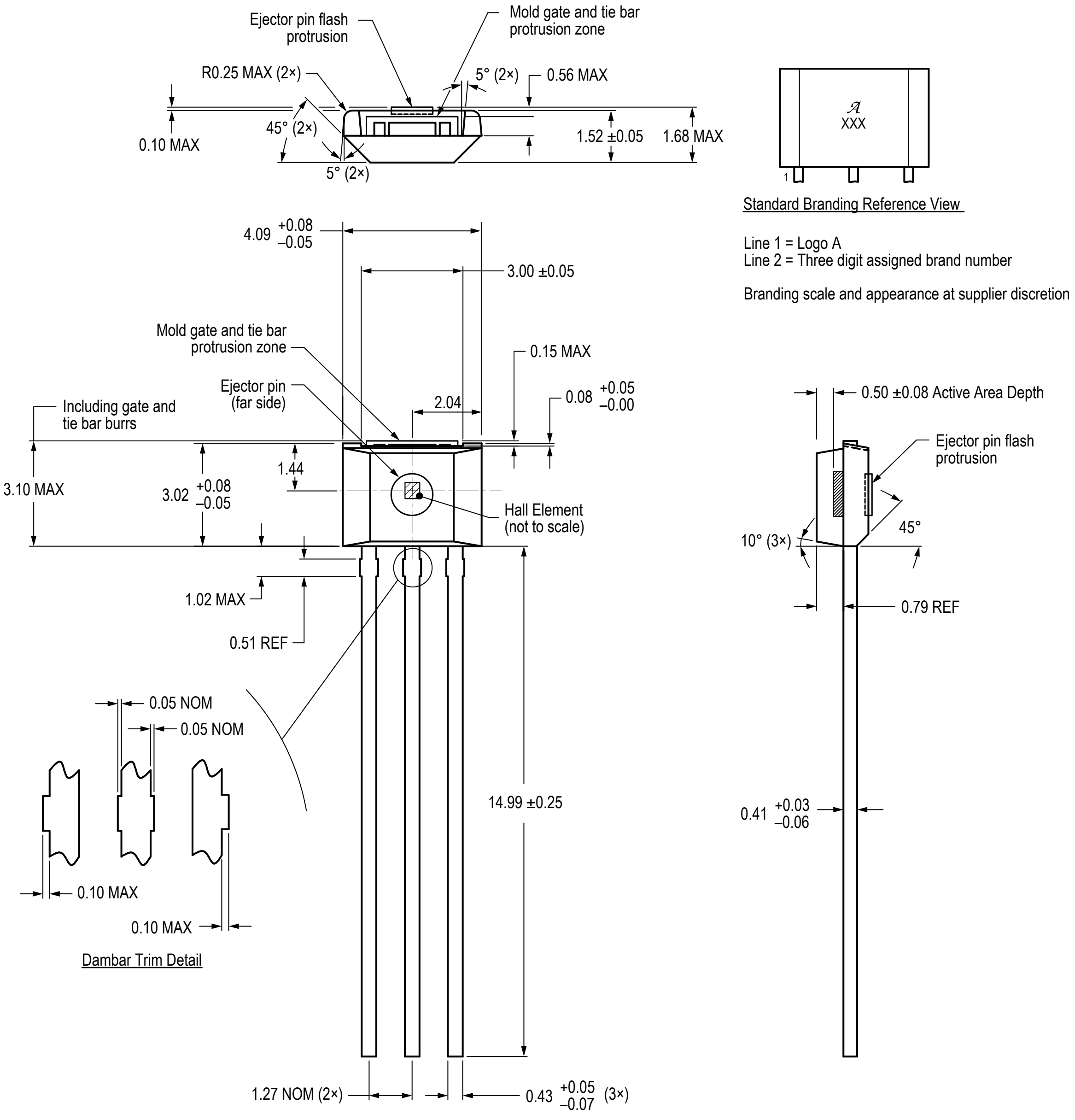
Line 1 = Three digit assigned brand number

Branding scale and appearance at supplier discretion

## Package UA, 3-Pin SIP

### For Reference Only – Not For Tooling Use

(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



Standard Branding Reference View

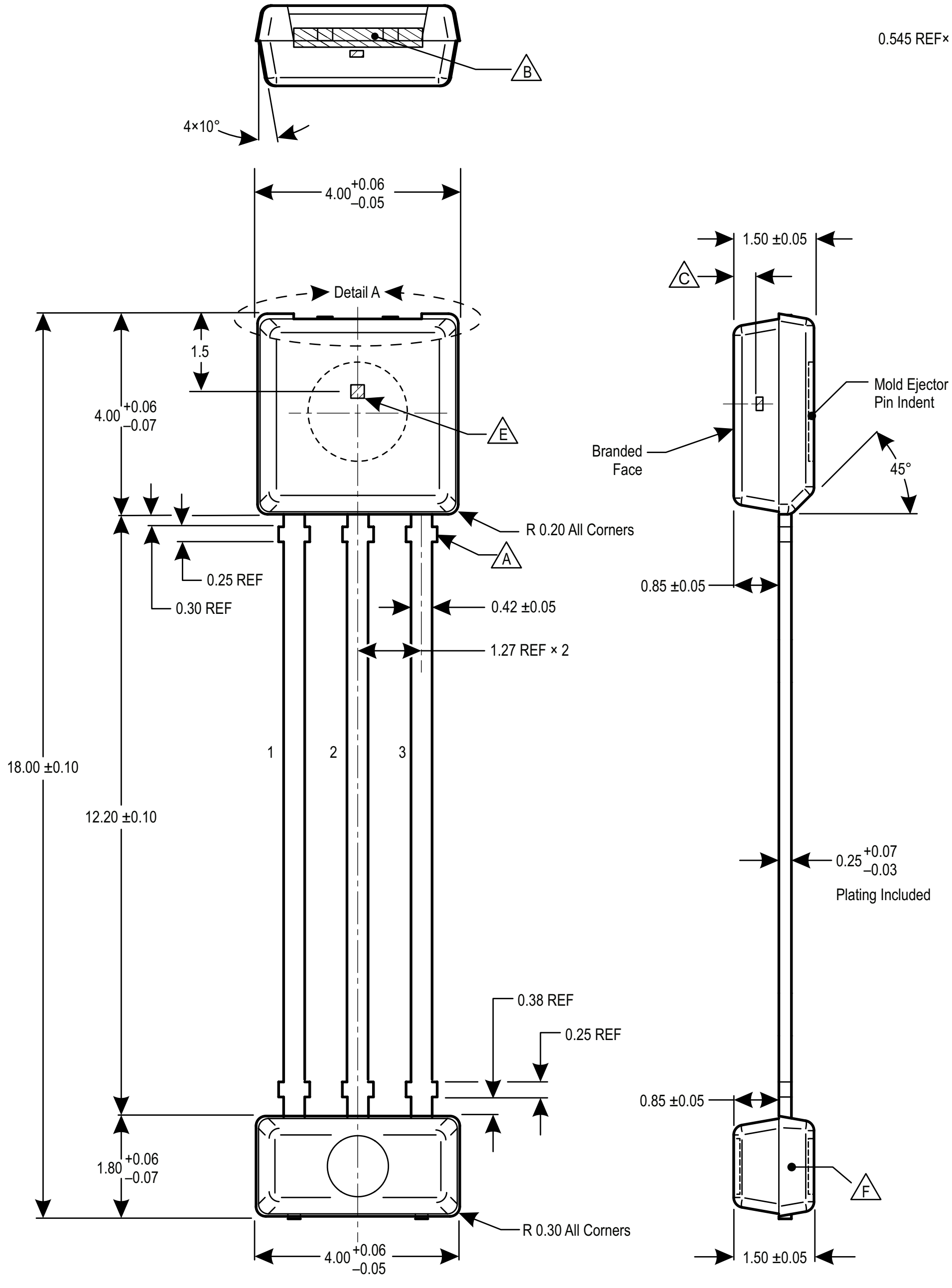
Line 1 = Logo A
Line 2 = Three digit assigned brand number

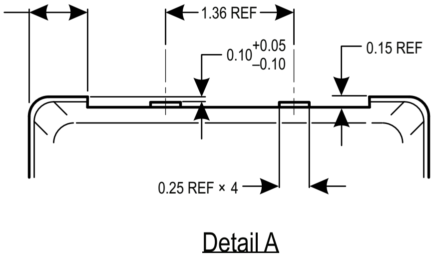
Branding scale and appearance at supplier discretion

## Package UC, 3-Pin SIP

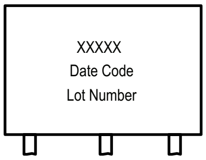
### For Reference Only – Not for Tooling Use

(Reference DWG-0000409, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





△E Standard Branding Reference View



Line 1, 2, 3: Max. 5 characters per line

Line 1: 5-digit Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

△A Dambar removal protrusion (12×)

△B Gate and tie burr area

△C Active Area Depth, 0.38 ±0.05 mm

△D Branding scale and appearance at supplier discretion

△E Hall element (not to scale)

△F Molded Lead Bar to prevent damage to leads during shipment

## REVISION HISTORY

| Number | Date | Description |
|---|---|---|
| – | March 23, 2018 | Initial release |
| 1 | September 11, 2018 | Updated Selection Guide table (page 3), Corrected supply current values and plots (pages 6 and 9); added UC package availability footnote to Complete Part Number Format diagram and Selection Guide table (page 2-3) |
| 2 | April 1, 2019 | Updated ASIL status (page 1 and 10) |
| 3 | April 3, 2020 | Minor editorial updates |
| 4 | April 14, 2022 | Updated package drawings (pages 16-18) |
| 5 | July 21, 2022 | Updated ASIL status (pages 1 and 10) and made minor editorial updates |