THE DATASHEET OF

A1186LLHLT

Ultrasensitive Two-Wire Field-Programmable Chopper-Stabilized Unipolar Hall-Effect Switches

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2011

Recommended Substitutions:

Currently available next generation replacement parts are available:

- for the A1185EUA-T use the *A1192LUA-T*
- for the A1185LUA-T and the A1186LUA-T use the *A1193LUA-T*
- for the A1185ELHLT-T use the *A1192LLHLX-T*
- for the A1186ELHLT-T and the A1186LLHLT-T use the *A1193LLHLX-T*

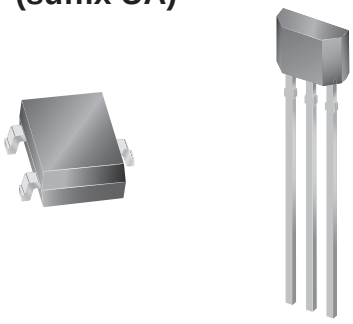
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Ultrasensitive Two-Wire Field-Programmable Chopper-Stabilized Unipolar Hall-Effect Switches

Features and Benefits

- Chopper stabilization
  - Low switchpoint drift over operating temperature range
  - Low sensitivity to stress
- Field programmable for optimized switchpoints
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
  - On-board voltage regulator
  - 3.5 to 24 V operation

Packages: 3 pin SOT23W (suffix LH), and 3 pin SIP (suffix UA)



Not to scale

Description

The A1185 and A1186 are ultrasensitive, two-wire, unipolar Hall effect switches. The operate point, B_{OP}, can be field-programmed, after final packaging of the device and placement into the application. This advanced feature allows the optimization of the device switching performance, by effectively accounting for variations caused by mounting tolerances for the device and the target magnet.

This family of devices are produced on the Allegro MicroSystems new DABIC5 BiCMOS wafer fabrication process, which implements a high-frequency, chopper-stabilization technique that achieves magnetic stability and eliminates the offsets that are inherent in single-element devices exposed to harsh application environments. Commonly found in a number of automotive applications, the A1185 and A1186 devices are utilized in sensing: seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position.

Two-wire unipolar switches are particularly advantageous in price-sensitive applications, because they require one less wire

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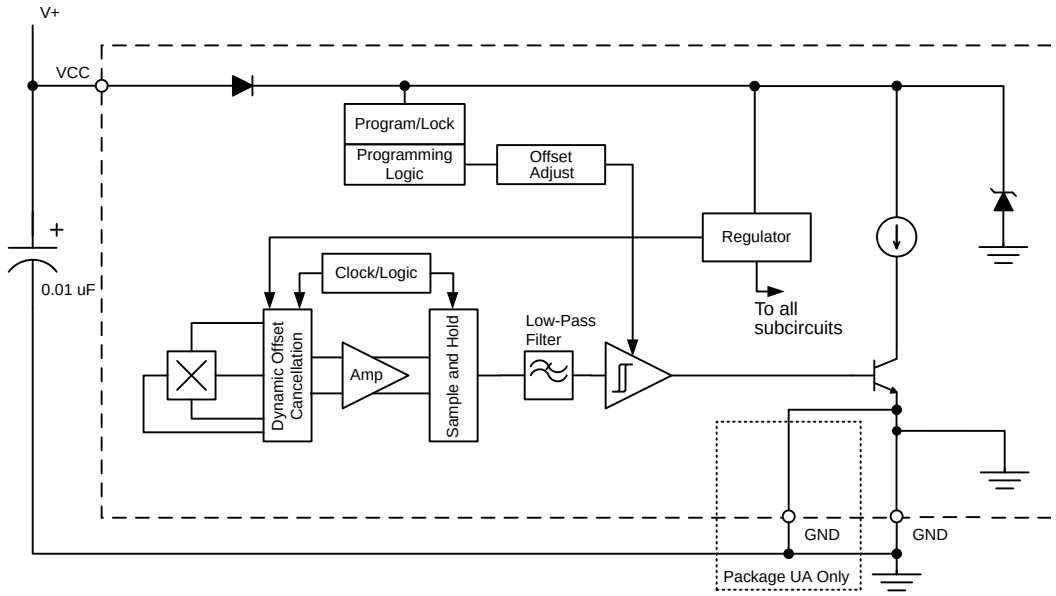
Functional Block Diagram



Description (continued)

than the more traditional open-collector output switches. Additionally, the system designer gains inherent diagnostics because output current normally flows in either of two narrowly-specified ranges. This provides distinct current ranges for $I_{OUT(H)}$ and $I_{OUT(L)}$. Any output current level outside of these two ranges is a fault condition.

Other features of the A1185 and A1186 devices include on-chip transient protection and a Zener clamp on the power supply to protect against overvoltage conditions on the supply line.

The output current of the A1186 switches HIGH in the presence of a south polarity magnetic field of sufficient strength; and switches LOW otherwise, including when there is no significant magnetic field present. The A1185 has an inverted output current level: switching LOW in the presence of a south polarity magnetic field of sufficient strength, and HIGH otherwise.

Both devices are offered in two package styles: LH, a SOT-23W miniature low-profile package for surface-mount applications, and UA, a three-lead ultramini Single Inline Package (SIP) for through-hole mounting. Each package is available in a lead (Pb) free version (suffix, *–T*) with 100% matte tin plated leadframe.

Factory-programmed versions are also available. Refer to: A1145 and A1146.

Selection Guide

Part Number	Packing[1]	Mounting	Ambient, T_A (°C)	Output South (+) Field[2]	Supply Current at Low Output, $I_{CC(L)}$ (mA)
A1185ELHLT-T	7-in. reel, 3000 pieces/reel	Surface mount	–40 to 85	Low	5 to 6.9
A1185EUA-T	Bulk, 500 pieces/bag	SIP through hole			
A1185LUA-T	Bulk, 500 pieces/bag	SIP through hole	–40 to 150		
A1186ELHLT-T	7-in. reel, 3000 pieces/reel	Surface mount	–40 to 85	High	
A1186LLHLT-T	7-in. reel, 3000 pieces/reel	Surface mount	–40 to 150		
A1186LUA-T	Bulk, 500 pieces/bag	SIP through hole			

[1]Contact Allegro for additional packing options.
[2]South (+) magnetic fields must be of sufficient strength.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

ELECTRICAL CHARACTERISTICS over the operating voltage and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage[1]	V_{CC}	Device powered on	3.5	–	24	V
Supply Current[2]	$I_{CC(L)}$	B > B_{OP} for A1185; B < B_{RP} for A1186	5	–	6.9	mA
	$I_{CC(H)}$	B > B_{OP} for A1186; B < B_{RP} for A1185	12	–	17	mA
Supply Zener Clamp Voltage	$V_{ZSupply}$	I_{CC} = $I_{CC(L)(Max)}$ + 3 mA; T_A = 25°C	28	–	40	V
Supply Zener Clamp Current[3]	$I_{ZSupply}$	V_{Supply} = 28 V	–	–	9.9	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V	–	–	1.6	mA
Output Slew Rate[4]	di/dt	No bypass capacitor; capacitance of the oscilloscope performing the measurement = 20 pF	–	36	–	mA/µs
Chopping Frequency	f_C		–	200	–	kHz
Power-On Time[5]	t_{on}	After factory trimming; with and without bypass capacitor (C_{BYP} = 0.01 µF)	–	–	25	µs
Power-On State[6,7]	POS	$t_{on} \le t_{on(max)}$; V_{CC} slew rate > 25 mV/µs	–	HIGH	–	–

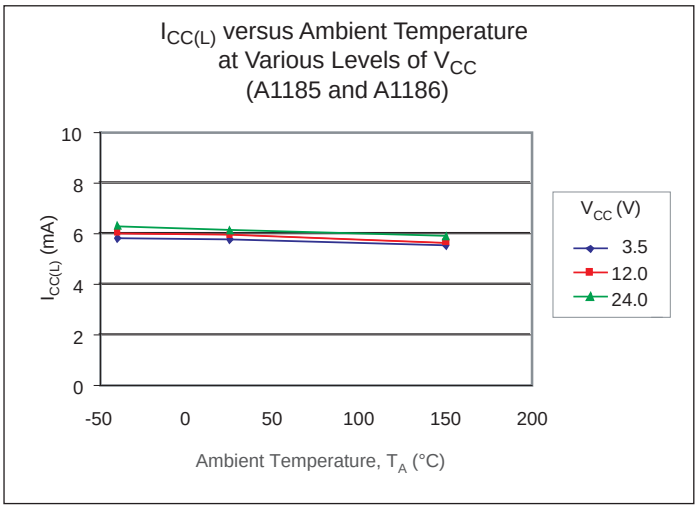
[1]V_{CC} represents the generated voltage between the VCC pin and the GND pin.
[2]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[3]$I_{ZSUPPLY(max)}$ = $I_{CCL(max)}$ + 3 mA.
[4]Measured without bypass capacitor between VCC and GND. Use of a bypass capacitor results in slower current change.
[5]Measured with and without bypass capacitor of 0.01 µF. Adding a larger bypass capacitor causes longer Power-On Time.
[6]POS is defined as true only with a V_{CC} slew rate of 25 mV/µs or greater. Operation with a V_{CC} slew rate less than 25 mV/µs can permanently harm device performance.
[7]POS is undefined for $t > t_{on}$ or $B_{RP} < B < B_{OP}$.

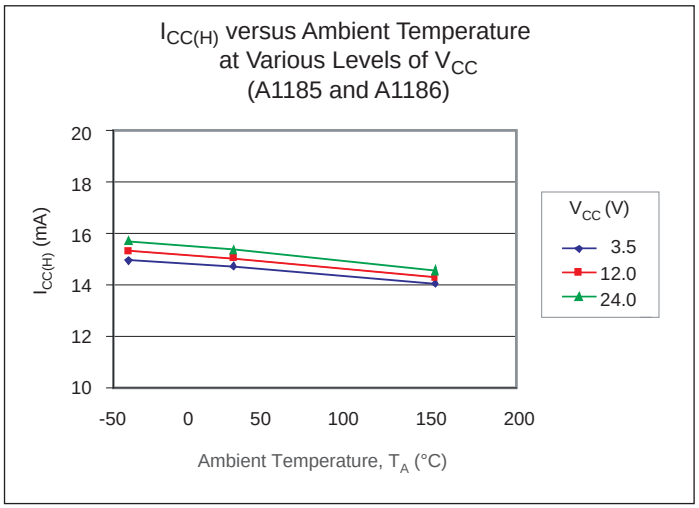
MAGNETIC CHARACTERISTICS[1] over the operating voltage and temperature ranges, unless otherwise specified

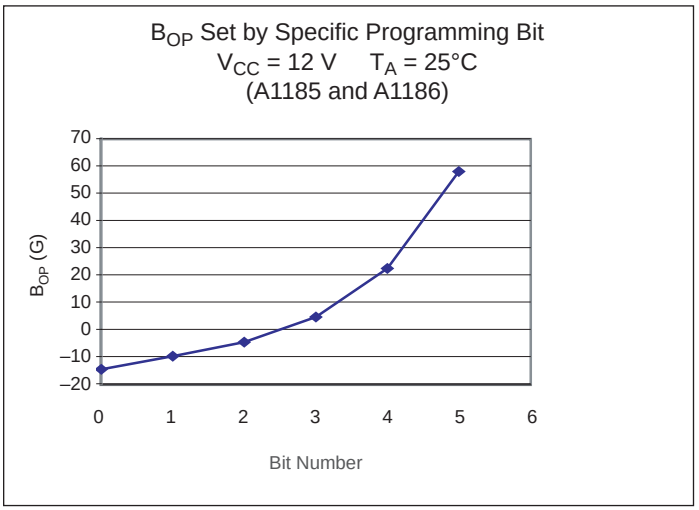
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programmable Operate Point Range	$B_{OPrange}$	I_{CC} = $I_{CC(L)}$ for A1185 I_{CC} = $I_{CC(H)}$ for A1186	10	–	60	G
Initial Operate Point Range	B_{OPinit}	V_{CC} = 12 V	–	–10	10	G
Switchpoint Step Size[2]	B_{RES}	V_{CC} = 5 V, T_A = 25°C	2	4	6	G
Number of Programming Bits	–	Switchpoint setting	–	5	–	Bit
		Programming locking	–	1	–	Bit
Temperature Drift of B_{OP}	ΔB_{OP}		–	–	±20	G
Hysteresis	B_{HYS}	B_{HYS} = B_{OP} – B_{RP}	5	15	30	G

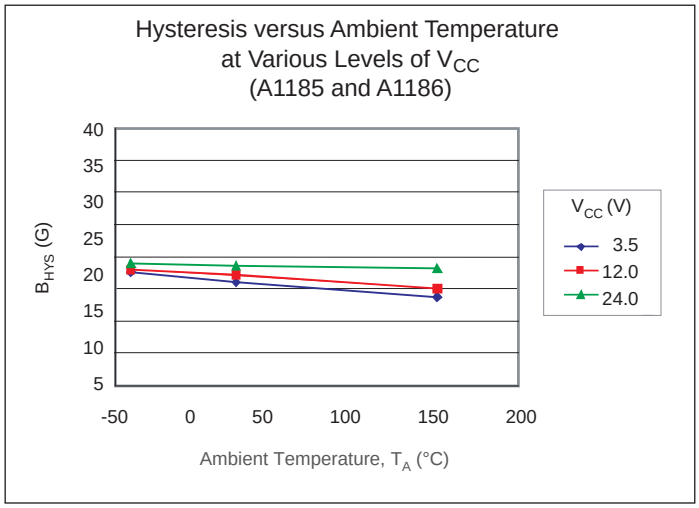
[1]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[2]The range of values specified for B_{RES} is a maximum, derived from the cumulative programming bit errors.

Characteristic Data









Device Qualification Program

Contact Allegro for information.

EMC (Electromagnetic Compatibility) Requirements

Contact your local representative for EMC results.

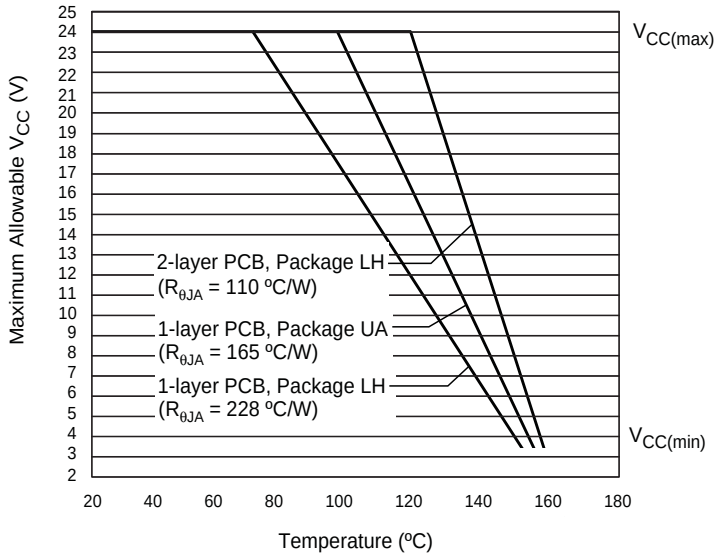
Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-2
Direct RF Injection	ISO 11452-7
Bulk Current Injection	ISO 11452-4
TEM Cell	ISO 11452-3

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

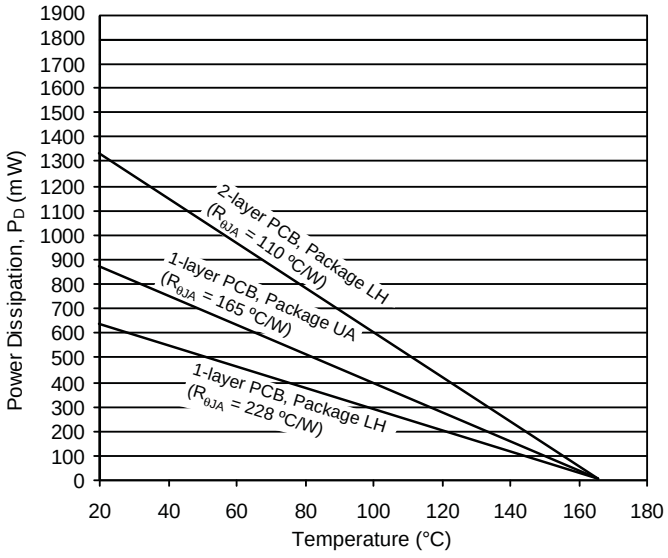
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro Web site.

Power Derating Curve



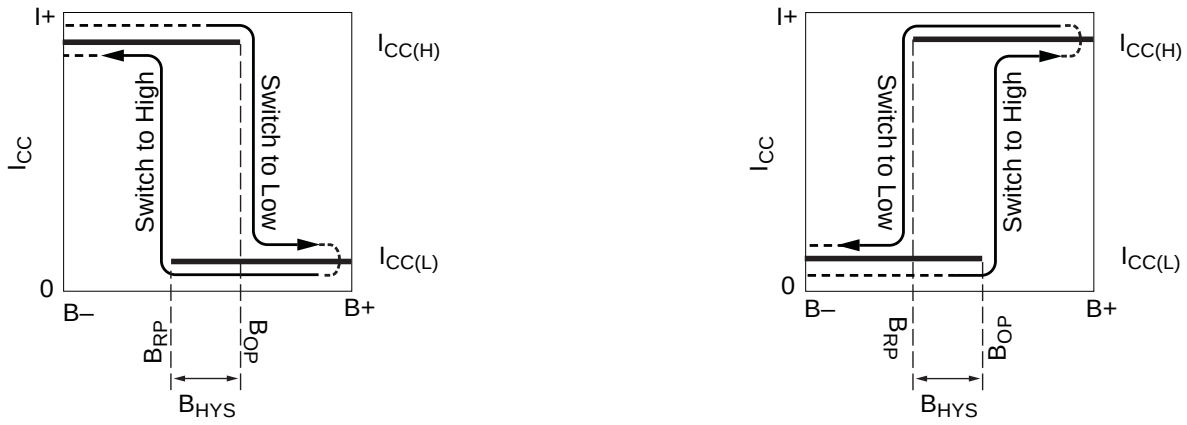
Power Dissipation versus Ambient Temperature



Functional Description

Operation

The output, I_{CC}, of the A1185 switches low after the magnetic field at the Hall element exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes high. The differences between the magnetic operate and release point is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The A1186 device switches with opposite polarity for similar B_{OP} and B_{RP} values, in comparison to the A1185 (see figure 1).



(A) A1185

(B) A1186

Figure 1. Alternative switching behaviors are available in the A118x device family. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

Chopper Stabilization Technique

A limiting factor for switchpoint accuracy when using Hall effect technology is the small signal voltage developed across the Hall element. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall element device. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at base band while the DC offset becomes a high frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed.

The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample-and-hold technique is used, where the sampling is performed at twice the chopper frequency (400KHz). The sampling demodulation process produces higher accuracy and faster signal processing capability. Using this chopper stabilization approach, the chip is desensitized to the effects of temperature and stress. This technique produces devices that have an extremely stable quiescent Hall output voltage, is immune to thermal stress, and has precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of switching with a magnetic field is slightly affected using a chopper technique. The Allegro high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that may notice the degradation are those that require the precise sensing of alternating magnetic fields such as ring magnet speed sensing. For those applications, Allegro recommends the “low jitter” family of digital devices.

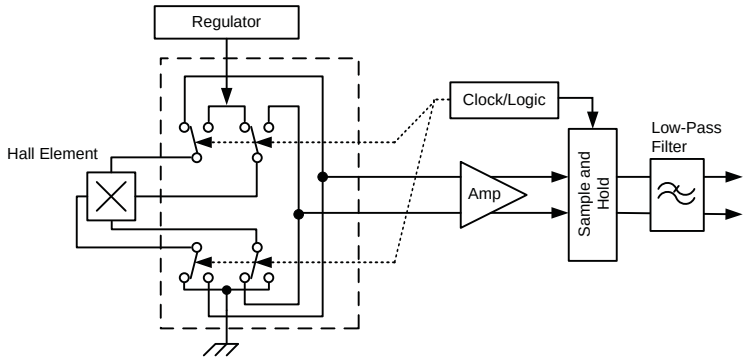


Figure 2. Chopper stabilization circuit (dynamic quadrature offset cancellation)

Application Information

For additional general application information, visit the Allegro Web site at www. allegromicro.com.

Typical Application and Programming Circuit

The A118x family of devices MUST be protected by an external bypass capacitor, C_{BYP}, connected between the supply pin, VCC, and the ground pin, GND, of the device. C_{BYP} reduces both external noise and the noise generated by the chopper-stabilization function. As shown in figure 3, a 0.01 µF capacitor is typical. (For programming the device, a 0.1 µF capacitor is recommended for proper fuse blowing.)

Installation of C_{BYP} must ensure that the traces that connect it to the A118x pins are no greater than 5 mm in length. (For programming the device, the capacitor may be further away from the device, including mounting on the board used for programming the device.)

C_{BYP} serves only to protect the A118x internal circuitry. All high-frequency interferences conducted along the supply lines are passed directly to the load through C_{BYP}. As a result, the load ECU (electronic control unit) must have sufficient protection, other than C_{BYP}, installed in parallel with the A118x.

A series resistor on the supply side, R_S (not shown), in combination with C_{BYP}, creates a filter for EMI pulses.

When determining the minimum V_{CC} requirement of the A118x device, the voltage drops across R_S and the ECU sense resistor, R_{SENSE}, must be taken into consideration. The typical value for R_{SENSE} is approximately 100 Ω. (All programming, including code and lock-bit programming, should be done with direct connections to VCC and GND, with the use of a 0.1uF bypass capacitor. Programming across the series resistor or sense resistor may not allow enough energy to properly blow the fuses in the device, as required for proper programming. The result would be incorrect switchpoints.

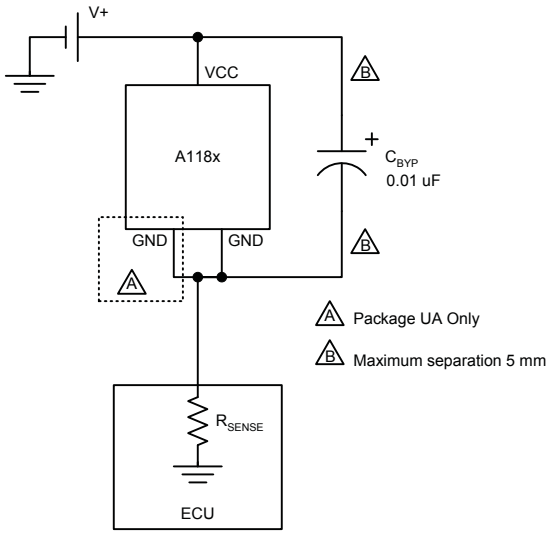


Figure 3. Typical application circuit

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 17 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91\ mW \div 17\ mA = 5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Programming Protocol

The operate switchpoint, B_{OP}, can be field-programmed. To do so, a coded series of voltage pulses through the VCC pin is used to set bitfields in onboard registers. The effect on the device output can be monitored, and the registers can be cleared and set repeatedly until the required B_{OP} is achieved. To make the setting permanent, bitfield-level solid state fuses are blown, and finally, a device-level fuse is blown, blocking any further coding. It is not necessary to program the release switchpoint, B_{RP}, because the difference between B_{OP} and B_{RP}, referred to as the hysteresis, B_{HYS}, is fixed.

The range of values between $B_{OP(min)}$ and $B_{OP(max)}$ is scaled to 31 increments. The actual change in magnetic flux (G) represented by each increment is indicated by B_{RES} (see the Operating Characteristics table; however, testing is the only method for verifying the resulting B_{OP}). For programming, the 31 increments are individually identified using 5 data bits, which are physically represented by 5 bitfields in the onboard registers. By setting these bitfields, the corresponding calibration value is programmed into the device.

Three voltage levels are used in programming the device: a low voltage, V_{PL}, a minimum required to sustain register settings; a mid-level voltage, V_{PM}, used to increment the address counter in the device; and a high voltage, V_{PH}, used to separate sets of V_{PM} pulses (when short in duration) and to blow fuses (when long in duration). A fourth voltage level, essentially 0 V, is used to clear the registers between pulse sequences. The pulse values are shown in the Programming Protocol Characteristics table and in figure 4.

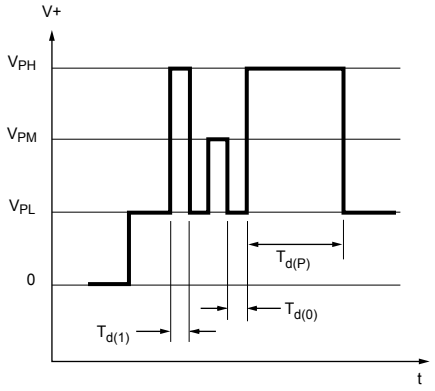


Figure 4. Pulse amplitudes and durations

Additional information on device programming and programming products is available on www. allegromicro.com. Programming hardware is available for purchase, and programming software is available free of charge.

Code Programming. Each bitfield must be individually set. To do so, a pulse sequence must be transmitted for each bitfield that is being set to 1. If more than one bitfield is being set to 1, all pulse sequences must be sent, one after the other, without allowing V_{CC} to fall to zero (which clears the registers).

The same pulse sequence is used to provisionally set bitfields as is used to permanently set bitfield-level fuses. The only difference is that when provisionally setting bitfields, no fuse-blowing pulse is sent at the end of the pulse sequence.

PROGRAMMING PROTOCOL CHARACTERISTICS, over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programming Voltage[1]	V_{PL}	Minimum voltage range during programming	4.5	5.0	5.5	V
	V_{PM}		11.5	12.5	13.5	V
	V_{PH}		25	26	27	V
Programming Current[2]	I_{PP}	t_r = 11 µs; 5 V → 26 V; C_{BYP} = 0.1 µF	-	190	-	mA
Pulse Width	$t_{d(0)}$	OFF time between programming bits	20	-	-	µs
	$t_{d(1)}$	Pulse duration for enable and addressing sequences	20	-	-	µs
	$t_{d(P)}$	Pulse duration for fuse blowing	100	300	-	µs
Pulse Rise Time	t_r	V_{PL} to V_{PM}; V_{PL} to V_{PH}	5	-	20	µs
Pulse Fall Time	t_f	V_{PM} to V_{PL}; V_{PH} to V_{PL}	5	-	100	µs

[1]Programming voltages are measured at the VCC pin.
[2]A bypass capacitor with a minimum capacitance of 0.1 µF must be connected from VCC to the GND pin of the A118x device in order to provide the current necessary to blow the fuse.

The pulse sequences consist of the following groups of pulses:

1. An enable sequence.
2. A bitfield address sequence.
3. When permanently setting the bitfield, a long V_{PH} fuse-blowing pulse. (Note: Blown bit fuses cannot be reset.)
4. When permanently setting the bitfield, the level of V_{CC} must be allowed to drop to zero between each pulse sequence, in order to clear all registers. However, when provisionally setting bitfields, V_{CC} must be maintained at V_{PL} between pulse sequences, in order to maintain the prior bitfield settings while preparing to set additional bitfields.

Bitfields that are not set are evaluated as zeros. The bitfield-level fuses for 0 value bitfields are never blown. This prevents inadvertently setting the bitfield to 1. Instead, blowing the device-level fuse protects the 0 bitfields from being accidentally set in the future.

When provisionally trying the calibration value, one pulse sequence is used, using decimal values. The sequence for setting the value 5_{10} is shown in figure 5.

When permanently setting values, the bitfields must be set individually, and 5_{10} must be programmed as binary 101. Bit 3 is set to 1 (000100_2, which is 4_{10}), then bit 1 is set to 1 (000001_2, which is 1_{10}). Bit 2 is ignored, and so remains 0.Two pulse sequences for permanently setting the calibration value 5 are shown in figure 6. The final V_{PH} pulse is maintained for a longer period, enough to blow the corresponding bitfield-level fuse.

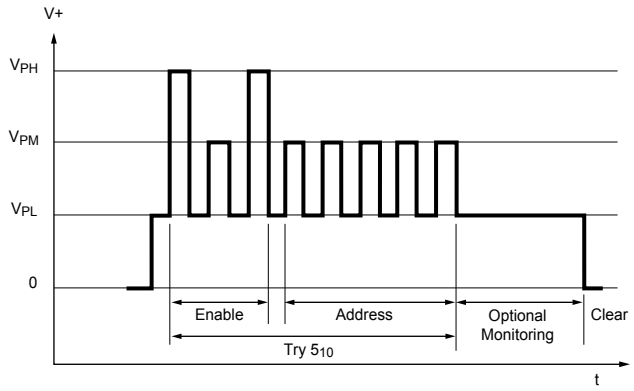


Figure 5. Pulse sequence to provisionally try calibration value 5.

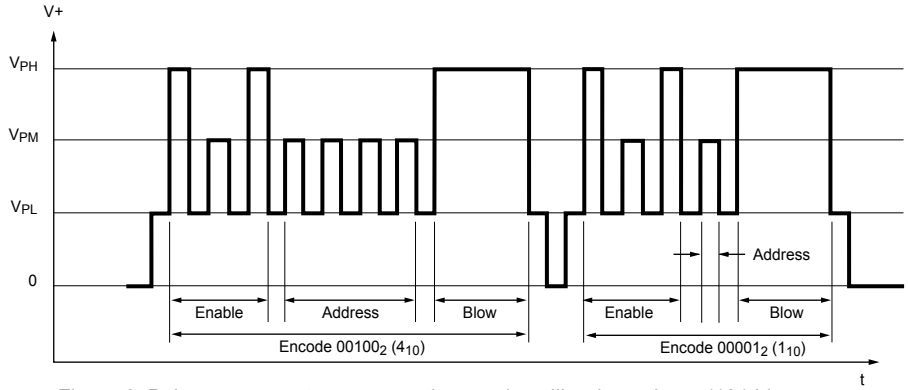


Figure 6. Pulse sequence to permanently encode calibration value 5 (101 binary, or bitfield address 3 and bitfield address 1).

Enabling Addressing Mode. The first segment of code is a keying sequence used to enable the bitfield addressing mode. As shown in figure 7, this segment consists of one short V_{PH} pulse, one V_{PM} pulse, and one short V_{PH} pulse, with no supply interruptions. This sequence is designed to prevent the device from being programmed accidentally, such as by noise on the supply line.

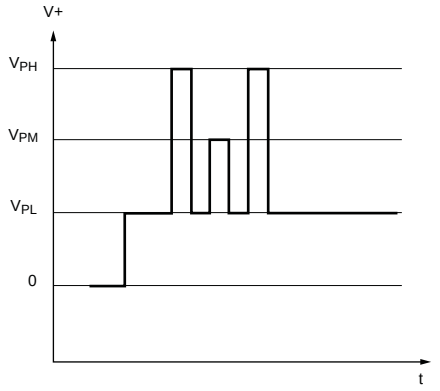


Figure 7. Addressing mode enable pulse sequence

Address Selection. After addressing mode is enabled, the target bitfield address, is indicated by a series of V_{PM} pulses, as shown in figure 8.

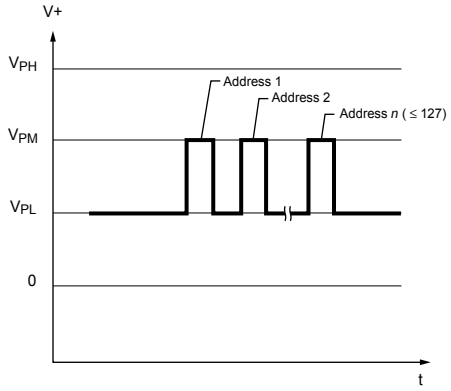


Figure 8. Pulse sequence to select addresses

Lock Bit Programming. After the desired B_{OP} calibration value is programmed, and all of the corresponding bitfield-level fuses are blown, the device-level fuse should be blown. To do so, the lock bit (bitfield address 32) should be encoded as 1 and have its fuse blown. This is done in the same manner as permanently setting the other bitfields, as shown in figure 9.

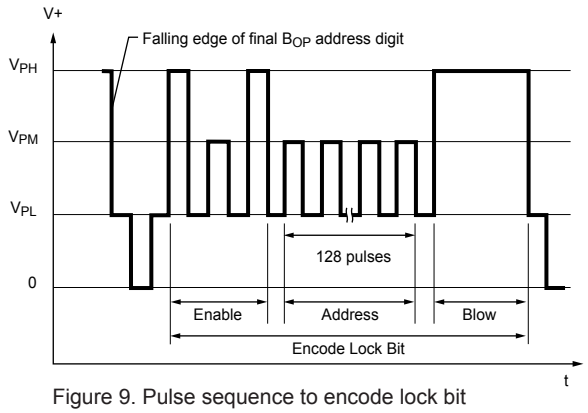
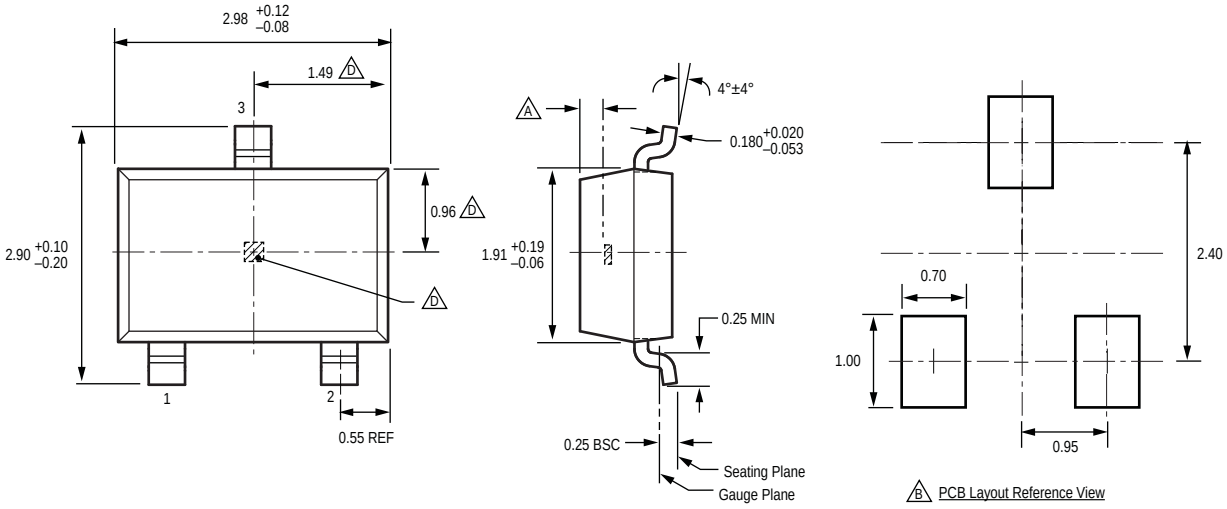


Figure 9. Pulse sequence to encode lock bit

Package LH, 3-Pin (SOT-23W)



N = Last two digits of device part number
T = Temperature code

For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

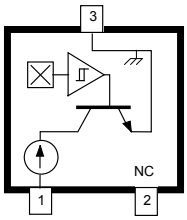
C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Pin-out Drawings

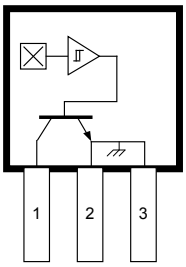
Package LH, 3-pin SOT

1. VCC
2. No connection
3. GND

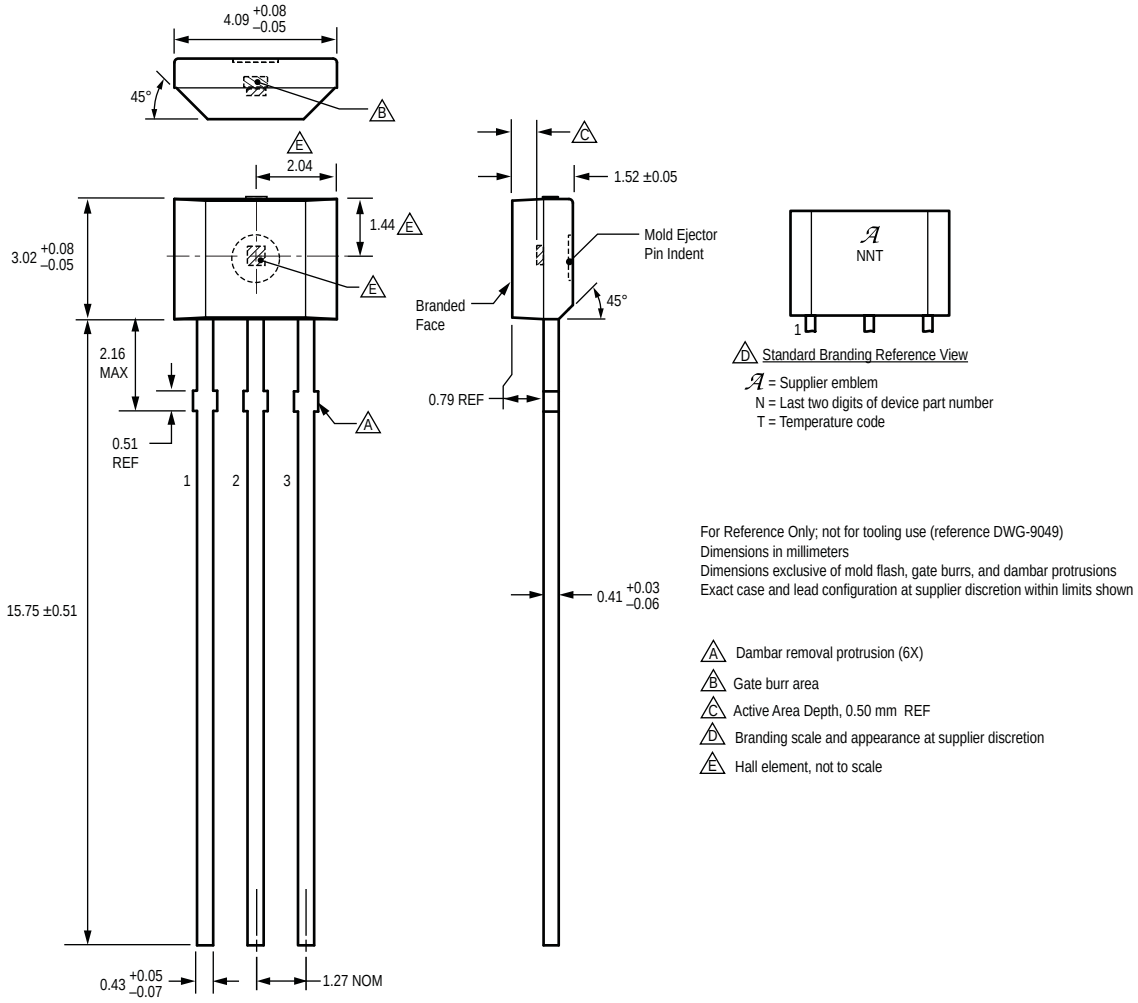


Package UA, 3-pin SIP

1. VCC
2. GND
3. GND



Package UA, 3-Pin SIP



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