THE DATASHEET OF

CYII4SM6600-EVAL

www.win-source.net 0086-755-83957316

IBIS4-6600 CYII4SM6600AB

6.6 MP CMOS Image Sensor

Features

- 2210 (H) x 3002 (V) Active Pixels
- 3.5 µm X 3.5 µm Square Pixels
- 1 inch Optical Format
- Monochrome or Color Digital Output
- Frame Rate:
  - 5 fps (2210 x 3002)
  - 89 fps (640 x 480)
- High Dynamic Range Modes: Double Slope, Non Destructive Read out (NDR)
- Electronic Rolling Shutter
- Master Clock: 40 MPS/40 MHz
- Limited Supplies: 2.5V and 3.3V
- -30°C to +65°C Operational Temperature Range
- 68-Pin LCC Package
- Power Dissipation: 0.19W

Applications

- Machine vision
- Biometry
- Document Scanning

Description

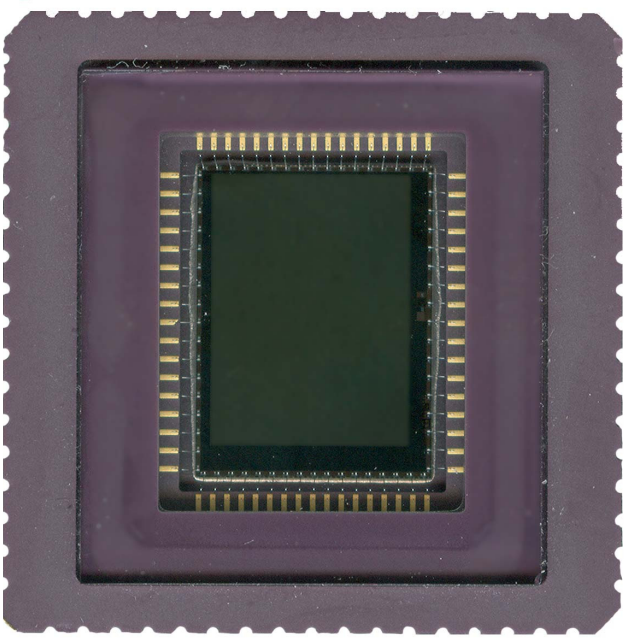
The IBIS4-6600 is a solid-state CMOS image sensor that integrates complete analog image acquisition, and a digitizer and digital signal processing system on a single chip. This image sensor has a resolution of 6.6 MPixel with 2210 x 3002 active pixels. The image size is fully programmable for user-defined windows. The pixels are on a 3.5 µm pitch. This sensor is available in a Monochrome version or Bayer (RGB) patterned color filter array.

The user programmable row and column start and stop positions enable windowing down to 2x1 pixel window for digital zoom. Sub sampling reduces resolution while maintaining the constant field of view. The analog video output of the pixel array is processed by an on-chip analog signal pipeline. Double Sampling (DS) eliminates the fixed pattern noise.

The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a three-wire Serial-Parallel (SPI) interface. It operates with a single 2.5V power supply and requires only one master clock for operation up to 40 MHz. It is housed in a 68-pin ceramic LCC package.

This data sheet enables you to develop a camera system, based on the described timing and interfacing given in the following sections.

Figure 1. IBIS4-6600 Image Sensor



Ordering Information

Marketing Part Number	Description	Package
CYII4SM6600AB-QDC	Mono with Glass	68-pin LCC
CYII4SM6600AB-QWC	Mono without Glass	
CYII4SE6600AB-QDC	Color micro lens with Glass	
CYII4SE6600AB-QFCH	Color micro lens with IR Coating, High Grade	
CYII4SM6600-EVAL	Mono Demo Kit	Demo Kit
CYII4SC6600-EVAL	Color Demo Kit	

Specifications

General Specifications

Parameter	Specification	Remarks
Pixel Architecture	3T-Pixel	
Pixel Size	3.5 µm x 3.5 µm	The resolution and pixel size results in a 7.74 mm x 10.51 mm optical active area.
Resolution	2210 x 3002	
Pixel Rate	40 MHz	Using a 40 MHz system clock and 1 or 2 parallel outputs
Shutter Type	Electronic Rolling Shutter	
Full Frame Rate	5 frames/second	Increases with ROI read out and/or subsampling

Electro Optical Specifications

Parameter	Specification	Remarks
FPN (local)	<0.20%	RMS% of saturation signal
PRNU (local)	<1.5%	RMS of signal level
Conversion Gain	Conversion Gain	At output (measured)
Output Signal Amplitude	0.6V	At nominal conditions
Saturation Charge	21.500 e-	
Sensitivity (peak)	411 V.m^2/W.s 4.83 V/lux.s	At 650 nm (85 lux = 1 W/m^2)
Sensitivity (visible)	328 V.m^2/W.s 2.01 V/lux.s	400-700 nm (163 lux = 1 W/m^2)
Peak QE * FF Peak Spectral Response	25% 0.13 A/W	Average QE*FF = 22% (visible range) Average SR*FF = 0.1 A/W (visible range) See the section Spectral Response Curve on page 3.
Fill Factor	35%	Light sensitive part of pixel (measured)
Dark Current	3.37 mV/s 78 e-/s	Typical value of average dark current of the whole pixel array (at 21°C)
Dark Signal Non Uniformity	8.28 mV/s 191 e-/s	Dark current RMS value (at 21°C)
Temporal Noise	24 RMS e-	Measured at digital output (in the dark)
S/N Ratio	895:1 (59 dB)	Measured at digital output (in the dark)
Spectral Sensitivity Range	400 - 1000 nm	
Optical Cross Talk	15% 4%	To the first neighboring pixel To the second neighboring pixel
Power Dissipation	190 mW	Typical (including ADCs)

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Spectral Response Curve

Figure 2. Spectral Response Curve

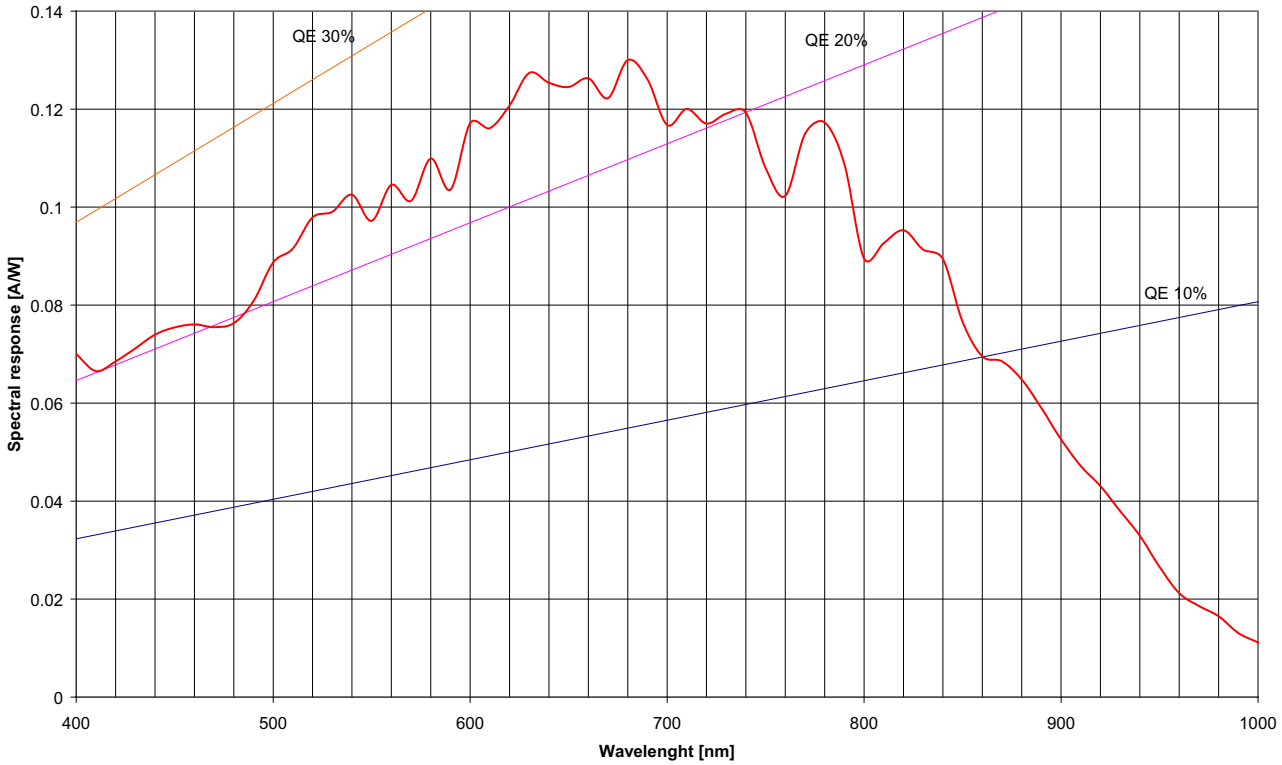

Figure 2 shows the characteristics of the spectral response. The curve is measured directly on the pixels. It includes the effects of nonsensitive areas in the pixel, for example, interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is 25% approximately 650 nm. In view of a fill factor of 35%, the QE is close to 70% between 500 and 700 nm.

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Electro Voltaic Response Curve

Figure 3. Electro Voltaic Response Curve

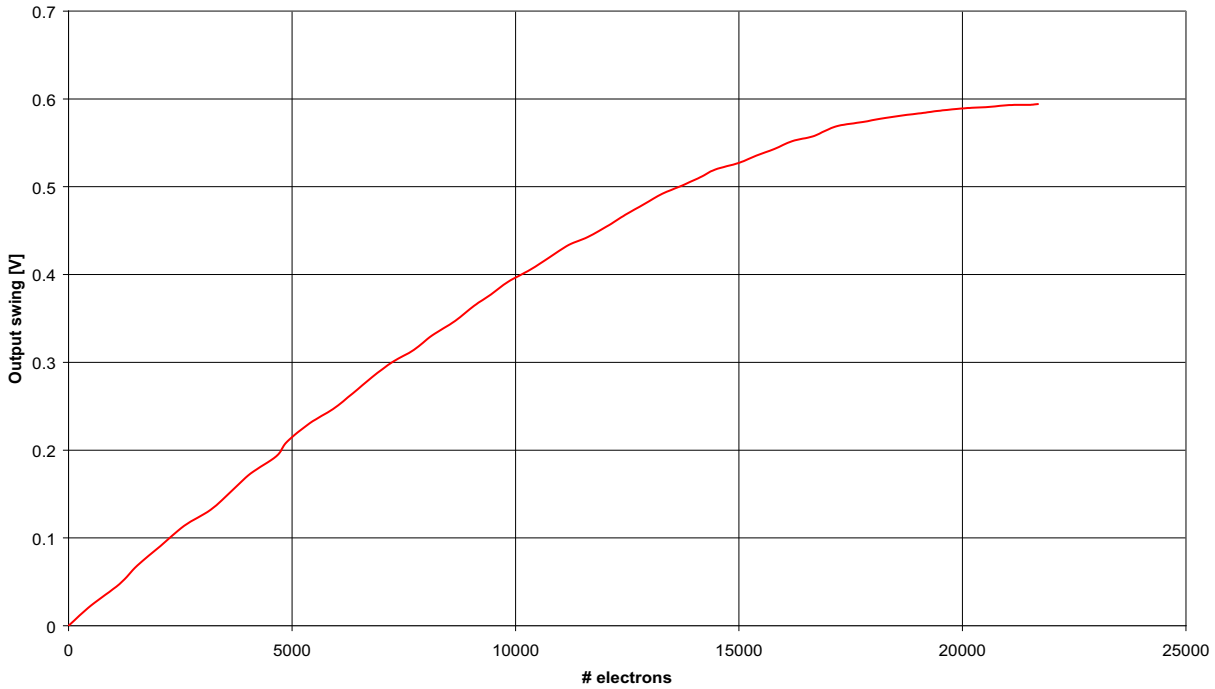

Figure 3 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters, for example, integration time. The voltage to electrons conversion gain is 43 µV/electron.

Table 1. Features and General Specifications

Feature	Specification/Description
Electronic shutter type	Rolling shutter
Integration time control	60 µs - 1/frame period
Windowing (ROI)	Randomly programmable ROI read out
Sub Sampling Modes	Several sub sample modes can be programmed (refer Table 7 on page 12)
Extended Dynamic Range	Dual slope (up to 90 dB optical dynamic range) and nondestructive read out mode
Analog Output	The output rate of 40 Mpixels/s can be achieved with two analog outputs, each working at 20 Mpixel/s
Digital Output	Two on-chip 10-bit ADCs at 20 Msamples/s are multiplexed to one digital 10-bit output at 40 Msamples/s
Supply Voltage V_{DD}	Nominal 2.5V (some supplies require 3.3V for extended dynamic range)
Logic Levels	2.5V
Interface	Serial-to Parallel Interface (SPI)
Package	68-pins LCC

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Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested. Stresses beyond those listed under Table 2 may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}[1]	DC Supply Voltage	–0.5 to 3.3	V
V_{IN}	DC Input Voltage	–0.5 to (V_{DD} + 0.5)	V
V_{OUT}	DC Output Voltage	–0.5 to (V_{DD} + 0.5)	V
I_{IO}	DC Current Drain Per Pin; Any Single Input or Output	± 50	mA
T_L	Lead Temperature (5 seconds soldering)	350	°C
T_{ST}	Storage Temperature	–30 to +85	°C
H	Humidity (Relative)	85% at 85 °C	
ESD	ESD Susceptibility	2000	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	DC Supply Voltage	2.5	2.5	3.3	V
T_A	Commercial Operating Temperature	–30	24	+65	°C

All parameters are characterized for DC conditions after thermal equilibrium is established. Unused inputs must always be tied to an appropriate logic level, for example, V_{DD} or GND.

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields. However, you must take normal precautions to avoid applying voltages higher than the maximum rated voltages to this high impedance circuit.

DC Electrical Conditions

Symbol	Characteristic	Condition	Min	Max	Unit
V_{IH}	Input High Voltage		V_{DD}-0.5		V
V_{IL}	Input Low Voltage		–0.6	0.6	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or GND	–10	+10	µA
V_{OH}	Output High Voltage	V_{DD}=min; I_{OH}= –100 mA	V_{DD}-0.5		V
V_{OL}	Output Low Voltage	V_{DD}=min; I_{OH}= 100 mA		0.5	V
I_{DD}	Operating Current	System clock <= 40 MHz	70	80	mA

Note
1. V_{DD} = V_{DDD} = V_{DDA} (V_{DDD} is supply to digital circuit, V_{DDA} to analog circuit).

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Sensor Architecture and Operation

Floor Plan

Figure 4. Floor Plan

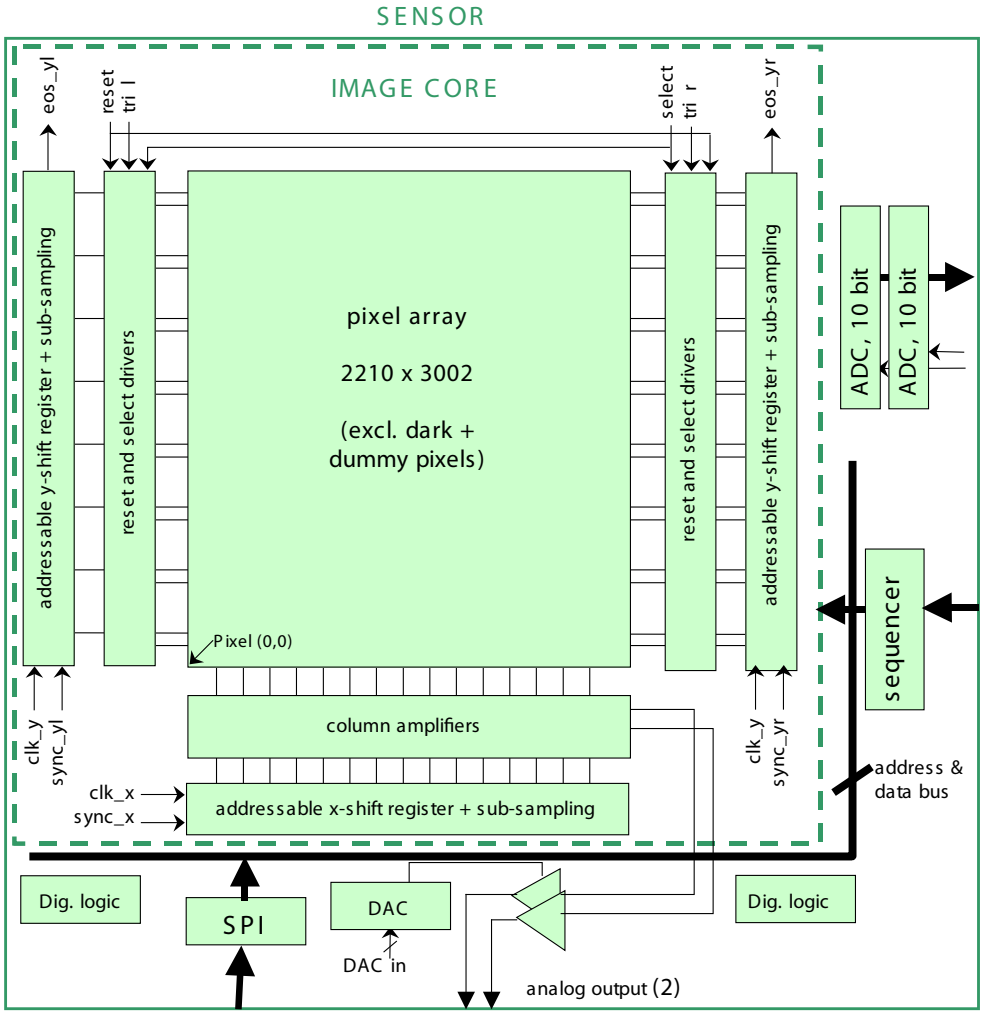

Figure 4 shows the architecture of the designed image sensor. It consists of the pixel array, shift registers for the readout in x and y direction, parallel analog output amplifiers, and column amplifiers that correct for the fixed pattern noise caused by threshold voltage nonuniformities. Reading out the pixel array starts by applying a y clock pulse to select a new row, followed by a calibration sequence to calibrate the column amplifiers (row blanking time). Depending on external bias resistors and timing, typically this sequence takes about seven seconds every line (baseline). This sequence is necessary to remove the Fixed Pattern Noise of the pixel and of the column amplifiers themselves (by a Double Sampling technique). Pixels can also be read out in a nondestructive manner.

Two DACs are added to make the offset level of the pixel values adjustable and equal for the two output buses. A third DAC is used to connect the buses to a stable voltage during the row blanking period, or reset the buses continuously in case of a nondestructive readout.

Two 10-bit ADCs running at 20 Msamples/s convert the analog pixel values. The digital outputs are multiplexed to one digital 10-bit output at 40 Msamples/s. Note that these blocks are electrically completely isolated from the sensor part, except for the multiplexer, for which the settings are uploaded through the shared address and data bus.

The x and y shift registers have a programmable starting point. The possibilities of the starting point are limited because of limitations imposed by subsampling requirements. The start address is uploaded through the serial to parallel interface.

Most of the signals for the image core shown in Figure 4 are generated on-chip by the sequencer. This sequencer also allows running the sensor in basic modes, not fully autonomous.

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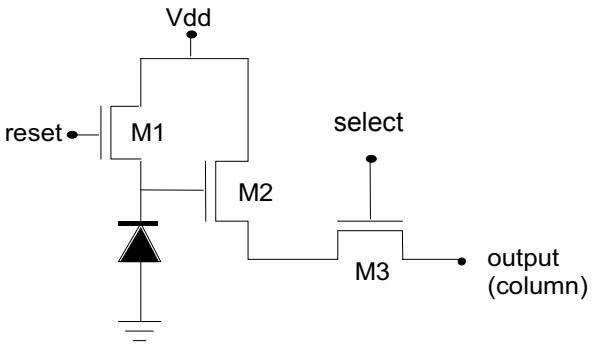
Pixel

Architecture

The pixel architecture is the classic three-transistor pixel, as shown in Figure 5 The pixel is implemented using the high fill factor technique patented by FillFactory (US patent No. 6,225,670 and others).

Figure 5. 3T Pixel Architecture



FPN and PRNU

Fixed Pattern Noise correction is done on-chip. Raw images taken by the sensor typically feature a residual (local) FPN of 0.35% RMS of the saturation voltage.

The Photo Response Non Uniformity (PRNU), caused by the mismatch of photodiode node capacitances, is not corrected on chip. Measurements indicate that the typical PRNU is about 1.5% RMS of the signal level.

Color Filter Array

The IBIS4-6600 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a green filter and is situated on a green-red row. Green1 and Green2 are separately processed color filters and have a different spectral response. Green1 pixels are located on a blue-green row, and green2 pixels are located on a green-red row.

Figure 6. RGB Bayer Alignment

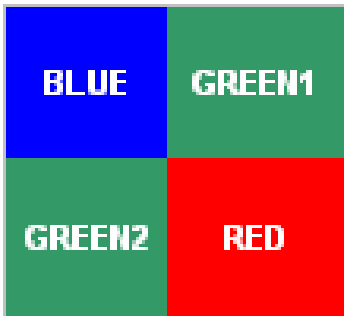


Figure 7 shows the response of the color filter array as function of the wavelength.

Figure 7. Typical Response Curve of the RGB Filters

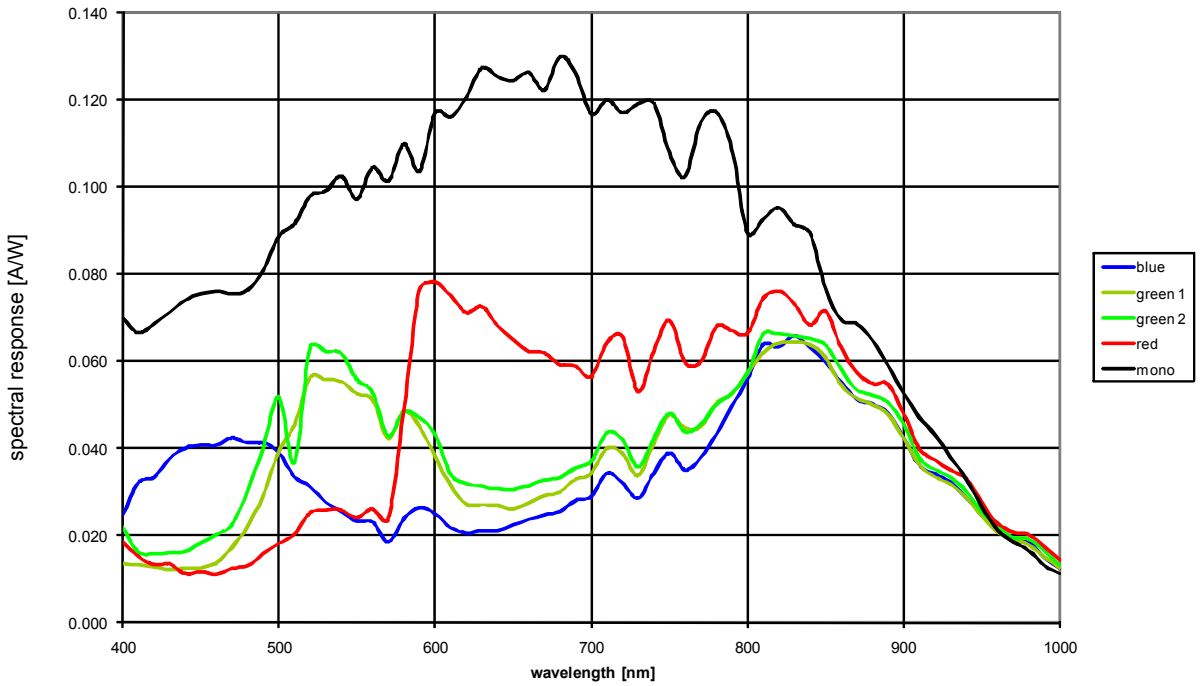


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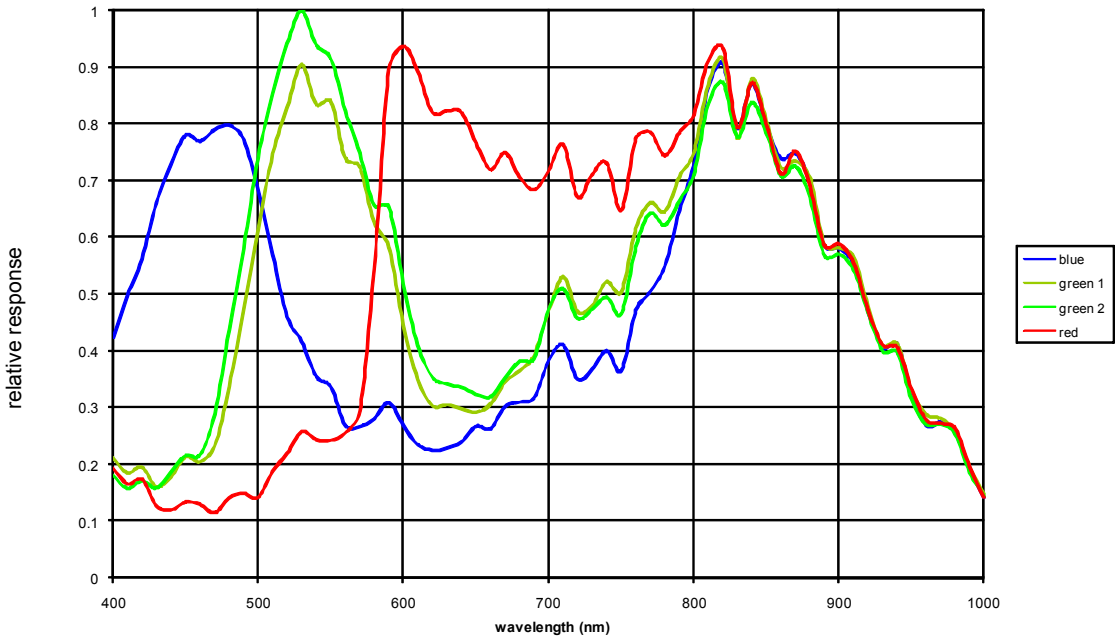
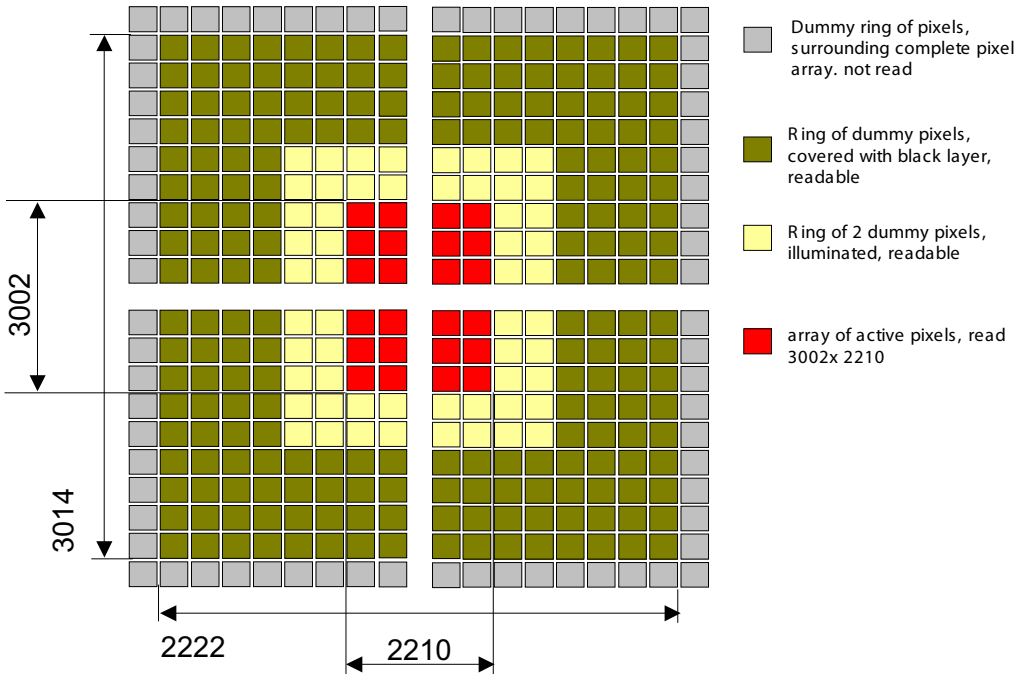
Figure 8. Relative Response Graph



Dark and Dummy Pixels

Figure 9 shows a plan of the pixel array. The sensor is designed in portrait orientation. A ring of dummy pixels surrounds the active pixels. Black pixels are implemented as "optical" black pixels.

Figure 9. Floor Plan Pixel Array



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Pixel Rate

The pixel rate for this sensor is high enough to support a frame rate greater than 75 Hz for a window size of 640 x 480 pixels (VGA format), and 23 pixels over scan in both directions. Taking into account a row blanking time of 7.2 µs (as baseline, refer the following calculations), this requires a minimum pixel rate of approximately 40 MHz. The final bandwidth of the column amplifiers, output stage, and more is determined by external bias resistors. Taking into account a pixel rate of 40 MHz, a full frame rate of a little more than 5 frames/s is obtained.

The frame period of the IBIS4-6600 sensor is calculated as:

=> Frame period = (Nr. Lines * (RBT + pixel period * Nr. Pixels))

In this equation:

Nr. Lines: Number of Lines read out each frame (Y)

Nr. Pixels: Number of pixels read out each line (X)

RBT: Row Blanking Time = 7.2 µs (typical)

Pixel period: 1/40 MHz = 25 ns

Example: Read out time of the full resolution at nominal speed (40 MHz pixel rate):

=> Frame period = (3002 * (7.2 µs + 25 ns * 2210)) = 187.5 ms => 5.33 fps.

Region of Interest (ROI) Read Out

Windowing is easily achieved by uploading the starting point of the x and y-shift registers in the sensor registers (refer Table 10 on page 17). This downloaded starting point initiates the shift register in the x and y-direction, triggered by the Y_START (initiates the Y-shift register) and the Y_CLK (initiates the X-shift register) pulse. The minimum step size for the x-address is 24 (only even start addresses can be chosen) and 1 for the Y-address (every line can be addressed). The frame rate increases in an almost linear manner when fewer pixels are read out. Table 3 lists the achievable frame rates with ROI read out.

Table 3. Frame Rate vs. Resolution

Image Resolution (Y*X)	Frame Rate [frames/s]	Frame Readout Time [ms]	Comment
3002 x 2210	5	187.5	Full resolution
1501 x 1104	14	67	ROI read out
640 x 480	89	11	11

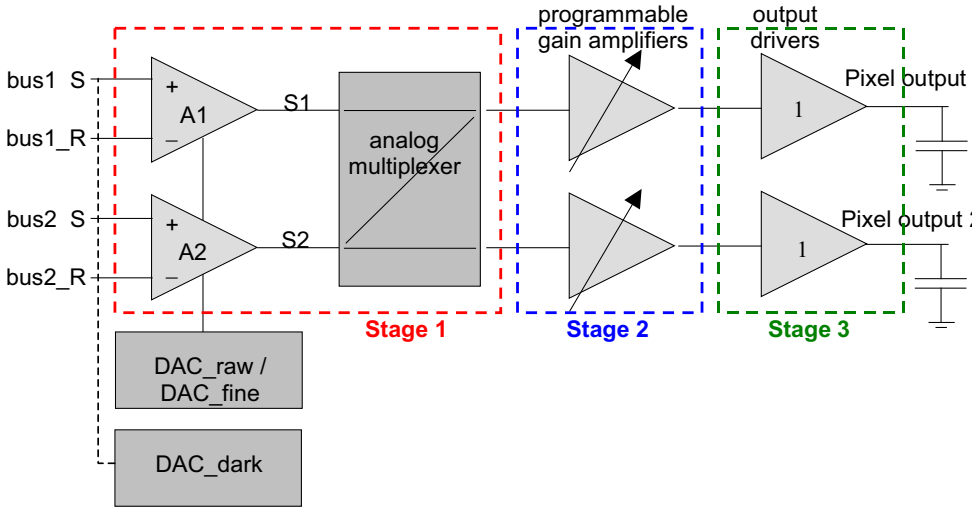
Output Amplifier

The output amplifier subtracts the reset and signal voltages from each other to cancel FPN as much as possible (shown in Figure 10). The DAC that is used for offset adjustment consists of two DACs. One DAC is used for the main offset (DAC_raw). The other enables fine tuning to compensate the offset difference between the signal paths arriving at the two amplifiers A1 and A2 (DAC_fine). With the analog multiplexer, the signals S1 and S2 from the two buses can be combined to one pixel output at full pixel rate (40 MHz). However, the two analog signals S1 and S2 can also be available on two separate output pins to allow a higher pixel rate.

The third DAC (DAC_dark) puts its value on the buses during the calibration of the output amplifier. In case of nondestructive readout (no double sampling), bus1_R and bus2_R are continuously connected to the output of the DAC_fine to provide a reference for the signals on bus1_S and bus2_S.

The complete output amplifier can be put in standby by setting the corresponding bit in the AMPLIFIER register.

Figure 10. Output Amplifier Architecture



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Stage 1: Offset, FPN Correction, and Multiplexing

In the first stage, the signals from the buses are subtracted and the offset from the DACs is added. After a system reset, the analog multiplexer is configured for two outputs (see the bit settings in the AMPLIFIER Register on page 22). In case ONE_OUT is set to 1, the two signals S1 and S2 are multiplexed to one output (output 1). The amplifiers of Stage 2 and Stage 3 of the second output path are then put in standby. The speed and power consumption of the first stage can be controlled through the resistor connected to CMD_OUT_1.

Stage 2: Programmable Gain Amplifier

The second stage provides the gain, which is adjustable between 1.36 and 17.38 in steps of approximately 20.25 (~1.2). An overview of the gain settings is given in Table 4. The speed and power consumption of the second stage can be controlled through the resistor connected to CMD_OUT_2.

Table 4. PGA Gain Settings

Bits	DC Gain	Bits	DC Gain
0000	1.36	1000	5.40
0001	1.64	1001	6.35
0010	1.95	1010	7.44
0011	2.35	1011	8.79
0100	2.82	1100	10.31
0101	3.32	1101	12.36
0110	3.93	1110	14.67
0111	4.63	1111	17.38

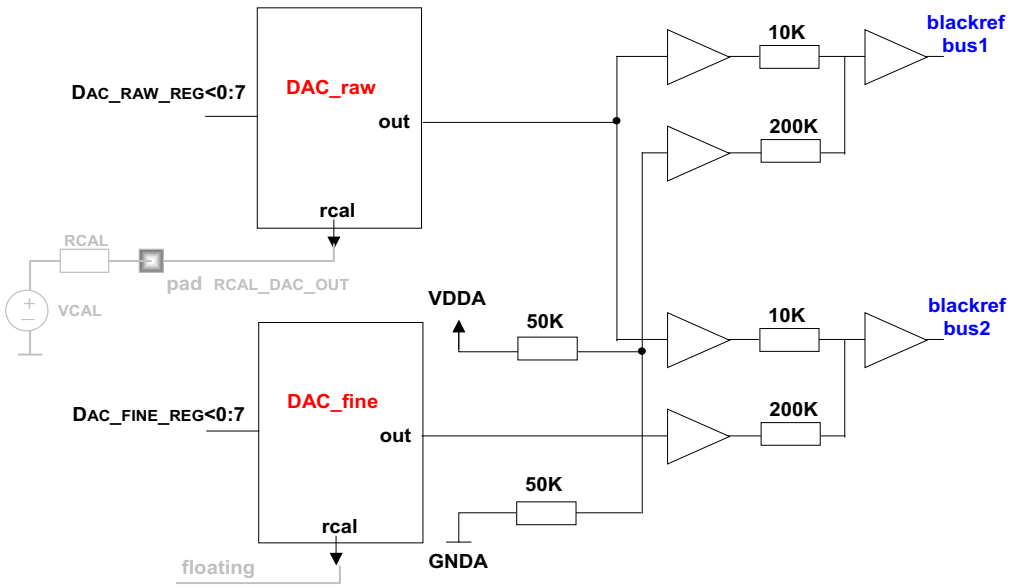
Stage 3: Output Drivers

The speed and power consumption of the third stage can be controlled through the resistor connected to CMD_OUT_3. The output drivers are designed to drive a 20 pF output load at 40 Msamples/s with a bias resistor of 100 kΩ.

Offset DACs

Figure 11 shows how the DAC registers influence the black reference voltages of the two different channels. The offset is mainly given through DAC_raw. DAC_fine can be used to shift the reference voltage of bus 2 up or down to compensate for different offsets in the two channels.

Figure 11. Offset for the Two Channels through DAC_RAW and DAC_FINE



Note that in this figure, "K" represents KΩ.

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Assume that $V_{outfull}$ is the voltage that depends on the bit values that are applied to the DAC and ranges from:

$$V_{outfull} : 0 \ (bit\ values\ 00000000\ ) \ \rightarrow \ VDDA\ (1-\frac{1}{2^8})\ (bit\ values\ 11111111\ )$$

Externally, the output range of DAC_raw can be changed by connecting a resistor Rcal to RCAL_DAC_OUT and applying a voltage V_{cal}. The output voltage V_{out} of DAC_raw follows the relation (R = 10 kΩ).

$$V_{out} = \frac{R + R_{cal}}{2R + R_{cal}} V_{outfull} + \frac{R}{2R + R_{cal}} V_{cal}$$

Special case:

R_{cal} = then $V_{out} = V_{outfull}$ (for example, for DAC_fine)

Rcal = 0, Vcal = GND ..... then $V_{out} = V_{outfull}/2$

A similar relation holds for the output range of DAC_DARK (RCAL_DAC_DARK can be used to tune the output range of this DAC).

Analog to Digital Converter

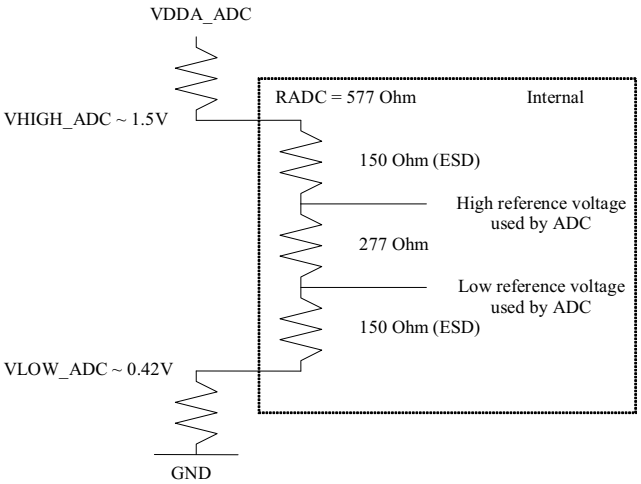
The IBIS4-6600 has a two 10-bit flash analog digital converters. The ADCs are electrically separated from the image sensor. The inputs of the ADC must be tied externally to the outputs of the output amplifiers. One ADC samples the even columns and the other samples the odd columns. Alternatively, one ADC can also sample all the pixels.

Table 5. ADC Specifications

Parameter	Specification
Input Range	Set by External Resistors (Refer the section Setting the ADC Reference Voltages)
Quantization	10 Bits
Nominal Data Rate	20 Msamples/s
DNL(Linear Conversion Mode)	Typ. < 0.4 LSB RMS
INL (Linear Conversion Mode)	Typ. < 3.5 LSB
Input Capacitance	< 2 pF
Conversion Law	Linear/Gamma corrected

Setting the ADC Reference Voltages

Figure 12. ADC Resistor Ladder



The internal resistance has a value of approximately 577 Ω. Only 277 Ω of this internal resistance is actually used as reference for the internal ADC. This causes the actual ADC voltage range to become half of the voltage difference between VHIGH_ADC and VLOW_ADC. This results in the values listed Table 6 for the external resistors.

Table 6. ADC Resistor Values

Resistor	Value (Ω)
RVHIGH_ADC	560
RInternal	577
RVLOWADC	220

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Sub Sample Modes

To increase the frame rate for lower resolution and regions of interest, several sub sampling modes are implemented. The possible sub sample modes are listed in Table 7. The bits can be programmed in the IMAGE_CORE register (refer Table 10 on page 17). To preserve the color information, two adjacent pixels are read in any mode. The number of pixels that is not read varies from mode to mode. This is designed as a repeated block 24 pixels wide, which is the lowest common multiple of the modes described. Including the dummy pixels and the two additional rows/columns, the number of starting coordinates for the x and y shift register is 99 in the X direction and 138 in the Y direction. The total number of pixels, excluding dummy pixels, is a multiple of 24, and two additional pixels to have the same window edges independently of the sub sampling mode.

In the X direction, two columns are always addressed at the same moment, because the signals from the odd and even columns must be put simultaneously on the corresponding bus. In the Y direction, the rows are addressed one by one. This results in slightly different implementations of the sub-sampling modes for the two directions (Refer Figure 13 and Figure 14 on page 13).

Table 7. Subsample Patterns

Mode	Bits	Read	Step	Description
A	000	2	2	Default mode
B	001	2	4	(Skip 2)
C	010	2	6	(Skip 4)
D	011	2	8	(Skip 6)
E	1xx	2	12	(Skip 10)

Figure 13. X-Sub Sampling

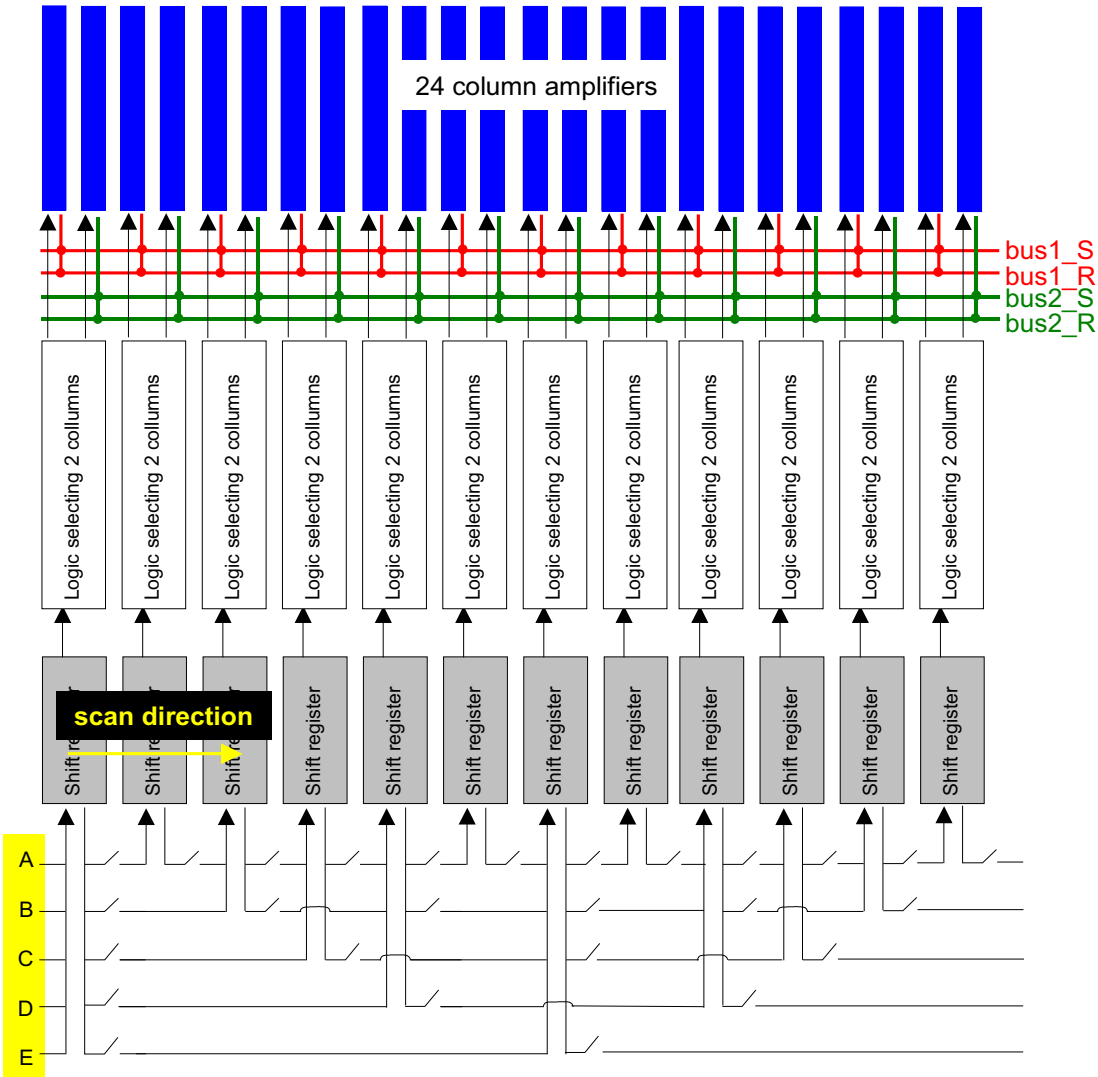

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Figure 14. Y-Sub Sampling

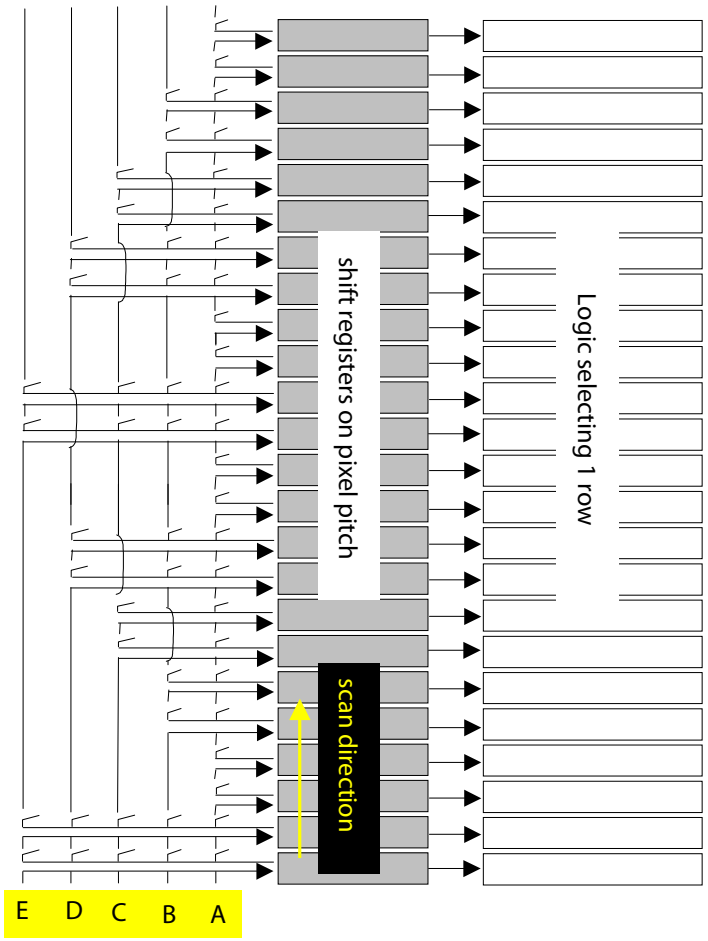

Table 8. Frame Rate vs. Sub Sample Mode

Mode	Ratio	Resolution (Y*X)	Frame time [mS]	Frame time [mS]
A	1:1	3002 x 2210	187.4	5.3
B	1:4	1502 x 1106	52.3	19.1
C	1:9	1002 x 738	25.7	38.9
D	1:16	752 x 554	15.8	63.2
63.2	1:36	502 x 370	8.2	121.2
VGA (p)		640 x 480	12.3	81.5
VGA (p) + 23		663 x 503	13.1	76.4
VGA (l)		480 x 640	11.1	89.9
VGA(l) + 23		503 x 663	11.9	83.7

Figure 15 on page 14 shows the pixels read out in each color sub sampling mode.

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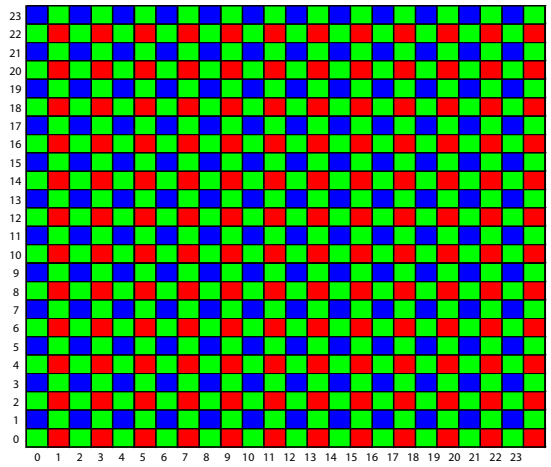
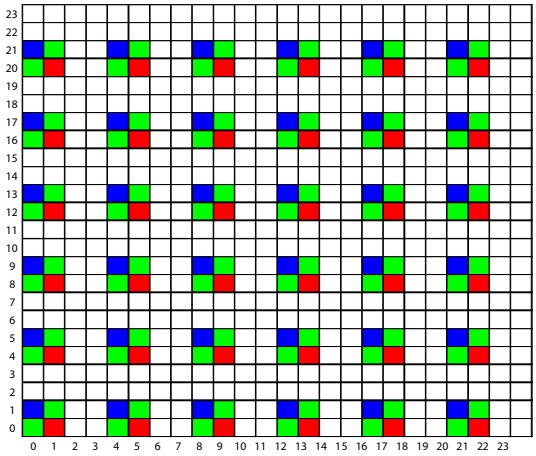
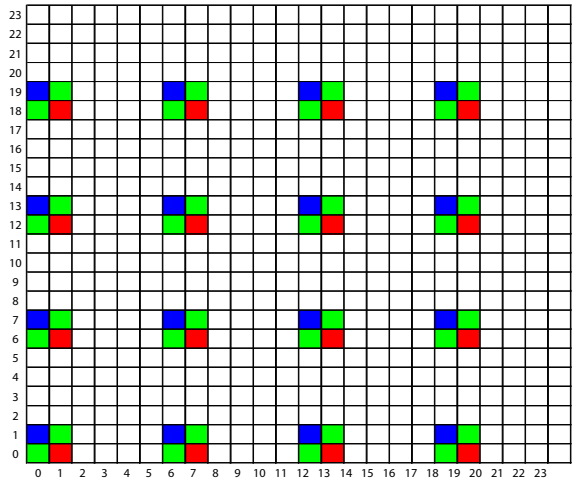
Figure 15. Pixel Readout in Various Subsample Modes



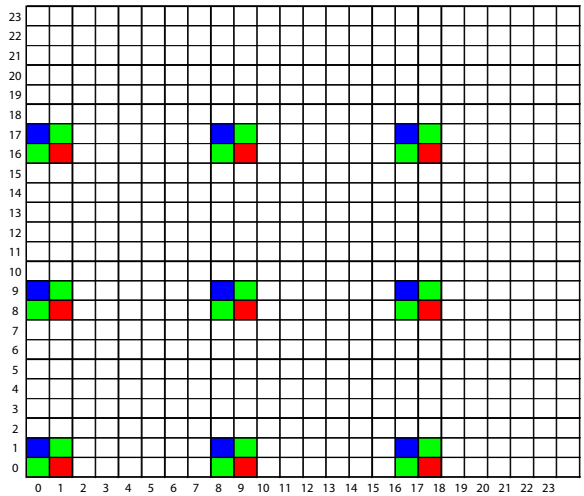
Mode A



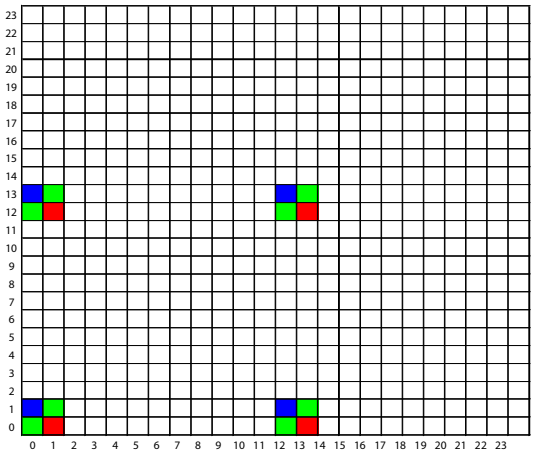
Mode B



Mode C



Mode D

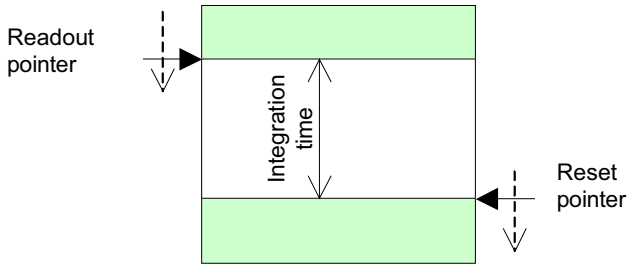


Mode E

Electronic Shutter

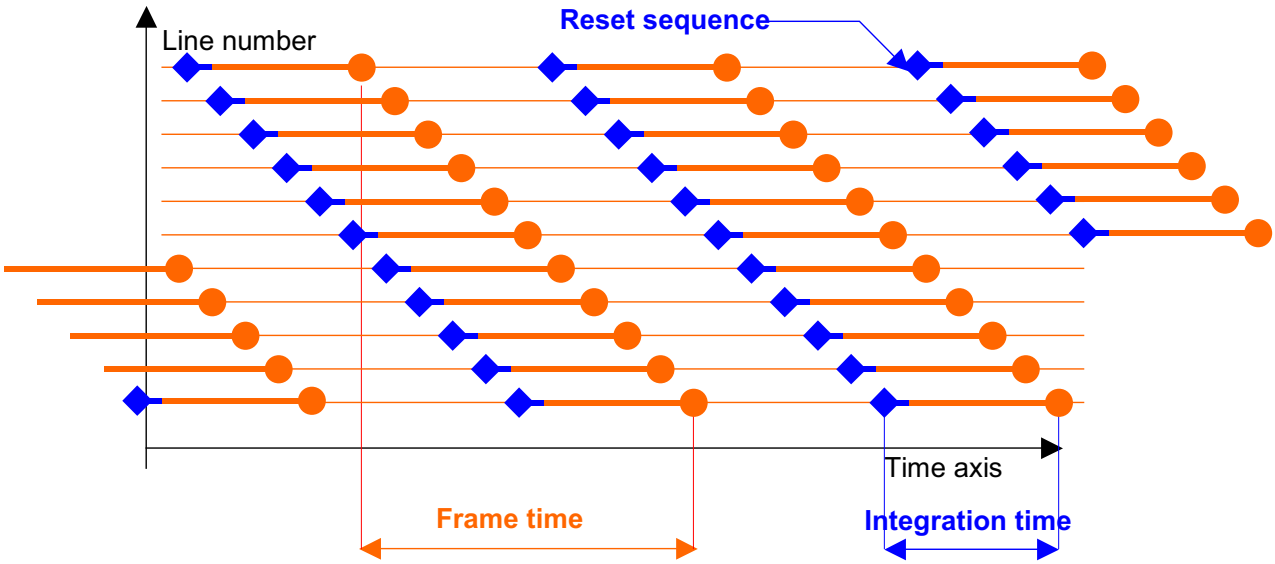
An electronic shutter similar to a rolling curtain is implemented on-chip. As shown in Figure 17, there are two Y shift registers. One shift register points to the row that is currently being read out. The other shift register points to the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

Figure 16. Electronic Shutter



In case of a mechanical shutter, the two shift registers can be combined to simultaneously apply the pulses from both sides of the pixel array. This is to halve the influence of the parasitic RC times of the reset and select lines in the pixel array. This can result in a reduction of the row blanking time. This is the case when FAST_RESET in the SEQUENCER register is set to 1, or in the nondestructive readout modes 1 and 2.

Figure 17. Electronic Rolling Shutter Operation



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High Dynamic Range Modes

Double Slope Integration

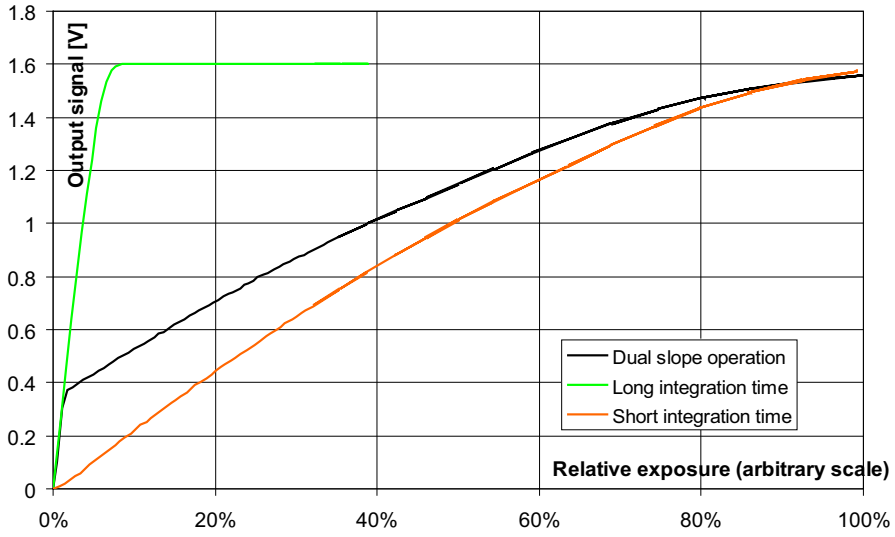
The IBIS4-6600 has a feature called double slope integration to increase the optical dynamic range of the sensor. The pixel response can be extended over a larger range of light intensities by using a "dual slope integration" (patents pending). This is obtained by adding charge packets from a long and a short integration time in the pixel during the same exposure time. Figure 18 shows the response curve of a pixel in dual slope integration mode. The curve also shows the response of the same pixel in linear integration mode at the same light levels, with a long and short integration time.

Dual slope integration is obtained by feeding a lower supply voltage to VDD_RESET_DS (for example, apply 2.0V to 2.5V). Note that for normal (single slope) operation, VDD_RESET_DS must have the same value as VDD_RESET. The difference between VDD_RESET_DS and VDD_RESET determines the range of the high sensitivity, and as a result the output signal level at which the transition between high and low sensitivity occurs.

Put the amplifier gain to the lowest value where the analog output swing covers digital input swing of the ADC. Increasing the amplification too much may boost the high sensitivity part over the whole ADC range.

The electronic shutter determines the ratio of integration times of the two slopes. The high sensitivity ramp corresponds to "no electronic shutter", thus maximal integration time (frame read out time). The low sensitivity ramp corresponds to the electronic shutter value that is obtained in normal operation.

Figure 18. Double Slope Response



NonDestructive Read Out (NDR)

The default mode of operation of the sensor is with FPN correction (double sampling). However, the sensor can also be read out in a nondestructive method. After a pixel is initially reset, it can be read multiple times, without being reset. The initial reset level and all intermediate signals can be recorded. High light levels saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, use the later or latest samples. Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence interprets the data. Table 9 on page 17 summarizes the advantages and disadvantages of nondestructive readout.

Figure 19. Principle of NonDestructive Readout

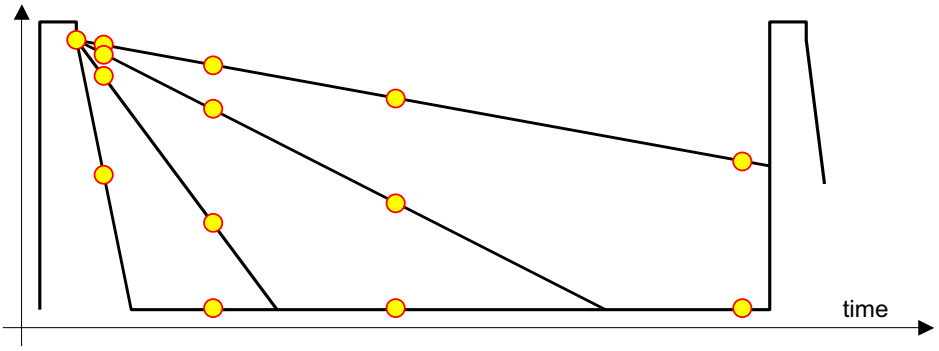


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Table 9. NDR: Advantages and Disadvantages

Advantages	Disadvantages
Low Noise, because it is true CDS. In the order of 10 e- or below.	System memory required to record the reset level and the intermediate samples.
High Sensitivity, because the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High Dynamic Range, because the results include signals for short and long integrations times.	Requires system level digital calculations.

Sequencer and Registers

Figure 4 on page 6 showed several control signals that are needed to operate the sensor in a particular sub sampling mode, with a certain integration time, output amplifier gain, and more. Most of these signals are generated on-chip by the sequencer that uses only a few control signals. These control signals must be generated by the external system:

- SYS_CLOCK, which defines the pixel rate (nominal 40 MHz),
- Y_START pulse, which indicates the start of a new frame,
- Y_CLOCK, which selects a new row and starts the row blanking sequence, including the synchronization and loading of the X-register.

The relative position of the pulses is determined by a number of data bits that are uploaded in internal registers through a Serial to Parallel interface (SPI).

Internal Registers

Table 10 lists the internal registers with a short description. The registers are discussed in more detail in the following sections.

Table 10. List of Internal Registers

Register	Bit	Name	Description
0 (0000)	11:0	SEQUENCER register	Selection of mode, granularity of the X sequencer clock, calibration, Default value <11:0>:"000100000000"
	0	NDR	Mode of readout: NDR = 0: normal readout (double sampling) NDR = 1: non-destructive readout
	1:2	NDR_mode	4 different modes of nondestructive readout (no influence if NDR = 0)
	3	RESET_BLACK	0 = normal operation 1 = reset of pixels before readout
	4	FAST_RESET	0 = electronic shutter operation 1 = addressing from both sides
	5	FRAME_CAL_MODE	0 = fast 1 = slow
	6	LINE_CAL_MODE	0 = fast 1 = slow
	7	CONT_CHARGE	0 = normal mode 1 = continuous precharge
	8	GRAN_X_SEQ_LSB	Granularity of the X sequencer clock
	9	GRAN_X_SEQ_MSB	
	10	BLACK	0 = normal mode 1 = disconnects column amplifiers from buses, output of amplifier equals dark reference level
	11	RESET_ALL	0 = normal mode 1 = continuous reset of all pixels
1 (0001)	10:0	NROF_PIXELS	Number of pixels to count (X direction). Max. 2222/2 (2210 real + 12 dummy pixels). Default value <10:0>:"01000000000"

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Table 10. List of Internal Registers (continued)

Register	Bit	Name	Description
2 (0010)	11:0	NROF_LINES	Number of lines to count (Y direction) Max. 3014 (3002 real + 12 dummy pixels) Default value <11:0>:"101111000110"
3 (0011)	11:0	INT_TIME	Integration time Default value <11:0>:"000000000001"
4 (0100)	7:0	DELAY	Delay of sequencer pulses Default value <7:0>:"00000011"
	0:3	DELAY_PIX_VALID	Delay of PIX_VALID pulse
	4:7	DELAY_EOL/EOF	Delay of EOL/EOF pulses
5 (0101)	6:0	X_REG	X start position (0 to 98) Default value <6:0>:"0000000"
6 (0110)	7:0	Y_REG	Y start position (0 to 137) Default value <7:0>:"00000000"
7 (0111)	7:0	IMAGE CORE register	Default value <7:0>:"00000000"
	1:0	TEST_mode	LSB: odd, MSB: even 0 = normal operation
	4:2	X_SUBSAMPLE	sub sampling mode in X-direction
	7:5	Y_SUBSAMPLE	sub sampling mode in X-direction
8 (1000)	9:0	AMPLIFIER register	Default value <9:0>:"0000010000"
	3:0	GAIN<3:0>	Output amplifier gain setting
	4	UNITY	0 = gain setting by GAIN<3:0> 1 = unity gain setting
	5	ONE_OUT	0 = two analog outputs 1 = multiplexing to one output (out_1)
	6	STANDBY	0 = normal operation 1 = amplifier in standby mode
	7:9	DELAY_CLK_AMP	Delay of pixel clock to output amplifier
9 (1001)	7:0	DAC_RAW_REG	Amplifier DAC raw offset Default value <7:0>:"10000000"
10 (1010)	7:0	DAC_FINE_REG	Amplifier DAC fine offset Default value <7:0>:"10000000"
11 (1011)	7:0	DAC_DARK_REG	DAC dark reference on output bus Default value <7:0>:"10000000"

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Table 10. List of Internal Registers (continued)

Register	Bit	Name	Description
12 (1100)	10:0	ADC register	Default value <10:0>:"00000000000"
	0	STANDBY_1	0 = normal operation 1 = ADC in standby
	1	STANDBY_2	
	2	ONE	0 = multiplexing of two ADC outputs 1 = disable multiplexing
	3	SWITCH	if ONE = 0: delay of output with one (EXT_CLK = 0) or half (EXT_CLK = 1) clock cycle if ONE = 1: switch between two ADCs
	4	EXT_CLK	0 = internal clock (same as clock to X shift register and output amplifier) 1 = external clock
	5	TRISTATE	0 = normal operation 1 = outputs in tristate mode
	6:8	DELAY_CLK_ADC	Delay of clock to ADCs and digital multiplexer
	9	GAMMA	0 = linear conversion 1 = 'gamma' law conversion
	10	BITINVERT	0 = no inversion of bits 1 = inversion of bits
13 (1101)		Reserved	
14 (1110)		Reserved	
15 (1111)		Reserved	

Register Descriptions

SEQUENCER Register

a. NDR (Bit 0)

In normal operation (NDR = 0), the sensor operates in double sampling mode. At the start of each row readout, the signals from the pixels are sampled, the row is reset, and the signals from the pixels are sampled again. The values are subtracted in the output amplifier.

When NDR is set to 1, the sensor operates in nondestructive readout (NDR) mode (refer Table 11).

b. NDR_mode (Bit 1 and 2)

These bits only influence the operation of the sensor in case NDR (bit 0) is set to 1. There are two modes for nondestructive readout (mode 1 and 2). Each mode needs two different frame readouts (setting 1 and 2 for mode 1, setting 3 and 4 for mode 2). a reset/readout sequence (reset_seq) and then one or several pure readout sequences (called read_seq hereafter). Table 11 gives an overview of the different NDR modes.

Table 11. Overview of NDR Modes.

Setting	Bits	NDR mode	Sequence
1	00	1	reset
2	01	1	read
3	10	2	reset
4	11	2	read

Mode 1

In this mode, the sensor is readout in the same method as for the nondestructive readout. However, electronic shutter control is not possible in this case, that is, the minimal (integration) time between two readings is equal to the number of lines that has to be read out (frame read time). The row lines are clocked simultaneously (left and right clock pulses are equal).

Mode 2

In this mode, it is possible to have a shorter integration time than the frame read time. Rows are alternatingly read out with the left and right pointer. These two pointers can point to two different rows (see INT_TIME register). The integration time between two readings of the same row is equal to the number of lines that is set in the INT_TIME register multiplied by 2 plus 1, and is the minimal one line read time.

In setting 3, the row that is read out by the left pointer is reset and read out (first Y_CLOCK), and the row that is read out by the right pointer is read out without being reset (second Y_CLOCK).

In setting 4, both rows are read out without being reset (on the first Y_CLOCK the row is read out by the left pointer; on the second Y_CLOCK the row is read out by the right pointer).

For both modes, the signals are read out through the same path as with destructive readout (double sampling), but the buses that are carrying the reset signals in destructive readout, are set to the voltage given by DAC_DARK in nondestructive readout.

[+] Feedback

c. Reset_black (Bit 3)

If RESET_BLACK is set to 1, each line is reset before it is read out (except for the row that is read out by the right pointer in NDR Mode 2). This may be useful to obtain black pixels.

d. Fast_reset (Bit 4)

The fast reset option (FAST_RESET = 1) might be useful in case a mechanical camera shutter is used. The fast reset is done on a row-by-row basis, not by a global reset. A global reset means charging all the pixels at the same time, which may result in a huge peak current. Therefore, the rows can be scanned rapidly while the left and right shift registers are both controlled identically, so that the reset lines over the pixel array are driven from both sides. This reduces the reset (row blanking) time (when FAST_RESET = 1 the smallest X-granularity can be used). After the row blanking time, the row is reset and Y_CLOCK can be asserted to reset the next row.

After a certain integration time, the read out can be done in a similar method. The Y shift registers are again synchronized to the first row. Both shift registers are driven identically, and all rows and columns are scanned for (destructive) readout. FAST_RESET = 1 puts the sequencer in such mode that the left and right shift registers are both controlled identically.

e. Output Amplifier Calibration (Bit 5 and 6)

Bits FRAME_CAL_MODE and LINE_CAL_MODE define the calibration mode of the output amplifier.

During every row-blanking period, a calibration is done of the output amplifier. There are two calibration modes. The FAST mode (= 0) can force a calibration in one cycle. However, it is not accurate and suffers from kTC noise, while the SLOW mode (= 1) can only make incremental adjustments and is noise free. Approximately 200 or more "slow" calibrations have the same effect as one "fast" calibration.

Different calibration modes can be set at the beginning of the frame (FRAME_CAL_MODE bit) and for every subsequent row that is read (LINE_CAL_MODE bit).

f. Continuous Charge (Bit 7)

For some applications, it might be necessary to use continuous charging of the pixel columns instead of a precharge on every row sample operation.

Setting bit CONT_CHARGE to 1 activates this function. The resistor connected to pin CMD_COL is used to control the current level on every pixel column.

g. Internal Clock Granularities

The system clock is divided several times on-chip.

The X-shift-register that controls the column/pixel readout, is clocked by half the system clock rate. Odd and even pixel columns are switched to two separate buses. In the output amplifier, the pixel signals on the two buses can be combined to one pixel stream at 40 MHz.

The clock that drives the X-sequencer can be a multiple of 2, 4, 8, or 16 times the system clock. Table 12 lists the settings for the granularity of the X-sequencer clock and the corresponding row blanking time (for NDR = 0). A row blanking time of 7.18 µs is the baseline for almost all applications.

Table 12. Granularity of X-Sequencer Clock and Corresponding Row Blanking Time (for NDR = 0).

Gran_x_seq_msb/lsb	X-Sequencer Clock	Row Blanking Time	Row Blanking Time [µs]
00	2 x sys_clock	142 x TSYS_CLOCK	3.55
01	4 x sys_clock	282 x TSYS_CLOCK	7.05
10	8 x sys_clock	562 x TSYS_CLOCK	14.05
11	16 x sys_clock	1122 x TSYS_CLOCK	28.05

h. Black (Bit 10)

If BLACK is set to 1, the internal black signal is held high continuously. As a result, the column amplifiers are disconnected from the buses, and the buses are set to the voltage given by DAC_DARK. The output of the amplifier equals the voltages from the offset DACs.

i. Reset_all (Bit 11)

If RESET_ALL is set to 1, all the pixels are simultaneously put in a 'reset' state. In this state, the pixels behave logarithmically with light intensity. If this state is combined with one of the NDR modes, the sensor can be used in a nonintegrating, logarithmic mode with high dynamic range.

j. Nrof_pixels Register

After the internal X_SYNC is generated (start of the pixel readout of a particular row), the PIXEL_VALID signal goes high. The PIXEL_VALID signal goes low when the pixel counter reaches the value loaded in the NROF_PIXEL register and an EOL pulse is generated. Due to the fact that two pixels are addressed at each internal clock cycle, the amount of pixels read out in one row is 2*(NROF_PIXEL + 1).

k. Nrof_lines Register

After the internal YL_SYNC is generated (start of the frame readout with Y_START), the line counter increases with each Y_CLOCK pulse until it reaches the value loaded in the NROF_LINES register and an EOF pulse is generated. In NDR Mode 2, the line counter increments only every two Y_CLOCK pulses and the EOF pulse shows up only after the readout of the row indicated by the right shift register

INT_TIME Register

When the Y_START pulse is applied (start of the frame readout), the sequencer generates the YL_SYNC pulse for the left Y-shift register. This loads the left Y-shift register with the pointer loaded in Y_REG register. At each Y_CLOCK pulse, the pointer shifts to the next row and the integration time counter increases (increment only every two Y_CLOCK pulses in NDR mode 2) until it reaches the value loaded in the INT_TIME register. At that moment, the YR_SYNC pulse for the right Y-shift register is generated, which loads the right Y-shift register with the pointer loaded in Y_REG register (shown in Figure 20 on page 21).

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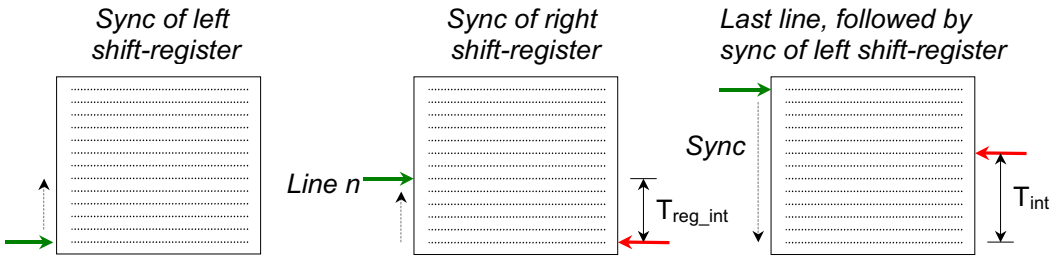
Figure 20. Syncing of Y-shift Registers



Treg_int: Difference between left and right pointer = integration counter until value "n" of INT_TIME register is reached = INT_TIME register

In case of NDR = 0, the actual integration time Tint is given by

TintL: Integration time [# lines] = NROF_LINES register - INT_TIME register + 1

In case of NDR = 1, NDR mode 1, the time Tint between two readings of the same row is given by:

Tint:Integration time [# lines] = NROF_LINES register + 1

In case of NDR = 1, NDR mode 2, the times Tint1 and Tint2 between two readings of the same row (alternatingly) are given by:

Tint1: Integration time [# lines] = 2 * INT_TIME register + 1

Tint2: Integration time [# lines] = 2 * (NROF_LINES register + 1) - (2 * INT_TIME register + 1)

DELAY Register

The DELAY register can be used to delay the PIXEL_VALID pulse (bits 0:3) and the EOL/EOF pulses (bits 4:7) to synchronize them to the real pixel values at the analog output or the ADC output (which give additional delays depending on their settings). The bit settings and corresponding delay are indicated in Table 13.

Table 13. Added Delay by Changing the DELAY Register Settings

Bits	Delay [# SYS_CLOCK periods]	Bits	Delay [# SYS_CLOCK periods]
0000	0	1000	6
0001	0	1001	7
0010	0	1010	8
0011	1	1011	9
0100	2	1100	10
0101	3	1101	11
0110	4	1110	12
0111	5	1111	13

X_REG Register

The X_REG register determines the start position of the window in the X-direction. In this direction, there are 2208 + 2 + 12 readable pixels. In the active pixel array, sub sampling blocks are 24 pixels wide and the columns are read two by two. Therefore, the number of start positions equals 2208/24 +2/2 +12/2 = 92 + 1 + 6 = 99.

Y_REG Register

The Y_REG register determines the start position of the window in the Y-direction. In this direction, there are 3000 + 2 + 12 readable pixels. In the active pixel array, sub sampling blocks are 24 pixels wide and the rows are read one by one. Therefore, the number of start positions equals 3000/24 + 2/2 +12 = 125 + 1 + 12 = 138.

Image_core Register

Bits 0:1 of the IMAGE_CORE register defines the several test modes of the image core. Setting 00 is the default and normal operation mode. If the bit is set to 1, the odd (bit 0) or even (bit 1) columns are tight to V_{DD}. These test modes can be used to tune the sampling point of the ADCs to an optimal position.

Bits 2:7 of the IMAGE_CORE register define the sub sampling mode in the X-direction (bits 2:4) and in the Y-direction (bits 5:7). The sub sampling modes and corresponding bit setting are given in the section Analog to Digital Converter on page 11.

[+] Feedback

AMPLIFIER Register

a. Gain (Bits 0:3)

The gain bits determine the gain setting of the output amplifier. They are effective only if UNITY = 0. The gains and corresponding bit setting are given in Table 4 on page 10.

b. Unity (Bit 4)

If UNITY = 1, the gain setting of GAIN is bypassed and the gain amplifier is put in unity feedback.

c. One_out

If ONE_OUT = 0, the two output amplifiers are active. If ONE_OUT = 1, the signals from the two buses are multiplexed to output OUT1. The gain amplifier and output driver of the second path are put in standby.

d. Standby

If STANDBY = 1, the complete output amplifier is put in standby. This reduces the power consumption significantly.

e. Delay_clk_amp

The clock that acts on the output amplifier can be delayed to compensate for any delay that is introduced in the path from shift register, column selection logic, column amplifier, and buses to the output amplifier. Setting '000' is used as a baseline.

Table 14. Added Delay by Changing the DELAY_CLK_AMP Bit Settings

Bits	Delay [ns]	Bits	Delay [ns]
000	1.7	100	Inversion + 8.3
001	2.9	2.9	Inversion + 9.7
010	4.3	110	Inversion + 11.1
011	6.1	111	Inversion + 12.3

Dac_raw_reg and Dac_fine_reg Register

These registers determine the black reference level at the output of the output amplifier. Bit setting 11111111 for DAC_RAW_REG register gives the highest offset voltage; bit setting 00000000 for DAC_RAW_REG register gives the lowest offset voltage. Ideally, if the two output paths have no offset mismatch, the DAC_FINE_REG register must be set to 10000000. Deviation from this value can be used to compensate the internal mismatch (see the section Offset DACs on page 10).

Dac_raw_dark Register

This register determines the voltage level that is put on the internal buses during calibration of the output stage. This voltage level is also continuously put on the reset buses in case of nondestructive readout (as a reset level for the double sampling FPN correction).

ADC Register

a. Standby_1 and standby_2

If only one or none of the ADCs is used, the other or both ADCs can be put in standby by setting the bit to 1. This significantly reduces the power consumption.

b. One

If OUT1 and OUT2 are both used and connected to ADC_IN1 and ADC_IN2 respectively, ONE must be 0 to use both ADCs and to multiplex their output to ADC_D<9:0>. If ONE = 1, the multiplexing is disabled.

c. Switch

If the two ADCs are used (ONE = 0) and internal pixel clock (EXT_CLK = 0), the ADC output is delayed with one system clock cycle if SWITCH = 1. If the two ADCs are used (ONE = 0) and an external ADC clock (EXT_CLK = 1) is applied, the ADC output is delayed with half ADC clock cycle if SWITCH = 1.

If only one ADC is used, the digital multiplexing is disabled by ONE = 1, but SWITCH selects which ADC output is on ADC_D<9:0> (SWITCH = 0: ADC_1, SWITCH = 1: ADC_2).

d. Ext_clk

If EXT_CLK = 0, the internal pixel clock (that drives the X-shift registers and output amplifier, that is, half the system clock) is used as input for the ADC clock. If EXT_CLK = 1, an external clock must be applied to pin ADC_CLK_EXT (pin 46).

e. Tristate

If TRISTATE = 1, the ADC_D<9:0> outputs are in tri-state mode.

f. Delay_clk_adc

The clock that finally acts on the ADCs can be delayed to compensate for any delay introduced in the path from the analog outputs to the input stage of the ADCs. The same settings apply for the delay that can be given to the clock acting on the output amplifier (see Table 14). The best setting also depends on the delay of the output amplifier clock and the load of the output amplifier. It must be used to optimize the sampling moment of the ADCs with respect to the analog pixel input signals. Setting '000' is used as a baseline.

g. Gamma

If GAMMA is set to 0, the ADC input to output conversion is linear, otherwise the conversion follows a 'gamma' law (more contrast in dark parts of the window, lower contrast in the bright parts).

h. Bitinvert

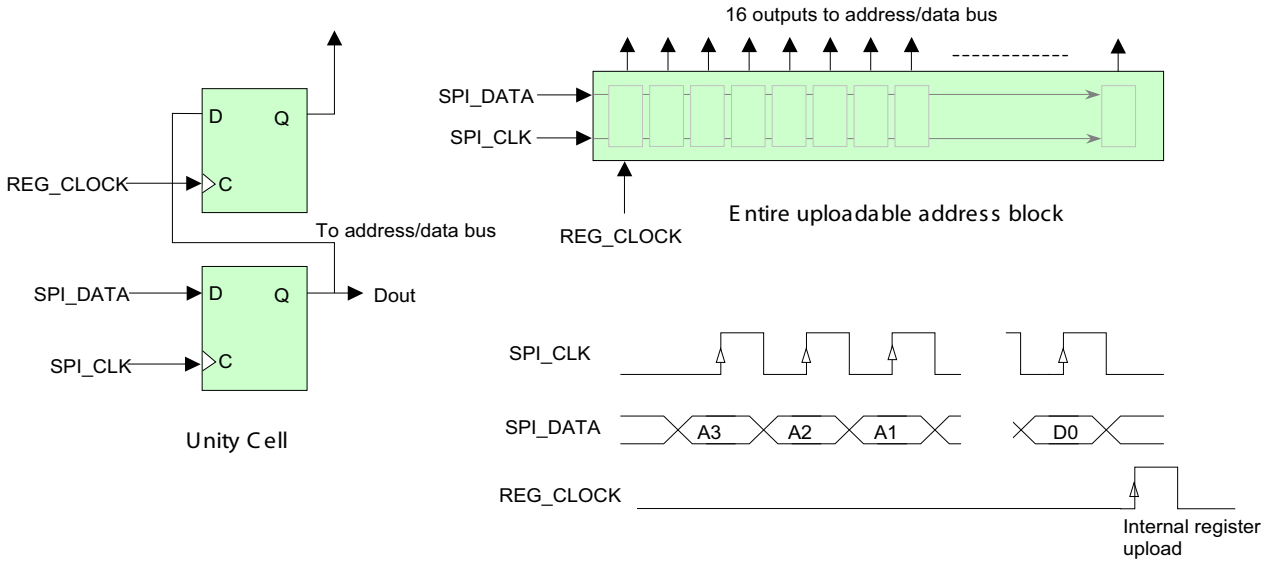
If BITINVERT = 0, 0000000000 is the conversion of the lowest possible input voltage, otherwise the bits are inverted.

Serial to Parallel Interface

To upload the sequencer registers, a dedicated serial to parallel interface (SPI) is implemented. 16 bits (4 address bits + 12 data bits) must be uploaded serially. The address must be uploaded first (MSB first), then the data (also MSB first).

The elementary unit cell is shown in Figure 21. Sixteen of these cells are connected in series, having a common SPI_CLK form the entire uploadable parameter block. Dout of one cell is connected to SPI_DATA of the next cell (maximum speed is 20 MHz). The uploaded settings on the address/data bus are loaded into the correct register of the sensor on the rising edge of signal REG_CLOCK and become effective immediately.

Figure 21. SPI Interface



Timing Diagrams

Sequencer Control Signals

There are 3 control signals that operate the image sensor:

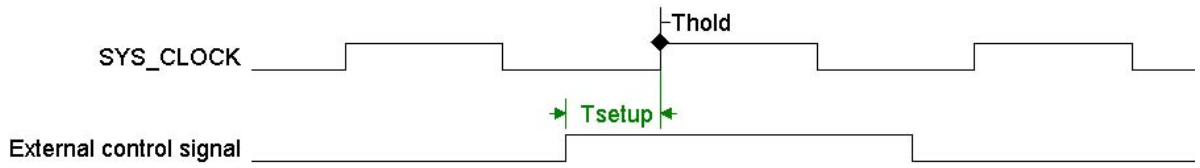
- SYS_CLOCK
- Y_CLOCK
- Y_START

These control signals must be generated by the external system with the following time constraints to SYS_CLOCK (rising edge = active edge):

- TSETUP >7.5 ns
- THOLD > 7.5 ns

It is important that these signals are free of any glitches.

Figure 22. Relative Timing of the Three Control Signals



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Basic Frame and Line Timing

The basic frame and line timing of the IBIS4-6600 sensor is shown in Figure 23.

The pulse width of Y_CLOCK must be a minimum of one clock cycle and three clock cycles for Y_START. As long as Y_CLOCK is applied, the sequencer stays in a suspended state.

T1 Row blanking time: During this period, the X-sequencer generates the control signals to sample the pixel signal and pixel reset levels, and start the readout of one line. It depends on the granularity of the X-sequencer clock (see Table 12 on page 20).

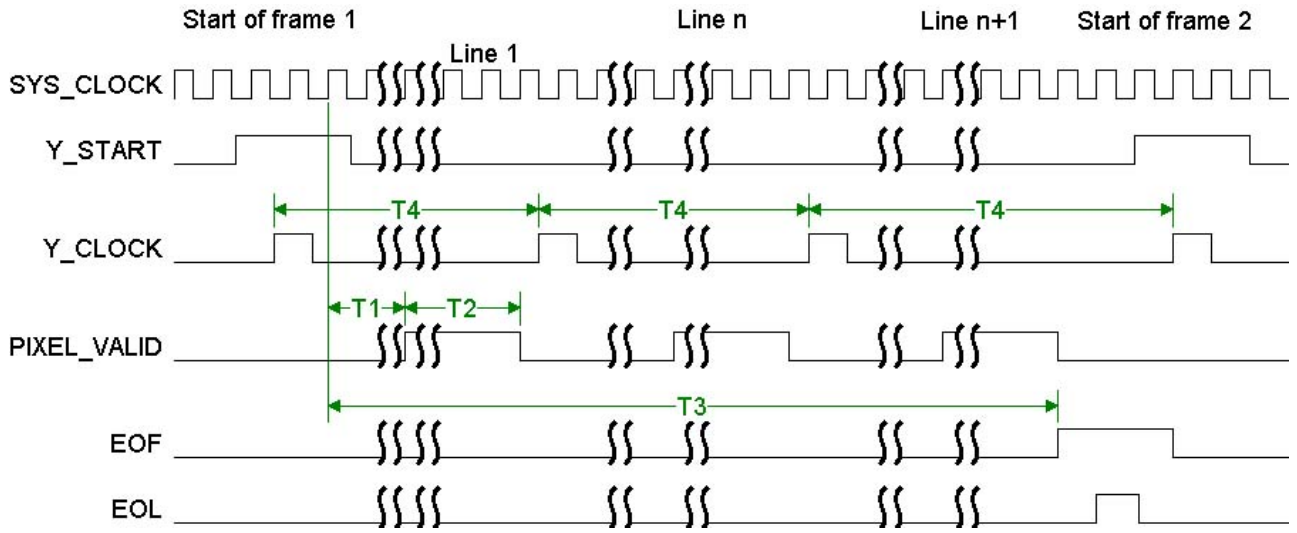
T2 Pixels counted by pixel counter until the value of Nrof_pixels register is reached. Pixel_valid goes high when the internal X_sync signal is generated. In other words, when the readout of the pixels is started. Pixel_valid goes low when the pixel counter reaches the value loaded in the Nrof_pixels register. Eol goes high Sys_clock cycle after the falling edge of Pixel_valid.

T3 EOF goes high when the line counter reaches the value loaded in the NROF_LINES register and the line is read (PIXEL_VALID goes low).

T4 The time delay between successive Y_CLOCK pulses needs to be equal to avoid any horizontal illumination (integration) discrepancies in the image.

Both EOF and EOL can be tied to Y_START (EOF) and Y_CLOCK (EOL) if both signals are delayed with at least 2 SYS_CLOCK periods to let the sensor run automatically.

Figure 23. Basic Frame and Line Timing

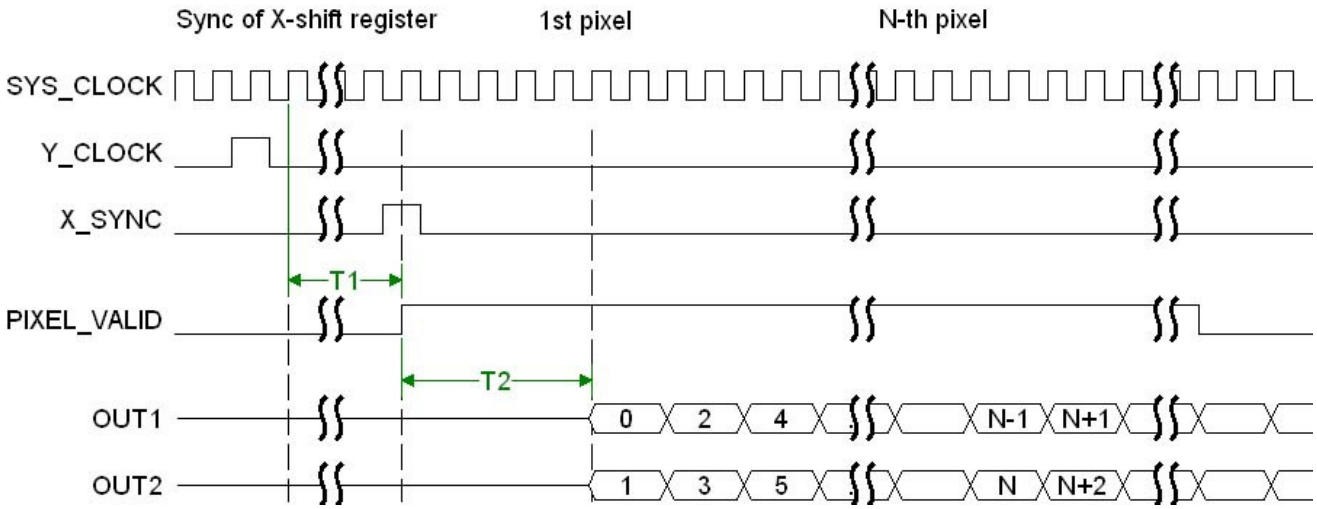


[+] Feedback

Pixel Output Timing

Using Two Analog Outputs

Figure 24. Pixel Output Timing using Two Analog Outputs



The pixel signal at the OUT1 (OUT2) output becomes valid after four SYS_CLOCK cycles when the internal X_SYNC (equal to start of PIXEL_VALID output) appears (see Figure 24). The PIXEL_VALID and EOL/EOF pulses can be delayed by the user through the DELAY register.

T1: Row blanking time (see Table 12 on page 20)

T2: 4 SYS_CLOCK cycles.

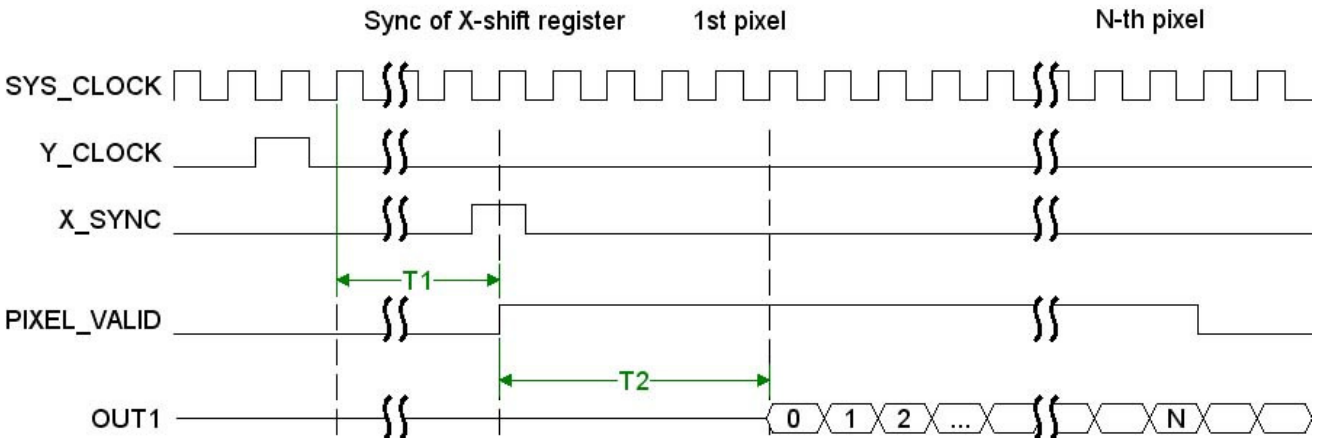
Multiplexing to One Analog Output

The pixel signal at the OUT1 output becomes valid after five SYS_CLOCK cycles when the internal X_SYNC (equal to start of PIXEL_VALID output) appears (see Figure 25). The PIXEL_VALID and EOL/EOF pulses can be delayed by the user through the DELAY register.

T1: Row blanking time

T2: 5 SYS_CLOCK cycles.

Figure 25. Pixel Output Timing Multiplexing to One Analog Output



[+] Feedback

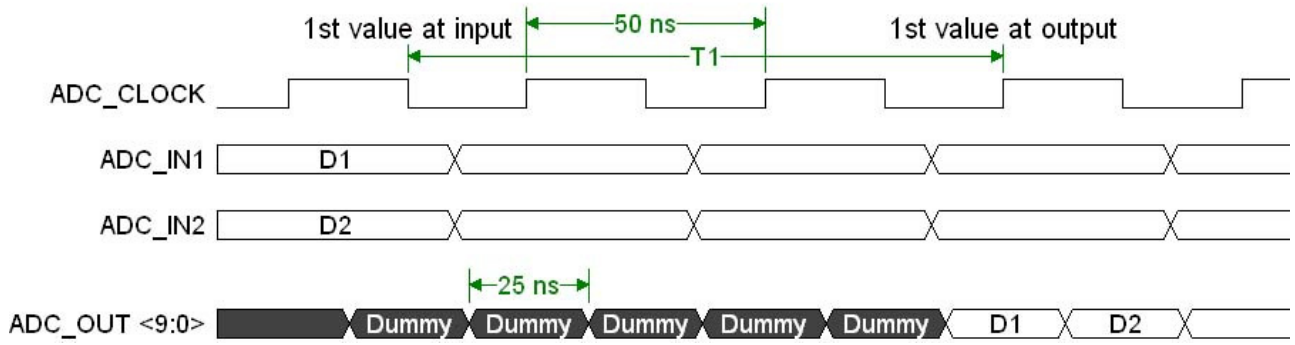
ADC Timing

Two Analog Outputs

Figure 26 shows the timing of the ADC using two analog outputs. Internally, the ADCs sample on the falling edge of the ADC_CLOCK (in case of internal clock, the clock is half the SYS_CLOCK).

T1: Each ADC has a pipeline delay of 2 ADC_CLOCK cycles. This results in a total pipeline delay of four pixels.

Figure 26. ADC Timing using Two Analog Outputs

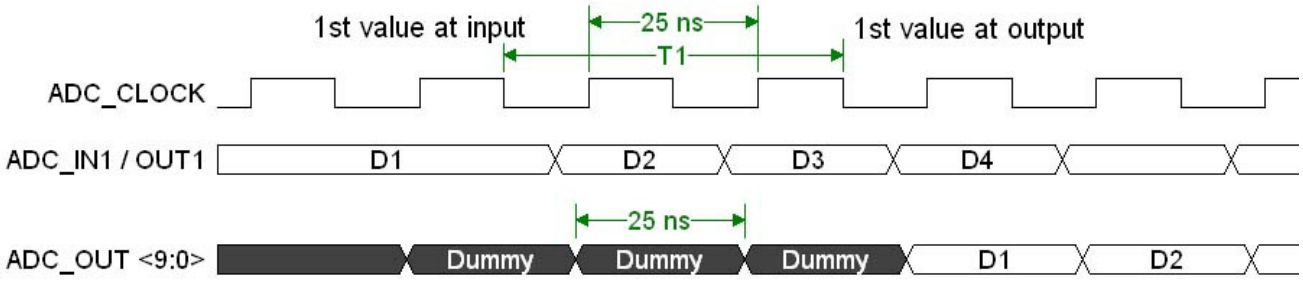


One Analog Output

Figure 27 shows the timing of the ADC using one analog output. Internally, the ADC samples on the falling edge of the ADC_CLOCK.

T1: The ADC has a pipeline delay of 2 ADC_CLOCK cycles.

Figure 27. ADC Timing using One Analog Output



[+] Feedback

Pin Information

The following table lists all the pins and their functions. There are a total of 68 pins. All pins with the same name can be connected together.

Table 15. Pin List

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
1	CMD_COL_CTU	Input	0	Biasing of columns (ctu). Decouple with 100 nF to GNDA.
2	CMD_COL	Input	1.08	Biasing of columns. Connect to V_{DDA} with R = 10 kΩ and decouple to GNDA with C = 100 nF.
3	CMD_COLAMP	Input	0.66	Biasing of column amplifiers. Connect to V_{DDA} with R = 100 kΩ and decouple to GNDA with C = 100 nF.
4	CMD_COLAMP_CTU	Input	0.37	Biasing of column amplifiers. Connect to V_{DDA} with R = 10 MΩ and decouple to GNDA with C = 100 nF.
5	RCAL_DAC_DARK	Input	1.27 at code 128 DAC_DARK reg	Biasing of DAC for dark reference. Can be used to set output range of DAC. Default: Decouple to GNDA with C = 100 nF
6	RCAL_DAC_OUT	Input	0	Biasing of DAC for output dark level. Can be used to set output range of DAC. Default: Connect to GNDA
7	V_{DDA}	Power	2.5	V_{DD} of analog part [2.5V]
8	GNDA	Power	0	GND (&substrate) of analog part
9	V_{DDD}	Power	2.5	V_{DD} of digital part [2.5V]
10	GNDD	Power	0	GND (&substrate) of digital part
11	CMD_OUT_1	Input	0.78	Biasing of first stage output amplifiers. Connect to VDDAMP with R = 50 kΩ and decouple to GNDAMP with C = 100 nF.
12	CMD_OUT_2	Input	0.97	Biasing of second stage output amplifiers. Connect to VDDAMP with R = 25 kΩ and decouple to GNDAMP with C = 100 nF.
13	CMD_OUT_3	Input	0.67	Biasing of third stage output amplifiers. Connect to VDDAMP with R = 100 kΩ and decouple to GNDAMP with C = 100 nF.
14	SPI_CLK	Input	-	Clock of digital parameter upload. Shifts on rising edge.
15	SPI_DATA	Input	-	Serial address and data input. 16-bit word. Address first. MSB first.
16	VDDAMP	Power	2.5	V_{DD} of analog output [2.5V] (Can be connected to V_{DDA})
17	CMD_FS_ADC	Input	0.73	Biasing of first stage ADC. Connect to VDDA_ADC with R = 50 kΩ and decouple to GNDA_ADC with C = 100 nF.
18	CMD_SS_ADC	Input	0.73	Biasing of second stage ADC. Connect to VDDA_ADC with R = 50 kΩ and decouple to GNDA_ADC.
19	CMD_AMP_ADC	input	0.59	Biasing of input stage ADC. Connect to VDDA_ADC with R = 180 kΩ and decouple to GNDA_ADC with C = 100 nF.
20	GNDAMP	Ground	0	GND (&substrate) of analog output
21	OUT1	Output	Black level: 1 at code 190 DAC_RAW register	Analog output 1
22	ADC_IN1	Input	See OUT1.	Analog input ADC 1
23	VDDAMP	Power	2.5	V_{DD} of analog output [2.5V] (Can be connected to V_{DDA})
24	OUT2	Output	Black level: 1 at code 190 DAC_RAW register	Analog output 2
25	ADC_IN2	Input	See OUT2.	Analog input ADC 2
26	V_{DDD}	Power	2.5	V_{DD} of digital part [2.5V]
27	GNDD	Power	0	GND (&substrate) of digital part
28	GNDA	Power	0	GND (&substrate) of analog part

[+] Feedback

Table 15. Pin List (continued)

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
29	V_{DDA}	Power	2.5	V_{DD} of analog part [2.5V]
30	REG_CLOCK	Input	-	Register clock. Data on internal bus is copied to corresponding registers on rising edge.
31	SYS_CLOCK	Input	-	System clock defining the pixel rate (nominal 40 MHz, 50% ± 5% duty cycle)
32	SYS_RESET	Input	-	Global system reset (active high)
33	Y_CLK	Input	-	Line clock
34	Y_START	Input	-	Start frame readout
35	GNDD_ADC	Power	0	GND (&substrate) of digital part ADC
36	VDDD_ADC	Power	2.5	V_{DD} of digital part [2.5V] ADC
37	GNDA_ADC	Power	0	GND (&substrate) of analog part
38	VDDA_ADC	Power	2.5	V_{DD} of analog part [2.5V]
39	VHIGH_ADC	Input	1.5	ADC high reference voltage (for example, connect to VDDA_ADC with R = 560 Ω and decouple to GNDA_ADC with C = 100 nF)
40	VLOW_ADC	Input	0.42	ADC low reference voltage (for example, connect to GNDA_ADC with R = 220 Ω and decouple to GNDA_ADC with C = 100 nF)
41	GNDA_ADC	Power	0	GND (&substrate) of analog part
42	VDDA_ADC	Power	2.5	V_{DD} of analog part [2.5V]
43	GNDD_ADC	Power	0	GND (&substrate) of digital part ADC
44	VDDD_ADC	Power	2.5	V_{DD} of digital part [2.5V] ADC
45	VDD_RESET_DS	Power	2.5 (for no dual slope)	Variable reset voltage (dual slope)
46	ADC_CLK_EXT	Input	-	External ADC clock
47	EOL	Output	-	Diagnostic end of line signal (produced by sequencer), can be used as Y_CLK
48	EOF	Output	-	Diagnostic end of frame signal (produced by sequencer), can be used as Y_START
49	PIX_VALID	Output	-	Diagnostic signal. High during pixel readout
50	TEMP	Output	-	Temperature measurement. Output voltage varies linearly with temperature.
51	ADC_D<9>	Output	-	ADC data output (MSB)
52	VDD_PIX	Power	2.5	V_{DD} of pixel core [2.5V]
53	GND_AB	Power	0	Anti-blooming ground. Set to 1V for improved anti-blooming behavior
54	ADC_D<8>	Output	-	ADC data output
55	ADC_D<7>	Output	-	ADC data output
56	ADC_D<6>	Output	-	ADC data output
57	ADC_D<5>	Output	-	ADC data output
58	ADC_D<4>	Output	-	ADC data output
59	ADC_D<3>	Output	-	ADC data output
60	VDD_RESET	Power	2.5	Reset voltage [2.5V]. Highest voltage to the chip. 3.3V for extended dynamic range or 'hard reset'.
61	ADC_D<2>	Output	-	ADC data output
62	ADC_D<1>	Output	-	ADC data output
63	ADC_D<0>	Output	-	ADC data output (LSB)

[+] Feedback

Table 15. Pin List (continued)

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
64	BS_RESET	Input	-	Boundary scan (allows debugging of internal nodes): Reset. Tie to GND if not used.
65	BS_CLOCK	Input	-	Boundary scan (allows debugging of internal nodes): Clock. Tie to GND if not used.
66	BS_DIN	Input	-	Boundary scan (allows debugging of internal nodes): In. Tie to GND if not used.
67	BS_BUS	Output	-	Boundary scan (allows debugging of internal nodes): Bus. Leave floating if not used.
68	CMD_DEC	Input	0.74	Biasing of X and Y decoder. Connect to V_{DDD} with R = 50 kΩ and decouple to GNDD with C = 100 nF.

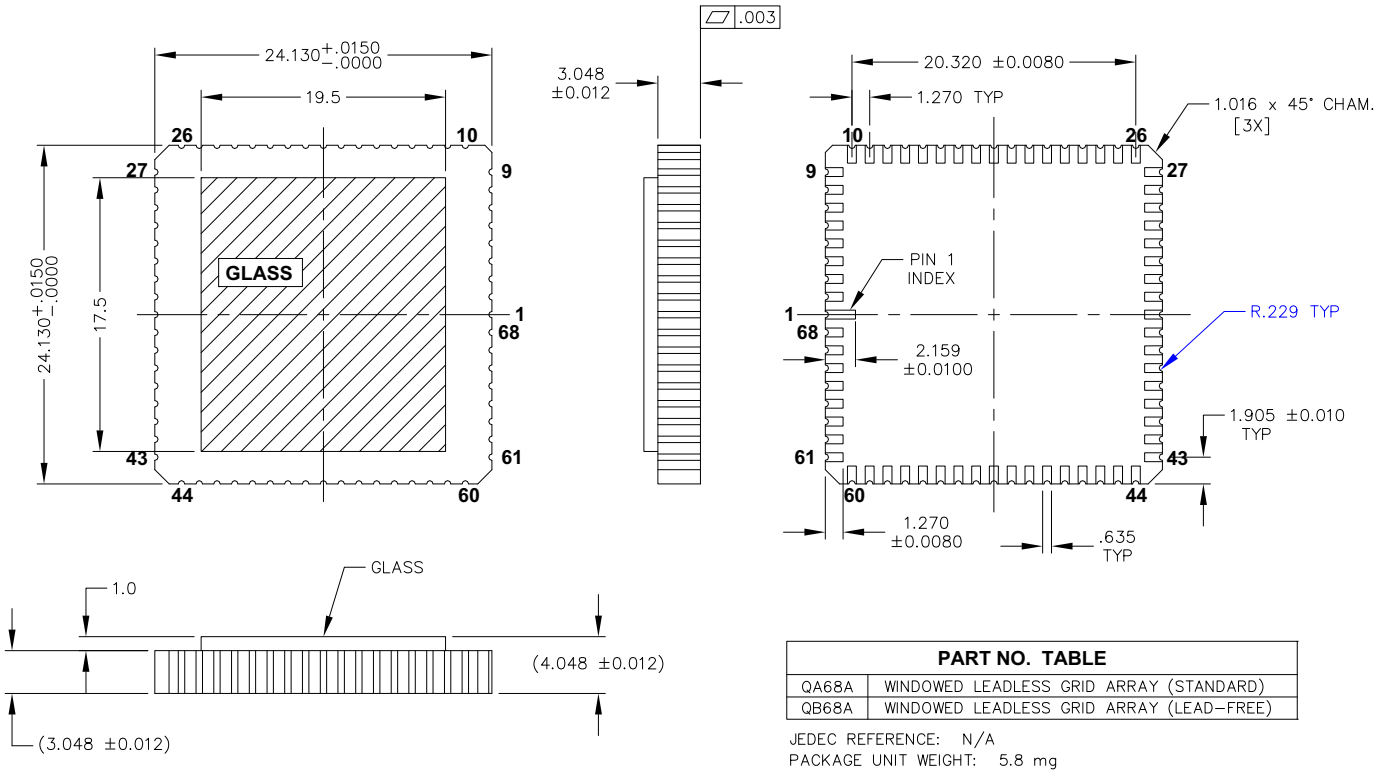
Note on Power On Behavior

At power on, the chip is in an undefined state. It is advised that the power on is accompanied by the assertion of the SYS_CLOCK and a SYS_RESET pulse that puts all internal registers in their default state (all bits are set to 0). The X-shift registers are in a defined state after the first X_SYNC, which occurs a few microseconds after the first Y_START and Y_CLOCK pulse. Before this X_SYNC, the chip may draw more current from the analog power supply V_{DDA}. It is therefore favorable to have separate analog and digital supplies. The current spike (if there are any) may also be avoided by a slower ramp up of the analog power supply or by disconnecting the resistor on pin 3 (CMD_COLAMP) at startup.

[+] Feedback

Package Information

Figure 28. 68 Pin LCC Packaging Outline (001-05458)

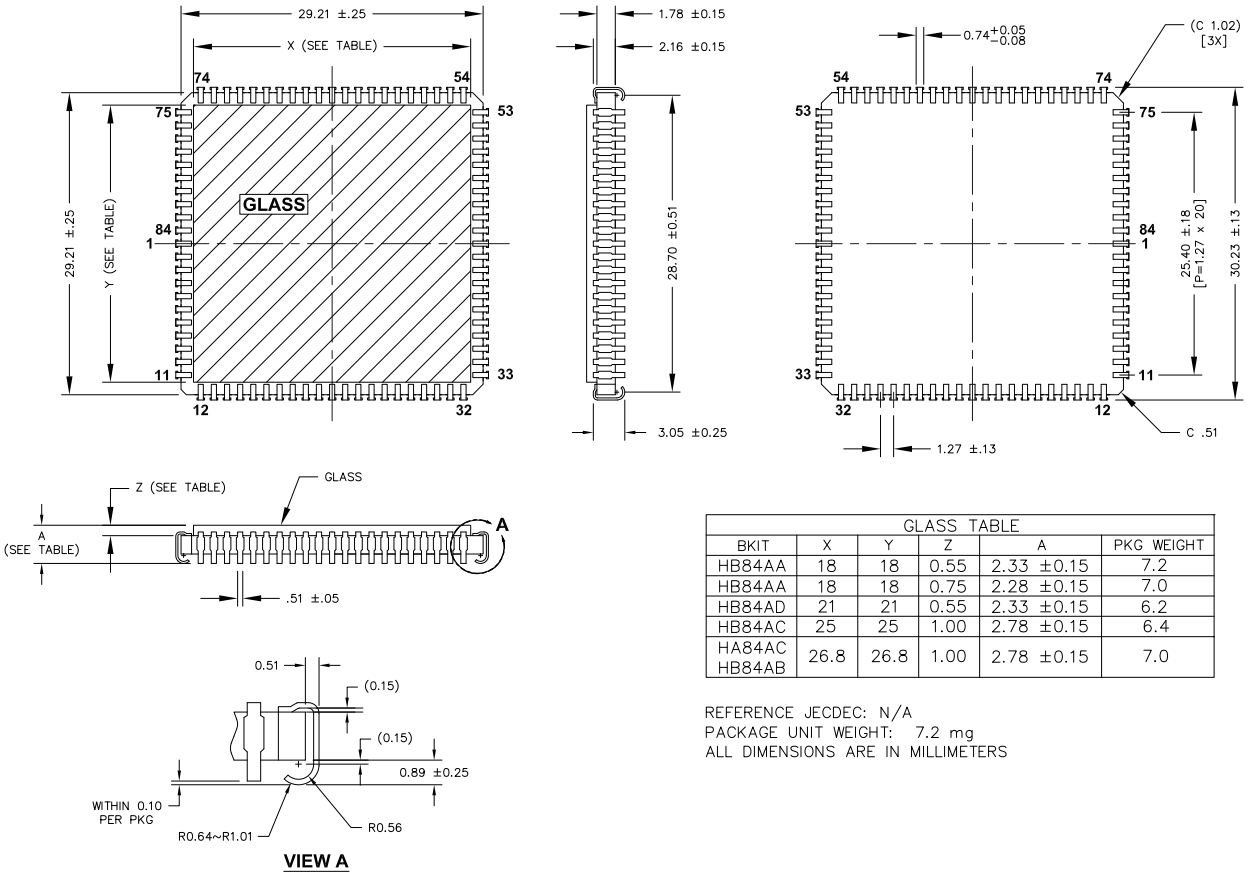


PART NO. TABLE	
QA68A	WINDOWED LEADLESS GRID ARRAY (STANDARD)
QB68A	WINDOWED LEADLESS GRID ARRAY (LEAD-FREE)

JEDEC REFERENCE: N/A
PACKAGE UNIT WEIGHT: 5.8 mg
ALL DIMENSIONS ARE IN MILLIMETERS

001-05458 **

Figure 29. 84 Pin JLCC Packaging Outline (001-05462)



GLASS TABLE					
BKIT	X	Y	Z	A	PKG WEIGHT
HB84AA	18	18	0.55	2.33 ±0.15	7.2
HB84AA	18	18	0.75	2.28 ±0.15	7.0
HB84AD	21	21	0.55	2.33 ±0.15	6.2
HB84AC	25	25	1.00	2.78 ±0.15	6.4
HA84AC HB84AB	26.8	26.8	1.00	2.78 ±0.15	7.0

REFERENCE JECDEC: N/A
PACKAGE UNIT WEIGHT: 7.2 mg
ALL DIMENSIONS ARE IN MILLIMETERS

001-05462 *A

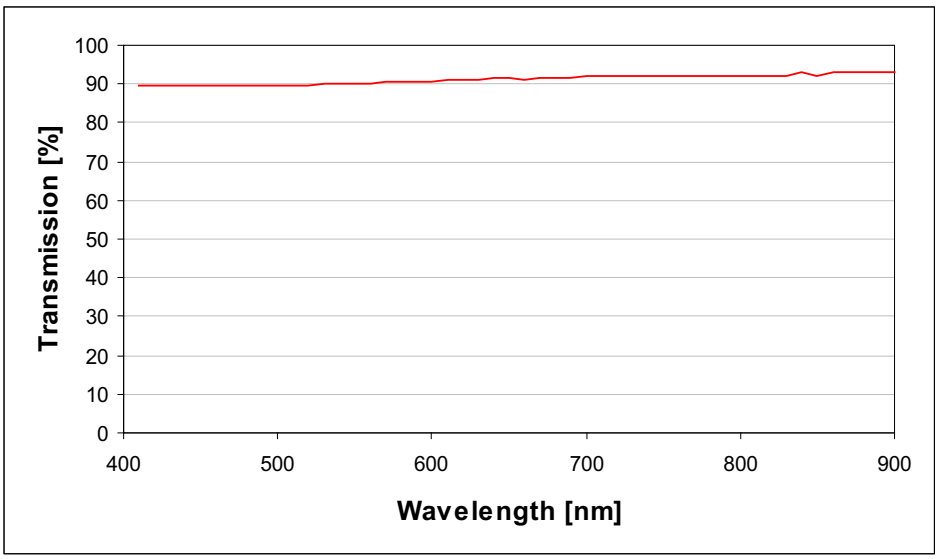
[+] Feedback

Glass Lid Specifications

Monochrome Sensor

A D263 glass is used as protection glass lid on top of the IBIS4-6600 monochrome sensors. The refraction index of the D263 glass lid is 1.52. Figure 30 shows the transmission characteristics of the D263 glass.

Figure 30. Transmittance Curve of the D263 Cover Glass Lid



Storage and Handling

Storage Conditions

Table 16. Storage Conditions

Description	Minimum	Maximum	Maximum
Temperature	–30	+85	°C

Handling and Soldering Conditions

Special care must be taken when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, because color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations ensure that sensor performance is not compromised during end-users assembly processes.

Board Assembly

Device placement onto boards must be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators must always wear all designated and approved grounding equipment. Grounded wrist straps at ESD protected workstations are recommended, including the use of ionized blowers. All tools must be ESD protected.

Manual Soldering

When a soldering iron is used, the following conditions must be observed:

- Use a soldering iron with temperature control at the tip. The soldering iron tip temperature must not exceed 350°C.
- The soldering period for each pin must be less than 5 seconds.

Reflow Soldering

Figure 31 on page 33 shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor may occur. See Figure 31 on page 33 for more details.

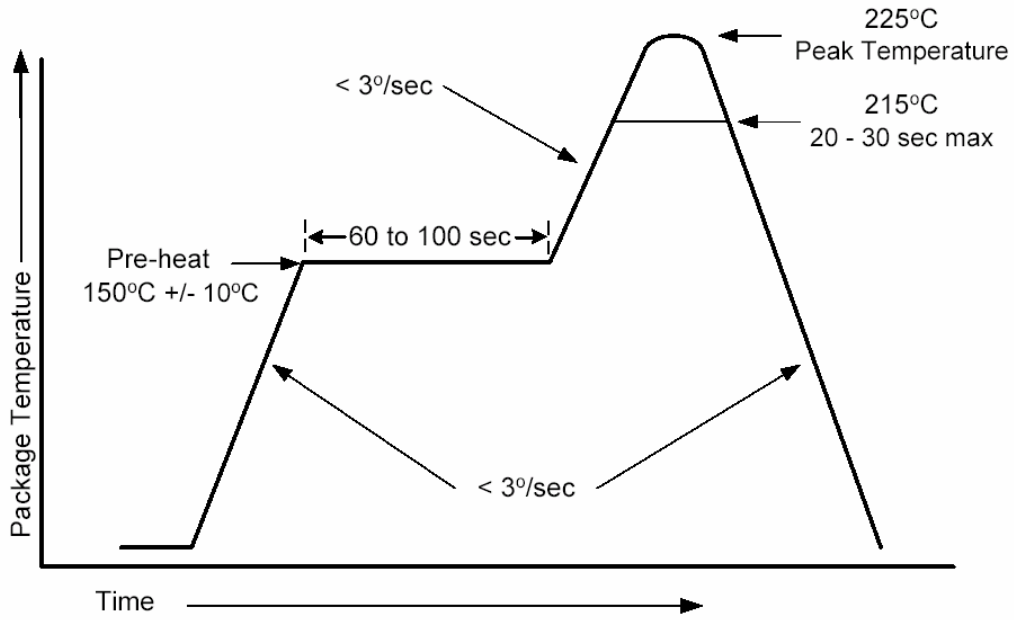
Precautions and Cleaning

Avoid spilling solder flux on the cover glass, because bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.

It is recommended that isopropyl alcohol (IPA) be used as a solvent for cleaning the image sensor glass lid. When using other solvents, it must be confirmed beforehand whether the solvent can dissolve the package and/or the glass lid.

[+] Feedback

Figure 31. Reflow Soldering Temperature Profile



RoHS (Pb-Free) Compliance

This section reports the use of Hazardous chemical substances as required by the RoHS Directive (excluding packing material).

Table 17. The Chemical Substances and Information about Any Intentional Content

Chemical Substance	Intentional Content	Portion Containing Intentional Content
Lead	NO	-
Cadmium	NO	-
Mercury	NO	-
Hexavalent chromium	NO	-
PBB (Polybrominated biphenyls)	NO	-
PBDE (Polybrominated diphenyl ethers)	NO	-

Pb-Free Soldering

IBIS4-A-6600-M2 (serial numbers beyond 3694): This product is successfully tested for Pb-free soldering processes, using a reflow temperature profile with maximum 260°C, minimum 40s at 255°C, and minimum 90s at 217°C.

IBIS4-A-6600-C2: This product does not withstand a lead-free soldering process. Maximum allowed reflow or wave soldering temperature is 220°C. Hand soldering is recommended for this part type.

Note that "Intentional content" is defined as any material demanding special attention is contained into the inquired product by following cases:

1. A case that the previously mentioned material is added as a chemical composition into the inquired product intentionally, to produce and maintain the required performance and function of the intended product.
2. A case that the previously mentioned material, which is used intentionally in the manufacturing process, is contained in or adhered to the inquired product.

The following case is not treated as "intentional content":

A case that the previously mentioned material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or is produced at a process, such as chemical composing or reaction and cannot be removed technically.

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Document History Page

Document Title: IBIS4-6600 CYII4SM6600AB 6.6 MP CMOS Image Sensor Document Number: 001-02366				
Rev.	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	384900	See ECN	FWU	Origination.
*A	402976	See ECN	FWU	Preliminary notice removed. Electro optical spec updated to characterization data.
*B	418669	See ECN	FVK	Table 15. ADC resistor values changed. ADC section added. Figure 33 p41 corrected
*C	502551	See ECN	QGS	Converted to Frame file
*D	642596	See ECN	FPW	Ordering information update
*E	2649816	03/17/2009	PCI/AESA	Final data sheet. Changed title from “IBIS4-A-6600 CMOS Image Sensor” to “IBIS4-6600 CYII4SM6600AB 6.6 MP CMOS Image Sensor”. Updated Typical Response Curve of the RGB Filters on page 7 and added Relative Response Graph on page 8. Updated Package Diagrams and data sheet template.
*F	2766198	09/19/09	NVEA	Updated Ordering Information table
*G	2902961	04/01/10	NVEA	Removed inactive part from the ordering information table.

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