THE DATASHEET OF

CY96F356RSBPMC1-GSUJF4E1

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CY96F353/F355
CY96F356

F²MC-16FX, CY96350 Series, 16-bit Proprietary Microcontroller

CY96350 series is based on Cypress's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4 MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

- Technology
  - 0.18 µm CMOS
- CPU
  - F²MC-16FX CPU
  - Up to 56 MHz internal, 17.8 ns instruction cycle time
  - Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
  - 8-byte instruction execution queue
  - Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
- System clock
  - On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
  - 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
  - Up to 56 MHz external clock
  - 32-100 kHz subsystem quartz clock
  - 100 kHz/2 MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
  - Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
  - Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
  - Clock modulator
- On-chip voltage regulator
  - Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
- Low voltage reset
  - Reset is generated when supply voltage is below minimum.
- Code Security
  - Protects ROM content from unintended read-out
- Memory Patch Function
  - Replaces ROM content
  - Can also be used to implement embedded debug support
- DMA
  - Automatic transfer function independent of CPU, can be assigned freely to resources
- Interrupts
  - Fast Interrupt processing
  - 8 programmable priority levels
  - Non-Maskable Interrupt (NMI)
- Timers
  - Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
  - Watchdog Timer
- CAN
  - Supports CAN protocol version 2.0 part A and B
  - ISO16845 certified
  - Bit rates up to 1 Mbit/s
  - 32 message objects
  - Each message object has its own identifier mask
  - Programmable FIFO mode (concatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation
- USART
  - Full duplex USARTs (SCI/LIN)
  - Wide range of baud rate settings using a dedicated reload timer
  - Special synchronous options for adapting to different synchronous serial protocols
  - LIN functionality working either as master or slave LIN device
- I²C
  - Up to 400 kbps
  - Master and Slave functionality, 7-bit and 10-bit addressing
- A/D converter
  - SAR-type
  - 10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, falling edge or rising & falling edge sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with 16-bit I/O Timer occurs
  - A pair of compare registers can be used to generate an output signal.
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
  - Can be triggered by software or reload timer
- Real Time Clock
  - Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
  - Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1 s clock
- External Interrupts
  - Edge sensitive or level sensitive
  - Interrupt mask and pending bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset
  - Once enabled, can not be disabled other than by reset.
  - Level high or level low sensitive
  - Pin shared with external interrupt 0.
- External bus interface
  - 8-bit or 16-bit bidirectional data
  - Up to 24-bit addresses
  - 6 chip select signals
  - Multiplexed address/data lines
  - Wait state request
  - External bus master possible
  - Timing programmable
- I/O Ports
  - Virtually all external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I^2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL
  - Bit-wise programmable pull-up resistor
  - Bit-wise programmable output driving strength for EMI optimization
- Package
  - 64-pin plastic LQFP
- Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the algorithm
  - Number of erase cycles: 10,000 times
  - Data retention time: 20 years
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase

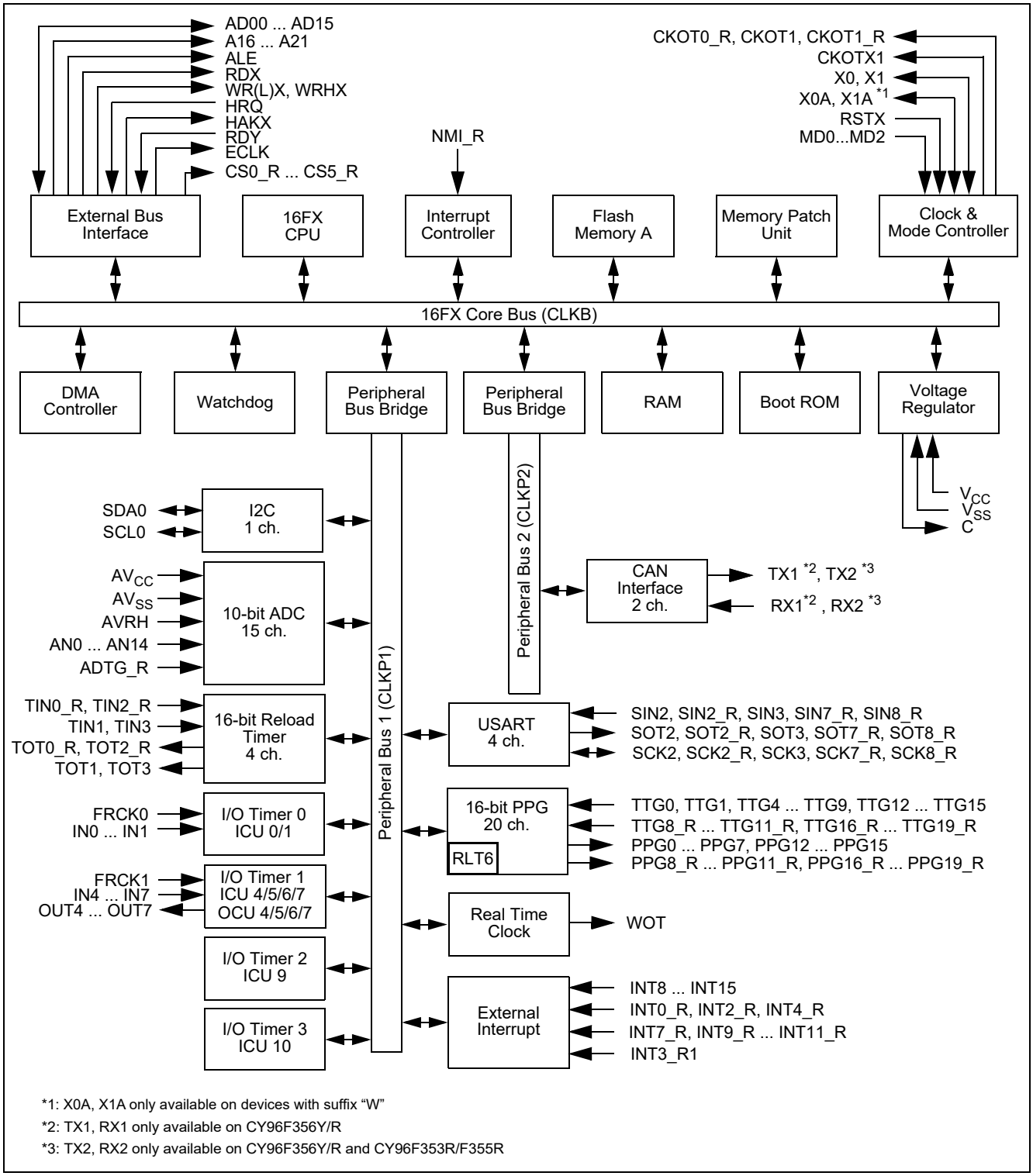
Contents

Product Lineup

Features		CY96V300C	CY96(F)35x
Product type		Evaluation sample	Flash product: CY96F35x Mask ROM product: CY9635x
Product options			
RS		NA	Low voltage reset can be disabled / Single clock devices
RW			Low voltage reset can be disabled / Dual clock devices
AS			No CAN / Low voltage reset can be disabled / Single clock devices
AW			No CAN / Low voltage reset can be disabled / Dual clock devices
Flash/ROM	RAM		
96 KB	8 KB	ROM/Flash memory emulation by external RAM, 92 KB internal RAM	CY96F353RS/RW/AS/AW
160 KB	8 KB		CY96F355RS/RW/AS/AW
288 KB	12 KB		CY96F356RS/RW/AS/AW
Package		BGA416	LQG064/LQD064
DMA		16 channels	4 channels
USART		10 channels	4 channels
I^2C		2 channels	1 channel
A/D Converter		40 channels	15 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	4 channels (2 channels with external clock input pin)
16-bit Output Compare		12 channels	4 channels
16-bit Input Capture		12 channels	6 channels (plus 2 channels for LIN USART)
16-bit Programmable Pulse Generator		20 channels	20 channels
CAN Interface		5 channels	CY96F35xA: no CY96F353R/F355R: 1 channel CY96F356R: 2 channels
External Interrupts		16 channels	13 channels
Non-Maskable Interrupt		1 channel	
Real Time Clock		1	
I/O Ports		136	49 for part number with suffix "W", 51 for part number with suffix "S"
External bus interface		Yes	
Chip select		6 signals	
Clock output function		2 channels	
Low voltage reset		Yes	
On-chip RC-oscillator		Yes	

Block Diagram

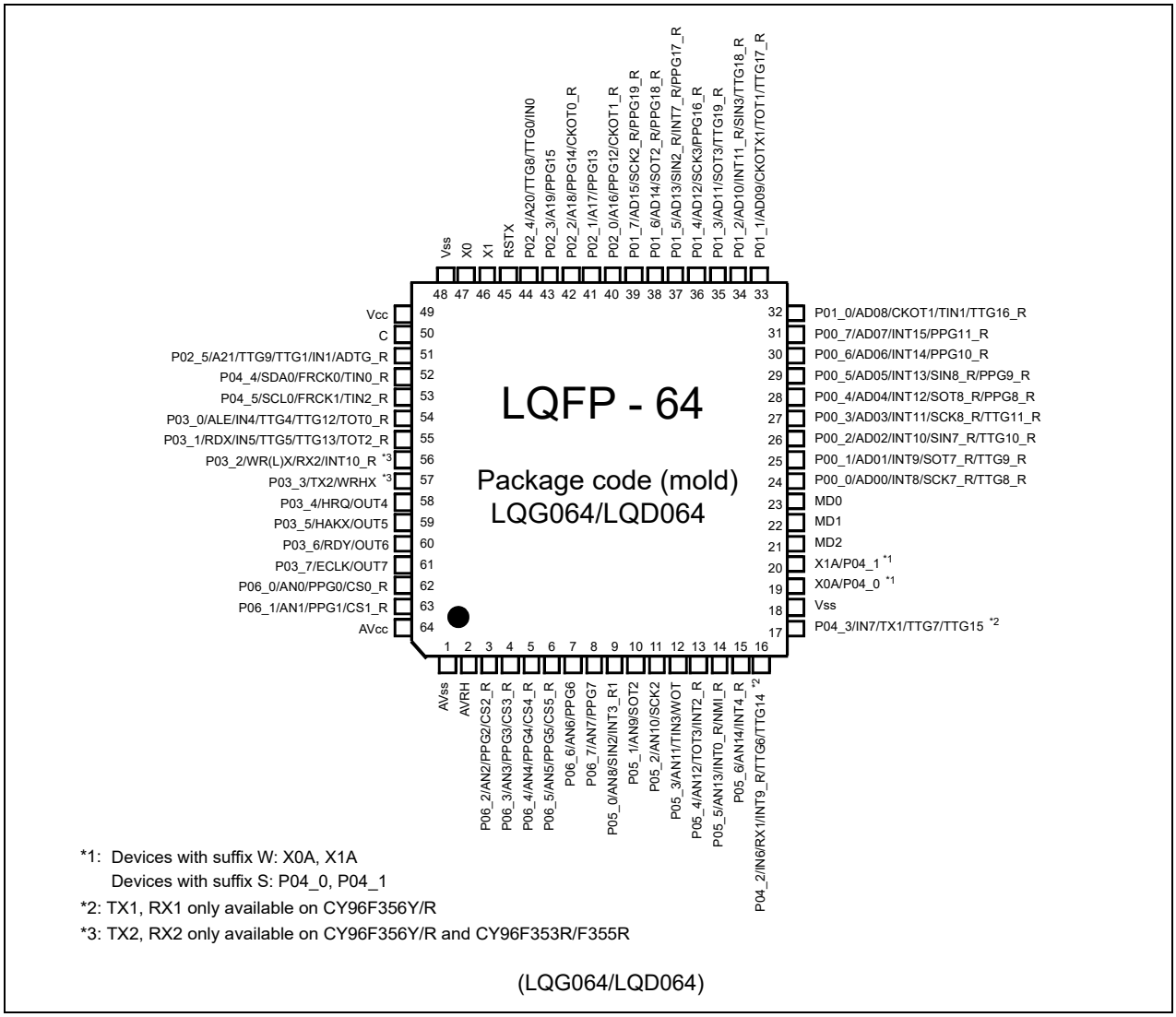
Figure 1. Block Diagram of CY96(F)35x



*1: X0A, X1A only available on devices with suffix “W”
*2: TX1, RX1 only available on CY96F356Y/R
*3: TX2, RX2 only available on CY96F356Y/R and CY96F353R/F355R

Pin Assignments

Figure 2. Pin Assignment of CY96(F)35x



*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1
*2: TX1, RX1 only available on CY96F356Y/R
*3: TX2, RX2 only available on CY96F356Y/R and CY96F353R/F355R

(LQG064/LQD064)

Remark:

CY96(F)35x products are pin-compatible to F^{2}MC-16LX family CY90350 series.

Pin Function Description

Table 1. Pin Function Description (1 / 2)

Pin Name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG_R	ADC	Relocated A/D converter trigger input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I^2C	I^2C interface n clock I/O input/output
SDAn	I^2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output

Table 1. Pin Function Description (2 / 2)

Pin Name	Feature	Description
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix “W”)
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix “W”)

Pin Circuit Type

Table 2. LQG064/LQD064

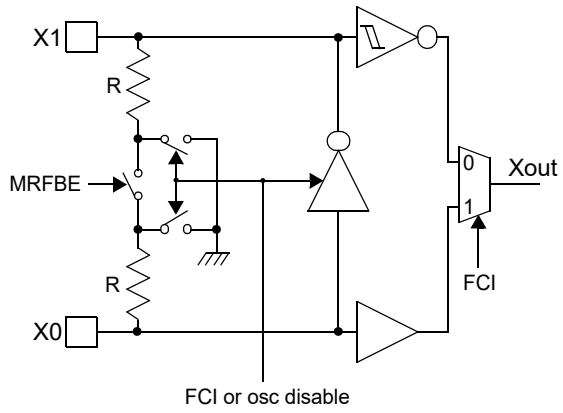
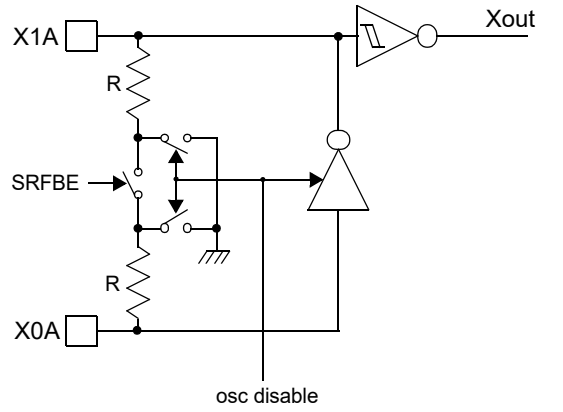
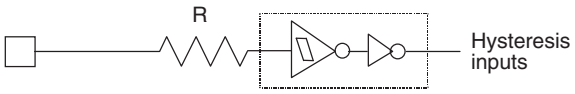
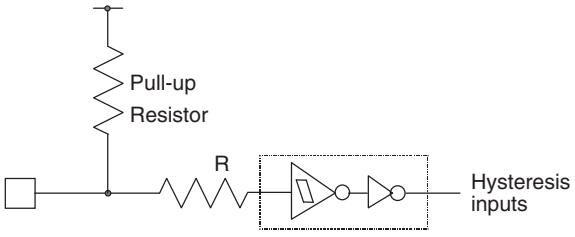
Pin No.	Circuit Type [*1]
1	Supply
2	G
3 to 15	I
16,17	H
18	Supply
19,20	B [*2]
19,20	H [*3]
21 to 23	C
24 to 44	H
45	E
46,47	A
48,49	Supply
50	F
51	H
52,53	N
54 to 61	H
62,63	I
64	Supply

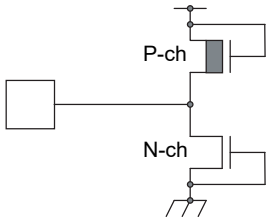
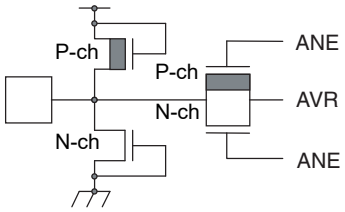
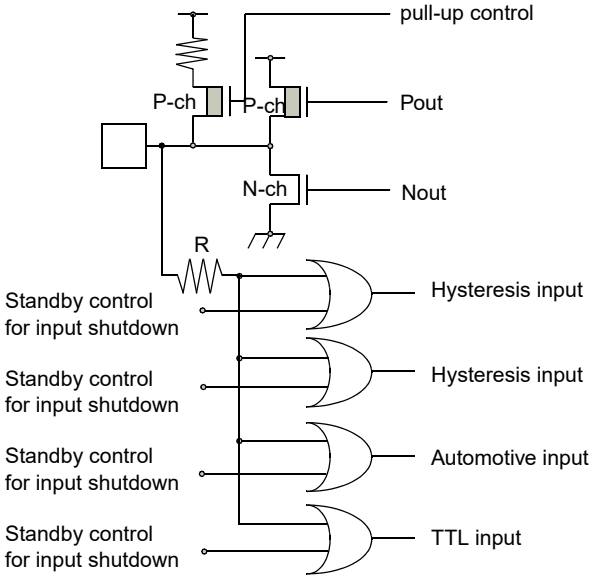
*1: Please refer to I/O Circuit Type for details on the I/O circuit types

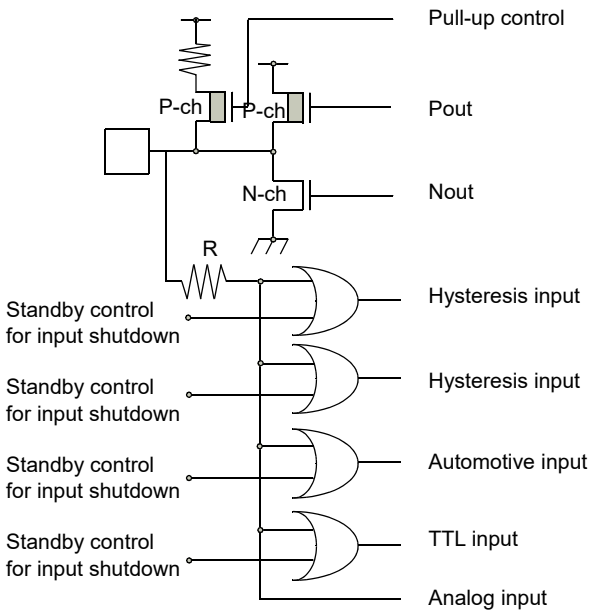
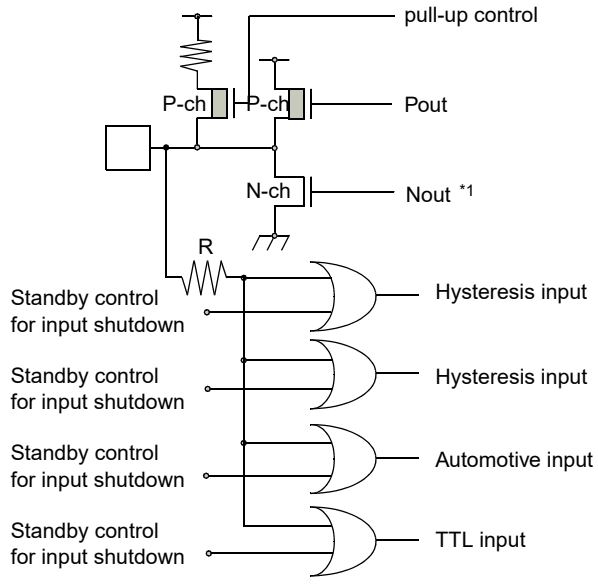
*2: Devices with suffix “W”

*3: Devices without suffix “W”

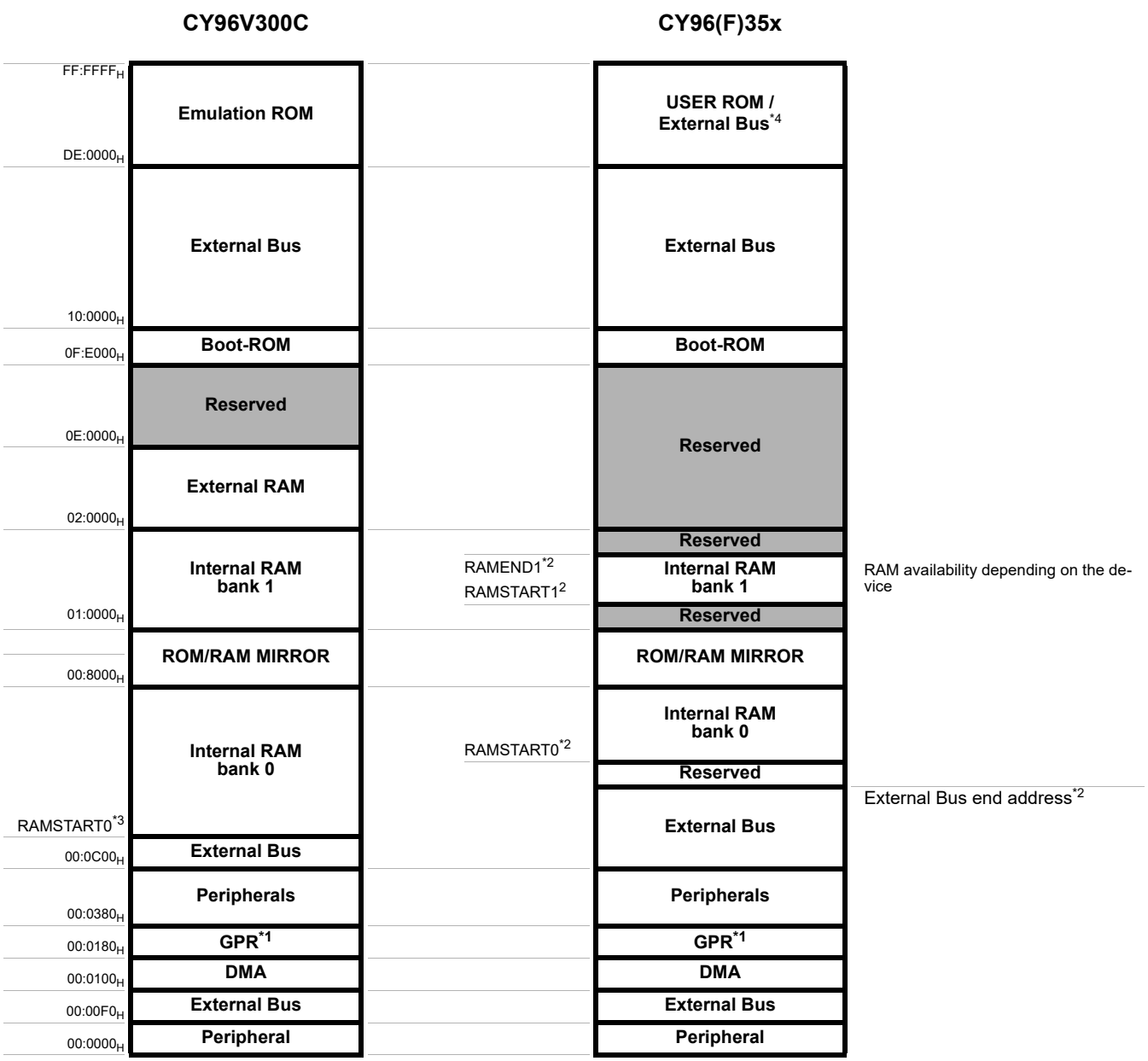
I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. 20 MΩ (X1A:19.5 MΩ, X0A:0.5 MΩ) Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device: CMOS Hysteresis input pin ■ Flash device: CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pin AVRH
H		■ CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown function ■ Programmable pull-up resistor: 50 kΩ approx. Note: CY96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown function. ■ Programmable pull-up resistor: 50 kΩ approx. ■ Analog input Note: CY96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = -3 mA) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown function ■ Programmable pull-up resistor: 50 kΩ approx. *1: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage Note: CY96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Memory Map

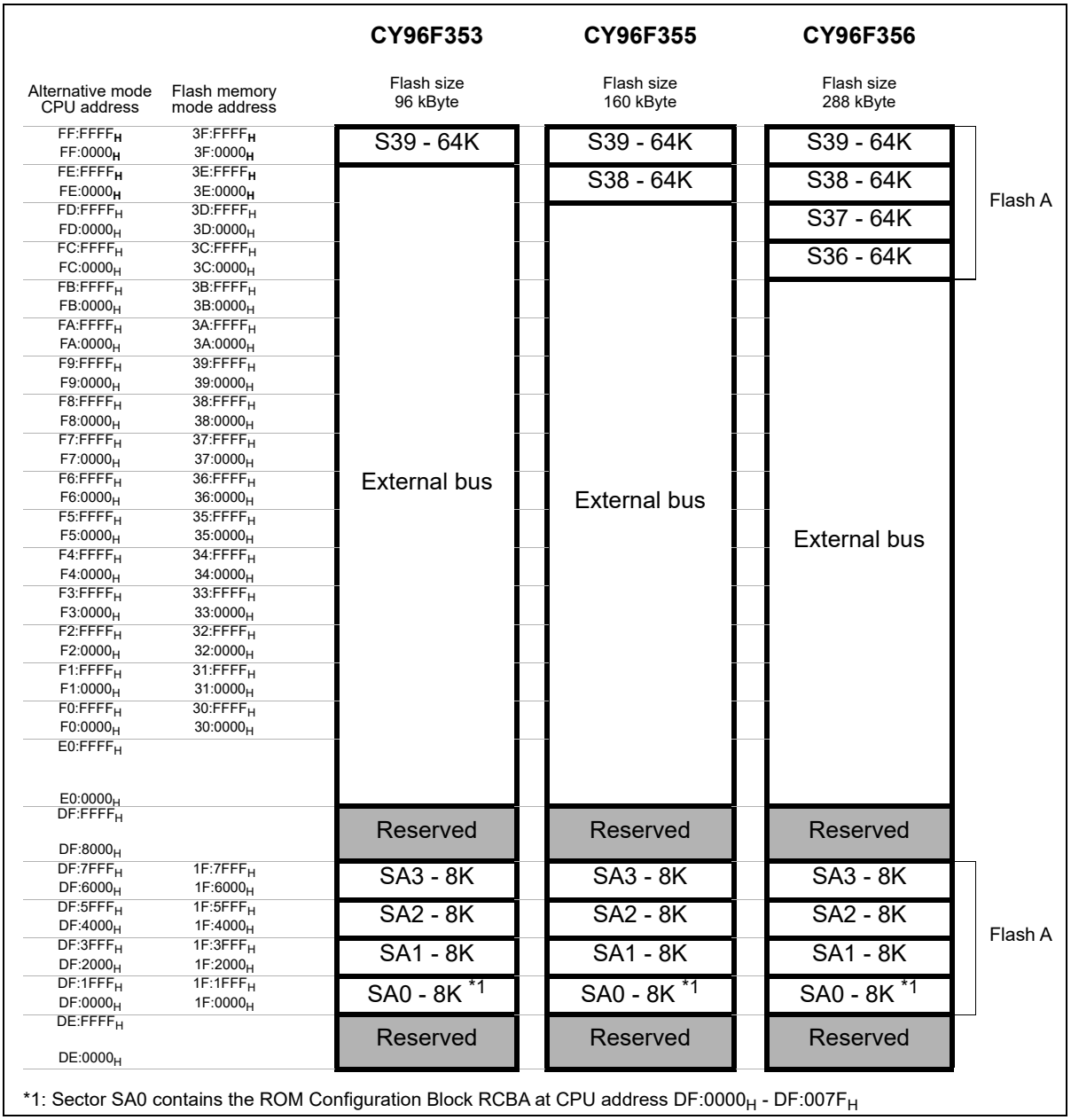


*1: Unused GPR banks can be used as RAM area
*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.
*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.
*4: For details about USER ROM area, see the User ROM Memory Map for Flash Devices on the following pages.
The External Bus area and DMA area are only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device.

RAMSTART/END and External Bus End Addresses

Devices	Bank 0 RAM Size	Bank 1 RAM Size	External Bus End Address	RAMSTART0	RAMSTART1	RAMEND1
CY96F353/F355	8 KByte	-	$00:51FF_H$	$00:6240_H$	-	-
CY96F356	12 KByte	-	$00:51FF_H$	$00:5240_H$	-	-

User ROM Memory Map for Flash Devices



Serial Programming Communication Interface

Table 3. USART pins for Flash serial programming (MD[2:0] = 010)

CY96F35x		
Pin Number	USART Number	Normal Function
LQFP-64		
9	USART2	SIN2
10		SOT2
11		SCK2
34	USART3	SIN3
35		SOT3
36		SCK3
26	USART7	SIN7_R
25		SOT7_R
24		SCK7_R
29	USART8	SIN8_R
28		SOT8_R
27		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 25.
If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O Map

Table 4. I/O Map CY96(F)35x (1 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000000_H	I/O Port P00 - Port Data Register	PDR00		R/W
000001_H	I/O Port P01 - Port Data Register	PDR01		R/W
000002_H	I/O Port P02 - Port Data Register	PDR02		R/W
000003_H	I/O Port P03 - Port Data Register	PDR03		R/W
000004_H	I/O Port P04 - Port Data Register	PDR04		R/W
000005_H	I/O Port P05 - Port Data Register	PDR05		R/W
000006_H	I/O Port P06 - Port Data Register	PDR06		R/W
000007_H-000017_H	Reserved			-
000018_H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019_H	ADC0 - Control Status register High	ADCSH		R/W
$00001A_H$	ADC0 - Data Register Low	ADCRL	ADCR	R
$00001B_H$	ADC0 - Data Register High	ADCRH		R
$00001C_H$	ADC0 - Setting Register		ADSR	R/W
$00001D_H$	ADC0 - Setting Register			R/W
$00001E_H$	ADC0 - Extended Configuration Register	ADECR		R/W
$00001F_H$	Reserved			-
000020_H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021_H	FRT0 - Data register of free-running timer			R/W
000022_H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023_H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024_H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025_H	FRT1 - Data register of free-running timer			R/W
000026_H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027_H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028_H-000033_H	Reserved			-
000034_H	OCU4 - Output Compare Control Status	OCS4		R/W
000035_H	OCU5 - Output Compare Control Status	OCS5		R/W
000036_H	OCU4 - Compare Register		OCCP4	R/W
000037_H	OCU4 - Compare Register			R/W
000038_H	OCU5 - Compare Register		OCCP5	R/W
000039_H	OCU5 - Compare Register			R/W
$00003A_H$	OCU6 - Output Compare Control Status	OCS6		R/W
$00003B_H$	OCU7 - Output Compare Control Status	OCS7		R/W
$00003C_H$	OCU6 - Compare Register		OCCP6	R/W
$00003D_H$	OCU6 - Compare Register			R/W
$00003E_H$	OCU7 - Compare Register		OCCP7	R/W
$00003F_H$	OCU7 - Compare Register			R/W
000040_H	ICU0/ICU1 - Control Status Register	ICS01		R/W

Table 4. I/O Map CY96(F)35x (2 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000041_H	ICU0/ICU1 - Edge register	ICE01		R/W
000042_H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043_H	ICU0 - Capture Register High	IPCPH0		R
000044_H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045_H	ICU1 - Capture Register High	IPCPH1		R
000046_H - $00004B_H$	Reserved			
$00004C_H$	ICU4/ICU5 - Control Status Register	ICS45		R/W
$00004D_H$	ICU4/ICU5 - Edge register	ICE45		R/W
$00004E_H$	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
$00004F_H$	ICU4 - Capture Register High	IPCPH4		R
000050_H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051_H	ICU5 - Capture Register High	IPCPH5		R
000052_H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053_H	ICU6/ICU7 - Edge register	ICE67		R/W
000054_H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055_H	ICU6 - Capture Register High	IPCPH6		R
000056_H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057_H	ICU7 - Capture Register High	IPCPH7		R
000058_H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059_H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
$00005A_H$	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
$00005B_H$	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
$00005C_H$	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
$00005D_H$	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
$00005E_H$	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
$00005F_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060_H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061_H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062_H	RLT0 - Reload Register - for writing		TMRLR0	W
000062_H	RLT0 - Reload Register - for reading		TMR0	R
000063_H	RLT0 - Reload Register - for writing			W
000063_H	RLT0 - Reload Register - for reading			R
000064_H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065_H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066_H	RLT1 - Reload Register - for writing		TMRLR1	W
000066_H	RLT1 - Reload Register - for reading		TMR1	R
000067_H	RLT1 - Reload Register - for writing			W
000067_H	RLT1 - Reload Register - for reading			R
000068_H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W

Table 4. I/O Map CY96(F)35x (3 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000069_H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
$00006A_H$	RLT2 - Reload Register - for writing		TMRLR2	W
$00006A_H$	RLT2 - Reload Register - for reading		TMR2	R
$00006B_H$	RLT2 - Reload Register - for writing			W
$00006B_H$	RLT2 - Reload Register - for reading			R
$00006C_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
$00006D_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
$00006E_H$	RLT3 - Reload Register - for writing		TMRLR3	W
$00006E_H$	RLT3 - Reload Register - for reading		TMR3	R
$00006F_H$	RLT3 - Reload Register - for writing			W
$00006F_H$	RLT3 - Reload Register - for reading			R
000070_H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071_H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074_H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075_H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076_H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077_H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078_H	PPG0 - Timer register		PTMR0	R
000079_H	PPG0 - Timer register			R
$00007A_H$	PPG0 - Period setting register		PCSR0	W
$00007B_H$	PPG0 - Period setting register			W
$00007C_H$	PPG0 - Duty cycle register		PDUT0	W
$00007D_H$	PPG0 - Duty cycle register			W
$00007E_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
$00007F_H$	PPG0 - Control status register High	PCNH0		R/W
000080_H	PPG1 - Timer register		PTMR1	R
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R

Table 4. I/O Map CY96(F)35x (4 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W
$0000A1_H$	PPG4 - Duty cycle register			W
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$	PPG5 - Timer register		PTMR5	R
$0000A5_H$	PPG5 - Timer register			R
$0000A6_H$	PPG5 - Period setting register		PCSR5	W
$0000A7_H$	PPG5 - Period setting register			W
$0000A8_H$	PPG5 - Duty cycle register		PDUT5	W
$0000A9_H$	PPG5 - Duty cycle register			W
$0000AA_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W
$0000AB_H$	PPG5 - Control status register High	PCNH5		R/W
$0000AC_H$	I2C0 - Bus Status Register	IBSR0		R
$0000AD_H$	I2C0 - Bus Control Register	IBCR0		R/W
$0000AE_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
$0000AF_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W

Table 4. I/O Map CY96(F)35x (5 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0000B0_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
$0000B1_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
$0000B2_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
$0000B3_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
$0000B4_H$	I2C0 - Data Register	IDAR0		R/W
$0000B5_H$	I2C0 - Clock Control Register	ICCR0		R/W
$0000B6_H$-$0000D3_H$	Reserved			-
$0000D4_H$	USART2 - Serial Mode Register	SMR2		R/W
$0000D5_H$	USART2 - Serial Control Register	SCR2		R/W
$0000D6_H$	USART2 - TX Register	TDR2		W
$0000D6_H$	USART2 - RX Register	RDR2		R
$0000D7_H$	USART2 - Serial Status	SSR2		R/W
$0000D8_H$	USART2 - Control/Com. Register	ECCR2		R/W
$0000D9_H$	USART2 - Ext. Status Register	ESCR2		R/W
$0000DA_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
$0000DB_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
$0000DC_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
$0000DD_H$	Reserved			-
$0000DE_H$	USART3 - Serial Mode Register	SMR3		R/W
$0000DF_H$	USART3 - Serial Control Register	SCR3		R/W
$0000E0_H$	USART3 - TX Register	TDR3		W
$0000E0_H$	USART3 - RX Register	RDR3		R
$0000E1_H$	USART3 - Serial Status	SSR3		R/W
$0000E2_H$	USART3 - Control/Com. Register	ECCR3		R/W
$0000E3_H$	USART3 - Ext. Status Register	ESCR3		R/W
$0000E4_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
$0000E5_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
$0000E6_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
$0000E7_H$-$0000EF_H$	Reserved			-
$0000F0_H$-$0000FF_H$	External Bus area	EXTBUS0		R/W
000100_H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101_H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102_H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103_H	DMA0 - DMA control register	DMACS0		R/W
000104_H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105_H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106_H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107_H	DMA0 - Data counter high byte	DCTH0		R/W
000108_H	DMA1 - Buffer address pointer low byte	BAPL1		R/W

Table 4. I/O Map CY96(F)35x (6 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000109_H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
$00010A_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
$00010B_H$	DMA1 - DMA control register	DMACS1		R/W
$00010C_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
$00010D_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
$00010E_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
$00010F_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110_H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111_H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112_H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113_H	DMA2 - DMA control register	DMACS2		R/W
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H-$00017F_H$	Reserved			-
000180_H-$00037F_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380_H	DMA0 - Interrupt select	DISEL0		R/W
000381_H	DMA1 - Interrupt select	DISEL1		R/W
000382_H	DMA2 - Interrupt select	DISEL2		R/W
000383_H	DMA3 - Interrupt select	DISEL3		R/W
000384_H-$00038F_H$	Reserved			—
000390_H	DMA - Status register low byte	DSRL	DSR	R/W
000391_H	DMA - Status register high byte	DSRH		R/W
000392_H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393_H	DMA - Stop status register high byte	DSSRH		R/W
000394_H	DMA - Enable register low byte	DERL	DER	R/W
000395_H	DMA - Enable register high byte	DERH		R/W
000396_H-$00039F_H$	Reserved			-
$0003A0_H$	Interrupt level register	ILR	ICR	R/W
$0003A1_H$	Interrupt index register	IDX		R/W

Table 4. I/O Map CY96(F)35x (7 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0003A2_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
$0003A3_H$	Interrupt vector table base register High	TBRH		R/W
$0003A4_H$	Delayed Interrupt register	DIRR		R/W
$0003A5_H$	Non Maskable Interrupt register	NMI		R/W
$0003A6_H$-$0003AB_H$	Reserved			-
$0003AC_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
$0003AD_H$	EDSU communication interrupt selection High	EDSU2H		R/W
$0003AE_H$	ROM mirror control register	ROMM		R/W
$0003AF_H$	EDSU configuration register	EDSU		R/W
$0003B0_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
$0003B1_H$	Memory patch control/status register ch 0/1			R/W
$0003B2_H$	Memory patch control/status register ch 2/3		PFCS1	R/W
$0003B3_H$	Memory patch control/status register ch 2/3			R/W
$0003B4_H$	Memory patch control/status register ch 4/5		PFCS2	R/W
$0003B5_H$	Memory patch control/status register ch 4/5			R/W
$0003B6_H$	Memory patch control/status register ch 6/7		PFCS3	R/W
$0003B7_H$	Memory patch control/status register ch 6/7			R/W
$0003B8_H$	Memory Patch function - Patch address 0 low	PFAL0		R/W
$0003B9_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W
$0003BA_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
$0003BB_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
$0003BC_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
$0003BD_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
$0003BE_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
$0003BF_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
$0003C0_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
$0003C1_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
$0003C2_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
$0003C3_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
$0003C4_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
$0003C5_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
$0003C6_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
$0003C7_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
$0003C8_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
$0003C9_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
$0003CA_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
$0003CB_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
$0003CC_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
$0003CD_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W

Table 4. I/O Map CY96(F)35x (8 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0003CE_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
$0003CF_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
$0003D9_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
$0003DA_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
$0003DB_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
$0003DC_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
$0003DD_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
$0003DE_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
$0003DF_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
$0003E0_H$-$0003F0_H$	Reserved			-
$0003F1_H$	Memory Control Status Register A	MCSRA		R/W
$0003F2_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
$0003F3_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
$0003F4_H$-$0003F8_H$	Reserved			-
$0003F9_H$	Flash Memory Write Control register 1	FMWC1		R/W
$0003FA_H$	Flash Memory Write Control register 2	FMWC2		R/W
$0003FB_H$	Flash Memory Write Control register 3	FMWC3		R/W
$0003FC_H$	Flash Memory Write Control register 4	FMWC4		R/W
$0003FD_H$	Flash Memory Write Control register 5	FMWC5		R/W
$0003FE_H$-$0003FF_H$	Reserved			-
000400_H	Standby Mode control register	SMCR		R/W
000401_H	Clock select register	CKSR		R/W
000402_H	Clock Stabilization select register	CKSSR		R/W
000403_H	Clock monitor register	CKMR		R
000404_H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405_H	Clock Frequency control register High	CKFCRH		R/W
000406_H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407_H	PLL Control register High	PLLCRH		R/W
000408_H	RC clock timer control register	RCTCR		R/W
000409_H	Main clock timer control register	MCTCR		R/W

Table 4. I/O Map CY96(F)35x (9 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$00040A_H$	Sub clock timer control register	SCTCR		R/W
$00040B_H$	Reset cause and clock status register with clear function	RCCSRC		R
$00040C_H$	Reset configuration register	RCR		R/W
$00040D_H$	Reset cause and clock status register	RCCSR		R
$00040E_H$	Watch dog timer configuration register	WDTC		R/W
$00040F_H$	Watch dog timer clear pattern register	WDTCP		W
000410_H-000414_H	Reserved			-
000415_H	Clock output activation register	COAR		R/W
000416_H	Clock output configuration register 0	COCR0		R/W
000417_H	Clock output configuration register 1	COCR1		R/W
000418_H	Clock Modulator control register	CMCR		R/W
000419_H	Reserved			-
$00041A_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
$00041B_H$	Clock Modulator Parameter register High	CMPRH		R/W
$00041C_H$-$00042B_H$	Reserved			-
$00042C_H$	Voltage Regulator Control register	VRCR		R/W
$00042D_H$	Clock Input and LVD Control Register	CILCR		R/W
$00042E_H$-$00042F_H$	Reserved			-
000430_H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431_H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432_H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433_H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434_H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W

Table 4. I/O Map CY96(F)35x (10 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473_H-$00047F_H$	Reserved			-
000480_H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481_H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482_H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483_H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484_H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485_H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486_H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487_H-$0004A7_H$	Reserved			-
$0004A8_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
$0004A9_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
$0004AA_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
$0004AB_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
$0004AC_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
$0004AD_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
$0004AE_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
$0004AF_H$-$0004BB_H$	Reserved			-
$0004BC_H$	I/O Port P00 - External Pin State Register	EPSR00		R
$0004BD_H$	I/O Port P01 - External Pin State Register	EPSR01		R
$0004BE_H$	I/O Port P02 - External Pin State Register	EPSR02		R
$0004BF_H$	I/O Port P03 - External Pin State Register	EPSR03		R
$0004C0_H$	I/O Port P04 - External Pin State Register	EPSR04		R
$0004C1_H$	I/O Port P05 - External Pin State Register	EPSR05		R
$0004C2_H$	I/O Port P06 - External Pin State Register	EPSR06		R
$0004C3_H$-$0004CF_H$	Reserved			-
$0004D0_H$	ADC analog input enable register 0	ADER0		R/W
$0004D1_H$	ADC analog input enable register 1	ADER1		R/W
$0004D2_H$	ADC analog input enable register 2	ADER2		R/W
$0004D3_H$	ADC analog input enable register 3	ADER3		R/W

Table 4. I/O Map CY96(F)35x (11 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0004D4_H$	ADC analog input enable register 4	ADER4		R/W
$0004D5_H$	Reserved			-
$0004D6_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
$0004D7_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
$0004D8_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
$0004D9_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
$0004DA_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
$0004DB_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
$0004DC_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
$0004DD_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$0004FF_H$	Reserved			-
000500_H	FRT2 - Data register of free-running timer		TCDT2	R/W
000501_H	FRT2 - Data register of free-running timer			R/W
000502_H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503_H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504_H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505_H	FRT3 - Data register of free-running timer			R/W

Table 4. I/O Map CY96(F)35x (12 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000506_H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507_H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508_H-000513_H	Reserved			-
000514_H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515_H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516_H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517_H	ICU8 - Capture Register High	IPCPH8		R
000518_H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519_H	ICU9 - Capture Register High	IPCPH9		R
$00051A_H$	ICU10/ICU11 - Control Status Register	ICS1011		R/W
$00051B_H$	ICU10/ICU11 - Edge Register	ICE1011		R/W
$00051C_H$	ICU10 - Capture Register Low	IPCPL10	IPCP10	R
$00051D_H$	ICU10 - Capture Register High	IPCPH10		R
$00051E_H$	ICU11 - Capture Register Low	IPCPL11	IPCP11	R
$00051F_H$	ICU11 - Capture Register High	IPCPH11		R
000520_H-$00053D_H$	Reserved			-
$00053E_H$	USART7 - Serial Mode Register	SMR7		R/W
$00053F_H$	USART7 - Serial Control Register	SCR7		R/W
000540_H	USART7 - Serial TX Register	TDR7		W
000540_H	USART7 - Serial RX Register	RDR7		R
000541_H	USART7 - Serial Status Register	SSR7		R/W
000542_H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543_H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544_H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545_H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546_H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547_H	Reserved			-
000548_H	USART8 - Serial Mode Register	SMR8		R/W
000549_H	USART8 - Serial Control Register	SCR8		R/W
$00054A_H$	USART8 - Serial TX Register	TDR8		W
$00054A_H$	USART8 - Serial RX Register	RDR8		R
$00054B_H$	USART8 - Serial Status Register	SSR8		R/W
$00054C_H$	USART8 - Ext. Control/Com. Register	ECCR8		R/W
$00054D_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
$00054E_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
$00054F_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550_H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551_H-000563_H	Reserved			-
000564_H	PPG6 - Timer register		PTMR6	R

Table 4. I/O Map CY96(F)35x (13 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000565_H	PPG6 - Timer register			R
000566_H	PPG6 - Period setting register		PCSR6	W
000567_H	PPG6 - Period setting register			W
000568_H	PPG6 - Duty cycle register		PDUT6	W
000569_H	PPG6 - Duty cycle register			W
$00056A_H$	PPG6 - Control status register Low	PCNL6	PCN6	R/W
$00056B_H$	PPG6 - Control status register High	PCNH6		R/W
$00056C_H$	PPG7 - Timer register		PTMR7	R
$00056D_H$	PPG7 - Timer register			R
$00056E_H$	PPG7 - Period setting register		PCSR7	W
$00056F_H$	PPG7 - Period setting register			W
000570_H	PPG7 - Duty cycle register		PDUT7	W
000571_H	PPG7 - Duty cycle register			W
000572_H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573_H	PPG7 - Control status register High	PCNH7		R/W
000574_H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575_H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576_H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577_H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578_H	PPG8 - Timer register		PTMR8	R
000579_H	PPG8 - Timer register			R
$00057A_H$	PPG8 - Period setting register		PCSR8	W
$00057B_H$	PPG8 - Period setting register			W
$00057C_H$	PPG8 - Duty cycle register		PDUT8	W
$00057D_H$	PPG8 - Duty cycle register			W
$00057E_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
$00057F_H$	PPG8 - Control status register High	PCNH8		R/W
000580_H	PPG9 - Timer register		PTMR9	R
000581_H	PPG9 - Timer register			R
000582_H	PPG9 - Period setting register		PCSR9	W
000583_H	PPG9 - Period setting register			W
000584_H	PPG9 - Duty cycle register		PDUT9	W
000585_H	PPG9 - Duty cycle register			W
000586_H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587_H	PPG9 - Control status register High	PCNH9		R/W
000588_H	PPG10 - Timer register		PTMR10	R
000589_H	PPG10 - Timer register			R
$00058A_H$	PPG10 - Period setting register		PCSR10	W
$00058B_H$	PPG10 - Period setting register			W

Table 4. I/O Map CY96(F)35x (14 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$00058C_H$	PPG10 - Duty cycle register		PDUT10	W
$00058D_H$	PPG10 - Duty cycle register			W
$00058E_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
$00058F_H$	PPG10 - Control status register High	PCNH10		R/W
000590_H	PPG11 - Timer register		PTMR11	R
000591_H	PPG11 - Timer register			R
000592_H	PPG11 - Period setting register		PCSR11	W
000593_H	PPG11 - Period setting register			W
000594_H	PPG11 - Duty cycle register		PDUT11	W
000595_H	PPG11 - Duty cycle register			W
000596_H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597_H	PPG11 - Control status register High	PCNH11		R/W
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$	PPG13 - Timer register		PTMR13	R
$0005A5_H$	PPG13 - Timer register			R
$0005A6_H$	PPG13 - Period setting register		PCSR13	W
$0005A7_H$	PPG13 - Period setting register			W
$0005A8_H$	PPG13 - Duty cycle register		PDUT13	W
$0005A9_H$	PPG13 - Duty cycle register			W
$0005AA_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
$0005AB_H$	PPG13 - Control status register High	PCNH13		R/W
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W

Table 4. I/O Map CY96(F)35x (15 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
$0005BD_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
$0005BE_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
$0005BF_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
$0005C0_H$	PPG16 - Timer register		PTMR16	R
$0005C1_H$	PPG16 - Timer register			R
$0005C2_H$	PPG16 - Period setting register		PCSR16	W
$0005C3_H$	PPG16 - Period setting register			W
$0005C4_H$	PPG16 - Duty cycle register		PDUT16	W
$0005C5_H$	PPG16 - Duty cycle register			W
$0005C6_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
$0005C7_H$	PPG16 - Control status register High	PCNH16		R/W
$0005C8_H$	PPG17 - Timer register		PTMR17	R
$0005C9_H$	PPG17 - Timer register			R
$0005CA_H$	PPG17 - Period setting register		PCSR17	W
$0005CB_H$	PPG17 - Period setting register			W
$0005CC_H$	PPG17 - Duty cycle register		PDUT17	W
$0005CD_H$	PPG17 - Duty cycle register			W
$0005CE_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
$0005CF_H$	PPG17 - Control status register High	PCNH17		R/W
$0005D0_H$	PPG18 - Timer register		PTMR18	R
$0005D1_H$	PPG18 - Timer register			R
$0005D2_H$	PPG18 - Period setting register		PCSR18	W
$0005D3_H$	PPG18 - Period setting register			W
$0005D4_H$	PPG18 - Duty cycle register		PDUT18	W
$0005D5_H$	PPG18 - Duty cycle register			W
$0005D6_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
$0005D7_H$	PPG18 - Control status register High	PCNH18		R/W
$0005D8_H$	PPG19 - Timer register		PTMR19	R
$0005D9_H$	PPG19 - Timer register			R

Table 4. I/O Map CY96(F)35x (16 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0005DA_H$	PPG19 - Period setting register		PCSR19	W
$0005DB_H$	PPG19 - Period setting register			W
$0005DC_H$	PPG19 - Duty cycle register		PDUT19	W
$0005DD_H$	PPG19 - Duty cycle register			W
$0005DE_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
$0005DF_H$	PPG19 - Control status register High	PCNH19		R/W
$0005E0_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
$0006E9_H$	External Bus - Area configuration register 4 High	EACH4		R/W
$0006EA_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
$0006EB_H$	External Bus - Area configuration register 5 High	EACH5		R/W
$0006EC_H$	External Bus - Area select register 2	EAS2		R/W
$0006ED_H$	External Bus - Area select register 3	EAS3		R/W
$0006EE_H$	External Bus - Area select register 4	EAS4		R/W
$0006EF_H$	External Bus - Area select register 5	EAS5		R/W
$0006F0_H$	External Bus - Mode register	EBM		R/W
$0006F1_H$	External Bus - Clock and Function register	EBCF		R/W
$0006F2_H$	External Bus - Address output enable register 0	EBAE0		R/W
$0006F3_H$	External Bus - Address output enable register 1	EBAE1		R/W
$0006F4_H$	External Bus - Address output enable register 2	EBAE2		R/W
$0006F5_H$	External Bus - Control signal register	EBCS		R/W
$0006F6_H$-$0007FF_H$	Reserved			-
000800_H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R

Table 4. I/O Map CY96(F)35x (17 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$-$00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814_H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815_H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816_H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817_H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818_H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819_H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
$00081A_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
$00081B_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
$00081C_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
$00081D_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
$00081E_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
$00081F_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820_H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821_H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822_H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823_H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824_H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825_H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826_H-$00083F_H$	Reserved			-
000840_H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841_H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842_H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843_H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844_H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W

Table 4. I/O Map CY96(F)35x (18 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000845_H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846_H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847_H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848_H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849_H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
$00084A_H$	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
$00084B_H$	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
$00084C_H$	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
$00084D_H$	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
$00084E_H$	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
$00084F_H$	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850_H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851_H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852_H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853_H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854_H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855_H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856_H-$00087F_H$	Reserved			-
000880_H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881_H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882_H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883_H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884_H-$00088F_H$	Reserved			-
000890_H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891_H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892_H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893_H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894_H-$00089F_H$	Reserved			-
$0008A0_H$	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
$0008A1_H$	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
$0008A2_H$	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
$0008A3_H$	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
$0008A4_H$-$0008AF_H$	Reserved			-
$0008B0_H$	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
$0008B1_H$	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
$0008B2_H$	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
$0008B3_H$	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
$0008B4_H$-$0008CD_H$	Reserved			-
$0008CE_H$	CAN1 - Output enable register	COER1		R/W

Table 4. I/O Map CY96(F)35x (19 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0008CF_H$-$0008FF_H$	Reserved			-
000900_H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901_H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902_H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903_H	CAN2 - Status register High (reserved)	STATRH2		R
000904_H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905_H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906_H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907_H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908_H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909_H	CAN2 - Interrupt Register High	INTRH2		R
$00090A_H$	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
$00090B_H$	CAN2 - Test Register High (reserved)	TESTRH2		R
$00090C_H$	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
$00090D_H$	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
$00090E_H$-$00090F_H$	Reserved			-
000910_H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911_H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912_H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913_H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914_H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915_H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916_H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917_H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W
000918_H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919_H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
$00091A_H$	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
$00091B_H$	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
$00091C_H$	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
$00091D_H$	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
$00091E_H$	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W
$00091F_H$	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920_H	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921_H	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922_H	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923_H	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924_H	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925_H	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W
000926_H-$00093F_H$	Reserved			-

Table 4. I/O Map CY96(F)35x (20 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
000940_H	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	R/W
000941_H	CAN2 - IF2 Command request register High	IF2CREQH2		R/W
000942_H	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	R/W
000943_H	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944_H	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	R/W
000945_H	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		R/W
000946_H	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	R/W
000947_H	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		R/W
000948_H	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	R/W
000949_H	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		R/W
$00094A_H$	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	R/W
$00094B_H$	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		R/W
$00094C_H$	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	R/W
$00094D_H$	CAN2 - IF2 Message Control Register High	IF2MCTRH2		R/W
$00094E_H$	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	R/W
$00094F_H$	CAN2 - IF2 Data A1 High	IF2DTA1H2		R/W
000950_H	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	R/W
000951_H	CAN2 - IF2 Data A2 High	IF2DTA2H2		R/W
000952_H	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	R/W
000953_H	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954_H	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W
000955_H	CAN2 - IF2 Data B2 High	IF2DTB2H2		R/W
000956_H-$00097F_H$	Reserved			-
000980_H	CAN2 - Transmission Request 1 Register Low	TREQR1L2	TREQR12	R
000981_H	CAN2 - Transmission Request 1 Register High	TREQR1H2		R
000982_H	CAN2 - Transmission Request 2 Register Low	TREQR2L2	TREQR22	R
000983_H	CAN2 - Transmission Request 2 Register High	TREQR2H2		R
000984_H-$00098F_H$	Reserved			-
000990_H	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991_H	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992_H	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993_H	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994_H-$00099F_H$	Reserved			-
$0009A0_H$	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
$0009A1_H$	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
$0009A2_H$	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
$0009A3_H$	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
$0009A4_H$-$0009AF_H$	Reserved			-
$0009B0_H$	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R

Table 4. I/O Map CY96(F)35x (21 / 21)

Address	Register	Abbreviation 8-bit Access	Abbreviation 16-bit Access	Access
$0009B1_H$	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
$0009B2_H$	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
$0009B3_H$	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R
$0009B4_H$-$0009CD_H$	Reserved			-
$0009CE_H$	CAN2 - Output enable register	COER2		R/W
$0009CF_H$-$000BFF_H$	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

Interrupt Vector Table

Table 5. Interrupt Vector Table CY96(F)35x (1 / 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	PLL_UNLOCK	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$				Reserved
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$				Reserved
23	$3A0_H$	EXTINT7	Yes	23	External Interrupt 7
24	$39C_H$	EXTINT8	Yes	24	External Interrupt 8
25	398_H	EXTINT9	Yes	25	External Interrupt 9
26	394_H	EXTINT10	Yes	26	External Interrupt 10
27	390_H	EXTINT11	Yes	27	External Interrupt 11
28	$38C_H$	EXTINT12	Yes	28	External Interrupt 12
29	388_H	EXTINT13	Yes	29	External Interrupt 13
30	384_H	EXTINT14	Yes	30	External Interrupt 14
31	380_H	EXTINT15	Yes	31	External Interrupt 15
32	$37C_H$	CAN1	No	32	CAN Controller 1 (only CY96F356Y/R)
33	378_H	CAN2	No	33	CAN Controller 2 (only CY96F356Y/R and CY96F353R/F355R)
34	374_H	PPG0	Yes	34	Programmable Pulse Generator 0
35	370_H	PPG1	Yes	35	Programmable Pulse Generator 1

Table 5. Interrupt Vector Table CY96(F)35x (2 / 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
36	$36C_H$	PPG2	Yes	36	Programmable Pulse Generator 2
37	368_H	PPG3	Yes	37	Programmable Pulse Generator 3
38	364_H	PPG4	Yes	38	Programmable Pulse Generator 4
39	360	PPG5	Yes	39	Programmable Pulse Generator 5
40	$35C_H$	PPG6	Yes	40	Programmable Pulse Generator 6
41	358_H	PPG7	Yes	41	Programmable Pulse Generator 7
42	354_H	PPG8	Yes	42	Programmable Pulse Generator 8
43	350_H	PPG9	Yes	43	Programmable Pulse Generator 9
44	$34C_H$	PPG10	Yes	44	Programmable Pulse Generator 10
45	348_H	PPG11	Yes	45	Programmable Pulse Generator 11
46	344_H	PPG12	Yes	46	Programmable Pulse Generator 12
47	340_H	PPG13	Yes	47	Programmable Pulse Generator 13
48	$33C_H$	PPG14	Yes	48	Programmable Pulse Generator 14
49	338_H	PPG15	Yes	49	Programmable Pulse Generator 15
50	334_H	PPG16	Yes	50	Programmable Pulse Generator 16
51	330_H	PPG17	Yes	51	Programmable Pulse Generator 17
52	$32C_H$	PPG18	Yes	52	Programmable Pulse Generator 18
53	328_H	PPG19	Yes	53	Programmable Pulse Generator 19
54	324_H	RLT0	Yes	54	Reload Timer 0
55	320_H	RLT1	Yes	55	Reload Timer 1
56	$31C_H$	RLT2	Yes	56	Reload Timer 2
57	318_H	RLT3	Yes	57	Reload Timer 3
58	314_H	PPGRLT	Yes	58	Reload Timer 6 - dedicated for PPG
59	310_H	ICU0	Yes	59	Input Capture Unit 0
60	$30C_H$	ICU1	Yes	60	Input Capture Unit 1
61	308_H				Reserved
62	304_H				Reserved
63	300_H	ICU4	Yes	63	Input Capture Unit 4
64	$2FC_H$	ICU5	Yes	64	Input Capture Unit 5
65	$2F8_H$	ICU6	Yes	65	Input Capture Unit 6
66	$2F4_H$	ICU7	Yes	66	Input Capture Unit 7
67	$2F0_H$				Reserved
68	$2EC_H$	ICU9	Yes	68	Input Capture Unit 9
69	$2E8_H$	ICU10	Yes	69	Input Capture Unit 10
70	$2E4_H$				Reserved
71	$2E0_H$	OCU4	Yes	71	Output Compare Unit 4
72	$2DC_H$	OCU5	Yes	72	Output Compare Unit 5
73	$2D8_H$	OCU6	Yes	73	Output Compare Unit 6

Table 5. Interrupt Vector Table CY96(F)35x (3 / 3)

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
74	$2D4_H$	OCU7	Yes	74	Output Compare Unit 7
75	$2D0_H$				Reserved
76	$2CC_H$				Reserved
77	$2C8_H$	FRT0	Yes	77	Free Running Timer 0
78	$2C4_H$	FRT1	Yes	78	Free Running Timer 1
79	$2C0_H$	FRT2	Yes	79	Free Running Timer 2
80	$2BC_H$	FRT3	Yes	80	Free Running Timer 3
81	$2B8_H$	RTC0	No	81	Real Timer Clock
82	$2B4_H$	CAL0	No	82	Clock Calibration Unit
83	$2B0_H$	IIC0	Yes	83	I2C interface
84	$2AC_H$	ADC0	Yes	84	A/D Converter
85	$2A8_H$	LINR2	Yes	85	LIN USART 2 RX
86	$2A4_H$	LINT2	Yes	86	LIN USART 2 TX
87	$2A0_H$	LINR3	Yes	87	LIN USART 3 RX
88	$29C_H$	LINT3	Yes	88	LIN USART 3 TX
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	FLASH_A	No	93	Flash memory A (only Flash devices)

Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Clock modulator

1. Latch-up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

2. Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

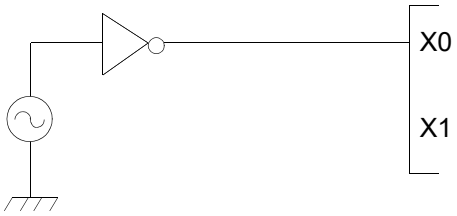
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

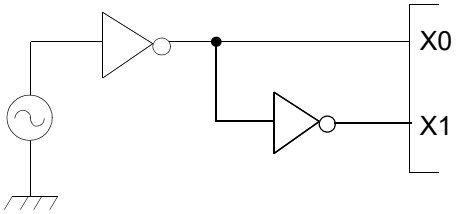
3. External Clock Usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock
   - When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



2. Opposite phase external clock
   - When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused Sub Clock Signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL Clock Mode Operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power Supply Pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

Please add the bypass capacitor of the power supply in order to not exceed 0.1V/µs.

7. Crystal Oscillator and Ceramic Resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin Handling when Not Using the A/D Converter

It is required to connect the unused pins of the A/D converter as AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 µs from 0.2 V to 2.7 V.

11. Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10 % of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1 V/µs or less in instantaneous fluctuation for power supply switching.

12. Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13. Clock modulator

Please contact Cypress before using this function.

Electrical Characteristics

Absolute Maximum Ratings

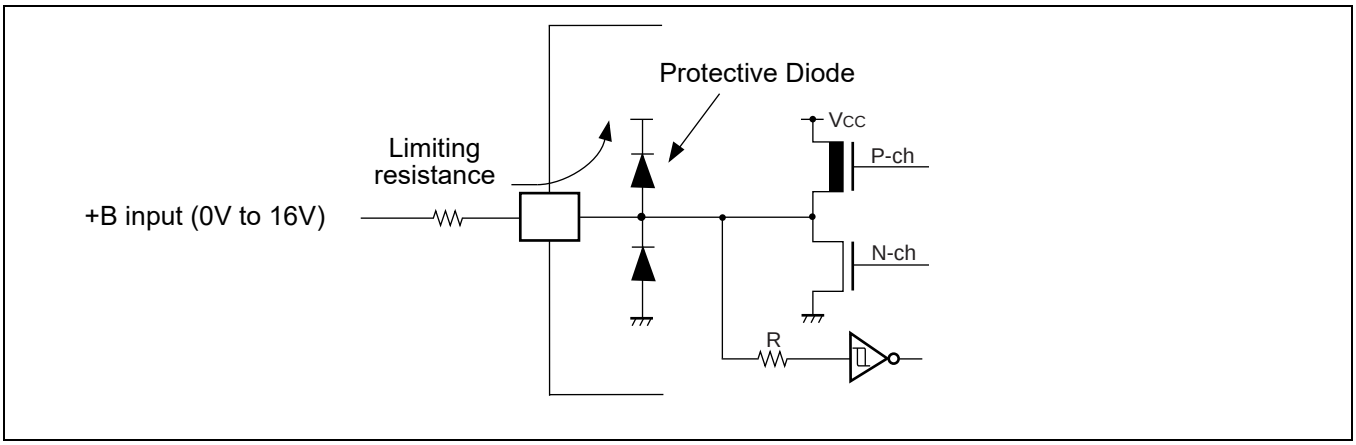
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *1
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3 V *2
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3 V *2
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purpose I/O pins *3
“L” level maximum output current	I_{OL1}	-	15	mA	Outputs with driving strength set to 2 mA /3 mA /5 mA
“L” level average output current	I_{OLAV2}	-	2	mA	Outputs with driving strength set to 2mA
	I_{OLAV3}	-	3	mA	Outputs of I/O circuit type “N”
	I_{OLAV5}	-	5	mA	Outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Outputs with driving strength set to 2 mA /3 mA /5 mA
”H” level average output current	I_{OHAV2}	-	-2	mA	Outputs with driving strength set to 2 mA
	I_{OHAV3}	-	-3	mA	Outputs of I/O circuit type “N”
	I_{OHAV5}	-	-5	mA	Outputs with driving strength set to 5 mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices) *4	P_D	-	320 *5	mW	T_A=105 °C
		-	640 *5	mW	T_A=85 °C
		-	800 *5	mW	T_A=75 °C
		-	400 *5	mW	T_A=125 °C, no Flash program/erase *6
		-	560 *5	mW	T_A=115 °C, no Flash program/erase *6
Operating ambient temperature	T_A	0	+70	°C	CY96V300C
		-40	+105		
		-40	+125		*6
Storage temperature	T_{STG}	-55	+150	°C	

*1: AVCC and VCC must be set to the same voltage. It is required that AVCC does not exceed VCC and that the voltage at the analog inputs does not exceed AVCC neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:

- Applicable to all general-purpose I/O pins (Pnn_m).
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = S (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)

I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.

I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified TA without air flow.

*6: Please contact Cypress for reliability limitations when using under these conditions.

WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7	15	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

DC Characteristics

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5$ V
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5$ V
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5$ V
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5$ V
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output H voltage	V_{OH2}	Normal outputs	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OH} = -2 mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2 mA (PODR:OD=1)
			3.0 V ≤ V_{CC} < 4.5 V I_{OH} = -1.6 mA					
	V_{OH5}	Normal outputs	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OH} = -5 mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5 mA (PODR:OD=0)
			3.0 V ≤ V_{CC} < 4.5 V I_{OH} = -3 mA					
	V_{OH3}	3 mA outputs	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OH} = -3 mA	V_{CC} - 0.5	-	-	V	I/O circuit type "N"
			3.0 V ≤ V_{CC} < 4.5 V I_{OH} = -2 mA					
Output L voltage	V_{OL2}	Normal outputs	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = +2 mA	-	-	0.4	V	Driving strength set to 2 mA
			3.0 V ≤ V_{CC} < 4.5 V I_{OL} = +1.6 mA					
	V_{OL5}	Normal outputs	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = +5 mA	-	-	0.4	V	Driving strength set to 5 mA
			3.0 V ≤ V_{CC} < 4.5 V I_{OL} = +3 mA					
	V_{OL3}	3 mA outputs	3.0 V ≤ V_{CC} ≤ 5.5 V I_{OL} = +3 mA	-	-	0.4	V	I/O circuit type "N"
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	µA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	V_{CC} = 3.3 V±10 %	40	100	160	kΩ	
			V_{CC} = 5.0 V±10 %	25	50	100	kΩ	

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes *1	I_{CCPLL}	PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped)	+25 °C	14.5	19.5	mA	CY96F353/F355
			+125 °C	16	23		
			+25 °C	15	20	mA	CY96F356
			+125 °C	16.5	23.5		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 32MHz, CLKP2 = 16MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25 °C	23	29	mA	CY96F353/F355
			+125 °C	25	33		
			+25 °C	24	30	mA	CY96F356
			+125 °C	26	34		
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz 0 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25 °C	26	38	mA	CY96F353/F355
			+125 °C	28	42		
			+25 °C	28	40	mA	CY96F356
			+125 °C	30	44		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25 °C	40	51	mA	CY96F353/F355
			+125 °C	42	55		
			+25 °C	41	52	mA	CY96F356
			+125 °C	43	56		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25 °C	43	56	mA	CY96F353/F355
			+125 °C	45	60		
			+25 °C	44	58	mA	CY96F356
			+125 °C	46	62		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4 MHz 1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+25 °C	4	5	mA	CY96F353/F355
			+125 °C	4.7	8		
			+25 °C	4.2	5.2	mA	CY96F356
			+125 °C	4.9	8.2		

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes *1	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2 MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25 °C	2.5	3.5	mA	CY96F353/F355
			+125 °C	3.2	6.5		
			+25 °C	2.7	3.7	mA	CY96F356
			+125 °C	3.4	6.7		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25 °C	0.18	0.3	mA	CY96F353/F355
			+125 °C	0.73	3.1		
			+25 °C	0.4	0.6	mA	CY96F356
			+125 °C	0.95	3.4		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/ erasing allowed)	+25 °C	0.15	0.25	mA	CY96F353/F355/356
			+125 °C	0.7	3.05		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32 kHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25 °C	0.1	0.2	mA	CY96F353/F355/356
			+125 °C	0.65	3		

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes *1	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1 = 16MHz, CLKP2 = 8MHz (CLKRC and CLKSC stopped)	+25 °C	4	6	mA	CY96F353/F355/F356
			+125 °C	4.7	9		
		PLL Sleep mode with CLKS1/2 = CLKP1= 32MHz, CLKP2 = 16MHz (CLKRC and CLKSC stopped)	+25 °C	7	9.5	mA	CY96F353/F355/F356
			+125 °C	8	12.5		
		PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped)	+25 °C	7	9	mA	CY96F353/F355/F356
			+125 °C	8	12		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25 °C	11	14.5	mA	CY96F353/F355/F356
			+125 °C	12	17.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25 °C	12	15	mA	CY96F353/F355/F356
			+125 °C	13	18		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4 MHz (CLKPLL, CLKSC and CLKRC stopped)	+25 °C	1	1.3	mA	CY96F353/F355
			+125 °C	1.6	4.1		
			+25 °C	1.3	1.8	mA	CY96F356
			+125 °C	1.9	4.6		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2 MHz (CLKMC, CLKPLL and CLKSC stopped)	+25 °C	0.55	1.1	mA	CY96F353/F355
			+125 °C	1.15	3.9		
			+25 °C	0.8	1.4	mA	CY96F356
			+125 °C	1.4	4.2		

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes *1	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100 kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25 °C	0.08	0.2	mA	CY96F353/F355
			+125 °C	0.59	2.95		
			+25 °C	0.3	0.5	mA	CY96F356
			+125 °C	0.8	3.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100 kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25 °C	0.05	0.15	mA	CY96F353/F355/F356
			+125 °C	0.56	2.9		
	I_{CCSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32 kHz (CLKMC, CLKPLL and CLKRC stopped)	+25 °C	0.04	0.12	mA	CY96F353/F355/F356
			+125 °C	0.53	2.9		
Power supply current in Timer modes *1	I_{CCTPLL}	PLL Timer mode with CLKMC = 4 MHz, CLKPLL = 48 MHz (CLKRC and CLKSC stopped.)	+25 °C	1.3	1.8	mA	CY96F353/F355
			+125 °C	1.9	4.8		
			+25 °C	1.5	2	mA	CY96F356
			+125 °C	2.1	5		

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes *	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25 °C	0.11	0.2	mA	CY96F353/F355
			+125 °C	0.63	3		
			+25 °C	0.35	0.5	mA	CY96F356
			+125 °C	0.85	3.3		
		Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25 °C	0.08	0.15	mA	CY96F353/F355/F356
			+125 °C	0.6	2.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25 °C	0.1	0.2	mA	CY96F353/F355
			+125 °C	0.63	3		
			+25 °C	0.35	0.5	mA	CY96F356
			+125 °C	0.85	3.3		
		RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25 °C	0.07	0.15	mA	CY96F353/F355/F356
			+125 °C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25 °C	0.06	0.15	mA	CY96F353/F355
			+125 °C	0.56	2.95		
			+25 °C	0.3	0.45	mA	CY96F356
			+125 °C	0.8	3.2		
		RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25 °C	0.03	0.1	mA	CY96F353/F355/F356
			+125 °C	0.53	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32 kHz (CLKMC, CLKPLL and CLKRC stopped)	+25 °C	0.035	0.1	mA	CY96F353/F355/F356
			+125 °C	0.53	2.85		

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8 V)	+25 °C	0.02	0.08	mA	CY96F353/F355/F356
			+125 °C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2 V)	+25 °C	0.015	0.06	mA	CY96F353/F355/F356
			+125 °C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25 °C	5	10	µA	CY96F353/F355
			+125 °C	7	20		Must be added to all current above
			+25 °C	90	140	µA	CY96F356
			+125 °C	100	150		Must be added to all current above
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

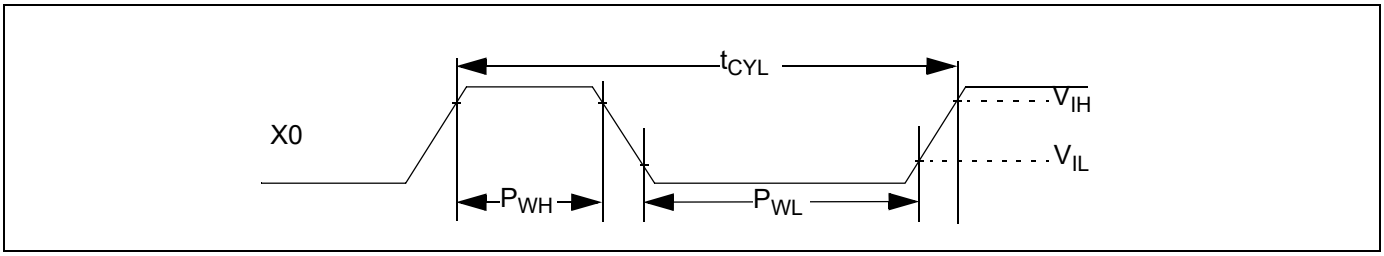
*: The power supply current is measured with a 4 MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

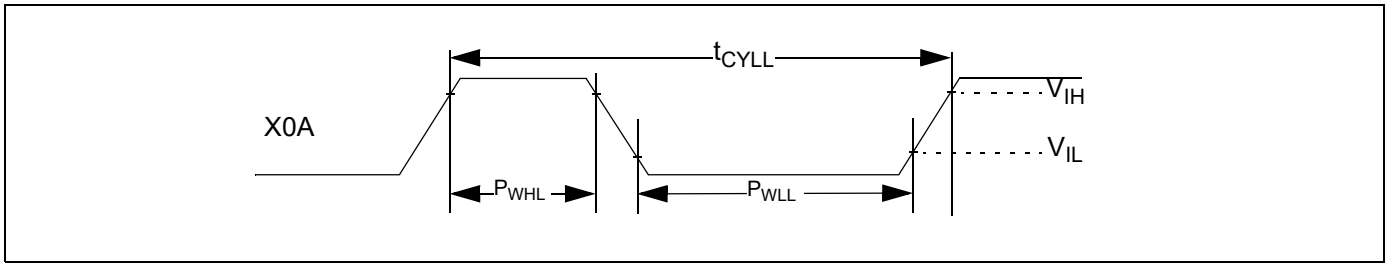
AC Characteristics

Source Clock Timing

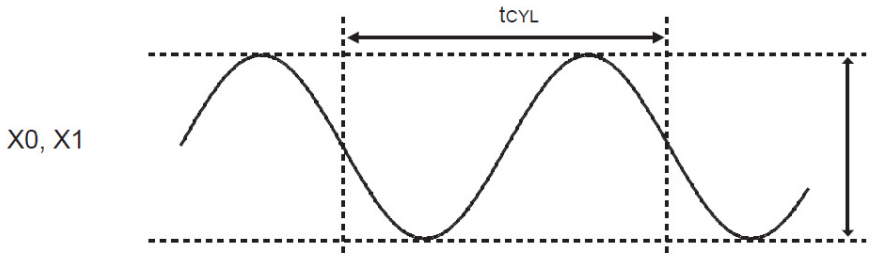
(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	64 or 256 RC clock cycles				Applied after any reset and when activating the RC oscillator. CY96F356: 64 cycles others: 256 cycles
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	±5	ns	For CLKMC (PLL input clock) ≥ 4 MHz, jitter coming from external oscillator, crystal or resonator is not covered.
Input clock pulse width	P_{WH}, P_{WL}	X0, X1	8	-	-	ns	Duty ratio is about 30 % to 70 %
Input clock pulse width	P_{WHL}, P_{WLL}	X0A, X1A	5	-	-	µs	



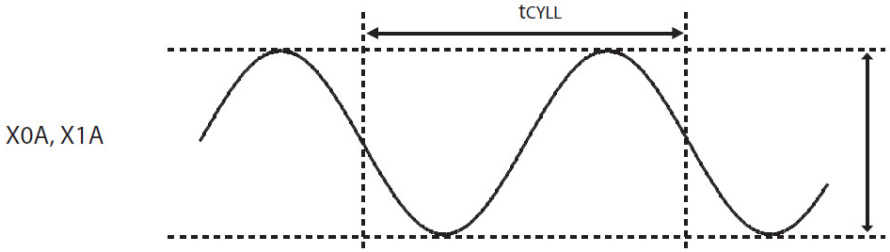


When using an oscillation circuit



Amplitude:
It varies depending on the external resistance, power rating and the different kind of device.
Reference values: 1 V to 2.5 V

When using an oscillation circuit



Amplitude:
It varies depending on the external resistance, power rating and the different kind of device.
Reference values: 1 V to 2.5 V

Internal Clock Timing

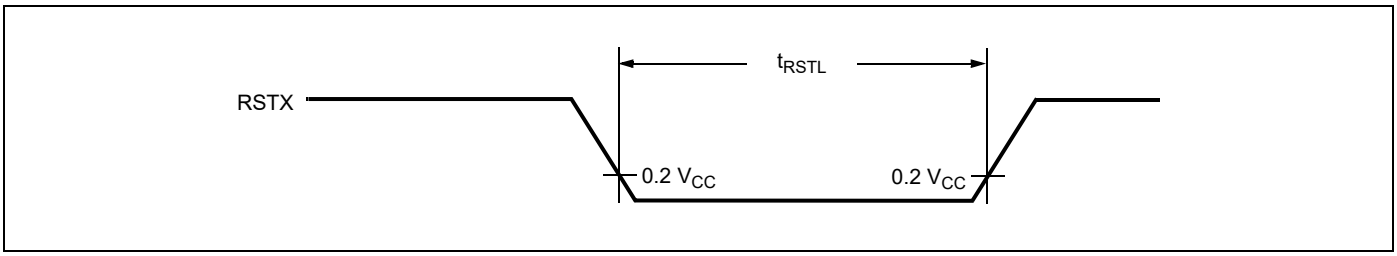
(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8 V		1.9 V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	88	0	96	MHz	CY96F356
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

External Reset Timing

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

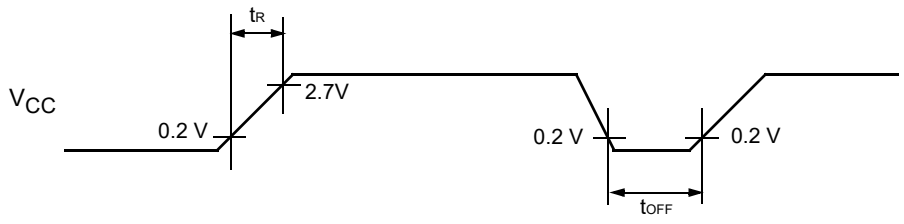
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset Timing

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



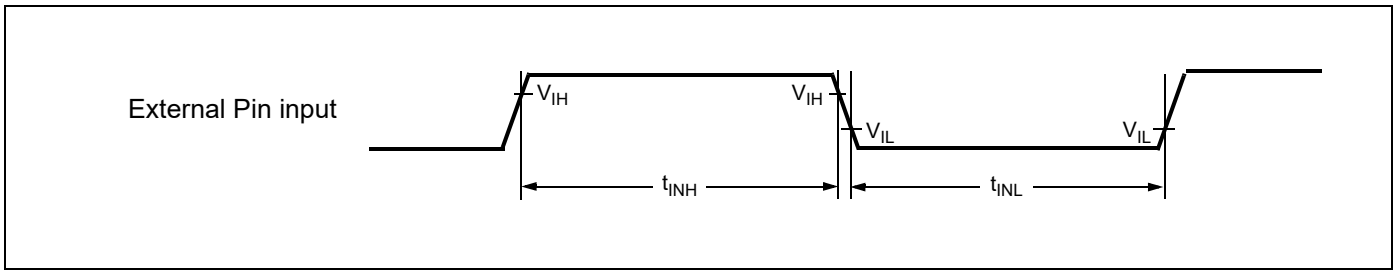
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

External Input Timing

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin Input Function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	-	200	-	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 (t_{CLKP1}=1/f_{CLKP1})	-	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



External Bus Timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5 mA. If IO_{drive} is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

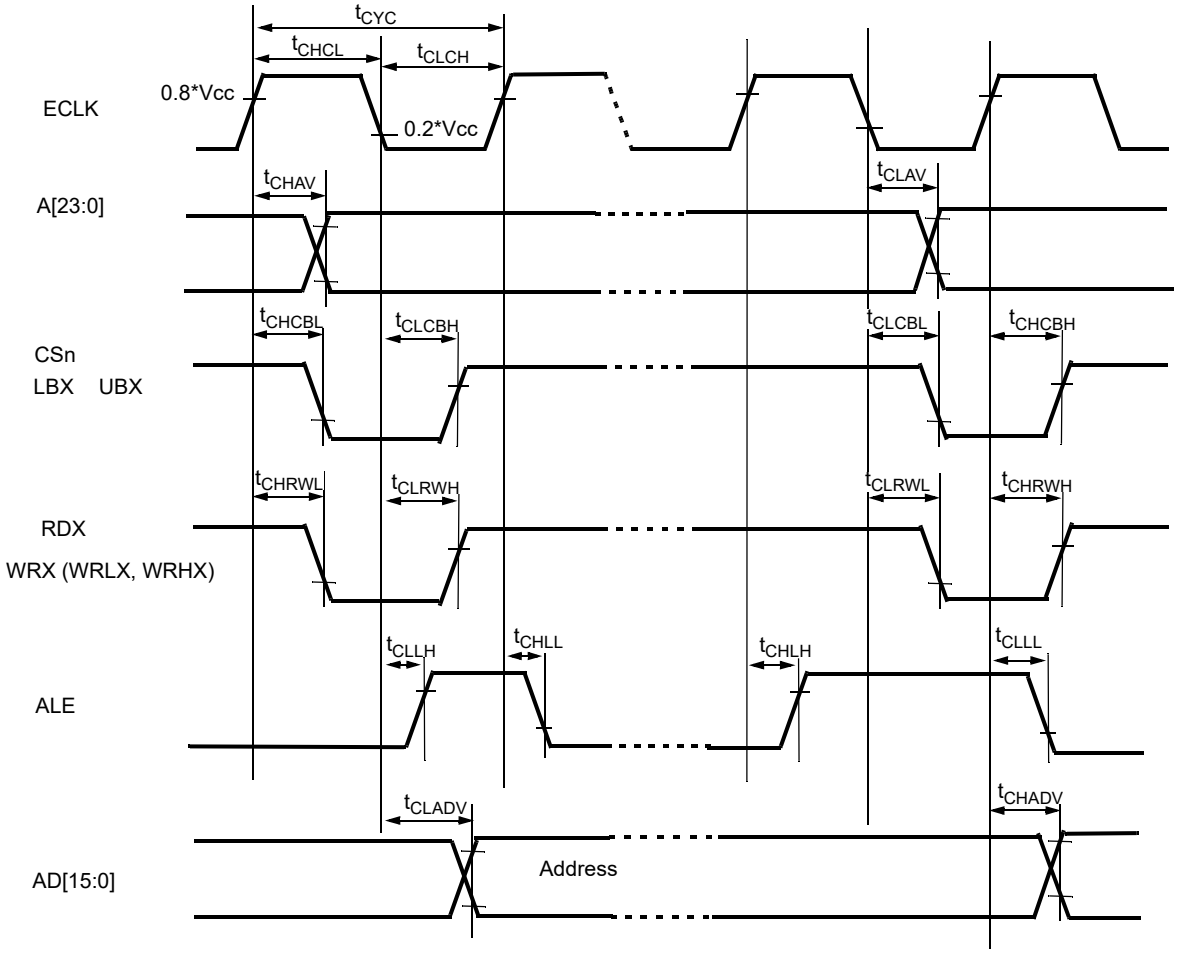
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	25	-	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-20	+20	ns	
	t_{CHCBL}			-20	+20		
	t_{CLCBH}			-20	+20		
	t_{CLCBL}			-20	+20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-10	+10	ns	
	t_{CHLL}			-10	+10		
	t_{CLLH}			-10	+10		
	t_{CLLL}			-10	+10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK		-15	+15	ns	
	t_{CLAV}			-15	+15		
	t_{CLADV}	AD[15:0], ECLK		-15	+15	ns	
	t_{CHADV}			-15	+15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	-	-10	+10	ns	
	t_{CHRWL}			-10	+10		
	t_{CLRWH}			-10	+10		
	t_{CLRWL}			-10	+10		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	+25	ns	
	t_{CHCBL}			-25	+25		
	t_{CLCBH}			-25	+25		
	t_{CLCBL}			-25	+25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	+15	ns	
	t_{CHLL}			-15	+15		
	t_{CLLH}			-15	+15		
	t_{CLLL}			-15	+15		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK		-20	+20	ns	
	t_{CLAV}			-20	+20		
	t_{CLADV}	AD[15:0], ECLK		-20	+20	ns	
	t_{CHADV}			-20	+20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	-	-15	+15	ns	
	t_{CHRWL}			-15	+15		
	t_{CLRWH}			-15	+15		
	t_{CLRWL}			-15	+15		



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Read)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2-5$	-	ns	
			EACL:STS=1	$t_{CYC}-5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2-5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC}-15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2-15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC}-15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2-15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2-15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	t_{CYC} −15	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2-15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC}-15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2-15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2-15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2-15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC}-15$	-	ns	
			EACL:ACE=1	$2t_{CYC}$ −15	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC}-55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC}-55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2-55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2-55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2-5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2-50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2-10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2-10$	-		

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

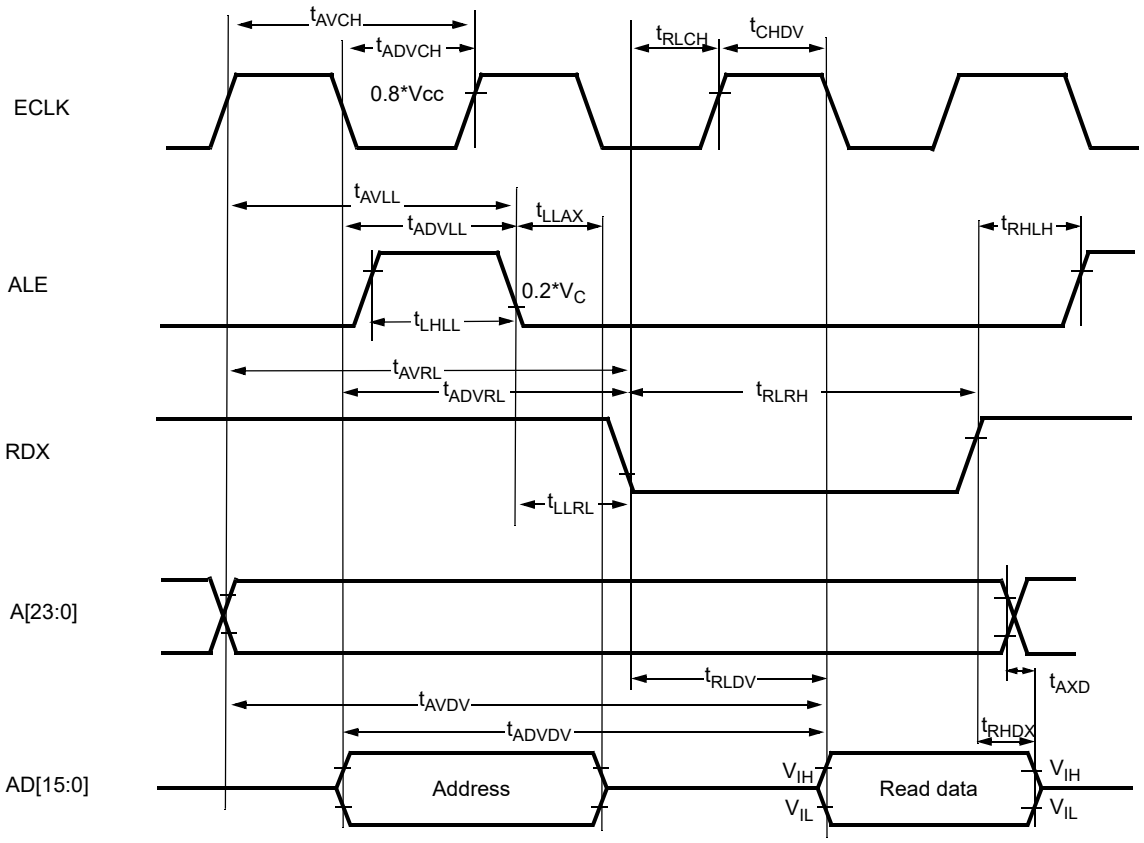
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	t_{CYC}–15	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		t_{CYC}/2–15	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	t_{CYC}/2–10	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	t_{CYC}/2–10	-	ns	
			EACL:STS=1	–10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	t_{CYC} – 50	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t_{CYC}/2–8	-	ns	EBM:NMS = 0
			EACL:STS=1	t_{CYC}–8	-		
			EACL:STS=0 and EACL:ACE=1	3t_{CYC}/2–8	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t_{CYC}–20	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t_{CYC}/2–20	-		
			EACL:STS=0 and EACL:ACE=1	2t_{CYC}–20	-		
			EACL:STS=1 and EACL:ACE=1	5t_{CYC}/2–20	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t_{CYC}/2–20	-	ns	
			EACL:STS=1 and EACL:ACE=0	t_{CYC}–20	-		
			EACL:STS=0 and EACL:ACE=1	3t_{CYC}/2–20	-		
			EACL:STS=1 and EACL:ACE=1	2t_{CYC}–20	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	t_{CYC}/2–20	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t_{CYC}/2-20	-	ns	
			EACL:ACE=1	5t_{CYC}/2-20	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t_{CYC}-20	-	ns	
			EACL:ACE=1	2t_{CYC}-20	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	3t_{CYC}-60	ns	w/o cycle extension
			EACL:ACE=1	-	4t_{CYC}-60		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	5t_{CYC}/2-60	ns	w/o cycle extension
			EACL:ACE=1	-	7t_{CYC}/2-60		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX pulse width	t_{RLRH}	RDX	-	$3t_{CYC}$/2-8	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3t_{CYC}$/2-55	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	-	0	-	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}$/2-15	-	ns	
			other ECL:STS, EACL:ACE setting	t_{CYC}/2-15	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	-	t_{CYC}-20	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		t_{CYC}/2-20	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	t_{CYC}/2-15	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	t_{CYC}/2-15	-	ns	
			EACL:STS=1	-15	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	t_{CYC}-55	ns	



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

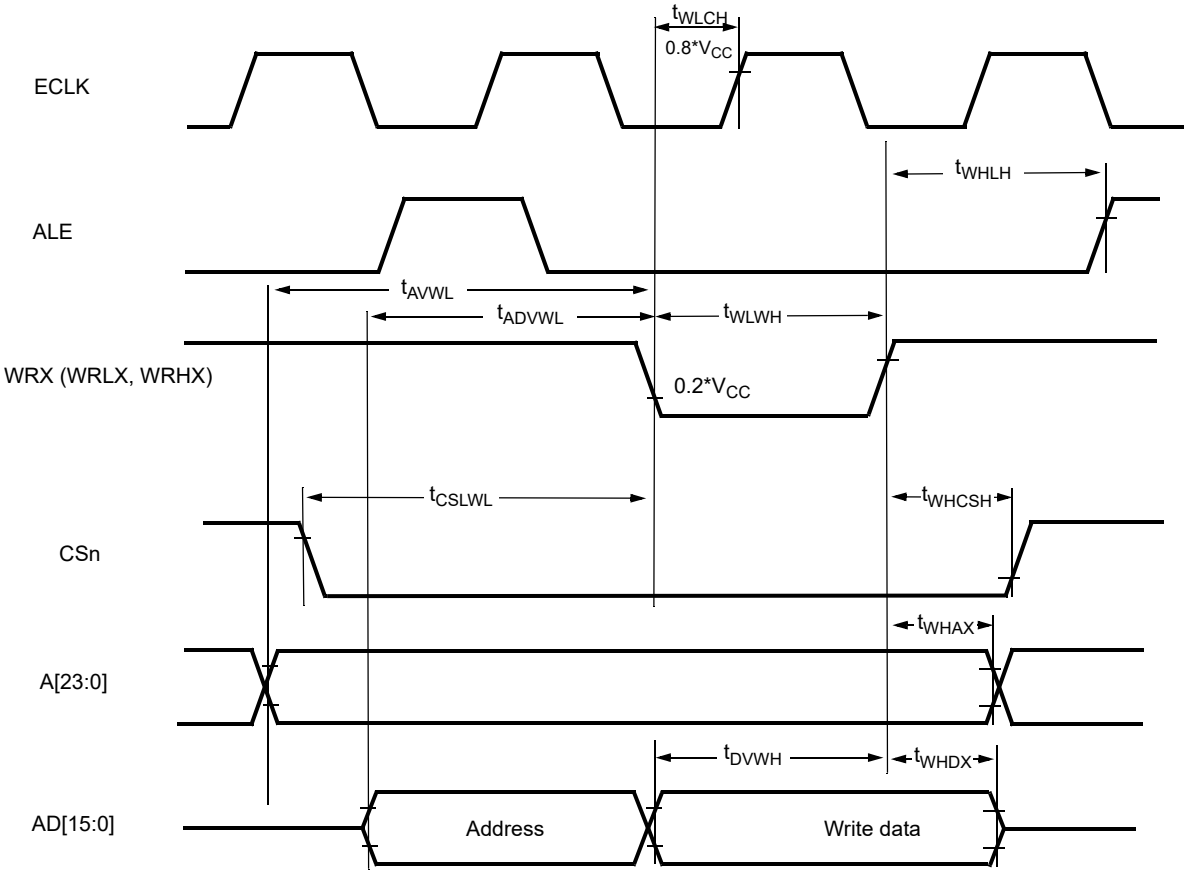
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$-15	-	ns	
			EACL:ACE=1	$5t_{CYC}/2$-15	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC}-15	-	ns	
			EACL:ACE=1	$2t_{CYC}$-15	-		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	t_{CYC}-5	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC}-20	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2$-15	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2$-15	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$-10	-	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC}-10	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2$-10	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	-	$3t_{CYC}/2$-15	ns	
			EACL:ACE=1 EBM:NMS=0	-	$5t_{CYC}/2$-15		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2$-15	-	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$-20	-	ns	
			EACL:ACE=1	$5t_{CYC}/2$-20	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC}-20	-	ns	
			EACL:ACE=1	$2t_{CYC}$-20	-		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	t_{CYC}-8	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC}-25	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC}/2-20	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	t_{CYC}/2-20	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$-15	-	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC}-15	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	t_{CYC}/2-15	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}$/2-20	ns	
			EACL:ACE=1	-	$5t_{CYC}$/2-20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	t_{CYC}/2-20	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

Ready Input Timing

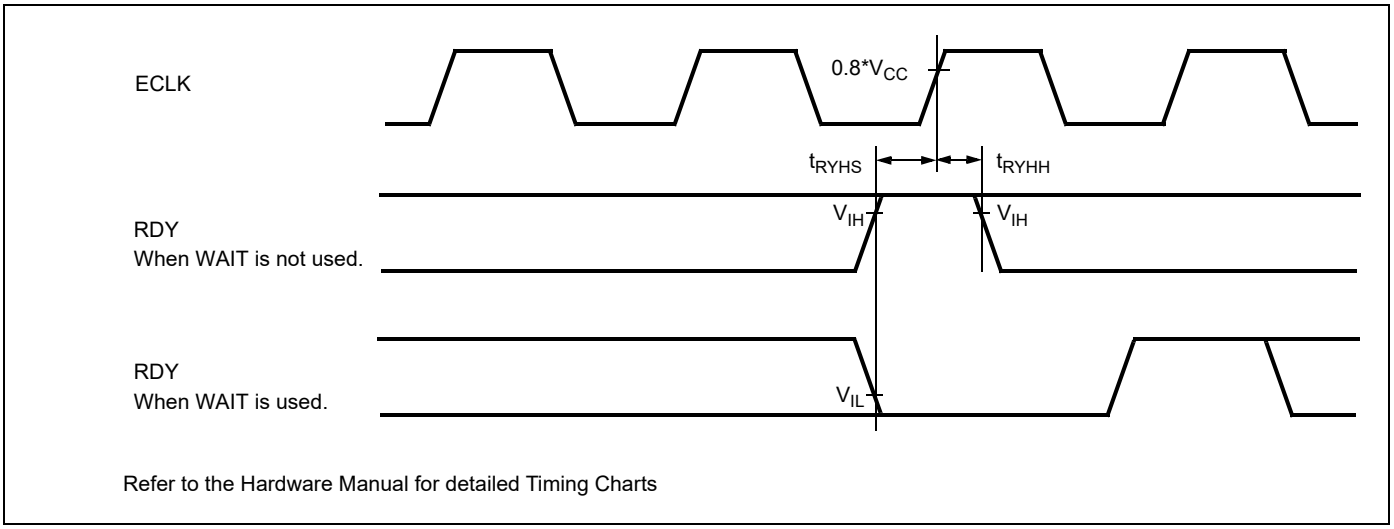
(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	35	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	45	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



Refer to the Hardware Manual for detailed Timing Charts

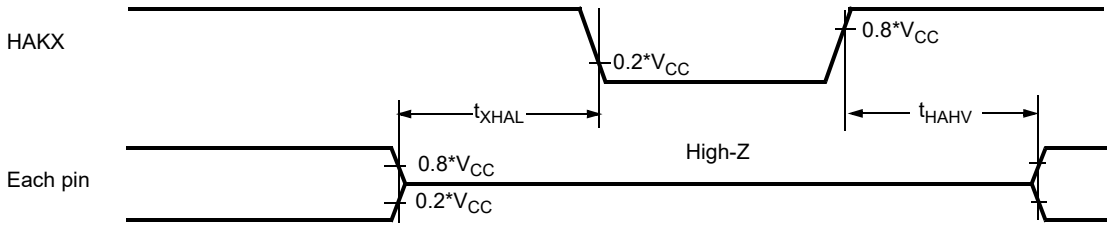
Hold Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC}-20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC}-20	t_{CYC} + 20	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5 V, V_{SS} = 0.0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC}-25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC}-25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

USART Timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5 mA. If IO_{drive} is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

(T_A = -40 °C to 125 °C, V_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, IO_{drive} = 5 mA, C_L = 50 pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5 V to 5.5 V		V_{CC} = AV_{CC}= 3.0 V to 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 *1	-	N*t_{CLKP1} - 30 *1	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

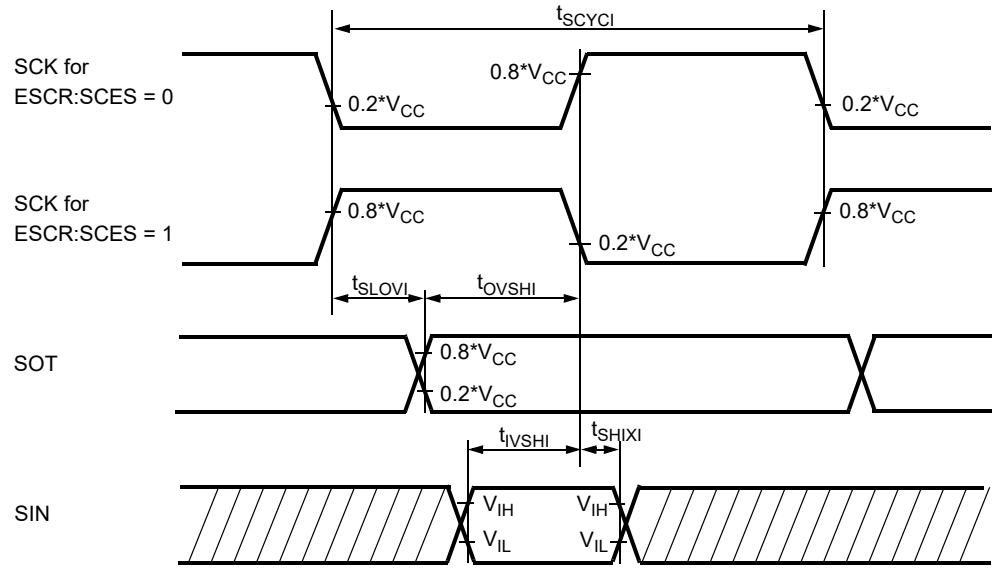
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “CY96300 Super series Hardware Manual”
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on tSCYCI and can be calculated as follows:

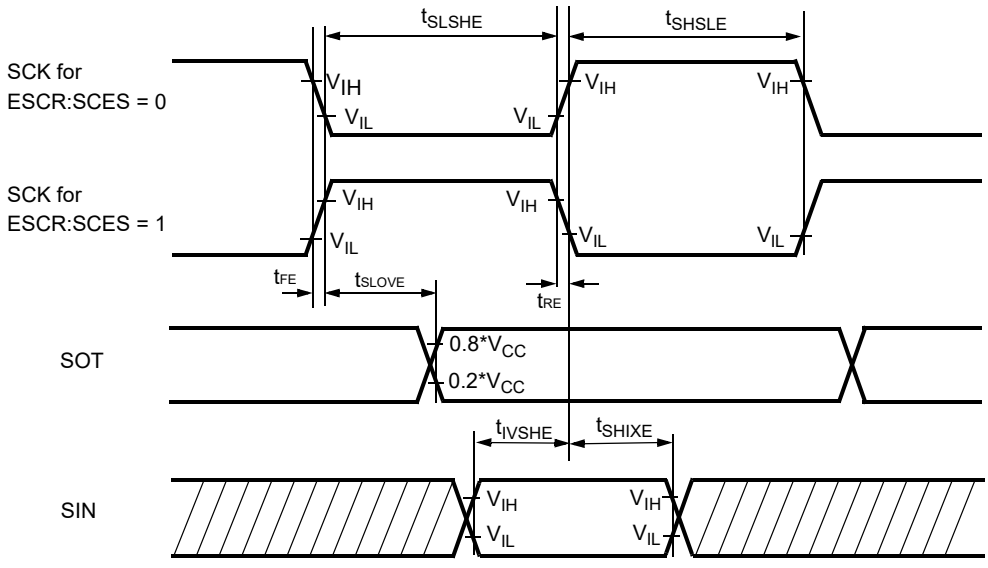
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...



Internal Shift Clock Mode



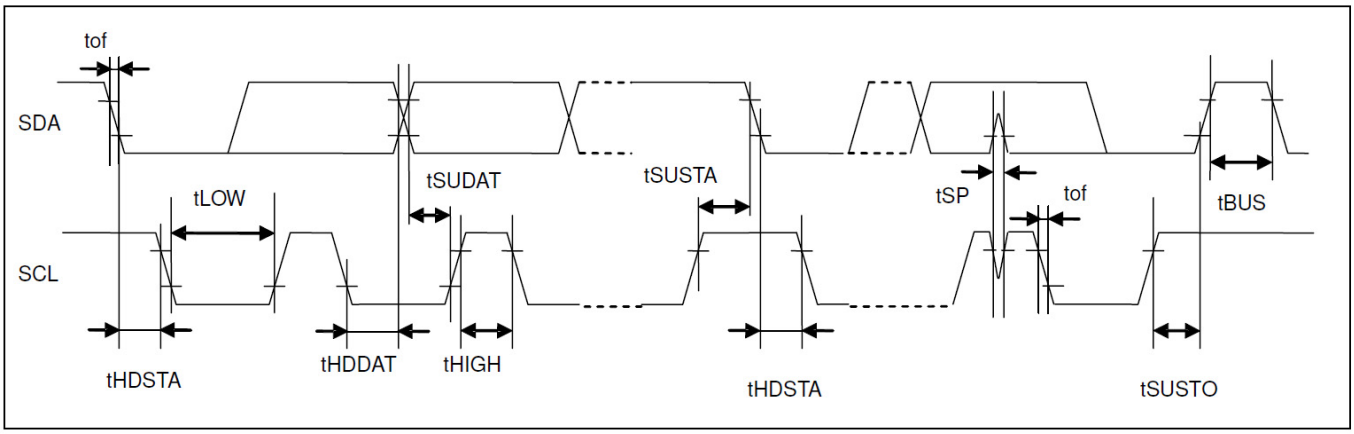
External Shift Clock Mode

I^2C Timing

(T_A = -40 °C to 125 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Standard-mode		Fast-mode *1		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}	4.0	-	0.6	-	µs
"L" width of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
"H" width of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}	4.7	-	0.6	-	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}	0	3.45	0	0.9	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}	250	-	100	-	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}	4.7	-	1.3	-	µs
Output fall time from 0.7*Vcc to 0.3*Vcc with a bus capacitance from 10 pF to 400 pF	t_{of}	20 + 0.1*C_b *2	300	20 + 0.1*C_b *2	300	ns
Capacitive load for each bus line	C_b	-	400	-	400	pF
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	N/A	N/A	0	1*t_{CLKP1} *3	ns

*1: For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.
*2: C_b = capacitance of one bus line in pF.
*3: t_{CLKP1} is the cycle time of the peripheral clock CLKP1.



- V_{OH} = 0.7 * VCC
- VOL = 0.3 * VCC
- CMOS Hysteresis 0.7/0.3 input selected

Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	±3	LSB	
Nonlinearity error	-	-	-	-	±2.5	LSB	
Differential nonlinearity error	-	-	-	-	±1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL- 1.5 LSB	AVRL+ 0.5 LSB	AVRL+ 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH- 3.5 LSB	AVRH- 1.5 LSB	AVRH+ 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			2.0	-	-	µs	3.0 V ≤ AV_{CC} < 4.5 V
Sampling time	-	-	0.5	-	-	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
			1.2	-	-	µs	3.0 V ≤ AV_{CC} < 4.5 V
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A ≤ 105 °C, AVSS, AVRL < VI < AVCC, AVRH
			-1.2	-	+1.2	µA	105 °C < T_A ≤ 125 °C, AVSS, AVRL < VI < AVCC, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

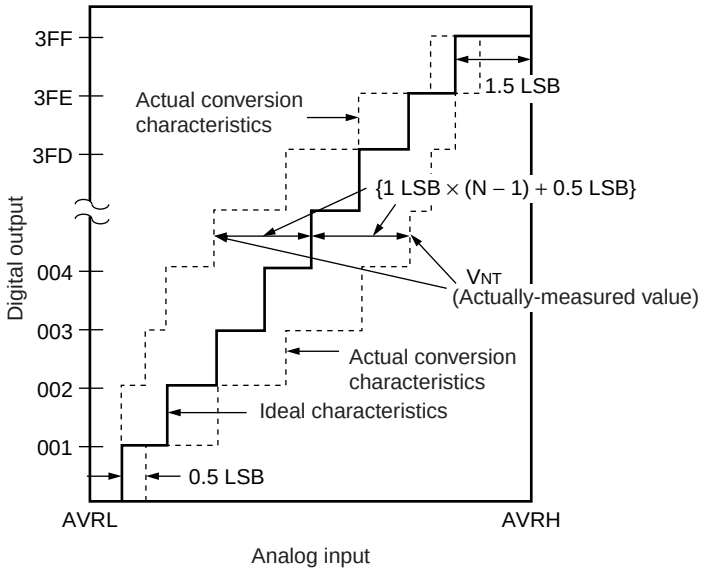
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

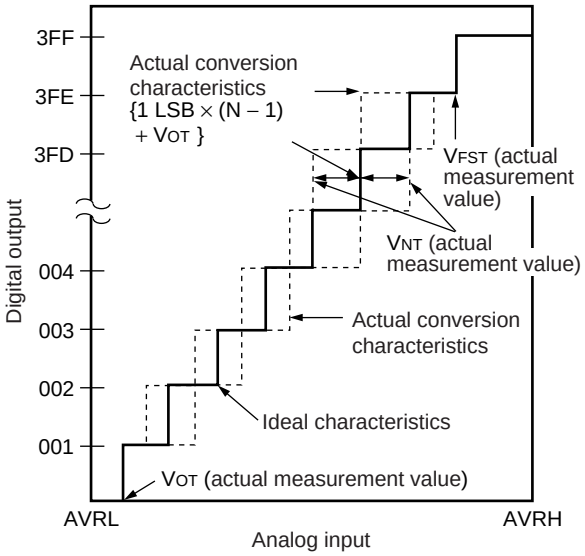
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

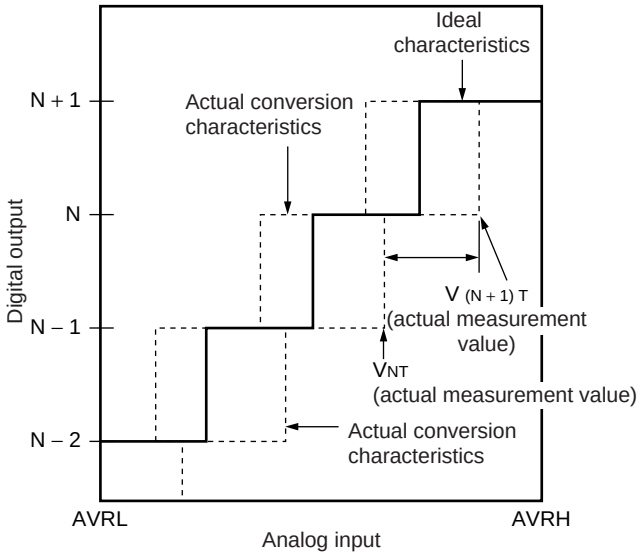
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N: A/D converter digital output value

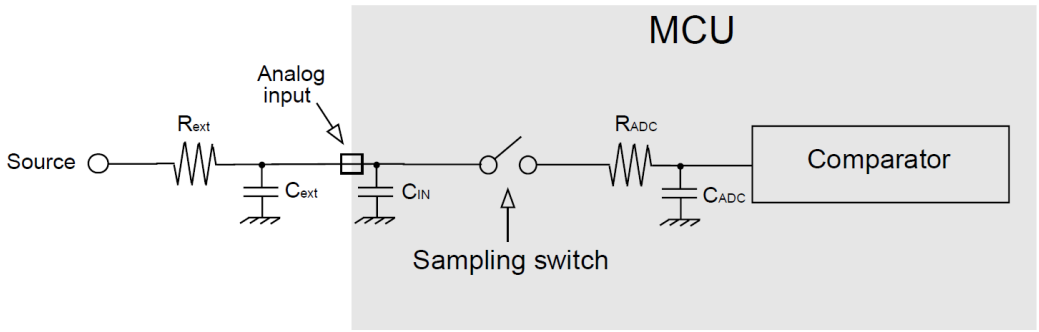
V_{OT}: Voltage at which digital output transits from "000_H" to "001_H."

V_{FST}: Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance Rext, the board capacitance of the A/D converter input pin Cext and the AVcc voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance
C_{ext}: capacitance of PCB at A/D converter input
C_{IN}: capacitance of MCU input pin: 15pF (max)
R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \leq AV_{CC} \leq 5.5V$
12kΩ (max) for $3.0V \leq AV_{CC} < 4.5V$
C_{ADC}: sampling capacitance within MCU: 10pF (max)

The sampling time should be set to minimum “7τ“. The following approximation formula for the replacement model above can be used:

T_{samp} [min] = 7 × (R_{ext} × (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) × C_{ADC})

- Do not select a sampling time below the absolute minimum permitted value
  (0.5µs for 4.5V ≤ AVcc ≤ 5.5V; 1.2 µs for 3.0V ≤ AVcc < 4.5V).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Low Voltage Detector Characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0 V - 5.5 V, V_{ss} = AV_{ss} = 0 V)

Parameter	Symbol	Value *1		Value *2		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.5	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.9	3.1	2.8	3.2	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3.1	3.3	3	3.4	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.5	3.75	3.35	3.8	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.6	3.85	3.5	3.95	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.7	3.95	3.6	4.1	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.8	4.05	3.7	4.2	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.9	4.15	3.8	4.3	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	4.0	4.25	3.9	4.4	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	4.1	4.35	3.95	4.5	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used		not used		-	
Level 11	V_{DL11}	not used		not used		-	
Level 12	V_{DL12}	not used		2.6	3	V	CILCR:LVL[3:0]=”1100”
Level 13	V_{DL13}	not used		not used		-	
Level 14	V_{DL14}	not used		not used		-	
Level 15	V_{DL15}	not used		not used		-	

*1: Valid for all devices except devices listed under “*2”

*2: Valid for: CY96F353/F355

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004 \frac{V}{\mu s}$.

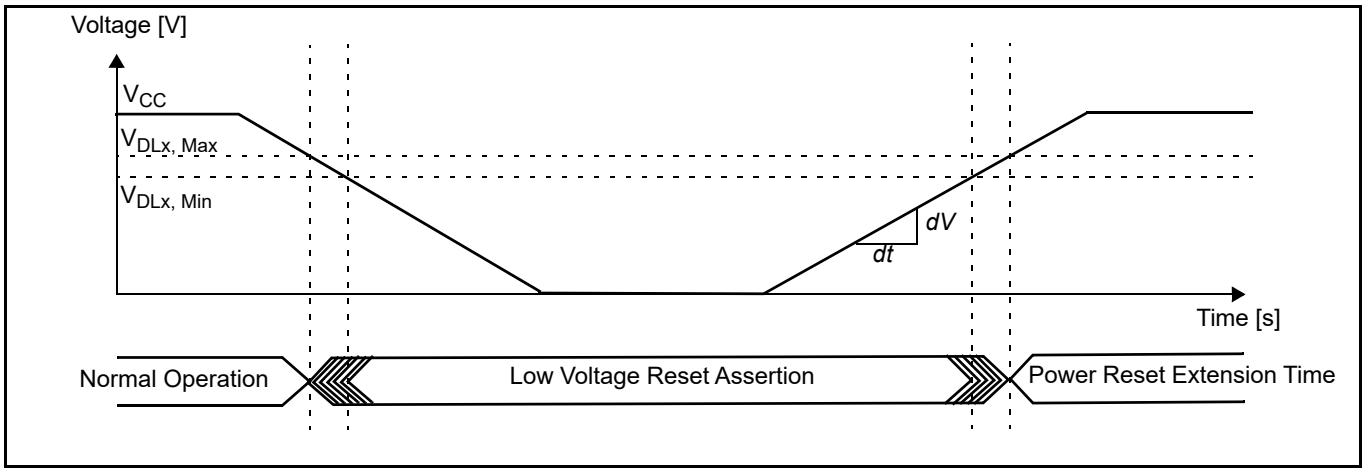
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7 V. The electrical characteristics however are only valid in the specified range (usually down to 3.0 V).

Please use the inclination of the power-supply voltage with 0.1V/µs or less.

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



Flash Memory Program/Erase Characteristics

(T_A = -40 °C to 105 °C, V_{CC} = AV_{CC} = 3.0 V to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85 °C)

Example Characteristics

Temperature dependency of power supply currents

The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:

- VCC = AVCC = 5.0 V
- Main clock = 4 MHz external clock
- Sub clock = 32 kHz external clock

Operation Mode Details

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1}$ = 56MHz ■ f_{CLKP2} = 28MHz ■ Regulator in High Power Mode ■ Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) ■ 2 Flash/ROM wait states (MTCRA=$233A_H$) ■ RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 96MHz ■ $f_{CLKB} = f_{CLKP1}$ = 48MHz ■ f_{CLKP2} = 24MHz ■ Regulator in High Power Mode ■ Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) ■ 1 Flash/ROM wait states (MTCRA=$6B09_H$) ■ RC oscillator and Sub oscillator stopped
PLL Run 24	PLL Run mode current I_{CCPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 48MHz ■ $f_{CLKB} = f_{CLKP1}$ = fCLKP2 = 24MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ 0 Flash/ROM wait states (MTCRA=2208_H) ■ RC oscillator and Sub oscillator stopped
Main Run	Main Run mode current I_{CCMAIN} with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 4MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ 1 Flash/ROM wait states (MTCRA=0239_H) ■ PLL, RC oscillator and Sub oscillator stopped

Operation Mode Details

Mode name	Details
RC Run 2M	RC Run mode current I_{CCRCH} with the following settings: ■ RC oscillator set to 2MHz (CKFCR:RCFS = 1) ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 2MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ 1 Flash/ROM wait states (MTCRA=0239_H) ■ PLL, Main oscillator and Sub oscillator stopped
RC Run 100k	RC Run mode current I_{CCRCL} with the following settings: ■ RC oscillator set to 100kHz (CKFCR:RCFS = 0) ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 100kHz ■ Regulator in Low Power Mode A (SMCR:LPMS = 1) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ 1 Flash/ROM wait states (MTCRA=0239_H) ■ PLL, Main oscillator and Sub oscillator stopped
Sub Run	Sub Run mode current I_{CCSUB} with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 32kHz ■ Regulator in Low Power Mode A (by hardware) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ 1 Flash/ROM wait states (MTCRA=0239_H) ■ PLL, RC oscillator and Main oscillator stopped
PLL Sleep 56	PLL Sleep mode current I_{CCSPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKP1}$ = 56MHz ■ f_{CLKP2} = 28MHz ■ Regulator in High Power Mode ■ Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) ■ RC oscillator and Sub oscillator stopped
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 96MHz ■ f_{CLKP1} = 48MHz ■ f_{CLKP2} = 24MHz ■ Regulator in High Power Mode ■ Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) ■ RC oscillator and Sub oscillator stopped

Operation Mode Details

Mode name	Details
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 48MHz ■ $f_{CLKP1} = f_{CLKP2}$ = 24MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 4MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ PLL, RC oscillator and Sub oscillator stopped
RC Sleep 2M	RC Sleep mode current I_{CCSRCH} with the following settings: ■ RC oscillator set to 2MHz (CKFCR:RCFS = 1) ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 2MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ PLL, Main oscillator and Sub oscillator stopped
RC Sleep 100k	RC Sleep mode current I_{CCSRCL} with the following settings: ■ RC oscillator set to 100kHz (CKFCR:RCFS = 0) ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 100kHz ■ Regulator in Low Power Mode A (SMCR:LPMSS = 1) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, Main oscillator and Sub oscillator stopped
Sub Sleep	Sub Sleep mode current I_{CCSSUB} with the following settings: ■ $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 32kHz ■ Regulator in Low Power Mode A (by hardware) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, RC oscillator and Main oscillator stopped
PLL Timer 48	PLL Timer mode current I_{CCTPLL} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 48MHz ■ Regulator in High Power Mode ■ Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) ■ RC oscillator and Sub oscillator stopped

Operation Mode Details

Mode name	Details
Main Timer	Main Timer mode current $I_{CCTMAIN}$ with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 4MHz ■ Regulator in Low Power Mode A (SMCR:LPMSS = 1) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, RC oscillator and Sub oscillator stopped
RC Timer 2M	RC Timer mode current I_{CCTRCH} with the following settings: ■ RC oscillator set to 2MHz (CKFCR:RCFS = 1) ■ $f_{CLKS1} = f_{CLKS2}$ = 2MHz ■ Regulator in Low Power Mode A (SMCR:LPMSS = 1) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, Main oscillator and Sub oscillator stopped
RC Timer 100k	RC Timer mode current I_{CCTRCL} with the following settings: ■ RC oscillator set to 100kHz (CKFCR:RCFS = 0) ■ $f_{CLKS1} = f_{CLKS2}$ = 100kHz ■ Regulator in Low Power Mode A (SMCR:LPMSS = 1) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, Main oscillator and Sub oscillator stopped
Sub Timer	Sub Timer mode current I_{CCTSUB} with the following settings: ■ $f_{CLKS1} = f_{CLKS2}$ = 32kHz ■ Regulator in Low Power Mode A (by hardware) ■ Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) ■ PLL, RC oscillator and Main oscillator stopped
Stop 1.8V	Stop mode current I_{CCH} with the following settings: ■ Regulator in Low Power Mode B (by hardware) ■ Core voltage at 1.8V (VRCR:LPMB[2:0] = 110_B)
Stop 1.2V	Stop mode current I_{CCH} with the following settings: ■ Regulator in Low Power Mode B (by hardware) ■ Core voltage at 1.2V (VRCR:LPMB[2:0] = 000_B)

Figure 3. CY96F353/F355 PLL Run and Sleep Mode Currents

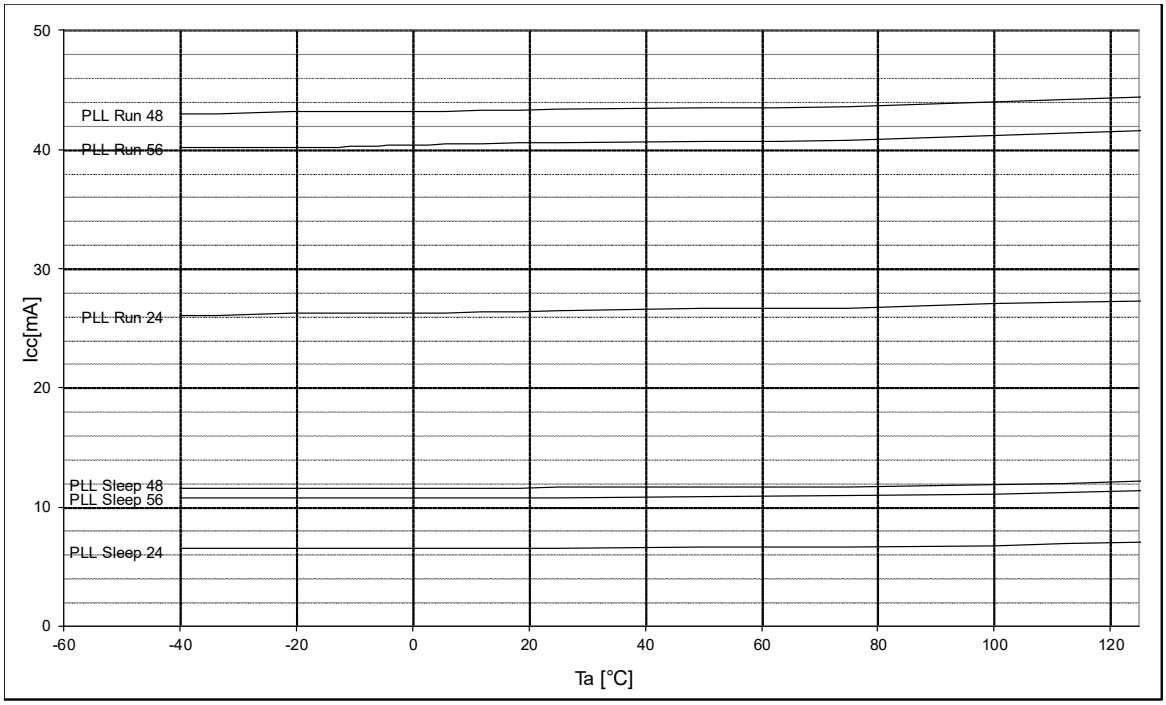


Figure 4. CY96F353/F355 Operation Modes with Medium Currents

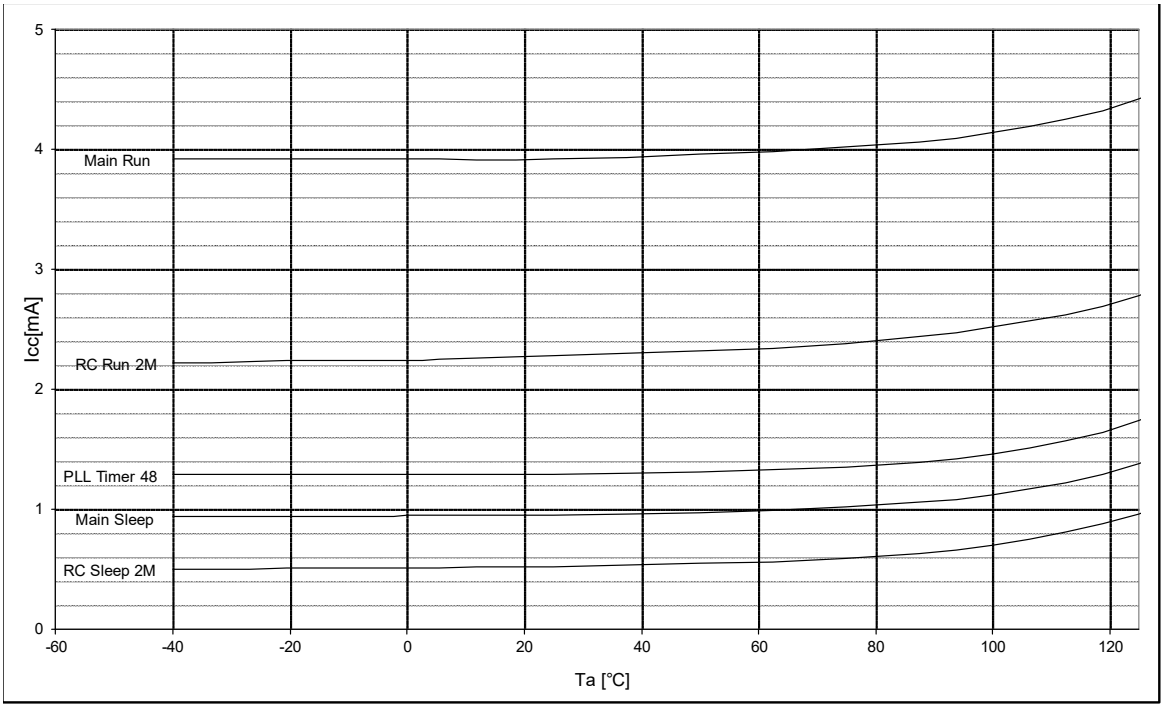


Figure 5. CY96F353/F355 Low Power Mode Currents

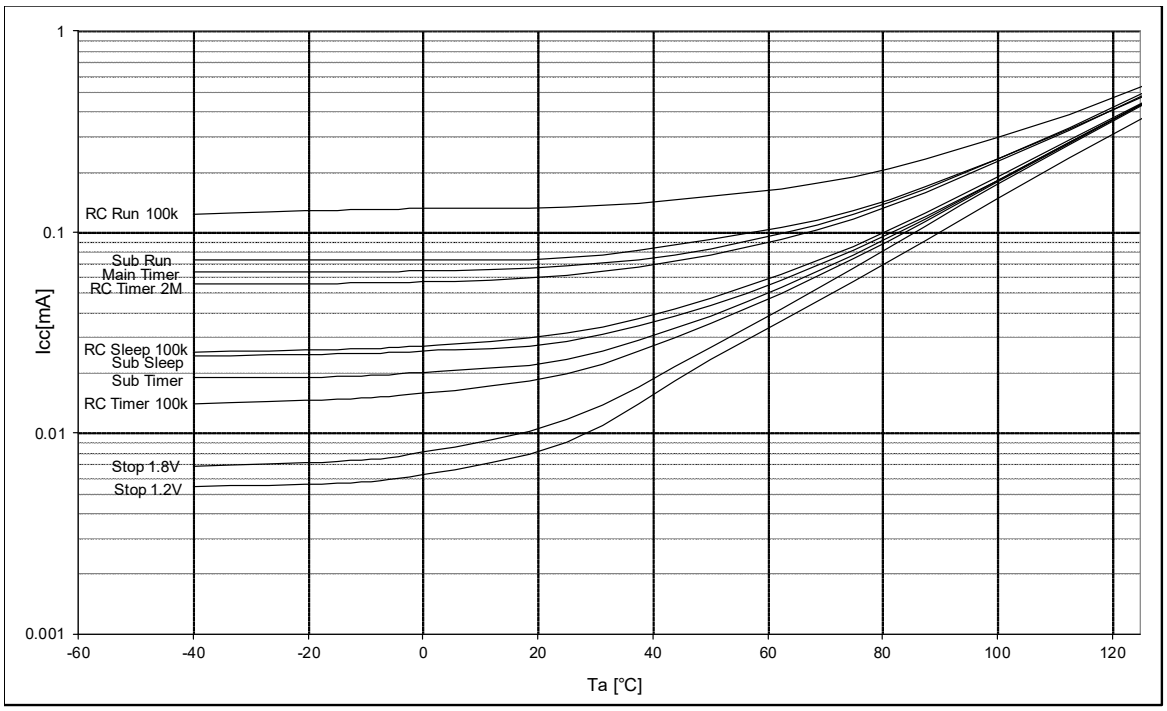


Figure 6. CY96F356 PLL Run and Sleep Mode Currents

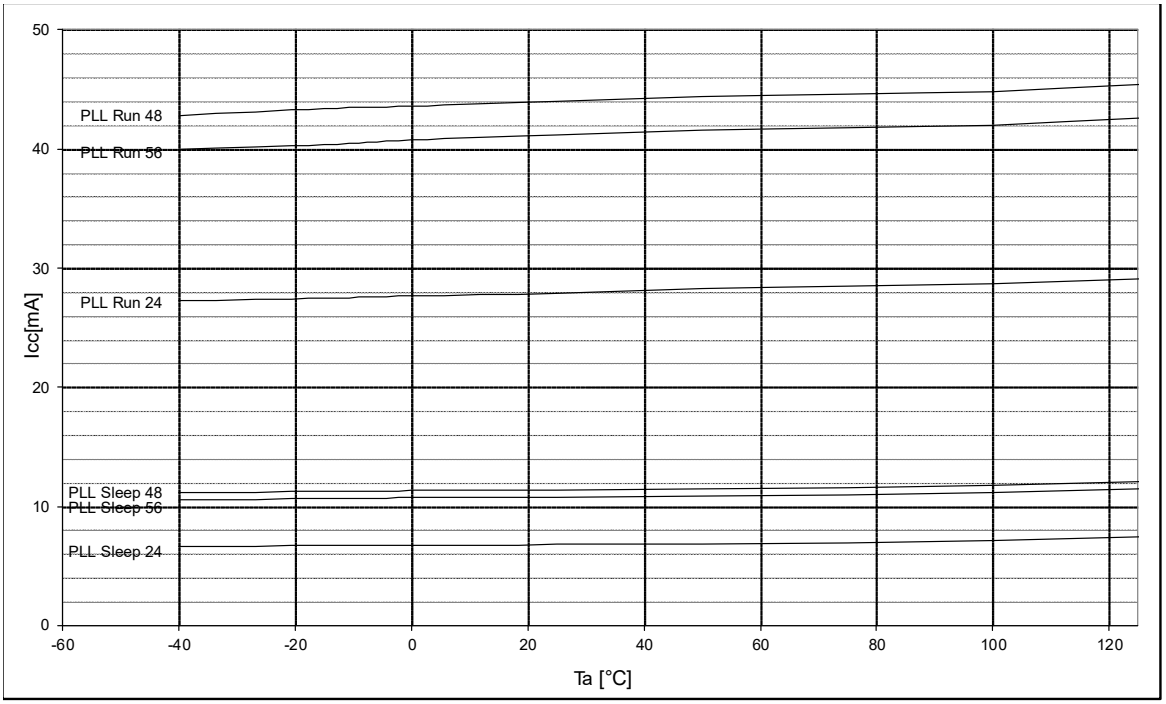


Figure 7. CY96F356 Operation Modes with Medium Currents

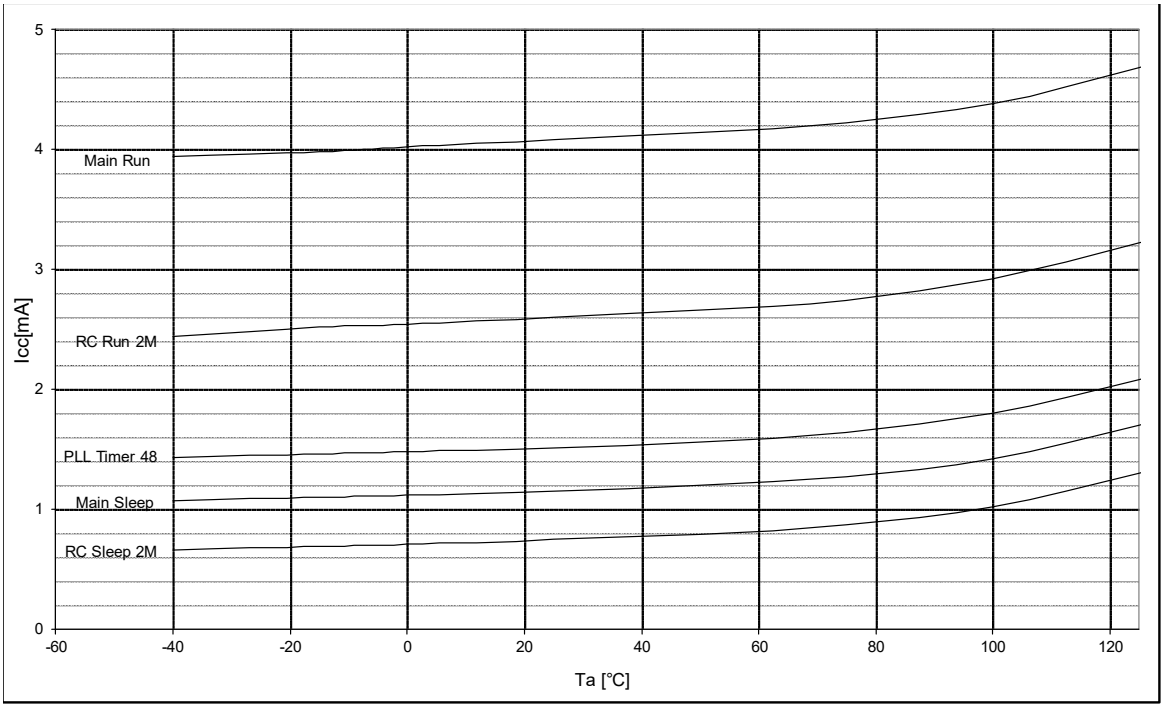
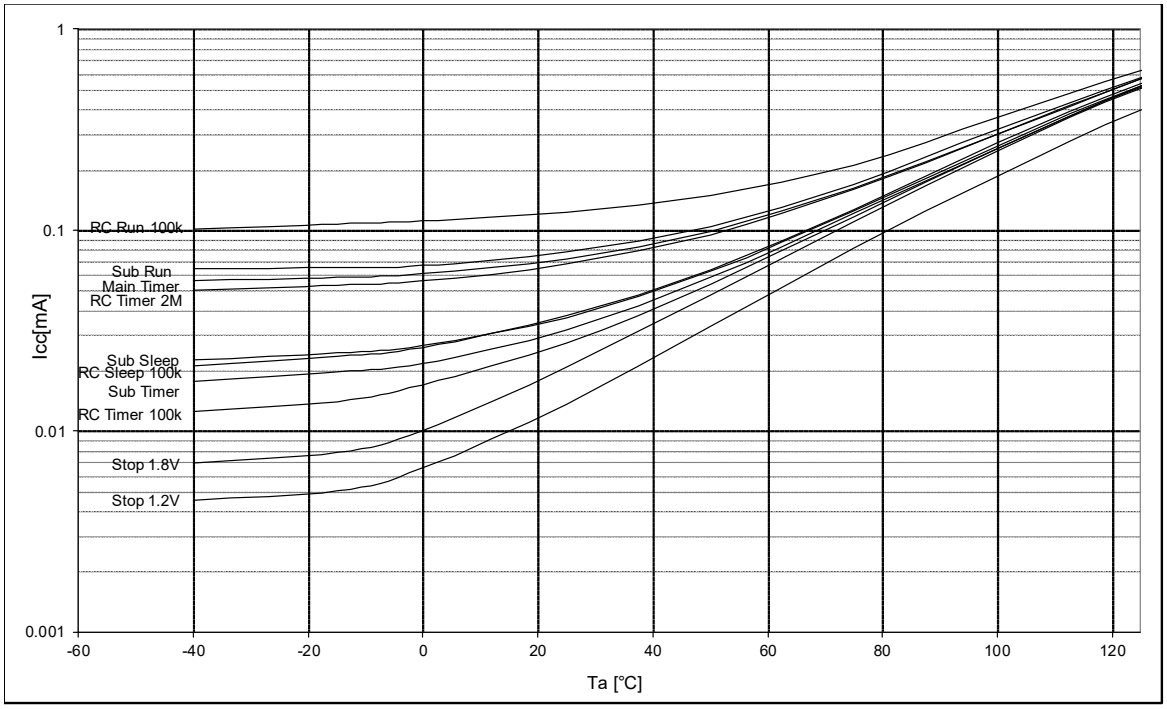


Figure 8. CY96F356 Low Power Mode Currents



Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.
Measurement conditions:

- VCC = AVCC = 5.0V
- Ta = 25°C
- $f_{CLKS1} = f_{CLKB}$ or $f_{CLKS1} = 2*f_{CLKB}$ as described in diagram
- $f_{CLKS2} = f_{CLKS1}$
- $f_{CLKP1} = f_{CLKB}$
- $f_{CLKP2} = f_{CLKB}/2$
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10B) or 1.9V (VRCR:HPM[1:0] = 11B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128H/2208H (0 Flash wait states, $f_{CLKS1} = 2*f_{CLKB}$)
  - MTCRA=0239H/2129H (1 Flash wait state, $f_{CLKS1} = f_{CLKB}$)
  - MTCRA=4C09H/6B09H (1 Flash wait state, $f_{CLKS1} = 2*f_{CLKB}$)
  - MTCRA=233AH (2 Flash wait states, $f_{CLKS1} = f_{CLKB}$)
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

Figure 9. CY96F353/F355 PLL Run Mode Currents

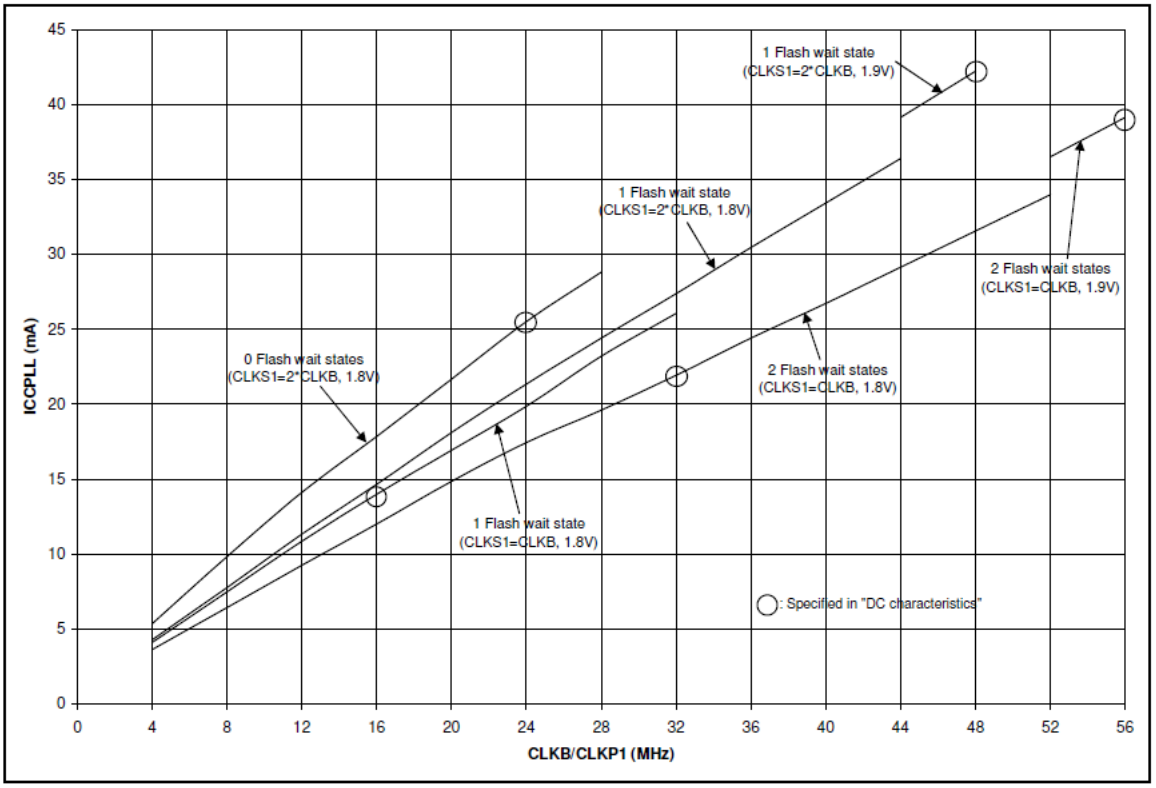
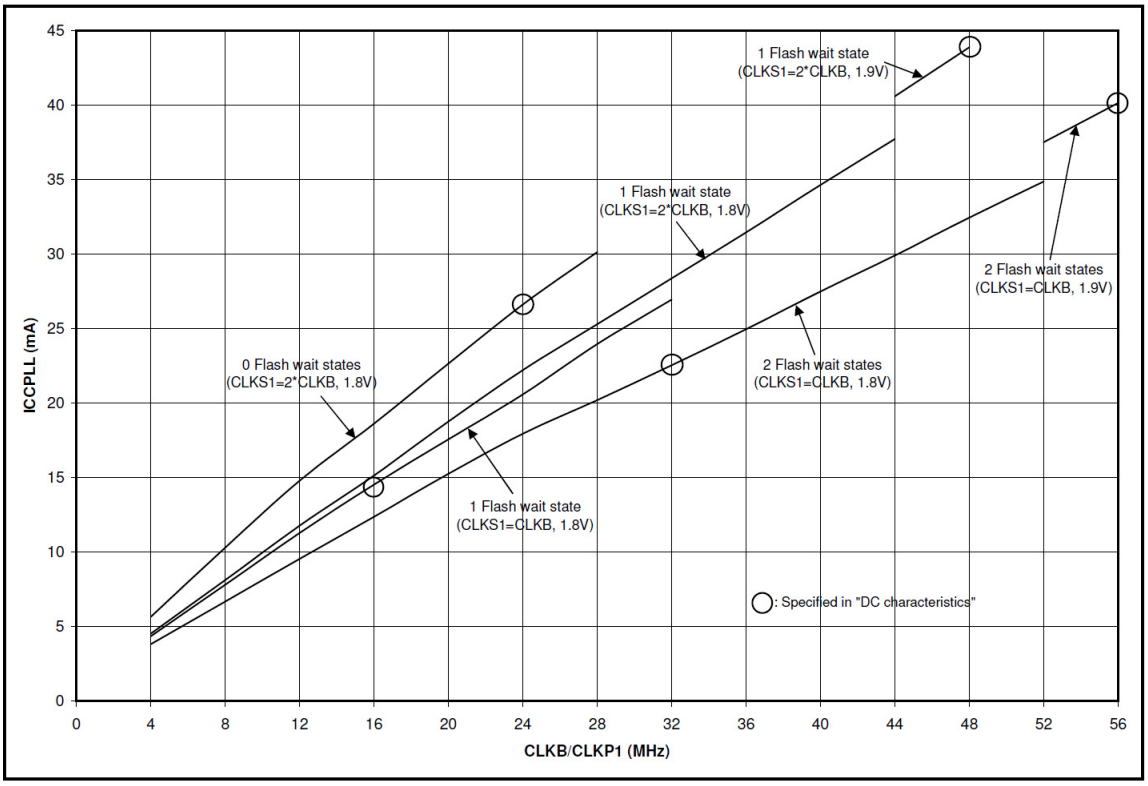
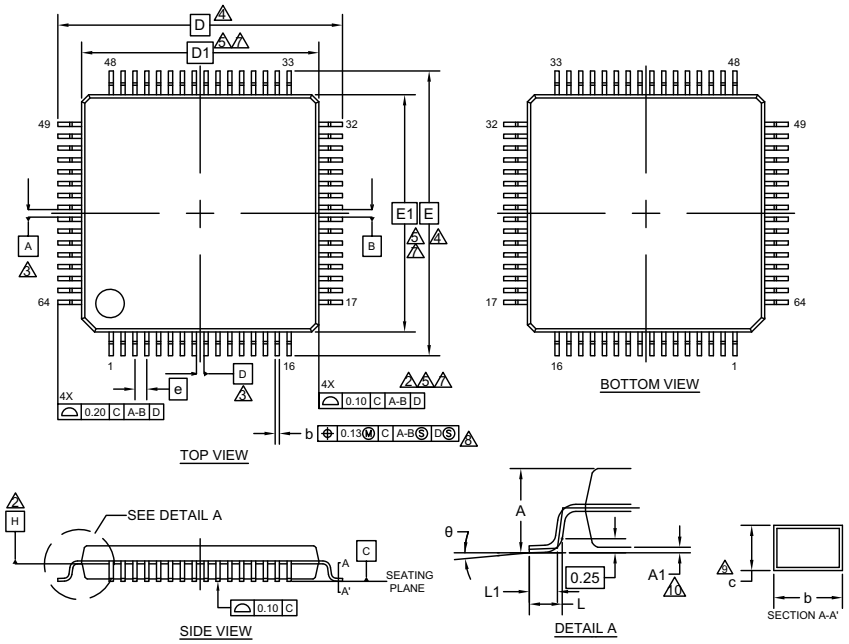


Figure 10. CY96F356 PLL Run Mode Currents



Package Dimension

CY96(F)35x LQFP 64 - LQG064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.27	0.32	0.37
c	0.09	——	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	——	8°

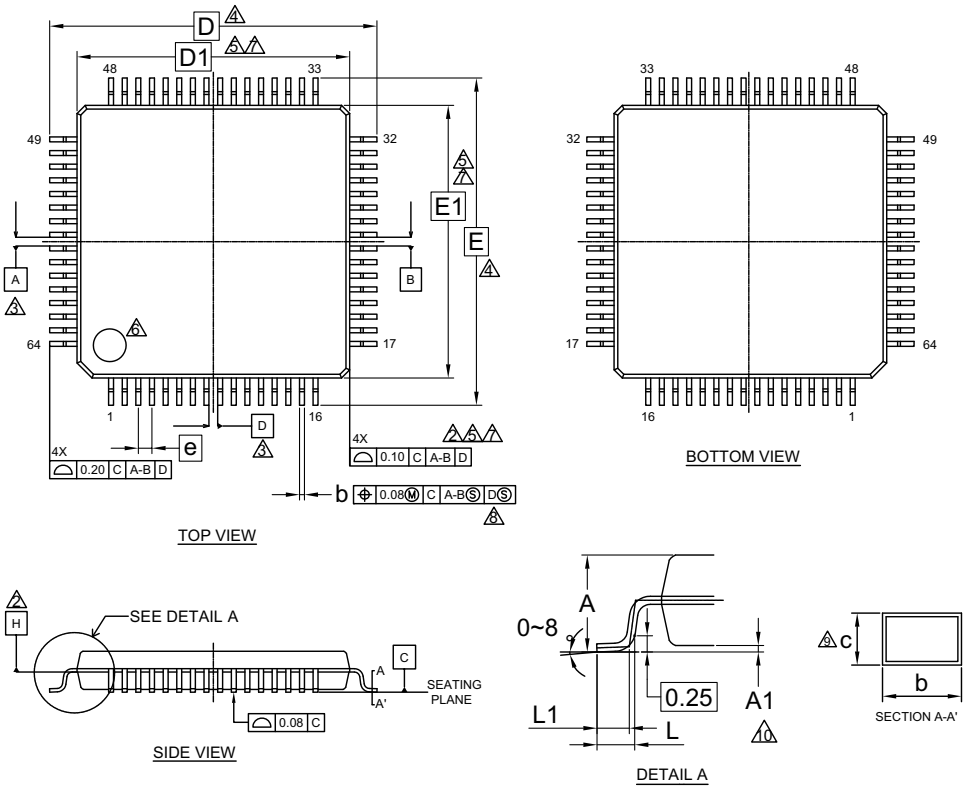
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

CY96(F)35x LQFP 64 - LQD064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D		12.00 BSC.	
D1		10.00 BSC.	
e		0.50 BSC	
E		12.00 BSC.	
E1		10.00 BSC.	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Ordering Information

MCU with CAN Controller

Part number	Flash/ROM	Subclock	Package
CY96F355RSBPMC-GS-UJE2	Flash A (160 KB)	No	64 pins Plastic LQFP (LQG064)
CY96F355RSBPMC1-GS-UJE2			64 pins Plastic LQFP (LQD064)
CY96F355RSBPMC1-GSUJERE2			64 pins Plastic LQFP (LQD064)
CY96F356RSBPMC1-GS-UJE1	Flash A (288 KB)	No	64 pins Plastic LQFP (LQD064)
CY96F356RSBPMC1-GS-UJE2			
CY96F356RSBPMC-GS-UJE2			64 pins Plastic LQFP (LQG064)
CY96F356RSBPMC-GS-UJERE2			64 pins Plastic LQFP (LQG064)
CY96F356RWBPMC1-GS-UJE2		Yes	64 pins Plastic LQFP (LQD064)
CY96F356RWBPMC-GS-UJE2			64 pins Plastic LQFP (LQG064)

MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
CY96F353ASBPMC1-GS-UJE2	Flash A (96 KB)	No	64 pins Plastic LQFP (LQD064)
CY96F356ASBPMC-GS-UJE2	Flash A (288 KB)	No	64 pins Plastic LQFP (LQG064)

This datasheet is also valid for the following outdated devices:

CY96F356YSA, CY96F356RSA, CY96F356YWA, CY96F356RWA, CY96F356ASA, CY96F356AWA, CY96F353RSA, CY96F353RWA, CY96F355RSA, CY96F355RWA, CY96F353ASA, CY96F353AWA, CY96F355ASA, CY96F355AWA.

Major Changes

Page	Section	Change Result
Rev *A		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
1	-	Deleted the following comment. Note: F2MC is the abbreviation of Fujitsu Flexible Microcontroller
6 87 89	Pin Assignment Package Dimension CY96(F)35x LQFP 64 - LQG064 Ordering Information	Package description modified to JEDEC description. (before) FPT-64P-M23 (after) LQG064
6 88 89	Pin Assignment Package Dimension CY96(F)35x LQFP 64 - LQD064 Ordering Information	Package description modified to JEDEC description. (before) FPT-64P-M24 (after) LQD064
15	Serial Programming Communication Interface	Corporate name changed from Fujitsu to Cypress.
89	Ordering Information	Deleted the following part number. MB96F353RSB PMC-GSE2, MB96F353RWB PMC-GSE2, MB96F353RSB PMC1-GSE2, MB96F353RWB PMC1-GSE2, MB96F355RWB PMC-GSE2, MB96F355RWB PMC1-GSE2, MB96F356RSB PMC-GSE2, MB96F356RWB PMC-GSE2, MB96F356RSB PMC1-GSE2, MB96F356RWB PMC1-GSE2, MB96V300CRB-ES (for evaluation), MB96F353ASB PMC-GSE2, MB96F353AWB PMC-GSE2, MB96F353AWB PMC1-GSE2, MB96F355ASB PMC-GSE2, MB96F355AWB PMC-GSE2, MB96F355ASB PMC1-GSE2, MB96F355AWB PMC1-GSE2, MB96F356ASB PMC-GSE2, MB96F356AWB PMC-GSE2, MB96F356ASB PMC1-GSE2, MB96F356AWB PMC1-GSE2 Revised the following parts number. (before) - MB96F355RSB PMC-GSE2 - MB96F355RSB PMC1-GSE2 - MB96F353ASB PMC1-GSE2 (after) - CY96F55RSBPMC-GS-UJE2 - CY96F355RSBPMC1-GS-UJE2 - CY96F353ASBPMC1-GS-UJE2 Changed and deleted the parts number in Note. (before) MB96F356YSA, MB96F356RSA, MB96F356YWA, MB96F356RWA, MB96F356ASA, MB96F356AWA, MB96F353RSA, MB96F353RWA, MB96F355RSA, MB96F355RWA, MB96F353ASA, MB96F353AWA, MB96F355ASA, MB96F355AWA. (after) CY96F356YSA, CY96F356RSA, CY96F356YWA, CY96F356RWA, CY96F356ASA, CY96F356AWA, CY96F353RSA, CY96F353RWA, CY96F355RSA, CY96F355RWA, CY96F353ASA, CY96F353AWA, CY96F355ASA, CY96F355AWA.

Page	Section	Change Result
90	Major Changes	Changed section title and section number. (before) MAJOR CHANGES IN THIS EDITION (after) Major Changes
95	Document History	Added Document History
Rev *B		
90	Ordering Information	Added the following parts number. MCU with CAN Controller - CY96F356RSBPMC1-GS-UJE1 - CY96F356RSBPMC1-GS-UJE2 - CY96F356RSBPMC-GS-UJE2 - CY96F356RWBPMC1-GS-UJE2 - CY96F356RWBPMC-GS-UJE2 MCU with CAN Controller - CY96F356ASBPMC-GS-UJE2

Revision History

Spansion Publication Number: **DS07-13806-3E**

Revision	Date	Modification
Prelim 1	2007-05-03	Creation
Prelim 2	2007-05-25	Electrical characteristics update
Prelim 3	2007-11-27	Package description is removed from cover page. Typos corrections in product lineup. Product option details added Electrical characteristics update Update of the block diagram Update of the IO map Pin circuit type, LVD characteristics and example characteristics chapters added
Prelim 4	2007-12-20	Update of the block diagram: external bus address lines, clock output function pins, AVRL removed from ADC block, re-layout. RAMSTART value is corrected IO map regenerated Memory map and Flash configuration reworked Few typos corrected across the document. Flash bank renaming. Ordering information: package type corrected. IO circuit drawings modified.

Revision	Date	Modification
Prelim 5	2008-02-04	■ Reload Timer RLT 6 for PPGs added ■ Block diagram corrected: ICU2 deleted, TTG2,3 deleted, TTG8,9 added ■ Pin function description corrected with all existing pin types ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ “Flash sector configuration” replaced by corrected "User ROM Memory map for Flash devices” ■ Parallel Flash programming spec removed ■ IO map table regenerated: - Port register: Naming style corrected - Memory control registers renamed (Main -> A) - addresses after 000BFFh removed ■ Handling devices: AD converter items added ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ Run and Sleep mode currents: more conditions added (1WS settings) ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1 frequency corrected at 1.8V ■ External bus timings: missing conditions added and readability improved ■ Ordering information updated ■ Typos and formatting corrected

Revision	Date	Modification
6	2009-01-09	■ Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ CANless devices added (MB96F356A) ■ I/O map: Added node about reserved registers ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Ordering information: column “Flash/ROM” added, column “Remarks” removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F353/F355 added (under development) ■ Free running timer (I/O Timer) 2 and 3 added (without clock input pin) ■ Input capture ICU9 and ICU10 added (without input pin, only for LIN USART) ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ “Preliminary” watermark removed

Revision	Date	Modification
7	2010-06-24	• AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg • Low voltage detector: Detection levels of MB96F353/F355 updated • Note added that PLL phase jitter spec does not include jitter coming from Main clock • Note added in DC characteristics how to select driving strength of ports • I^2C AC spec updated: tof, Cb and tSP spec added, wrong footnotes and Condition removed • I/O Circuit type: Note added for type “N” (slew rate control according to I^2C spec) • Example characteristics updated, new figures added showing dependency of PLL Run mode current on frequency • Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values) • Package dimension: Added the following sentence under the figure: “Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/package/en-search/” • AD converter: Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time • Added specification of RC clock stabilization time • Ordering information updated: MB96F353/F355**A -> MB96F353/F355**B, the device development is finished • Feature description I^2C: ‘8-bit addressing’ corrected to ‘7-bit addressing’ • Feature description PPG: ‘Reload timer overflow as clock input’ corrected to ‘Reload timer underflow as clock input’ • ICCLVD specification updated, at 125deg typical value is 7uA and maximum value is 20uA • Company name updated on the cover page: Fujitsu Microelectronics Limited -> Fujitsu Semiconductor Limited

Page	Section	Change Result
Front Page	-	Remove following description: " *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice. "
7	Product Lineup	Remove following description: " *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice. "
13	I/O Circuit Type	Error correction in Remarks of Type B.
15	I/O Circuit Type	Added Remarks in Type N.
52	Handling Devices	Item “6. Power supply pins (Vcc/Vss)”: Added note for bypass capacitor.
53	Handling Devices	Added new item “Clock modulator”.
54	Electrical Characteristics	Added output current spec for 2mA and 3mA outputs.
59	DC Characteristics	Added Port drive condition in Remarks.
60 to 64	DC Characteristics	Added Mode Conditions. Changed proper value for flash devices.
66	AC Characteristics	Added RC clock stabilization time. Added remark in “PLL Phase Jitter”
67	When using an oscillation circuit	Added Figure of Amplitude.
85	I^2C Timing	Added new parameter “Output fall time” ,”Capacitive load for each bus line” and “Pulse width of spikes”.
86	Analog Digital Converter	Deleted double expression for I_{AIN} and corrected value.

Page	Section	Change Result
89	Accuracy and setting of the A/D Converter sampling time	Changed to a more accurate estimation for sampling time by R_{ext}, C_{ext}, C_{IN}, R_{ADC} and C_{ADC}
90	Low Voltage Detector characteristics	Added note description for inclination of the power-supply voltage.
93 to 100	Example Characteristics	Added new section.
101, 102	Ordering Information	Remove following description: " *1: These devices are under development and specification is preliminary. These products under development may change its specification without notice. "

Document History

Document Title: CY96F353/F355, CY96F356, F^{2}MC-16FX, CY96350 Series, 16-bit Proprietary Microcontroller Document Number: 002-04588			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	—	07/18/2013	Migrated to Cypress and assigned document number 002-04588. No change to document contents or format.
*A	6213848	06/21/2018	Updated to Cypress template. Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. Pin Assignments Package Dimension Ordering Information Renamed Chapter Name of MAJOR CHANGES IN THIS EDITION For details, please see Major Changes section
*B	6351866	10/16/2018	Added Marketing Part Number in Ordering Information. For details, please see Major Changes section
*C	6896470	06/10/2020	Added the part numbers CY96F355RSBPMC1-GSUJERE2 and CY96F356RSBPMC-GS-UJERE2 in Ordering Information.

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