



**THE DATASHEET OF  
BLA9H0912LS-700GU**



# BLA9H0912L(S)-700; BLA9H0912L(S)-700G

Power LDMOS transistor

Rev. 1 — 24 May 2019

AMPLEON

Product data sheet

## 1. Product profile

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### 1.1 General description

700 W LDMOS power transistor for avionics applications in the frequency range from 960 MHz to 1215 MHz.

**Table 1. Typical information**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 50\text{ }\mu\text{s}$ ;  $\delta = 2\%$ ;  $I_{DQ} = 100\text{ mA}$ ; in a class-AB demo circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)
pulsed RF	1030	50	700	20	62

### 1.2 Features and benefits

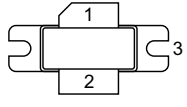
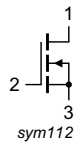
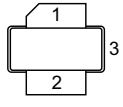
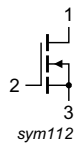
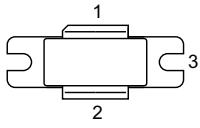
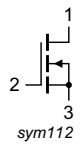
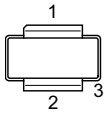
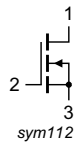
- High efficiency
- Excellent ruggedness
- Designed for avionics band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- Avionics transmitter applications in the frequency range from 960 MHz to 1215 MHz

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLA9H0912L-700 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9H0912LS-700 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9H0912L-700G (SOT502F)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9H0912LS-700G (SOT502E)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLA9H0912L-700	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA9H0912LS-700	-	earless flanged ceramic package; 2 leads	SOT502B
BLA9H0912L-700G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA9H0912LS-700G	-	earless flanged ceramic package; 2 leads	SOT502E

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	106	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 700\text{ W}$		
		$t_p = 32\text{ }\mu\text{s}; \delta = 2\%$	0.055	K/W
		$t_p = 10\text{ }\mu\text{s}; \delta = 10\%$	0.068	K/W
		$t_p = 64\text{ }\mu\text{s}; \delta = 1\%$	0.076	K/W
		$t_p = 2.4\text{ ms}; \delta = 6.4\%$	0.24	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4\text{ mA}$	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 400\text{ mA}$	1.5	2.0	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	60	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 400\text{ mA}$	-	3.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 14\text{ A}$	-	0.060	-	$\Omega$

**Table 7. RF characteristics**

Test signal: pulsed RF;  $f = 1030 \text{ MHz}$ ;  $t_p = 50 \mu\text{s}$ ;  $\delta = 2 \%$ ; RF performance at  $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 100 \text{ mA}$ ;  $T_{case} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 700 \text{ W}$	19	20	-	dB
$\eta_D$	drain efficiency	$P_L = 700 \text{ W}$	59	62	-	%
$RL_{in}$	input return loss	$P_L = 700 \text{ W}$	-	-15	-	dB
$P_{droop(pulse)}$	pulse droop power	$P_L = 700 \text{ W}$	-	0.2	0.5	dB
$P_{L(2dB)}$	output power at 2 dB gain compression		-	725	-	W

## 7. Test information

### 7.1 Ruggedness in class-AB operation

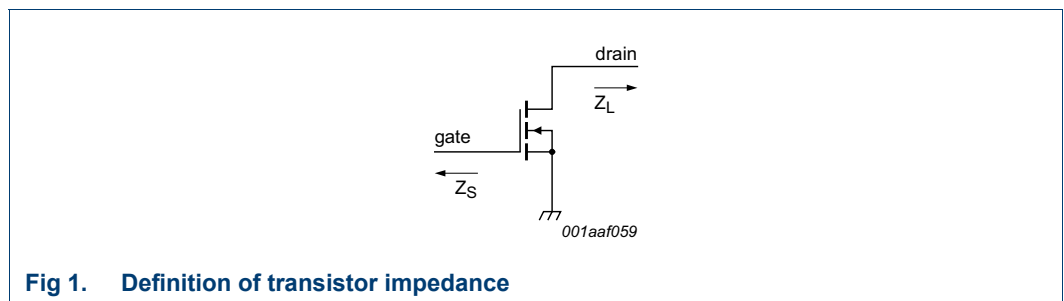
The BLA9H0912L-700, BLA9H0912LS-700, BLA9H0912L-700G and BLA9H0912LS-700G are capable of withstanding a load mismatch corresponding to  $VSWR = 20 : 1$  through all phases under the following conditions:  $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 100 \text{ mA}$ ;  $P_L = 700 \text{ W}$ ;  $t_p = 50 \mu\text{s}$ ;  $\delta = 2 \%$ .

### 7.2 Impedance information

**Table 8. Typical impedance**

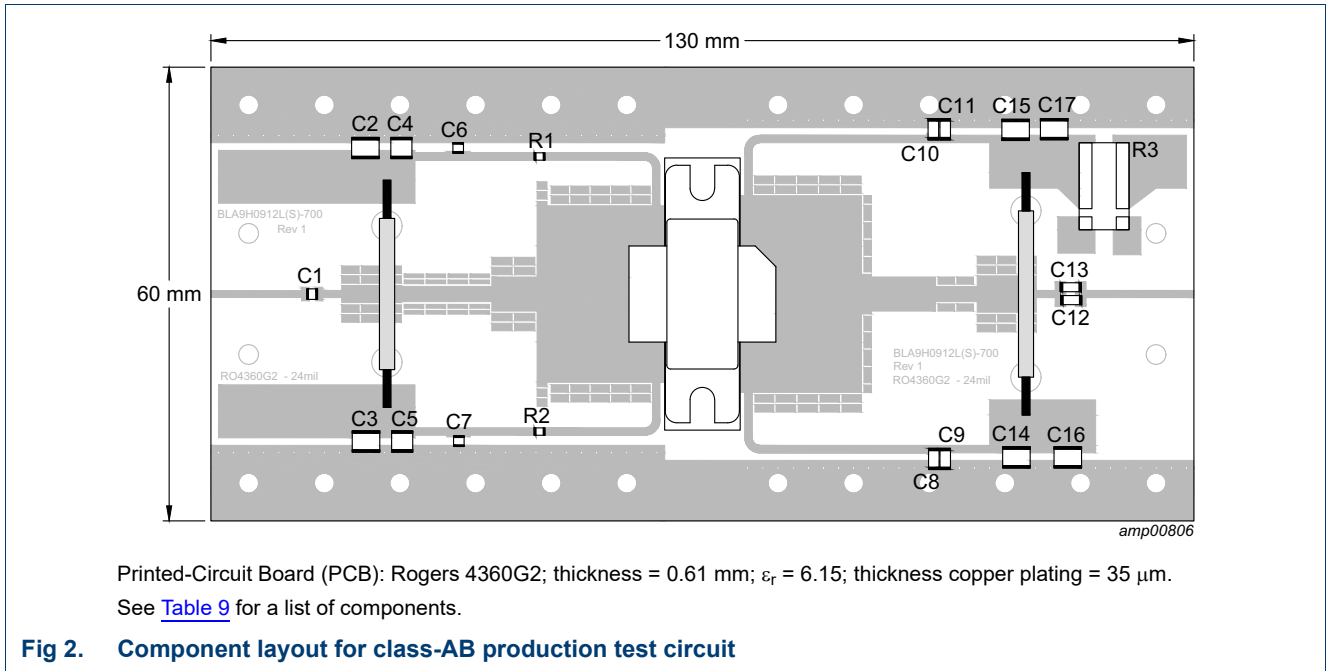
Typical values unless otherwise specified.

f (MHz)	$Z_s$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
950	$0.717 - j1.793$	$0.965 - j1.305$
1000	$0.953 - j1.886$	$1.049 - j1.561$
1050	$1.091 - j1.910$	$1.032 - j1.780$
1100	$1.353 - j0.443$	$1.291 - j1.952$
1150	$1.962 - j1.061$	$1.474 - j2.081$
1200	$0.837 - j0.936$	$1.514 - j2.413$



**Fig 1. Definition of transistor impedance**

7.3 Test circuit

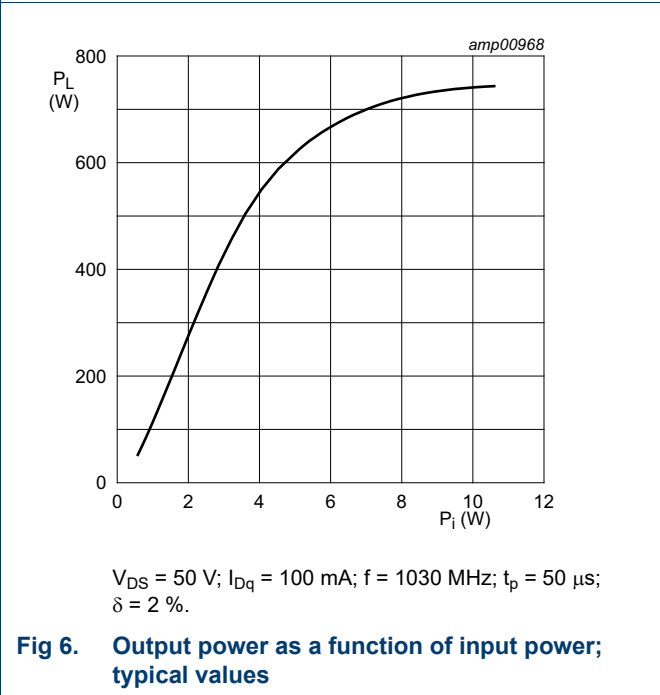
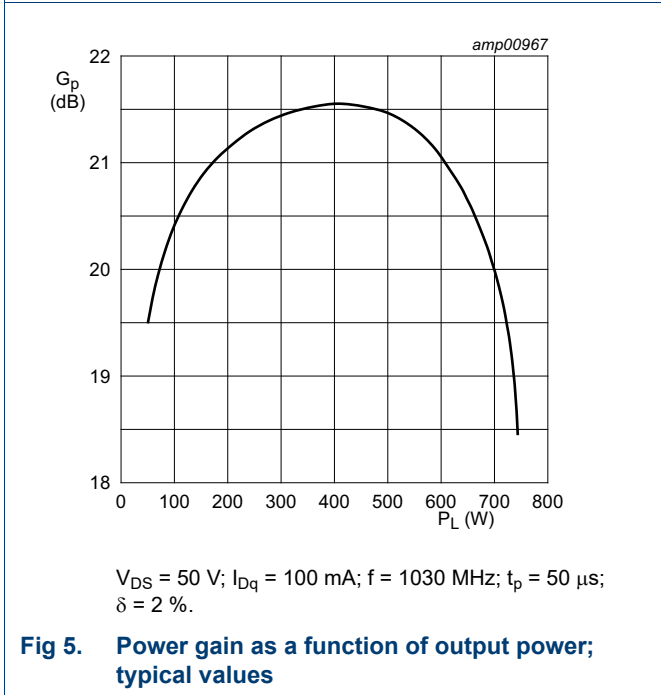
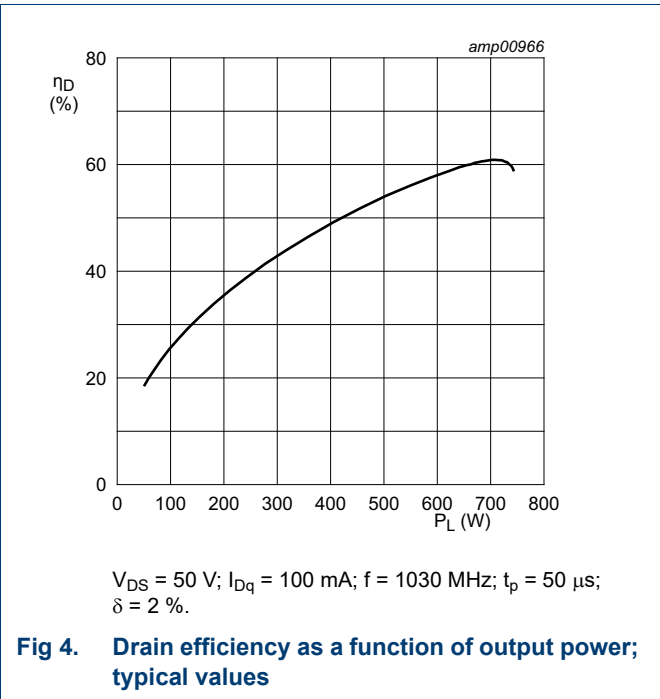
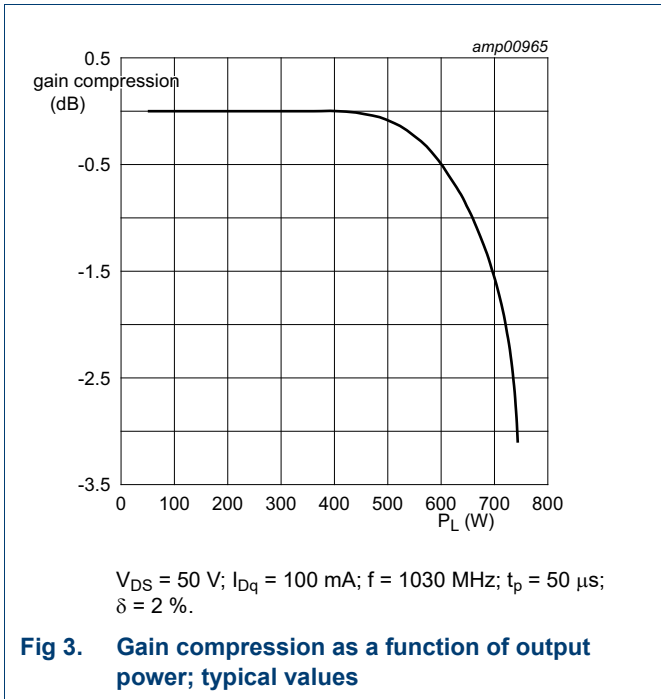


**Table 9. Demo test circuit list of components**

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	62 pF	ATC 100A
C2, C3, C16, C17	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 100 V	GMR42 258K7S 475K 100 H53
C4, C5, C14, C15	multilayer ceramic chip capacitor	1 nF	ATC 100B
C6, C7	multilayer ceramic chip capacitor	200 pF	ATC 800B
C8, C9, C10, C11, C12, C13	multilayer ceramic chip capacitor	68 pF	ATC 800B
R1, R2	resistor	5.1 k $\Omega$	SMD 0603
R3	resistor	10 m $\Omega$	FC4L110R010FER

7.4 Graphical data



8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

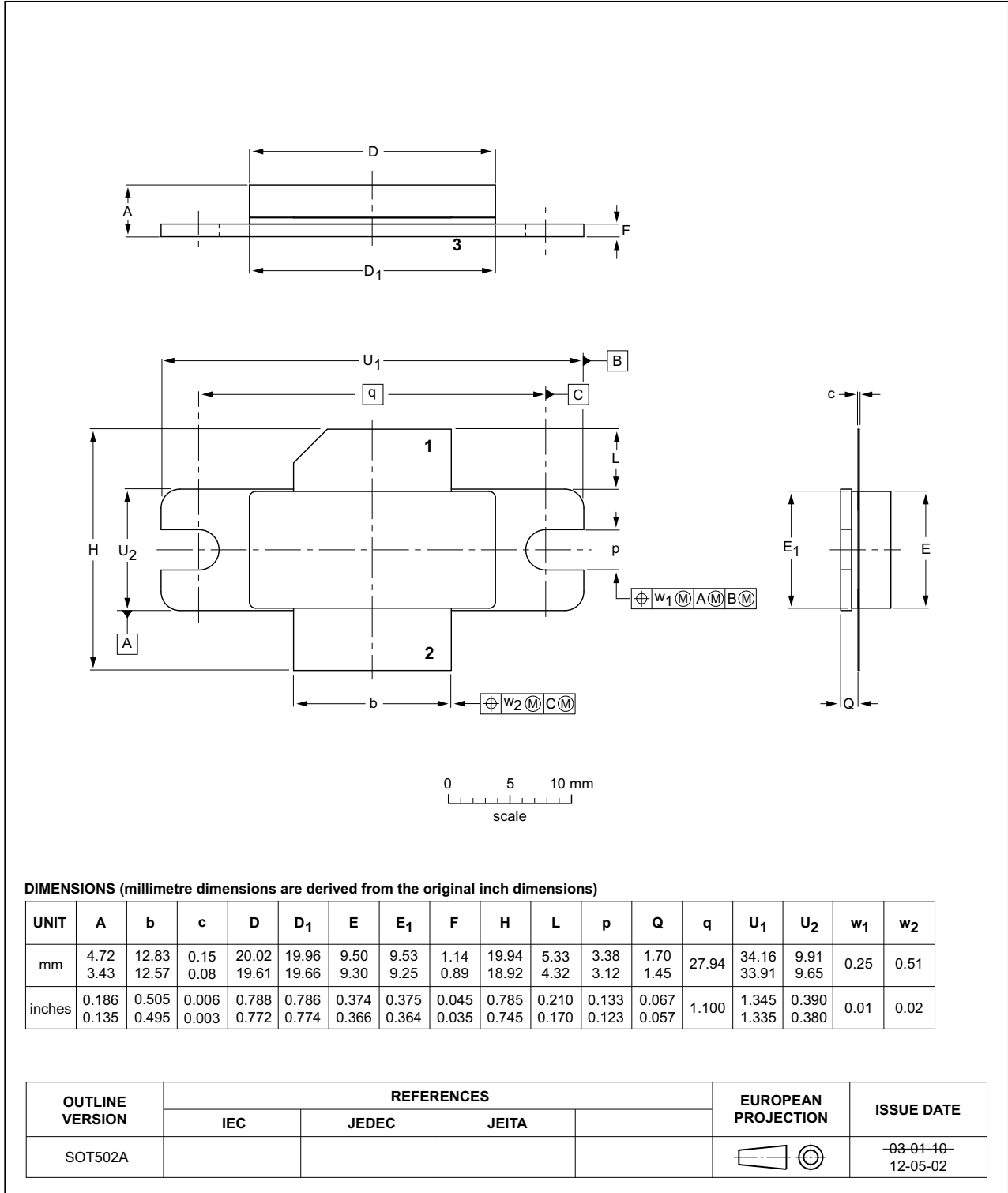


Fig 7. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

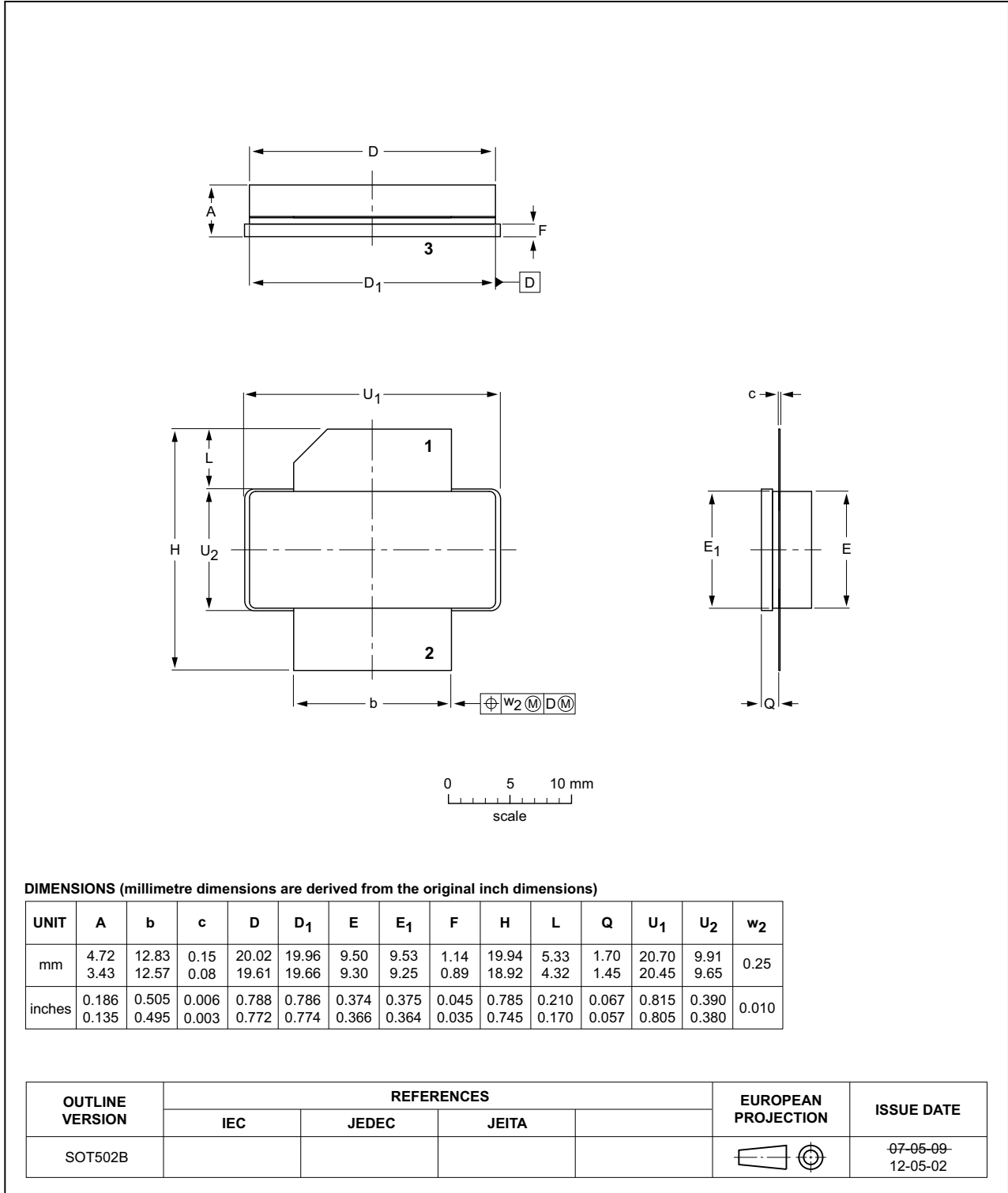


Fig 8. Package outline SOT502B

Earless flanged ceramic package; 2 leads

SOT502E

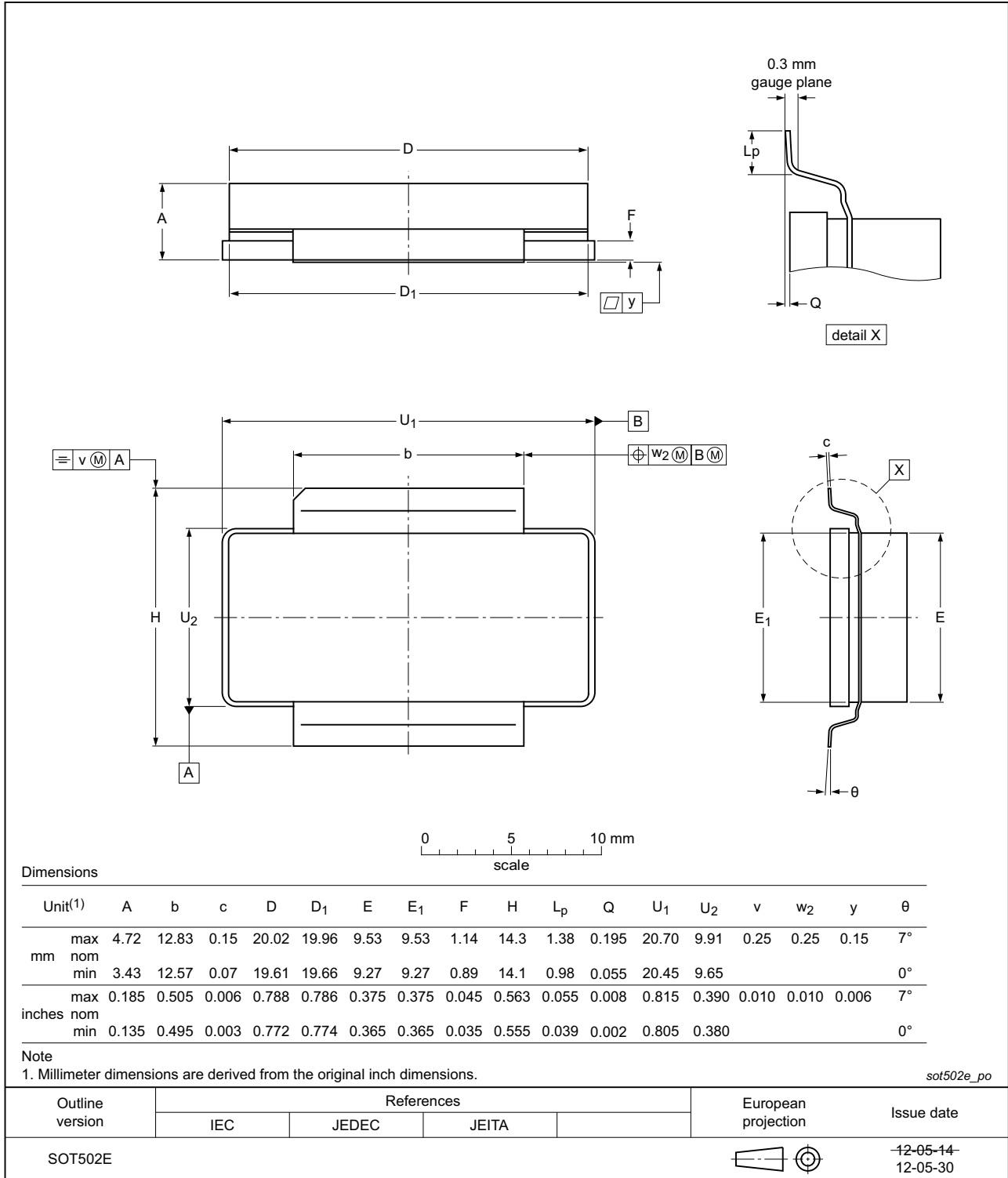


Fig 9. Package outline SOT502E

Eared flanged ceramic package; 2 leads; 2 mounting holes

SOT502F

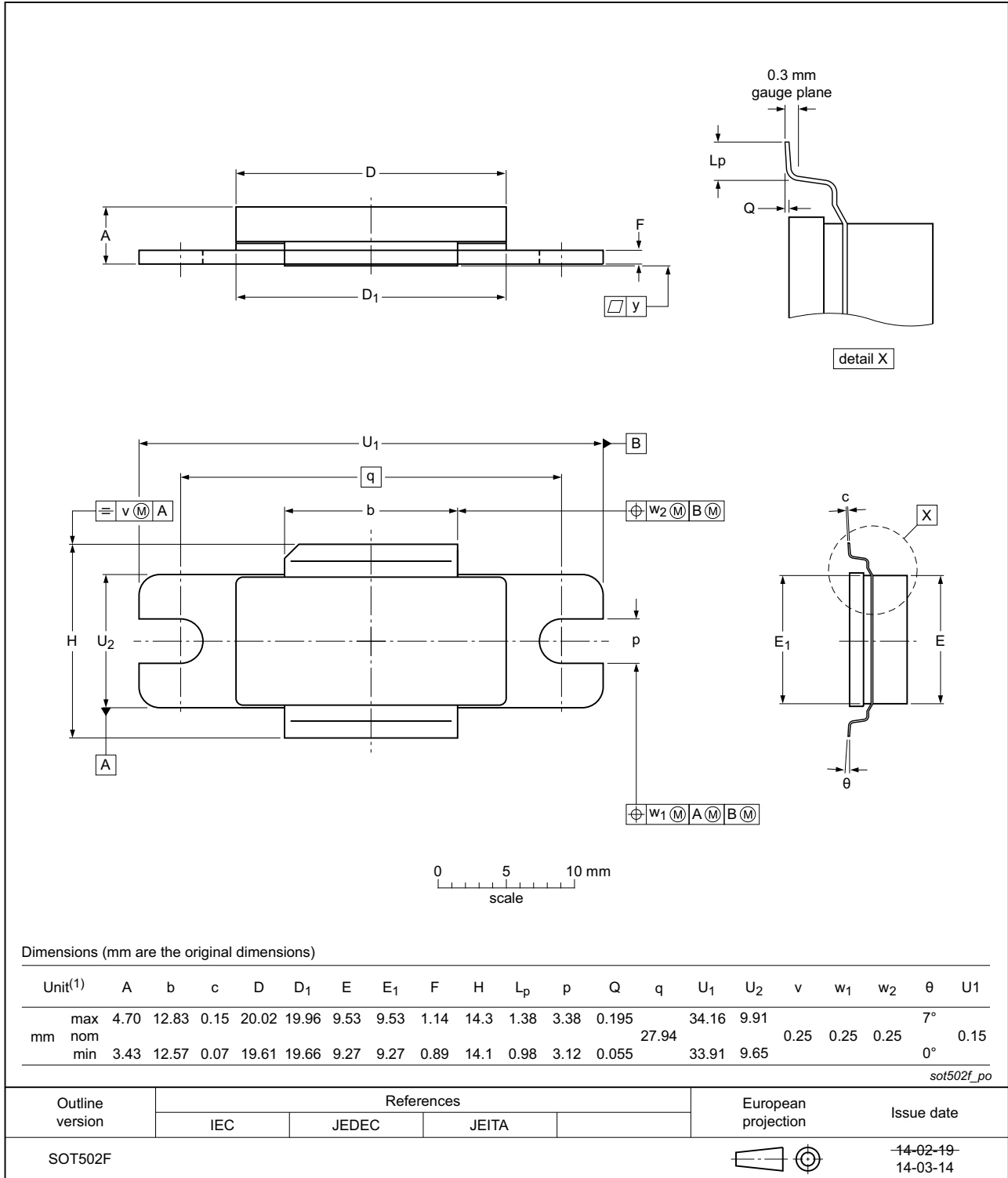


Fig 10. Package outline SOT502F

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.  
Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9H0912L-700_LS-700_L-700G_LS-700G v.1	20190524	Product data sheet		-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

1 **Product profile** . . . . . 1

1.1 General description . . . . . 1

1.2 Features and benefits . . . . . 1

1.3 Applications . . . . . 1

2 **Pinning information** . . . . . 2

3 **Ordering information** . . . . . 2

4 **Limiting values** . . . . . 3

5 **Thermal characteristics** . . . . . 3

6 **Characteristics** . . . . . 3

7 **Test information** . . . . . 4

7.1 Ruggedness in class-AB operation . . . . . 4

7.2 Impedance information . . . . . 4

7.3 Test circuit . . . . . 5

7.4 Graphical data . . . . . 6

8 **Package outline** . . . . . 7

9 **Handling information** . . . . . 11

10 **Abbreviations** . . . . . 11

11 **Revision history** . . . . . 11

12 **Legal information** . . . . . 12

12.1 Data sheet status . . . . . 12

12.2 Definitions . . . . . 12

12.3 Disclaimers . . . . . 12

12.4 Trademarks . . . . . 13

13 **Contact information** . . . . . 13

14 **Contents** . . . . . 14

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