THE DATASHEET OF

LTC3110HUF#TRPBF

2A Bidirectional Buck-Boost DC/DC Regulator and Charger/Balancer

FEATURES

- **V_{CAP} Operating Range: 0.1V to 5.5V**
- **V_{SYS} Operating Range: 1.71V to 5.25V**
- **Automatic Switchover from Charge to Backup Mode**
- **Programmable ±2% Accurate Charge Input Current Limit from 125mA to 2A**
- **±1% Backup Voltage Accuracy**
- **Automatic Backup Capacitor Balancing**
- Fixed 1.2MHz Switching Frequency
- Burst Mode® Operation: 40µA Quiescent Current
- Built-In Programmable Multipurpose Comparator with Open-Collector Output
- Open-Collector Outputs to Indicate Direction of Operation and End of Charge
- Thermally Enhanced TSSOP-24 and 4mm × 4mm QFN-24 Packages

APPLICATIONS

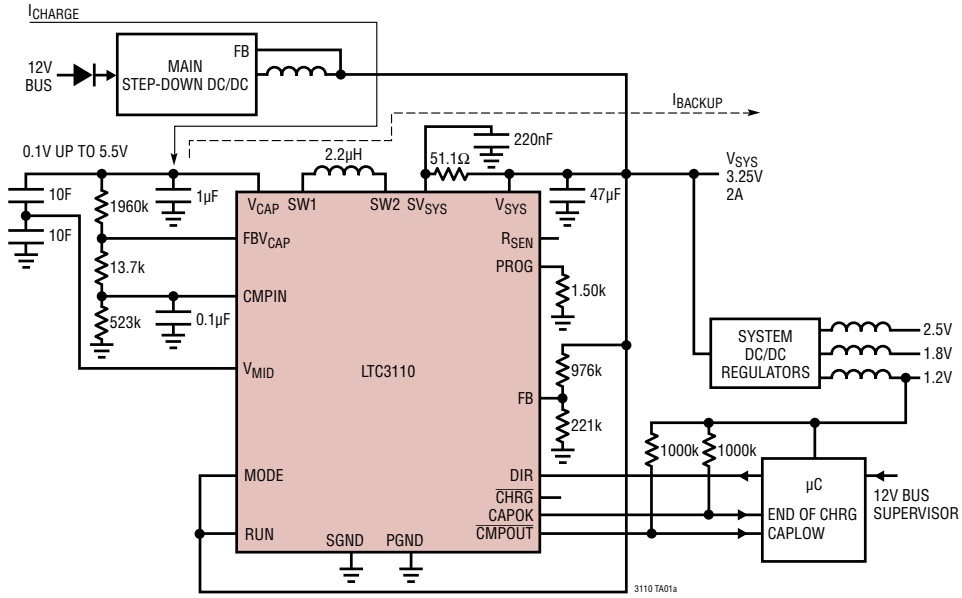
- Supercapacitor Backup Converter and Charger
- Battery Backup Converter and Charger
- Servers, RAID Systems
- RF Systems with Battery/Capacitor Backup

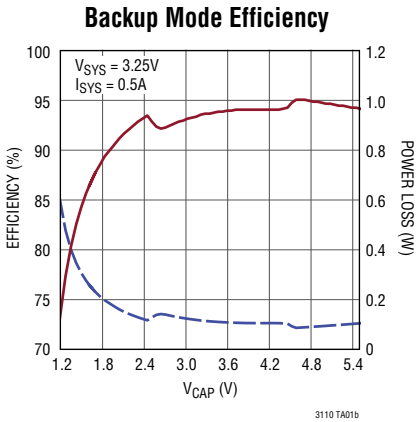
DESCRIPTION

The LTC®3110 is a 2A bidirectional buck-boost DC/DC regulator with capacitor charger and balancer. Its wide 0.1V to 5.5V capacitor/battery voltage and 1.8V to 5.25V system backup voltage ranges make it well suited to a wide variety of backup applications using supercapacitors or batteries. A proprietary low noise switching algorithm optimizes efficiency with capacitor/battery voltages that are above, below or equal to the system output voltage.

The LTC3110 can autonomously transition from charge to backup mode or switch modes based on an external command. Pin-selectable Burst Mode operation reduces standby current and improves light-load efficiency, which combined with a 1µA shutdown current make the LTC3110 ideally suited for backup applications. Additional features include voltage supervisors for direction control and end of charge, and a general purpose comparator with open-collector output for interfacing with a µC. The LTC3110 is available in thermally enhanced, low profile 24-lead TSSOP and 4mm × 4mm QFN packages.

TYPICAL APPLICATION



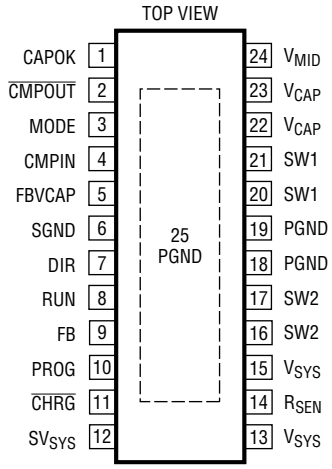


Rev C

ABSOLUTE MAXIMUM RATINGS (Note 1)

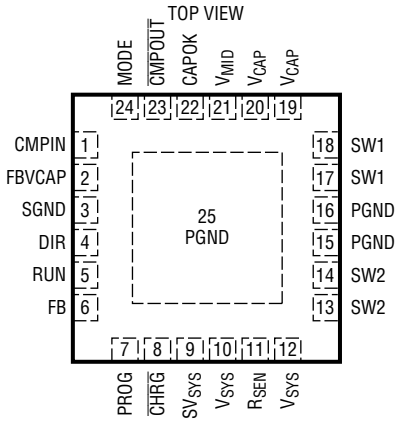
V_{CAP}, V_{SYS}, SV_{SYS}, V_{MODE}, V_{CMPIN}, V_{DIR}, V_{RUN}, V_{CAPOK}, V_{CMPOUT}, $V_{\overline{CHRG}}$ ..... –0.3V to 6V
R_{SEN} DC Current 1.6A
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Soldering Temperature (Soldering, 10 sec) TSSOP ..... 300°C
Reflow Peak Body Temperature (30sec max) QFN ..... 260°C

PIN CONFIGURATION



FE PACKAGE
24-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 5°C/W, 4 LAYER BOARD
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 37°C/W, θ_{JC} = 4.5°C/W, 4 LAYER BOARD
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3110EFE#PBF	LTC3110EFE#TRPBF	LTC3110FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3110IFE#PBF	LTC3110IFE#TRPBF	LTC3110FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3110HFE#PBF	LTC3110HFE#TRPBF	LTC3110FE	24-Lead Plastic TSSOP	–40°C to 150°C
LTC3110EUF#PBF	LTC3110EUF#TRPBF	3110	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3110IUF#PBF	LTC3110IUF#TRPBF	3110	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3110HUF#PBF	LTC3110HUF#TRPBF	3110	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CAP} = 3.3V, V_{SYS} = 3.3V, V_{DIR} = V_{SGND}, V_{MODE} = V_{RUN} = V_{SYS} = SV_{SYS} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CAP} No-Load Operating Range in Backup Operation	$V_{SYS} \geq 1.8V$		0.1		5.5	V
V_{CAP} Start-Up	V_{SYS} < Undervoltage Lockout Threshold	●	1.8			V
V_{SYS} Operating Range in Charge Operation	$V_{DIR} = V_{SYS}$	●	1.8		5.25	V
Undervoltage Lockout Threshold	V_{SYS} Ramping Down, V_{CAP} = 0V V_{SYS} Ramping Up, V_{CAP} = 0V	 ●	1.55		 1.71	V V
	V_{CAP} Ramping Down, V_{SYS} = 0V, $V_{RUN} = V_{CAP}$ V_{CAP} Ramping Up, V_{SYS} = 0V, $V_{RUN} = V_{CAP}$	 ●	1.55		 1.71	V V
FB Feedback Voltage	0°C < T_J < 85°C (Note 5) –40°C < T_J < 150°C	 ●	0.592 0.589	0.6 0.6	0.608 0.611	V V
FB Feedback Pin Input Current				0.1	50	nA
FBV_{CAP} End-of-Charge Threshold Rising	$DIR = V_{SYS}$	●		1.095	1.117	V
FBV_{CAP} End-of-Charge Threshold Falling	$DIR = V_{SYS}$	●	1.040	1.061		V
FBV_{CAP} Input Current	V_{FBVCAP} = 1.1V			0.1	50	nA
FBV_{CAP} Overcharge Threshold Rising			1.125	1.150	1.175	V
FBV_{CAP} Overcharge Hysteresis				35		mV
Quiescent Current, Burst Mode Operation (I_{VCAP} + I_{VSYS} + I_{SVSYS})	V_{MODE} = 0V			40		µA
Quiescent Current, End of Charge (I_{VCAP} + I_{VSYS} + I_{SVSYS})	$V_{DIR} = V_{SYS}$			40		µA
Quiescent Current, Shutdown (I_{VCAP})	V_{RUN} = 0V, $V_{SYS} = SV_{SYS}$ = 0V			0.05	1	µA
Peak Current Limit in Backup Operation	(Note 4)		5	6	7	A
DC Current Limit in Backup Operation	(Note 4)	●	3.5	4.5		A
Peak Current Limit in Charge Operation	(Note 4)		5	6	7	A
Reverse Current Limit in Backup Operation	(Note 4)		1	1.2	2	A
Switch Leakage	Switch B, C: $V_{CAP} = V_{SW1}$ = 5.5V, $V_{SYS} = V_{SW2}$ = 5.25V,			0.1		µA
	Switch A, D: V_{CAP} = 5.5V, V_{SYS} = 5.25V $V_{SW1} = V_{SW2}$ = 0V			0.1		µA
Switch On-Resistance	Switch A (Note 6) Switch B (Note 6) Switch C (Note 6) Switch D Including Sense Resistor (Note 6)			64 49 49 86		mΩ mΩ mΩ mΩ
Oscillator Frequency	 V_{CAP} = 0.2V V_{SYS} = 0.2V	●	900	1200 300 300	1500	kHz kHz kHz
Soft Start-Up Time in Backup Mode	From V_{RUN} rising to V_{FB} = 90%		0.8	1.3	1.8	ms
Maximum Duty Cycle in Boost Mode	 V_{CAP} = 0.2V	●	91	93 98	96	% %
Minimum Duty Cycle in Buck Mode		●			0	%
MODE Input Logic Threshold	Enable Burst Mode Operation Enable PWM Mode Operation		 1		0.3	V V
MODE Input Pull-Down Resistor				6		MΩ
DIR Threshold Rising		●	1.073	1.095	1.117	V
DIR Threshold Falling		●	1.024	1.045	1.066	V
DIR Hysteresis		●	30	50	70	mV
DIR Input Current	V_{DIR} = 1.1V			0.1	50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CAP} = 3.3V, V_{SYS} = 3.3V, V_{DIR} = V_{SGND}, V_{MODE} = V_{RUN} = V_{SYS} = SV_{SYS} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMPIN Threshold Rising			0.638	0.65	0.662	V
CMPIN Threshold Falling		●	0.575	0.59	0.605	V
CMPIN Input Current	V_{CMPIN} = 5.5V			0.1	50	nA
PROG Voltage	V_{FBVCAP} = 1V, DIR = V_{SYS}			0.6		V
PROG Current Gain	DIR = V_{SYS}			200		µA/A
I_{VSYS} Input Current Limit	R_{PROG} = 24.3k (Notes 7, 8), DIR = V_{SYS}		119	123	128	mA
	R_{PROG} = 24.3k (Notes 7, 8, 9), DIR = V_{SYS}, T_J = –40°C to 125°C		115	123	135	mA
	R_{PROG} = 12.1k (Notes 7, 8), DIR = V_{SYS}		241	248	255	mA
	R_{PROG} = 12.1k (Notes 7, 8, 9), DIR = V_{SYS}, T_J = –40°C to 125°C		234	248	270	mA
	R_{PROG} = 6.04k (Notes 7, 8), DIR = V_{SYS}		487	497	507	mA
	R_{PROG} = 6.04k (Notes 7, 8, 9), DIR = V_{SYS}, T_J = –40°C to 125°C		473	497	525	mA
	R_{PROG} = 3.01k (Notes 7, 8), DIR = V_{SYS}		977	997	1017	mA
	R_{PROG} = 3.01k (Notes 7, 8, 9), DIR = V_{SYS}, T_J = –40°C to 125°C		948	997	1046	mA
	R_{PROG} = 1.5k (Notes 7, 8), DIR = V_{SYS}		1960	2000	2040	mA
	R_{PROG} = 1.5k (Notes 7, 8, 9), DIR = V_{SYS}, T_J = –40°C to 125°C		1900	2000	2100	mA
V_{MID} to V_{CAP} Voltage Ratio	V_{MID} = Open Load, V_{CAP} = 5V		0.492	0.5	0.508	
V_{MID} Balancing Current	V_{CAP} = 5V, V_{MID} = 5V	●	150	300		mA
	V_{CAP} = 5V, V_{MID} = 0V	●		–300	–150	mA
V_{MID} Current in Shutdown	V_{RUN} = 0V			0.1	1	µA
V_{MID} Suspend Charging Threshold	V_{MID} Rising, V_{CAP} = 5V			2.6	2.62	V
	V_{MID} Falling, V_{CAP} = 5V		2.38	2.4		V
$\overline{CHRG}$, CAPOK, $\overline{CMPOUT}$ Open-Drain Output Voltage	I = 10mA	●		0.1	0.3	V
RUN Input Logic Threshold		●	0.3		1	V
RUN Pull-Down Resistor				6		MΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3110 is tested under pulsed load conditions such that $T_J \sim T_A$. The LTC3110E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3110I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature range. The LTC3110H is guaranteed to meet specifications over the full –40°C to 150°C operating junction temperature range. High temperatures degrade operating lifetime; operating life time is derated for junction temperatures greater than 125°C.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Current measurements are performed when the LTC3110 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

Note 5: Guaranteed by design characterization and correlation with statistical process controls.

Note 6: Guaranteed by design, correlation and bench measurements.

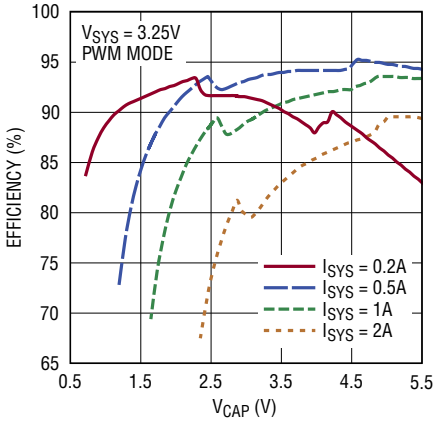
Note 7: Current measurements are made when the output is not switching.

Note 8: Accuracy of this specification is directly related to the accuracy of the resistor used to program the parameter.

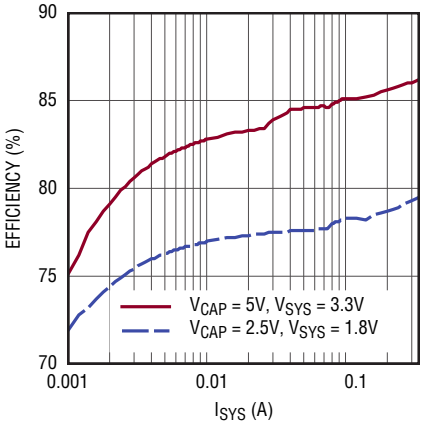
Note 9: The Input Current Limit is reduced at junction temperatures above 125°C. See Thermal Foldback of Charge Current in the Operation section, and the graph V_{PROG} Programming Voltage vs Temperature in the Typical Performance Characteristics section.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

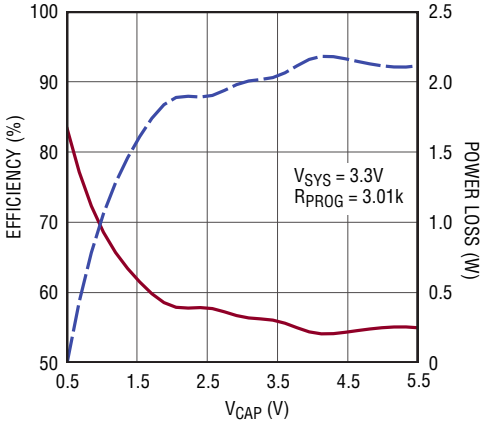
Efficiency vs V_{CAP} Voltage



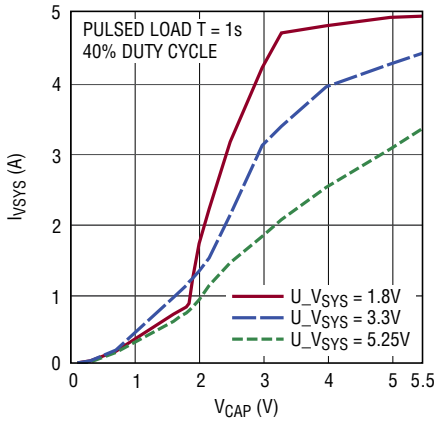
Burst Mode Efficiency



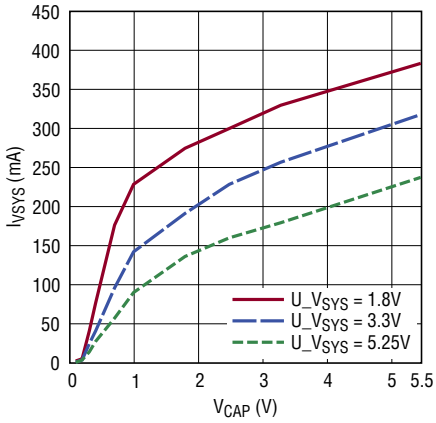
Charge Efficiency



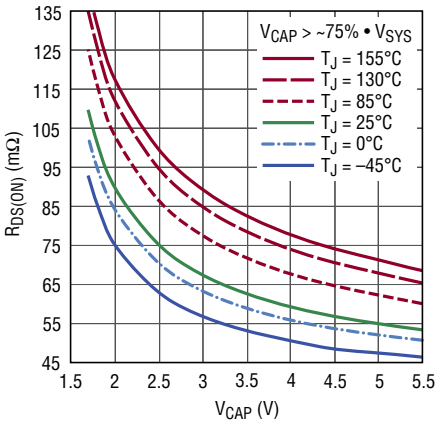
Maximum Load Current in PWM Mode



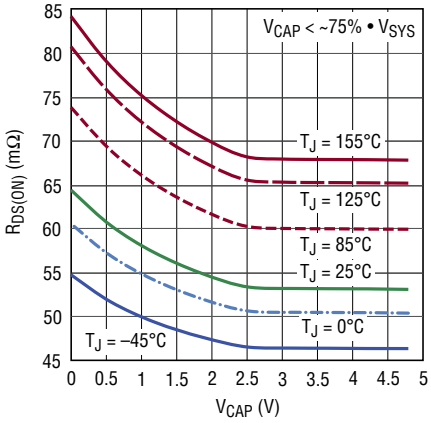
Maximum Load Current in Burst Mode Operation



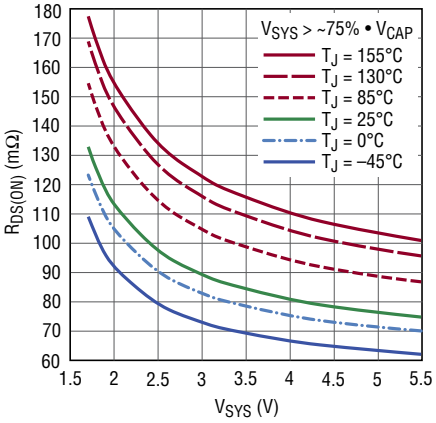
$R_{DS(ON)}$ of SWA Dynamic



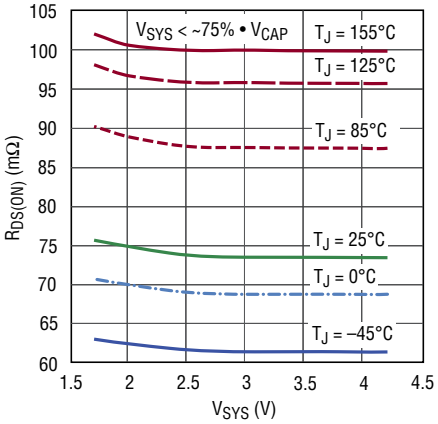
$R_{DS(ON)}$ of SWA Static



$R_{DS(ON)}$ of SWD Dynamic Including Sense Resistor

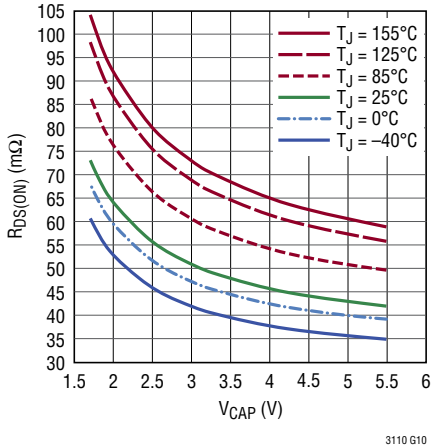


$R_{DS(ON)}$ of SWD Static Including Sense Resistor

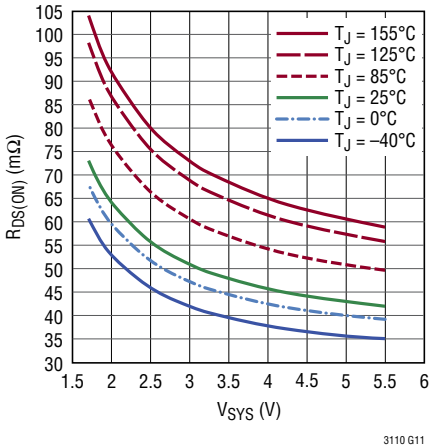


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

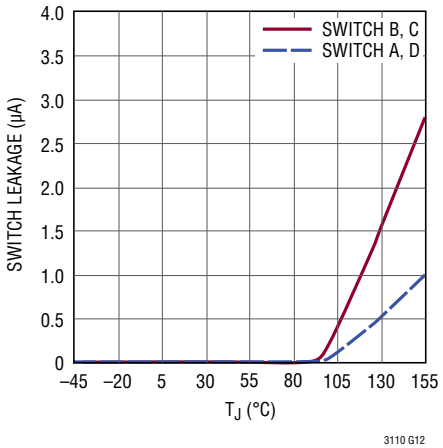
$R_{DS(ON)}$ of SWB



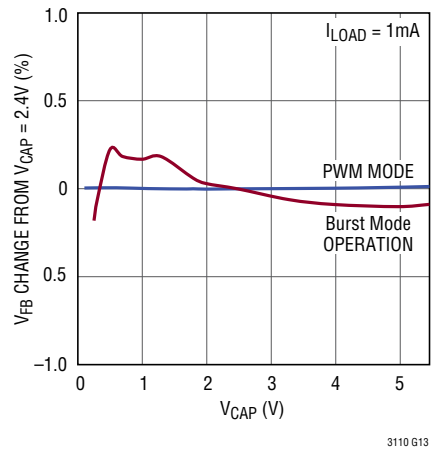
$R_{DS(ON)}$ of SWC



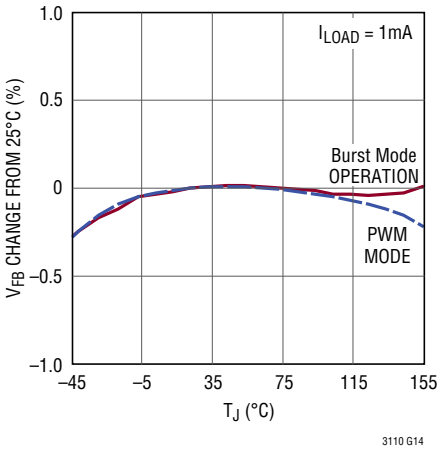
Switch Leakage vs Temperature



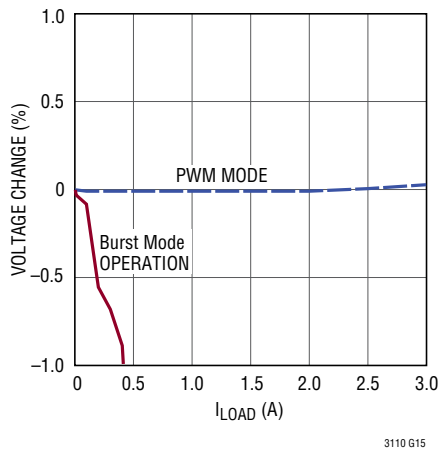
Feedback Voltage vs V_{CAP}



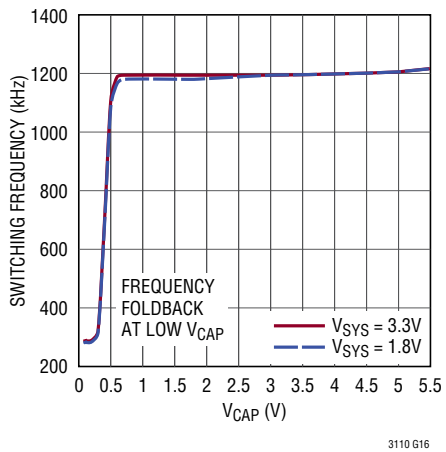
Feedback Voltage vs Temperature



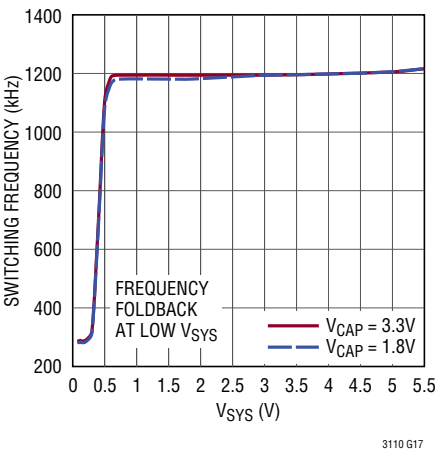
V_{SYS} Load Regulation



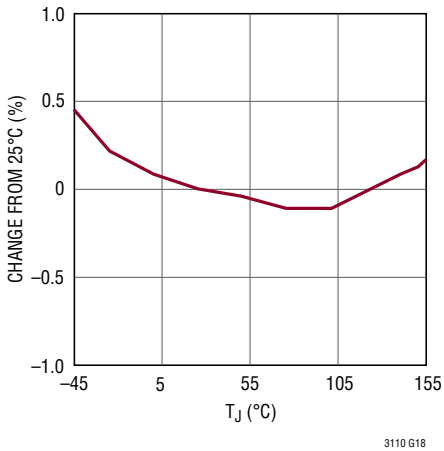
Switching Frequency vs V_{CAP}



Switching Frequency vs V_{SYS}

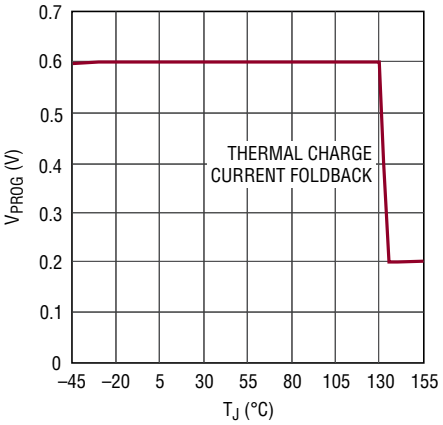


Switching Frequency vs Temperature

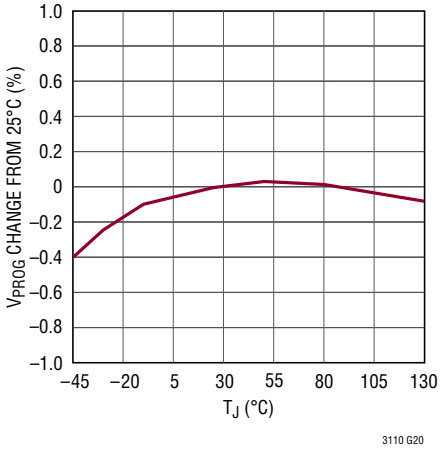


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

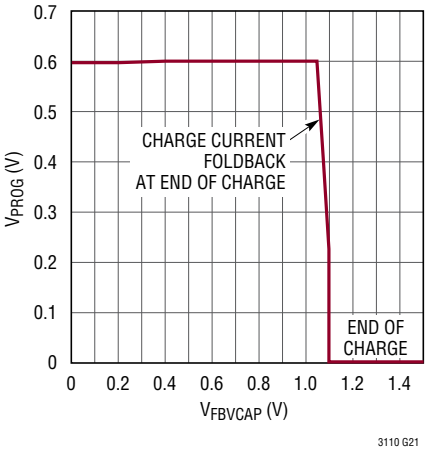
V_{PROG} Programming Voltage vs Temperature



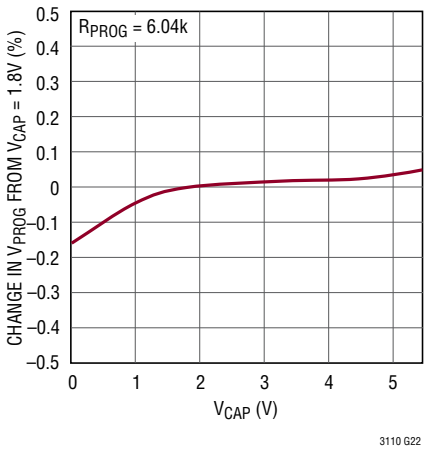
V_{PROG} Programming Voltage vs Temperature



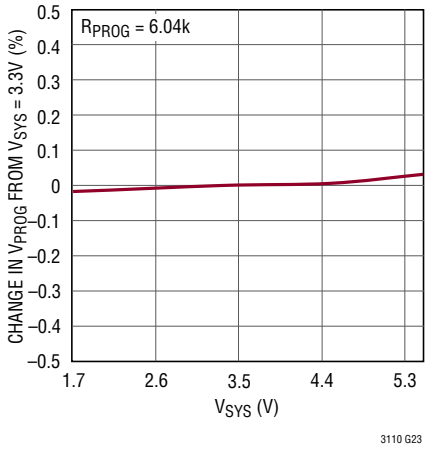
V_{PROG} Programming Voltage vs V_{FBVCAP}



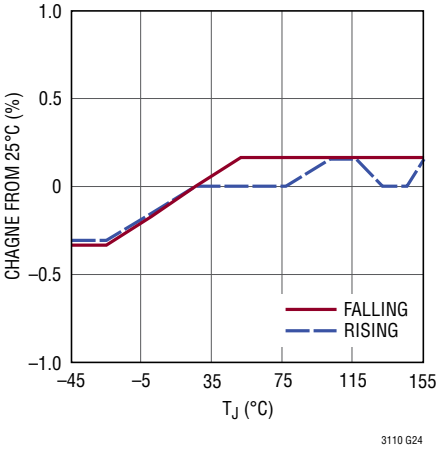
V_{PROG} Programming Voltage vs V_{CAP}



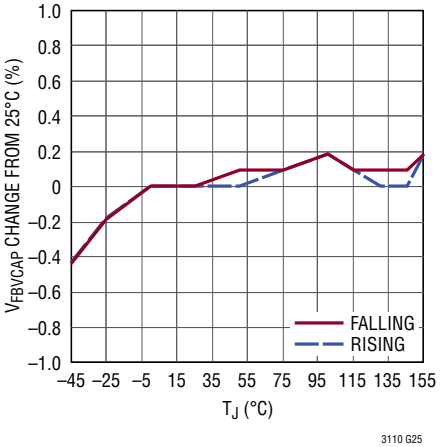
V_{PROG} Programming Voltage vs V_{SYS}



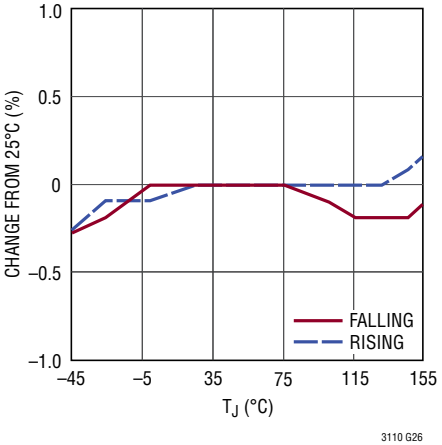
CMPIN Threshold Voltage vs Temperature



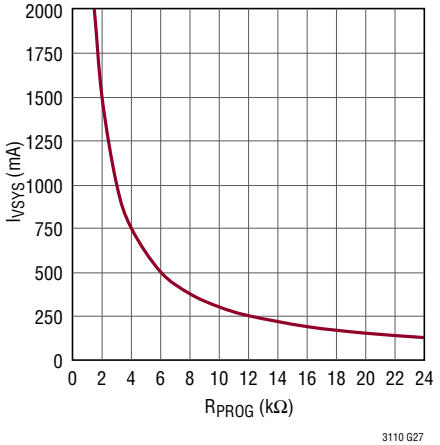
FBV_{CAP} Comparator Thresholds vs Temperature



DIR Thresholds vs Temperature

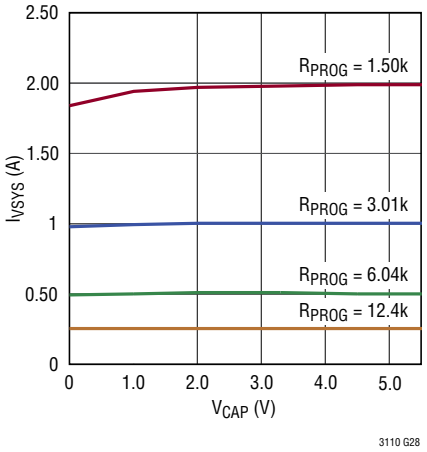


I_{VSYS} Input Current Limit vs R_{PROG}

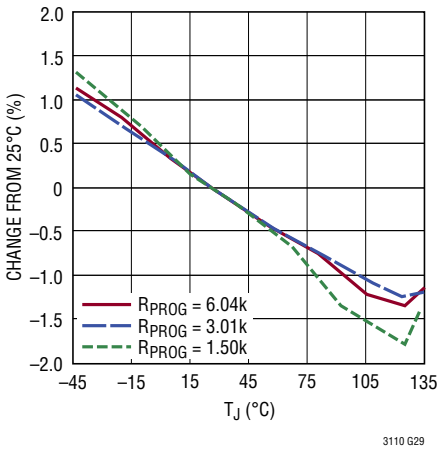


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

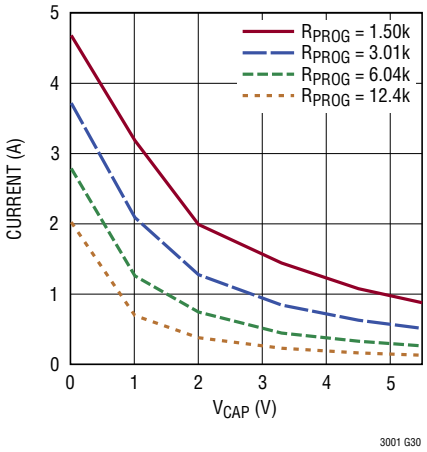
I_{VSYS} Input Current vs V_{CAP}



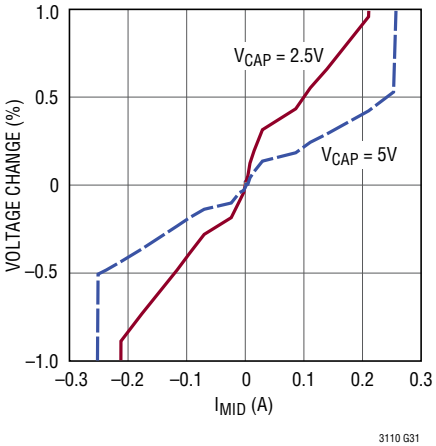
PROG Current Gain vs Temperature



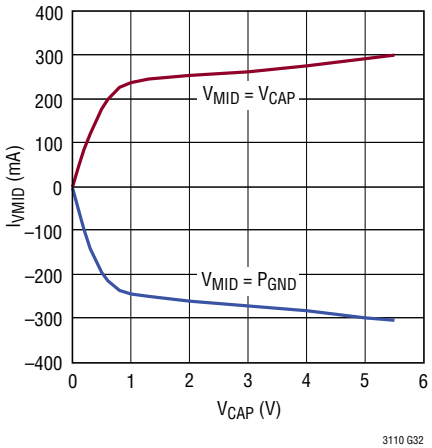
I_{VCAP} Charge Current vs V_{CAP}



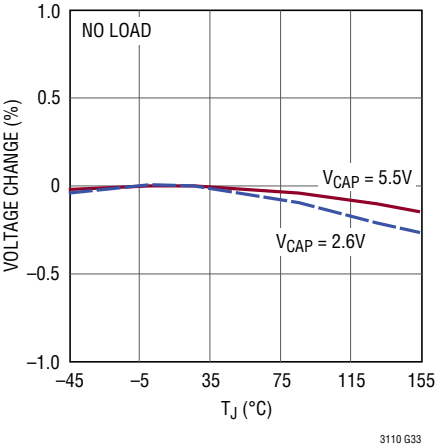
V_{MID} Load Regulation



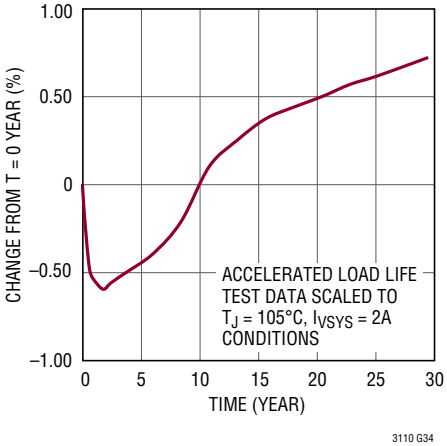
V_{MID} Buffer Current vs V_{CAP}



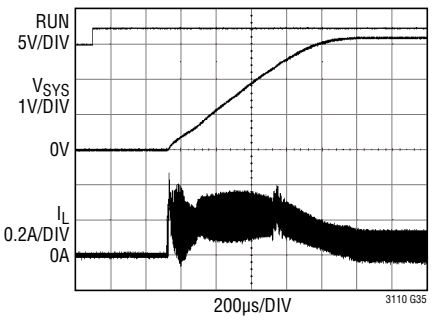
V_{MID} vs Temperature



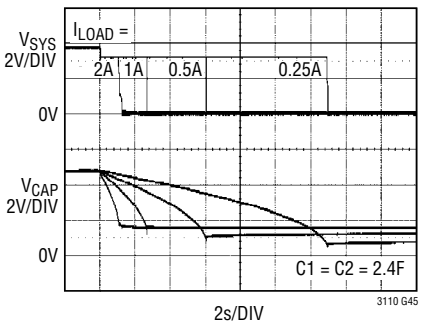
Input Current Limit Aging



Backup Soft-Start

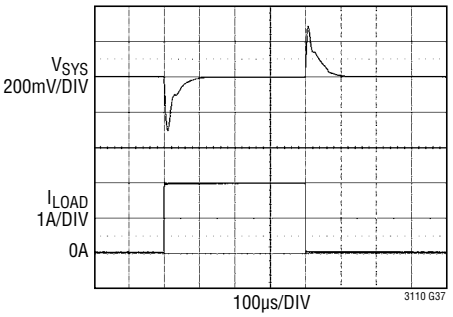


Backup Time

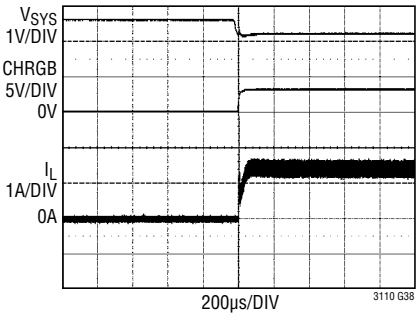


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

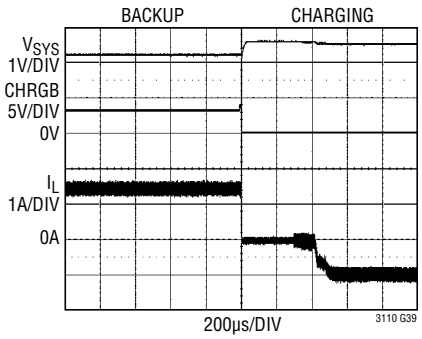
Load Step 0A to 2A



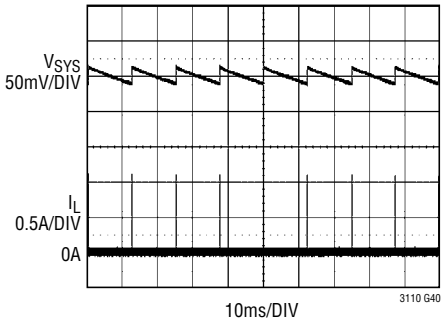
Charge Sleep to Backup Transient in Autonomous Application



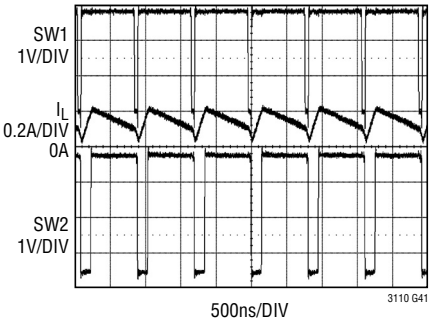
Backup to Charge Transient in Autonomous Application



Burst Mode Operation

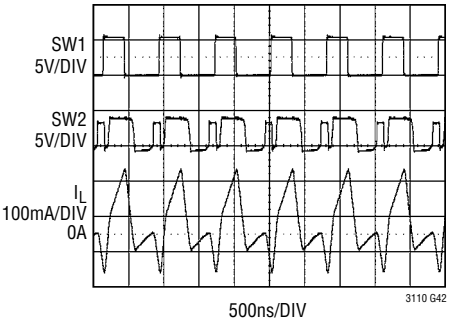


PWM Mode Operation



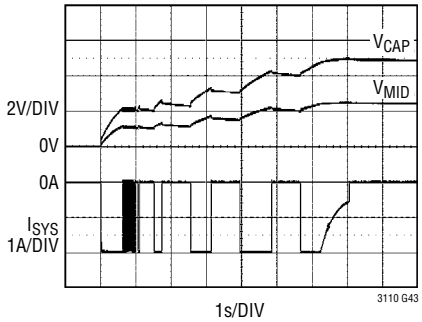
I_{SYS} = 100mA

PWM Mode Operation in V_{CAP} Overvoltage Failure Condition

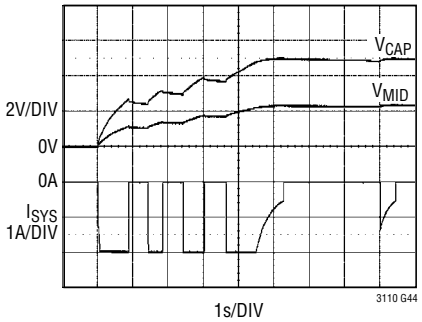


FB_{VCAP} = 1.2V
V_{DIR} = 0V

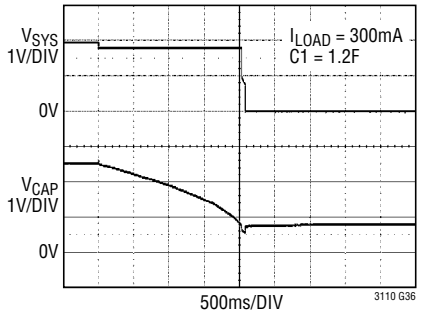
Charge Balancer Operation C1 > C2



Charge Balancer Operation C1 < C2



Single Capacitor Backup



PIN FUNCTIONS (FE/UFD)

CAPOK (Pin 1/Pin 22): V_{CAP} Voltage OK Indicator Output. The open-drain output is pulled low if the FBV_{CAP} voltage is lower than the FBV_{CAP} falling threshold. The output is released if FBV_{CAP} is higher than the rising threshold.

$\overline{\text{CMPOUT}}$ (Pin 2/Pin 23): General Purpose Comparator Output. The open-drain output is pulled low while the CMPIN pin voltage is above the comparator rising threshold. The output is released when CMPIN is below the falling threshold.

MODE (Pin 3/Pin 24): Burst/PWM Mode Selection Input. Driving MODE to a logic 1 state programs fixed frequency, low noise PWM operation. Driving MODE low programs Burst Mode operation. Note that the MODE pin has no effect when operating in charger mode.

CMPIN (Pin 4/Pin 1): General Purpose Comparator Positive Input with Hysteresis. The voltage at CMPIN is compared to an internal reference voltage. The pin can be driven digitally or configured as voltage supervisor with the help of an external resistor divider. If driven from a resistor divider or from a source with >200Ω impedance, connect a 0.1µF capacitor between CMPIN and GND for best performance. The CMPIN rising threshold is 0.65V and the falling threshold is 0.59V.

FBV_{CAP} (Pin 5/Pin 2): V_{CAP} End-Of-Charge Voltage Programming Feedback Divider Input with Hysteresis. The end-of-charge threshold can be adjusted from 1.1V to 5.5V. The FBV_{CAP} rising threshold is 1.095V and falling threshold is 1.061V.

SGND (Pin 6/Pin 3): Signal Ground Connection. A ground plane is highly recommended. Sensitive analog components terminated at ground should connect to the SGND pin with a Kelvin connection, separated from the high current path in PGND.

DIR (Pin 7/Pin 4): Charge/Backup Mode Selector Input with Hysteresis. A voltage on DIR above the rising threshold enables the LTC3110 charger mode. A voltage below the falling threshold enables the backup mode. The pin can be driven digitally, e.g., from a µC. With the help of an external resistor divider the pin can be configured as voltage supervisor input monitoring any system voltage. The DIR rising threshold is 1.095V and the falling threshold is 1.045V.

RUN (Pin 8/Pin 5): Logic-Controlled Shutdown Input.

RUN ≥ 1.0V: Normal Operation

RUN ≤ 0.3V: Shutdown

FB (Pin 9/Pin 6): V_{SYS} Backup Voltage Feedback Pin. Connect resistor divider tap here. The V_{SYS} voltage can be adjusted from 1.8V to 5.25V. The feedback reference voltage is 0.6V.

PROG (Pin 10/Pin 7): Charger Input Current (I_{VSYS}) Programming Resistor. A resistor from PROG to SGND programs the average current flowing in V_{SYS} when operating in charging mode.

$$R_{PROG} = \frac{3k\Omega \bullet A}{I_{VSYS}} \text{ for } 1.5k\Omega < R_{PROG} < 24.3k\Omega$$

R_{PROG} can be increased to 48.7k if the charge current foldback is avoided with FBV_{CAP} held down < 1V or grounded.

PIN FUNCTIONS (FE/UFD)

$\overline{CHRG}$ (Pin 11/Pin 8): Charge/Backup Mode Indicator Output. The open-drain output is pulled low while the regulator is in charge mode. The open-drain output is released while the regulator is in backup mode.

SV_{SYS} (Pin 12/Pin 9): Signal Supply Voltage Input for Buck/Boost Controller Circuitry. Pin must be shorted to V_{SYS} or supplied from V_{SYS} through a RC filter. See the Applications Information section for details.

V_{SYS} (Pins 13, 15/Pins 10, 12): Bidirectional Power Supply Pin for System Backup Output Voltage and Charge Current Input Voltage. A bypass capacitor must be connected between V_{SYS} and PGND. Refer to the Typical Applications schematics and the Applications Information section for capacitor selection details.

R_{SEN} (Pin 14/Pin 11): Current Sense Resistor Tap at Junction of Internal Sense Resistor and Switch D. Pin R_{SEN} is internally shorted to pin V_{SYS} via low impedance. DC current in R_{SEN} must be limited to 1.6A.

SW2 (Pins 16, 17/Pin 13, 14): Switch Pin Connected to Internal Switches C and D of the Buck-Boost Regulator. Connect one side of the buck-boost inductor to SW2. Provide a short wide PCB trace from the inductor to SW2 to minimize voltage transients and noise.

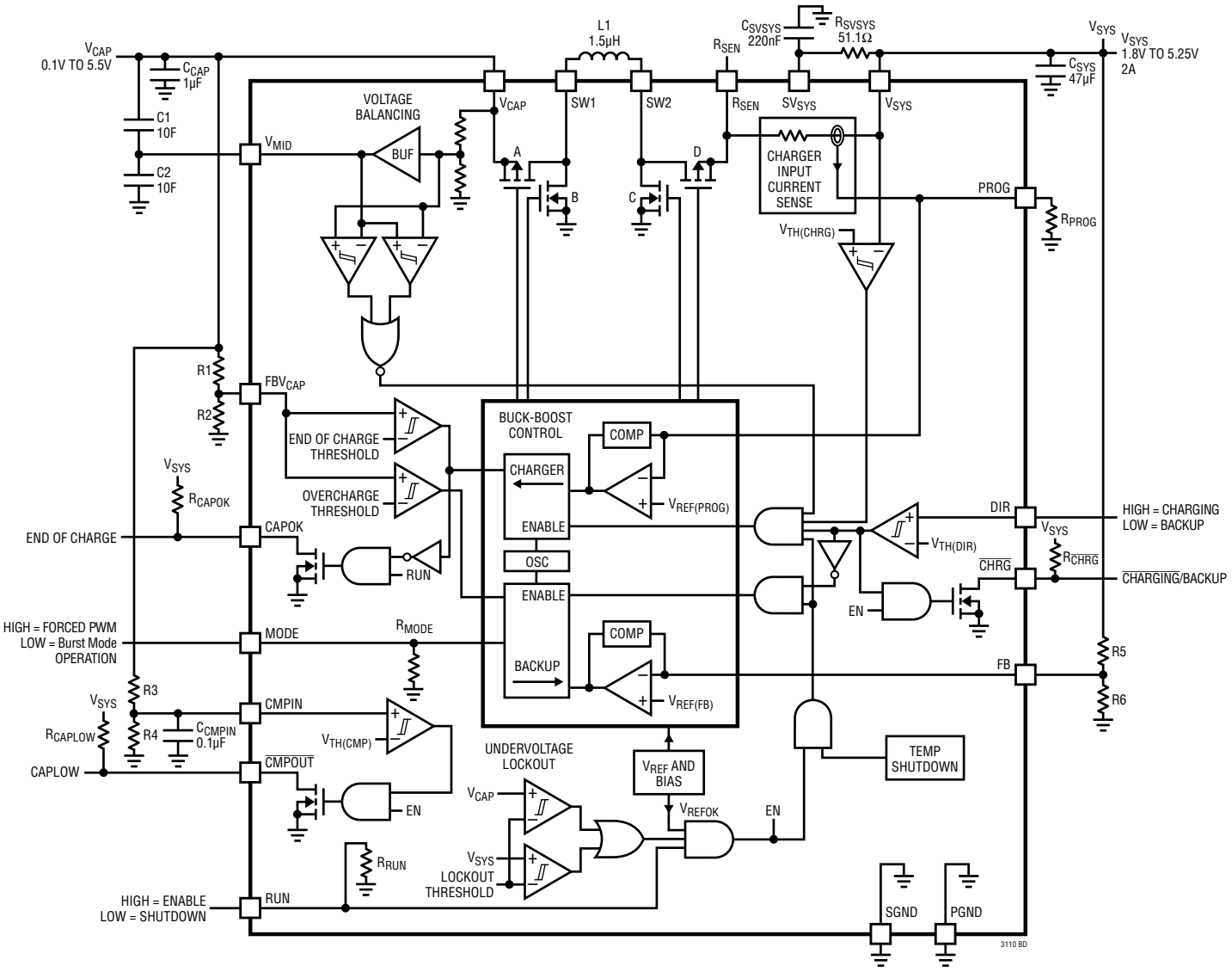
PGND (Pins 18, 19, Exposed Pad Pin 25/Pins 15, 16, Exposed Pad Pin 25): Power Ground Connection. Terminate all high current ground paths to PGND. The exposed pad must be soldered to the PCB ground for rated thermal performance.

SW1 (Pins 20, 21/Pins 17, 18): Switch Pin Connected to Internal Switches A and B of the Buck-Boost Regulator. Connect one side of the buck-boost inductor to SW1. Provide a short wide PCB trace from the inductor to SW1 to minimize voltage transients and noise.

V_{CAP} (Pins 22, 23/Pins 19, 20): Bidirectional Power Pin for Connection to Supercap Backup Capacitor(s) or Backup Battery(ies). When in charge mode a current flows out of pin V_{CAP} to charge the storage elements connected between V_{CAP} and PGND. When in backup mode the current is flowing into pin V_{CAP} and the stored energy is used to backup the load on V_{SYS}.

V_{MID} (Pin 24/Pin 21): Active Voltage Balancing Power Output. This pin should be tied to the junction of two series supercapacitors. If the output is not used, a compensation capacitor of 1nF must be connected between pins V_{MID} and PGND.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3110 is a monolithic buck-boost DC/DC regulator/charger combination with pin-selectable operation modes to utilize a single LTC3110 device for charging (V_{DIR} = high) as well as for system backup (V_{DIR} = low). During charging a limit for the average current drawn from the system power source can be accurately programmed with an external resistor. An integrated, active, voltage balancing buffer at pin V_{MID} prevents capacitor overvoltage conditions caused from capacitor mismatch while charging a stack of supercapacitors.

The buck-boost regulator utilizes a proprietary switching algorithm which allows the system voltage, V_{SYS}, to be regulated above, below, or equal to the voltage on the storage element, V_{CAP}, without discontinuity in inductor current or large voltage ripple in the backup voltage V_{SYS}.

With the DIR pin direction control circuitry, the LTC3110 can instantly reverse the inductor current and change between charging and backup operation modes, reacting quickly on a power failure condition by providing the backup voltage to the system (see Figure 1).

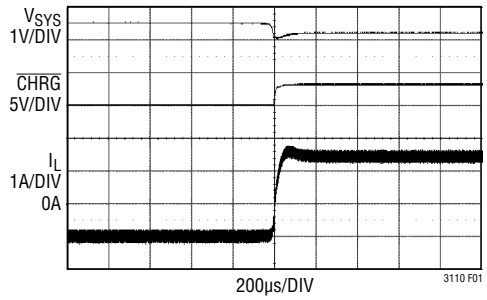


Figure 1. Transition from Charge⁻ into Backup Operation

The LTC3110 has been optimized to reduce quiescent current in shutdown and standby for applications that are sensitive to quiescent current drawn from the system voltage, V_{SYS}, or the storage element, V_{CAP}. In charge operation the standby current is only 40µA. In backup/Burst Mode operation, the no-load standby current is only 40µA. In shutdown the total supply current is reduced to less than 1µA.

Charging

When powered from the system voltage, V_{SYS}, the buck-boost regulator is usually set to operate in charge mode (V_{DIR} = high), that is, a voltage source connected to V_{SYS} is the power input into the LTC3110 and the converter charges a backup storage element connected between the V_{CAP} and PGND pins. When operating in charge mode, the LTC3110's average current limit circuitry is active. With a resistor between the PROG and SGND pins, the maximum average current drawn from V_{SYS} can be programmed to accurately limit the current demand.

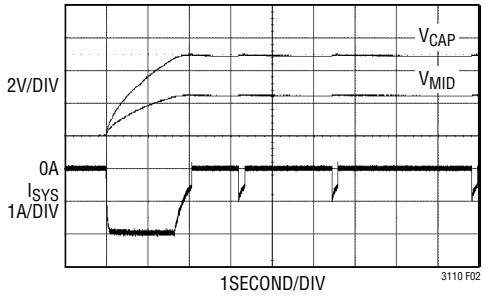


Figure 2. Charge Foldback and Charge Termination

Active Charge Balancer

While charging, the integrated linear charge balancing buffer regulates the mid-voltage, V_{MID}, of a stack of capacitors to half of V_{CAP} thus equalizing out voltage mismatches of top and bottom capacitor, see Figure 3. If the capacitor mismatch is exceeding the current capabilities of the charge balancer, charging is suspended until V_{MID} comes back to half of V_{CAP} (see charging waveforms in the Typical Performance Characteristics section). Note, the suspend charge function is only active for V_{CAP} > 2.2V = $V_{TH(CHRG)}$ with hysteresis. For V_{CAP} < 2V the charger operation is always continuous.

OPERATION

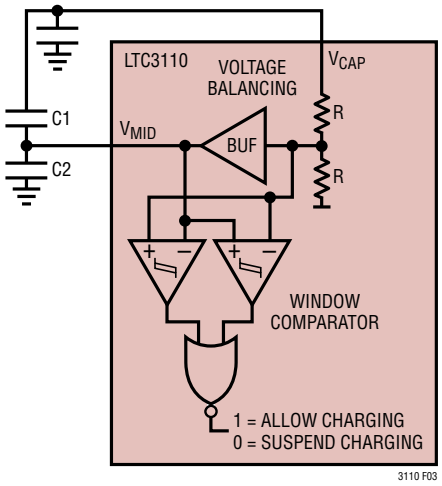


Figure 3. Active Charge Balancer

Charge Termination

The final charge voltage at pin V_{CAP} is programmed with a resistor divider at FBV_{CAP}, see Figure 10 in the Application Information Section.

If FBV_{CAP} exceeds typically 95% of its end of charge threshold, the PROG reference voltage and with it the charge current level begins to fold back (see Figure 2). Before charge termination the charge current is eventually folded back to a level of typically 30% of the programmed value (see charging waveforms in the Typical Performance Characteristic section). When the programmed voltage level is reached, the controller will terminate charging and switch off into a low quiescent current state wherein the charge balancer at the V_{MID} pin is disabled and the CAPOK pin is released. The low current state is maintained until the voltage on V_{CAP} decays and the FBV_{CAP} falling threshold is crossed. After this, controller and charge balancer will resume operation with the CAPOK pin pulled low until the regulation voltage is reached again. Note the IC cannot prevent outside sources leaking current into the capacitors from overvoltaging them.

Backup Operation in Fixed Frequency PWM Mode

With the MODE pin held high while V_{DIR} = low, the LTC3110 operates in a fixed-frequency pulse-width modulation (PWM) mode using a voltage mode control loop. This mode of operation maximizes the V_{SYS} backup current that can be delivered by the converter, reduces V_{SYS} voltage ripple, and yields a low noise fixed-frequency switching spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor current ripple, and loop transfer function throughout all regions of operation. These advantages result in increased efficiency, improved loop stability, and lower V_{SYS} voltage ripple in comparison to the traditional 4-switch buck-boost converter.

Figure 4 shows the topology of the LTC3110 power stage which is comprised of two P-channel MOSFET switches and two N-channel MOSFET switches and their associated gate drivers. In response to the error amplifier output, an internal pulse-width modulator generates the appropriate switch duty cycles to maintain regulation of the V_{SYS} voltage.

When the V_{CAP} voltage is significantly greater than the V_{SYS} voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse-width modulated to produce the required duty cycle to support the V_{SYS} regulation voltage. As the V_{CAP} voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 90%, the switch pair AC begins turning on for a small fraction of the switching period. As the V_{SYS} voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. At this point, switch A remains on continuously while switch pair CD is pulse-width modulated to obtain the desired V_{SYS} voltage. At this point, the converter is operating solely in boost mode.

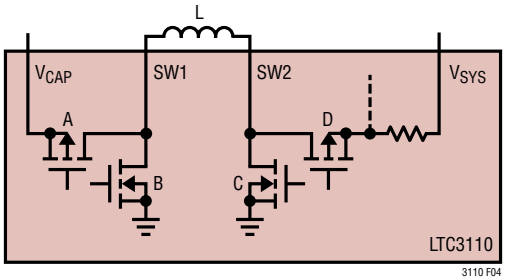


Figure 4. Buck-Boost Switch Topology

OPERATION

Backup in Burst Mode Operation

When MODE is held low while V_{DIR} = low, the buck-boost converter operates in Burst Mode operation using a variable frequency switching algorithm that minimizes the no-load input quiescent current and improves efficiency at light load by reducing the amount of switching to the minimum level required to support the load. The V_{SYS} current capability in Burst Mode operation is substantially lower than in PWM mode and is intended to support light stand-by loads. Curves showing the maximum Burst Mode load current as a function of the V_{CAP} and V_{SYS} voltage can be found in the Typical Performance Characteristics section of this data sheet. If the converter load in Burst Mode operation exceeds the maximum Burst Mode current capability, V_{SYS} will lose regulation. Each Burst Mode cycle is initiated when switches A and C turn on producing a linearly increasing current through the inductor. When the inductor current reaches the Burst Mode peak current limit, switches A and C are turned off and switches B and D are turned on, discharging the energy stored in the inductor into the V_{SYS} capacitor and load. Once the inductor current reaches zero, all switches are turned off and the cycle is complete. Current pulses generated in this manner are repeated as often as necessary to maintain regulation of the V_{SYS} voltage.

V_{CAP} Peak and DC-Current Limits (Backup Mode)

The LTC3110 has two current limit circuits that are designed to limit the peak inductor current to ensure that the switch currents remain within the capabilities of the IC during output short-circuit or overload conditions. First current limit: In PWM mode the V_{CAP} DC current limit operates by injecting a current into the feedback pin (FB). For this current limit feature being most effective, the Thevenin resistance (R_{BOT}//R_{TOP}) from FB to ground should exceed 100kΩ.

On a hard V_{SYS} short, with Burst Mode operation or PWM mode selected, it is possible for the inductor current to increase substantially beyond the DC current limit threshold. In this case the peak current, second current limit, turns off the power switch until the start of the next switching cycle.

Reverse Current Limit (Backup Mode)

In PWM mode operation the LTC3110 has the ability to actively conduct current away from V_{SYS} if it is necessary to maintain regulation. If V_{SYS} is held above the regulation voltage, it could result in large reverse currents. This situation can occur if V_{SYS} of the LTC3110 is held up by another supply. To prevent damage to the part in this condition, the LTC3110 has a reverse current comparator that monitors the current entering power switch D from the load. If this current exceeds 1.2A (typical), switch D is turned off for the remainder of the switching cycle. For a no-load current application, the inductor current ripple must be lower than double the minimum reverse current limit (1A • 2 = 2A maximum inductor current ripple). See the Inductor Selection section for information about how to calculate the inductor current ripple.

Preventing V_{CAP} Overcharge Failure Due to Reverse DC Current (Backup Mode)

If during PWM backup operation (MODE = high and DIR = low), an external power supply or any second DC/DC regulator wrongly drives V_{SYS} higher than the programmed back-up voltage level, the LTC3110 will reverse its V_{SYS} current and simultaneously create reverse current flow charging V_{CAP}. If the wrong V_{SYS} voltage level is kept for a longer period of time, FB_{VAP} may exceed the overcharge threshold and the LTC3110 stops reverse charging.

Charging through reverse DC current while V_{DIR} is low is not indicated at pin $\overline{CHRG}$, which remains high impedance.

The overcharge condition is generally prevented in the application by setting the LTC3110 into charge operation, if V_{SYS} is driven from an external source.

If the external source is supervised from the DIR comparator, the $\overline{CHRG}$ output can drive the gate of a PMOS and isolate the external source in backup operation, see applications with PFET on pages 29, 30, 31.

If V_{SYS} is supervised from the DIR comparator, the external source must be capable to deliver more than the maximum reverse current limit of the LTC3110 in backup direction, see autonomous application on page 36. Only if the external supply is strong enough, charge operation can be initiated reliably.

OPERATION

FB_{VCAP} Failure Condition

External component failures, e. g., open or shorted resistors or leakage currents at pin FBV_{CAP}, can cause V_{CAP} to charge up to a higher, undefined voltage. If V_{CAP} exceeds typically 5.95V, the LTC3110 suspends charging which protects the LTC3110 from substantially exceeding the absolute maximum ratings if FBV_{CAP} is shorted to ground.

Note supercapacitors and batteries often have a lower maximum voltage rating than 5.95V. In these cases the general purpose comparator can be configured to detect the overvoltage at V_{CAP} (see the figure General Purpose Comparator as redundant V_{CAP} supervisor in the Application Information section).

Soft-Start (Backup Mode)

To minimize V_{CAP} current transients on power-up, the LTC3110 incorporates an internal soft-start circuit. The soft-start is implemented by a linearly increasing ramp of the error amplifier reference voltage during the soft-start duration. During the soft-start period the regulator is always operating in PWM operation independent of the MODE pin setting. In case the V_{SYS} voltage at start-up is already pre-charged above 80% of the target value, the soft-start is skipped and the LTC3110 immediately enters the mode of operation that has been set with the MODE pin. The soft-start period is reset by thermal shutdown and from undervoltage lockout events.

Error Amplifier and Internal Compensation of V_{SYS} Backup Voltage Regulation

The buck-boost converter utilizes a voltage mode error amplifier with an internal compensation network.

Error Amplifier and Internal Compensation of V_{SYS} Average Current Limit Regulation

The buck-boost converter in charge mode (DIR = high) utilizes an error amplifier with an internal compensation network to regulate the average current flowing into the V_{SYS} pin. The current limit is programmable with R_{PROG}.

R_{SEN} Current Sense Resistor Tap

R_{SEN} connects to the junction of FET D and the integrated sense resistor.

The R_{SEN} pin can be left unconnected, otherwise a load current, I_{RSEN}, will simultaneously decrease the average charge current flowing out of the V_{CAP} pin. Note: A fast voltage step at V_{SYS} in the presence of a large R_{SEN} capacitor causes a large inrush current through the internal R_{SEN} resistor, e. g., closure of a mechanical power connection supplying V_{SYS}. In these cases, the value of the capacitor between R_{SEN} and ground is limited to a maximum of 10µF.

V_{CAPOK} End-Of-Charge Indicator and FBV_{CAP} Comparator

The LTC3110 includes an open-drain comparator output pin, V_{CAPOK}, which is used to indicate the charging state of the energy storage element.

The comparator input, FBV_{CAP}, is typically connected with a resistor divider from V_{CAP} to ground in order to program the final charge voltage. When FBV_{CAP} exceeds the rising threshold, the comparator output, V_{CAPOK}, is high impedance. When FBV_{CAP} drops below the falling threshold, V_{CAPOK} is pulled to ground. While RUN = high, CAPOK continues to pull down with reduced strength until both V_{CAP} and V_{SYS} are below the threshold of the internal pull-down transistor, maximum 1.4V.

The comparator operates in both charge and backup mode and is unconditionally released if the LTC3110 is shut down with RUN = low.

$\overline{CHRG}$ Operation Mode Indicator and DIR Comparator

The LTC3110 includes an open-drain DIR comparator output pin, $\overline{CHRG}$, which is typically used to indicate the operation mode of the chip: charge or backup. With the help of a pull-up resistor the output can be used to interface with a microcontroller, or connect to the gate of a p-channel MOSFET used as an input isolation switch (see USB application in the Typical Application section).

The DIR comparator has hysteresis and the $\overline{CHRG}$ pin is pulled low while V_{DIR} is greater than the comparator rising threshold and $\overline{CHRG}$ is released while V_{DIR} is lower than its falling threshold.

OPERATION

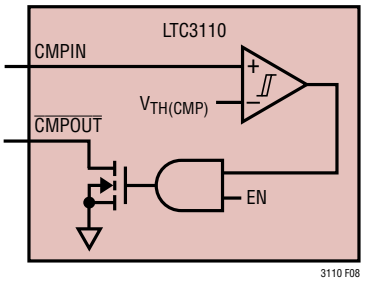


Figure 5. General Purpose Comparator

The $\overline{CHRG}$ pin is unconditionally released if the LTC3110 is shut down with RUN = low or in undervoltage condition. Note that the DIR pin can be driven above V_{CAP} or V_{SYS}, as long as the voltage is limited to less than the absolute maximum rating.

General Purpose Comparator

The LTC3110 includes a voltage comparator with its input accessible at the CMPIN pin and with a fixed internal reference voltage.

The comparator can be used to monitor V_{CAP}, V_{SYS} or any auxiliary supply voltage. The open-drain output, $\overline{CMPOUT}$, can interface to a microcontroller with the help of a pull-up resistor. The comparator is typically used to supervise V_{CAP} and to set a threshold for the lowest V_{CAP} voltage tolerated in backup mode before the system needs to reduce power consumption. The $\overline{CMPOUT}$ pin is unconditionally released if the LTC3110 is shut down with RUN = low or in undervoltage condition (see also the Applications Information section).

Shutdown

Shutdown of the LTC3110 is accomplished by pulling the RUN pin below 0.3V and IC operation is enabled by pulling the RUN pin above 1.0V. The RUN pin has an internal pull-down resistor. Note that RUN can be driven above V_{CAP} or V_{SYS}, as long as the voltage is limited to less than the absolute maximum rating.

Thermal Foldback of Charge Current

To help preventing the LTC3110 from going into thermal shutdown when charging very large capacitors, the LTC3110 is equipped with a thermal regulator. If the die temperature exceeds 130°C (typical) the average V_{SYS} current limit is lowered to help reduce the amount of power being dissipated in the package. The current limit is reduced to approximately 15% of the programmed limit just before thermal shutdown. The current limit will return to its full value when the die temperature drops below 130°C, typically.

Undervoltage Lockout

If either voltages at V_{CAP} and V_{SYS} drop below the undervoltage lockout falling threshold, the LTC3110 will stop operation and the SW1, SW2, V_{MID}, $\overline{CMPOUT}$, $\overline{CHRG}$ and PROG pins will be high impedance. CAPOK will continue to pull down with reduced strength until both V_{CAP} and V_{SYS} are below the threshold of the internal pull-down transistor, maximum 1.4V. The LTC3110 will resume operation when at least one pin, V_{CAP} or V_{SYS}, rises above the undervoltage lockout rising threshold.

THERMAL CONSIDERATIONS

The power switches in the LTC3110 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels there may be significant heat generated within the IC. As a result, careful consideration must be given to the thermal environment of the IC in order to optimize efficiency and ensure that the LTC3110 is able to provide its full-rated output current. Specifically, the exposed pad of both the QFN and TSSOP packages shall be soldered to the PC board and the PC board should be designed to maximize the conduction of heat out of the IC package. If the die temperature exceeds approximately 165°C, the IC will enter overtemperature shutdown, all switching will be inhibited and the charge balancer disabled. Note: Open-drain output pins CAPOK, $\overline{CMPOUT}$ and $\overline{CHRG}$ may still pull down while in thermal shutdown. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is reinitialized in overtemperature shutdown to provide a smooth recovery when the fault condition is removed.

APPLICATIONS INFORMATION

The standard LTC3110 application circuit is shown as the Typical Application on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, cost, V_{SYS} and V_{CAP} voltage, allowable ripple voltage, efficiency and thermal considerations. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

Inductor Selection

The choice of inductor used in LTC3110 application circuits influences the maximum deliverable backup and charge current, the magnitude of the inductor current ripple, and the power conversion efficiency. The inductor must have low DC series resistance or current capability and efficiency will be compromised. Larger inductance values reduce inductor current ripple and will therefore generally yield greater backup current capability. For a fixed DC resistance, a larger value of inductance will yield higher efficiency by reducing the peak current to be closer to the average backup current and therefore minimize resistive losses due to high RMS currents. However, a larger inductor within any given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage. An inductor used in LTC3110 applications should have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula:

$$\Delta I_{L(P\text{-}P)(BUCK)} = \frac{V_{SYS}}{1.2MHz \bullet L}\left(\frac{V_{CAP} - V_{SYS}}{V_{CAP}}\right)$$

$$\Delta I_{L(P\text{-}P)(BOOST)} = \frac{V_{CAP}}{1.2MHz \bullet L}\left(\frac{V_{SYS} - V_{CAP}}{V_{SYS}}\right)$$

L is the inductance in µH.

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output capability of the buck-boost converter particularly at low V_{CAP} voltages. In buck mode, the output current of the buck-boost converter is limited only by the inductor current reaching the current limit threshold. However, in boost mode, especially at large step-up ratios, the V_{SYS} backup current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance and PCB trace resistance. Use of an inductor with high DC resistance can degrade the V_{SYS} backup current capability from that shown in the Typical Performance Characteristics section of this data sheet. As a guideline, in most applications the inductor DC resistance should be significantly smaller than the typical power switch resistance of 60mΩ.

The minimum inductor value must guarantee that the worst-case average V_{CAP} current plus half the ripple current doesn't reach the V_{CAP} current limit threshold. For the fixed switching frequency of 1.2MHz the recommended typical inductor value is 1.5µH.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3110 applications.

Table 1. Recommended Inductors

VENDOR	PART/STYLE
Coilcraft www.coilcraft.com	XAL50xx Series (XAL5030-222ME_) XAL60xx Series (XAL6030-222ME_) EPL7040 Series (EPL7040-222ME_)
Würth Elektronik www.we-online.com	WE-HCI Series (744310150, 744314200) WE-LHMI Series (74437346018, 74437349022)
Coiltronics www. cooperindustries.com	DR73 Series (DR73-2R2-R) DRQ74 Series (DR74-2R2-R)
Vishay www.vishay.com	IHLP-2525 Series (IHLP-2525AH-01, IHLP-2525CZ-01) IHLP-2020 Series (IHLP-2020CZ-A1)
Sumida www.sumida.com	CDEP6D31ME Series (CDEP6D31MENP-2R2MC)
Murata www.murata.com	LQH66S Series (LQH66SN1R5M03)
Taiyo Yuden www.t-yuden.com	NR6012T2R5NE NR8040T2R0N
TDK www.component.tdk.com	CLF Series

APPLICATIONS INFORMATION

V_{SYS} Capacitor Selection

A low ESR capacitor should be utilized at the V_{SYS} pin in order to minimize V_{SYS} backup voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the V_{SYS} voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak V_{SYS} voltage ripple can be calculated by the following formulas, where C_{VSYS} is the V_{SYS} capacitance and I_{LOAD} is the V_{SYS} load current.

$$\Delta V_{P-P(BUCK)} = \frac{V_{SYS}}{8 \bullet (1.2MHz)^2 \bullet L \bullet C_{VSYS}} \left(\frac{V_{CAP} - V_{SYS}}{V_{CAP}} \right)$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{1.2MHz \bullet C_{VSYS}} \left(\frac{V_{SYS} - V_{CAP}}{V_{SYS}} \right)$$

Given the V_{SYS} current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. In addition to V_{SYS} voltage ripple generated across the V_{SYS} capacitance, there is also V_{SYS} voltage ripple produced across the internal resistance of the V_{SYS} capacitor. The ESR-generated V_{SYS} voltage ripple is proportional to the series resistance of the V_{SYS} capacitor.

Supercapacitor Selection and Additional Bypass

The LTC3110 is stable with a total C_{VCAP} capacitance value greater than 2mF, or 4mF for each stacked capacitor. Supercapacitors are much larger physically than ceramic or tantalum capacitors, and therefore usually cannot be placed close to the charger. To minimize layout contribution to capacitor ESR, the trace width connecting the capacitors to each other and the IC should be as large as possible. The V_{MID} pin trace is not as critical, as it only carries 300mA of average current. It is recommended that a local decoupling capacitor be placed from V_{CAP} to ground, and the capacitor should be placed as close to the IC as possible. Multilayer ceramic capacitors are an excellent choice for voltage decoupling as they have extremely low ESR and are available in small footprints. While a 10µF decoupling capacitor is sufficient for most applications, larger values may be used without limitation.

To minimize voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of 100nF and a second low ESR bypass capacitor of 10µF should be located as close to the V_{CAP} pin as possible. The traces connecting this capacitor to V_{CAP} and the ground plane should be made as short as possible. If using a single V_{SYS} capacitor where balancing is not required, a capacitor of at least 1nF must be connected between V_{MID} and PGND.

Recommended V_{CAP} and V_{SYS} Bypass Capacitors

The choice of capacitor technology is primarily dictated by a trade-off between cost, size and leakage current. Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors designed for power applications experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose more than 50% of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating than required in order to actually realize the intended capacitance at the full operating voltage. To ensure that the intended capacitance is realized in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage. The capacitors listed in Table 3 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3110 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss over temperature is minimized.

Maximum Capacitor Voltage and Balancing

The service lifetime of a supercapacitor is determined by its rated voltage, rated temperature, rated lifetime, actual operating voltage, and operating temperature. To extend the life of a supercapacitor the operating voltage and temperature should be reduced from the maximum ratings. The websites for Illinois Capacitor[1] and Maxwell[2] provide the means to determine their capacitor lifetime.

[1] http://www.illinoiscapacitor.com/tech-center/life-calculators.aspx

[2] http://www.maxwell.com/products/ultracapacitors/docs/APPLICATIONNOTE1012839_1.PDF

APPLICATIONS INFORMATION

Using the suggested derated voltage for each capacitor will improve lifetime. The LTC3110 will keep each capacitor voltage at $V_{CAP}/2$ once V_{CAP} is higher than typically 2.2V. To prevent an overvoltage on one of the supercapacitors during charging, the V_{MID} voltage is continuously driven from the voltage balancing buffer output with typically 300mA of current capability.

The LTC3110 has minimal current draw from V_{CAP} at end of charge. Care should be taken to limit sources of current that may pull V_{CAP} above its programmed regulation value, as there is no way for the LTC3110 to maintain regulation.

V_{SYS} Voltage Programming

The V_{SYS} voltage is set via an external resistor divider connected to the FB pin as shown in Figure 6.

The resistor divider values determine the V_{SYS} backup voltage according to the following formula:

$$V_{SYS} = 0.6V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \quad (1)$$

The buck-boost converter utilizes voltage mode control and in addition to setting the V_{SYS} voltage, the value of R_{TOP} plays an integral role in the dynamics of the feedback loop. In general, a larger value for R_{TOP} will increase stability and reduce the speed of the transient response. A smaller value of R_{TOP} will reduce stability but increase the speed of the transient response. A good starting point is to choose R_{TOP} = 1M and then calculate the required value of R_{BOT} to set the desired V_{SYS} voltage according to Equation 1. If a large V_{SYS} capacitor is used, the bandwidth of the converter is reduced. In such cases R_{TOP} can be reduced to improve the transient response. If a large inductor or small V_{SYS} capacitor is utilized the loop will be less stable and the phase margin can be improved by increasing the value of R_{TOP}.

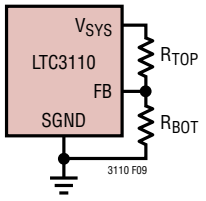


Figure 6. Setting the V_{SYS} Backup Voltage

V_{CAP} Voltage Programming

The V_{CAP} voltage is set via an external resistor divider connected to the FBV_{CAP} pin as shown in Figure 7.

The resistor divider values determine the maximum V_{CAP} voltage according to the following formula:

$$V_{CAP} = 1.095V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Care should be taken to limit sources of current that may pull V_{CAP} above its programmed maximum value, as there is no way for the LTC3110 to maintain V_{CAP} regulation in charger mode (see also Figure 15, Overvoltage Error Signal Provided to the µC).

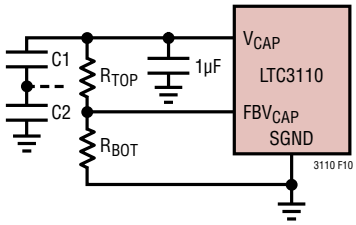


Figure 7. V_{CAP} Voltage Programming

V_{MID} Charge Balancer Output

This pin should be tied to the junction of two series supercapacitors. A push/pull buffer output forces the V_{MID} pin to half of the voltage of the V_{CAP} pin. Generally capacitors with equal value of at least 1nF should be connected from V_{CAP} to V_{MID} and from V_{MID} to PGND if the output is unused, e.g., for applications with a single supercapacitor or batteries.

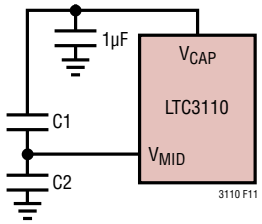


Figure 8. V_{MID} Charge Balancer Output

APPLICATIONS INFORMATION

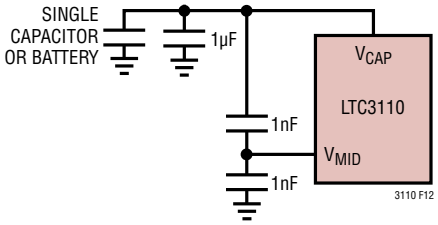


Figure 9. Charge Balancer Unused with Single Capacitor

DIR Backup Supervisor Threshold Voltage Programming

The backup supervisor threshold voltage is set via an external resistor divider connected to the DIR pin as shown in Figure 10.

The resistor divider values determine the DIR supervisor threshold voltage according to the following formula:

$$V_{TH(DIR\_RISING)} = 1.095V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

$$V_{TH(DIR\_FALLING)} = 1.045V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

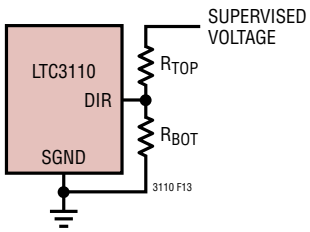


Figure 10. Setting the DIR Back-Up Supervisor Threshold Voltage

Programming Backup Voltage and DIR Threshold Voltage with Improved Accuracy

In applications with the DIR pin voltage and the FB pin voltage divided down from the same V_{SYS} voltage, a single resistor divider string is reducing the effect of resistor tolerances and saves one resistor component:

$$V_{TH(DIR\_RISING)} = 1.095V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT} + R_{MID}}\right)$$

$$V_{TH(DIR\_FALLING)} = 1.045V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT} + R_{MID}}\right)$$

$$V_{SYS} = 0.6V \bullet \left(1 + \frac{R_{TOP} + R_{MID}}{R_{BOT}}\right)$$

Note the direction supervisor threshold $V_{TH(DIR\_RISING)}$ must be higher and have enough voltage difference to the backup voltage V_{SYS} to accommodate for the resistor tolerances, ripple voltage and voltage dipping from load current steps. If necessary an RC filter in front of the DIR pin may reduce the reaction speed of the supervisor, see Figure 12.

Pay attention to the requirement, if the DIR input supervises V_{SYS} as in Figure 11 or in the autonomous applications on page 36, the external V_{SYS} supply must be capable to deliver more than the maximum reverse current limit of 2A of the LTC3110, in order to reliably change into charge operation.

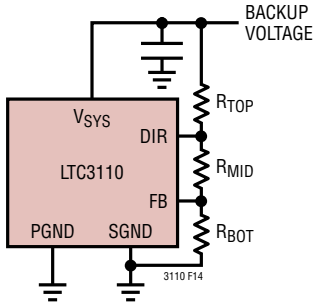


Figure 11. Voltage with Reduced Tolerances

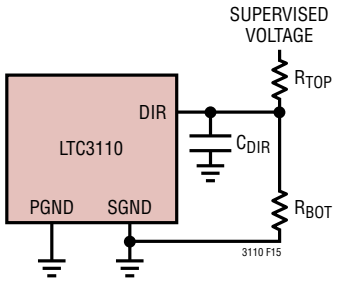


Figure 12. Filtering DIR voltage

APPLICATIONS INFORMATION

I_{VSYS} Average Current Limit Programming for Charger Operation (DIR = High)

The V_{SYS} average current limit is set via an external resistor connected between the PROG pin and signal ground, SGND, as shown in Figure 13.

The resistor value determines the average current into V_{SYS} according to the following formula:

$$I_{VSYS} = \frac{3k\Omega}{R_{PROG}}$$

For applications with a wide temperature range, the thermal coefficient of resistor R_{PROG} must be taken into account. If R_{PROG} is > 12.4k, additional R_{FLT} and C_{FLT} are required for filtering.

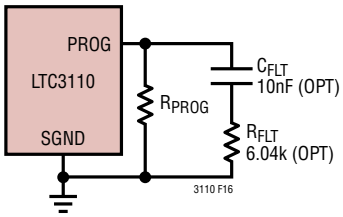


Figure 13. Setting the V_{SYS} Average Current Limit

CMPIN Configuration as General Purpose Voltage Supervisor with Hysteresis

The resistor divider values, see Figure 14, determine rising and falling threshold V_{TH} according to the following formula:

$$V_{TH(RISING)} = 0.65V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

$$V_{TH(FALLING)} = 0.59V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

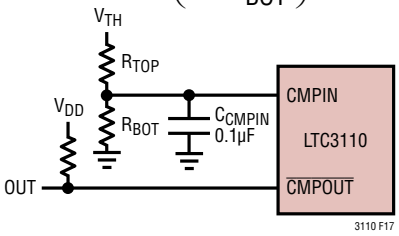


Figure 14. General Purpose Voltage Supervisor

If CMPIN is driven from a resistor divider or from any output with >200Ω impedance, connect a 0.1µF capacitor between CMPIN and GND for best performance, see Figure 14.

General Purpose Comparator Configuration as Redundant V_{CAP} Supervisor for Overvoltage Failure Detection

Component failures interrupting the V_{CAP} voltage feedback (FBV_{CAP}) can potentially cause an over voltage condition at V_{CAP} during charging. The general purpose comparator can be configured as the supervisor providing an overvoltage error signal to the microcontroller (see Figure 15).

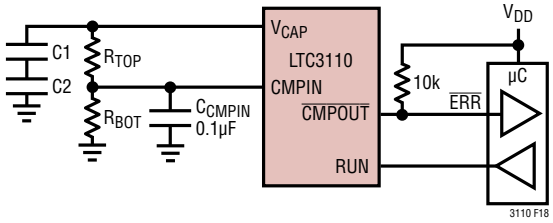


Figure 15. Overvoltage Error Signal Provided to the µC

SV_{SYS} Filtering

In many noise critical applications it is useful to filter the signal supply pin, SV_{SYS}, with a small RC filter on the PCB, see Figure 16. Note, if the filter is added any further loads connected to the SV_{SYS} pin must be checked if they are small with respect to the resistor impedance and not creating undesired voltage drops at SV_{SYS}.

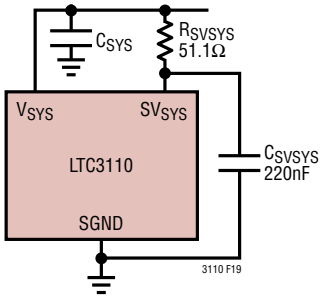


Figure 16. SV_{SYS} Filtering

RUN, DIR, MODE, CMPIN Inputs Digitally Controlled

The RUN, DIR, MODE and CMPIN comparator inputs can be driven digitally from an external microcontroller.

APPLICATIONS INFORMATION

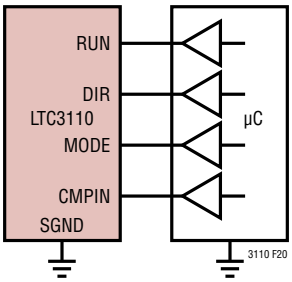


Figure 17. Inputs RUN, DIR, MODE, CMPIN Driven from a Microcontroller

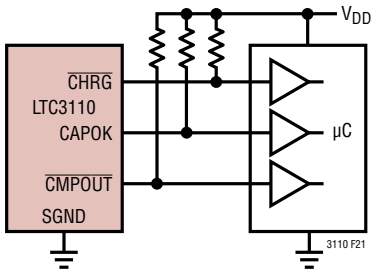


Figure 18. Outputs $\overline{\text{CHRG}}$, CAPOK, $\overline{\text{CMPOUT}}$ Interfacing to µC

Open-Collector Outputs

$\overline{\text{CHRG}}$, CAPOK and $\overline{\text{CMPOUT}}$ open-collector outputs can be connected together with other external signals in wired OR configuration and pull-up resistors for level shifting when interfacing into µC Inputs.

The open-collector outputs can also be used to drive small loads up to 20mA, e.g., miniature lamps or LEDs.

Table 2. Recommended Supercapacitors and Ultracapacitors

VENDOR	VALUE (F)	ESR (mΩ)	VOLTAGE (V)	TEMPERATURE RANGE (°C)	SIZE (mm) W × L × H
Murata Electronics					
DMF3R5R5L334M3DTA0	0.33	60	4.2 (5.5 Peak)	–30 to 70	14.0 × 21.0 × 2.5
DMF3Z5R5H474M3DTA0	0.47	40	4.2 (5.5 Peak)	–30 to 70	14.0 × 21.0 × 3.2
Tecate					
TPL-10/10X30F	10	85	2.7	–40 to 65	10.0 × 10.0 × 30.0
TPL-25/16X26F	25	42	2.7	–40 to 65	16.0 × 16.0 × 26.0
TPL-100/22X45F	100	15	2.7	–40 to 65	22.0 × 22.0 × 45.0
TPLE-25/16X26F	25	42	2.3	–40 to 85	16.0 × 16.0 × 26.0
TPLE-100/22X45F	100	15	2.3	–40 to 85	22.0 × 22.0 × 45.0
TPLS-400/35X60F	400	12	2.7	–40 to 65	35.0 × 35.0 × 60.0
AVX					
BZ015A503Z_B	0.05	160	5.5	–20 to 70	28.0 × 17.0 × 4.1
BZ015A104Z_B	0.1	80	5.5	–20 to 70	28.0 × 17.0 × 6.7
CAP-XX					
HS206F	0.6	70	5.5	–40 to 85	39.0 × 17.0 × 2.5
HS230	1.2	50	5.5	–40 to 85	39.0 × 17.0 × 3.8
Cooper Bussmann					
A1635-2R5475-R	4.7	25	2.5	–25 to 70	16.0 × 16.0 × 35.0
M1325-2R5905-R	9	20	2.5	–40 to 60	13.0 × 13.0 × 26.0
HB1625-2R5256-R	25	36	2.5	–25 to 70	16.0 × 16.0 × 25.0
HV1860-2R7107-R	100	10	2.7	–40 to 65	18.0 × 18.0 × 60.0
Illinois Capacitor					
506DER2R5SLZ	50	30	2.5	–40 to 70	18.0 × 18.0 × 60.0
357DER2R5SEZ	100	12	2.5	–40 to 70	35.0 × 35.0 × 60.0
Maxwell					
BCAP0005	5	170	2.7	–40 to 65	10.0 × 10.0 × 20.0
BCAP0100T01	100	15	2.7	–40 to 65	22.0 × 22.0 × 45.0
Taiyo Yuden					
PAS2026FR2R5504	0.5	55	2.5	–25 to 60	26.0 × 20.0 × 0.9
PAS0815LS2R5105	1	70	2.5	–25 to 70	8.0 × 8.0 × 15.0
LIC2540R3R8207	200	50	2.2 to 3.8	–25 to 70	25.0 × 25.0 × 40.0

APPLICATIONS INFORMATION

Table 3. Representative Bypass and V_{SYS} Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	FOOTPRINT
AVX			
12066D106K	10	6.3	0603
12066D226K	22	6.3	0805
12066D476K	47	6.3	0805
Kemet			
C0603C106M9PACTU	10	6.3	0603
C0805C226M9PACTU	22	6.3	0805
C0805C476M9PACTU	47	6.3	0805
Murata			
GRM188D70J106MA73	10	6.3	0603
GRM219B30J226ME47	22	6.3	0805
GRM21BB30J476ME15	47	6.3	0805
TDK			
C1608X7S0J106M080AC	10	6.3	0603
C2012X5R0J226M085AB	22	6.3	0805
C2012X5R0J476M125AC	47	6.3	0805
Taiyo Yuden			
JMK107BJ106MA	10	6.3	0603
JMK212ABJ226MD	22	6.3	0805
JMK212BBJ476MG	47	6.3	0805

PCB Layout Considerations

The LTC3110 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise-free operation. Figures 19 and 20 depict the recommended PCB layout to be utilized for the LTC3110, if a 2-layer PCB is being used. A 4-layer PCB layout is recommended for thermal and noise reasons. A few key guidelines follow:

1. All circulating high current paths should be kept as short as possible. This can be accomplished keeping the routes to the components in Figures 19 and 20 as short and as wide as possible. Capacitor ground connections should be connect by vias down to the ground plane in the shortest route possible. The bypass capacitors C_{SYS} and C_{CAP} should be placed as close to the IC as possible and should have the shortest possible path to ground.
2. The components shown and their connections should all be placed over a complete ground plane.
3. Use of vias in the die attach pad will enhance the thermal environment of the charger, especially if the vias extend to a ground plane region on the exposed bottom surface of the PCB.
4. Keep the connections to the FB, PROG, DIR, CMPIN and FBV_{CAP} pins as short as possible and away from the switch pin connections.

APPLICATIONS INFORMATION

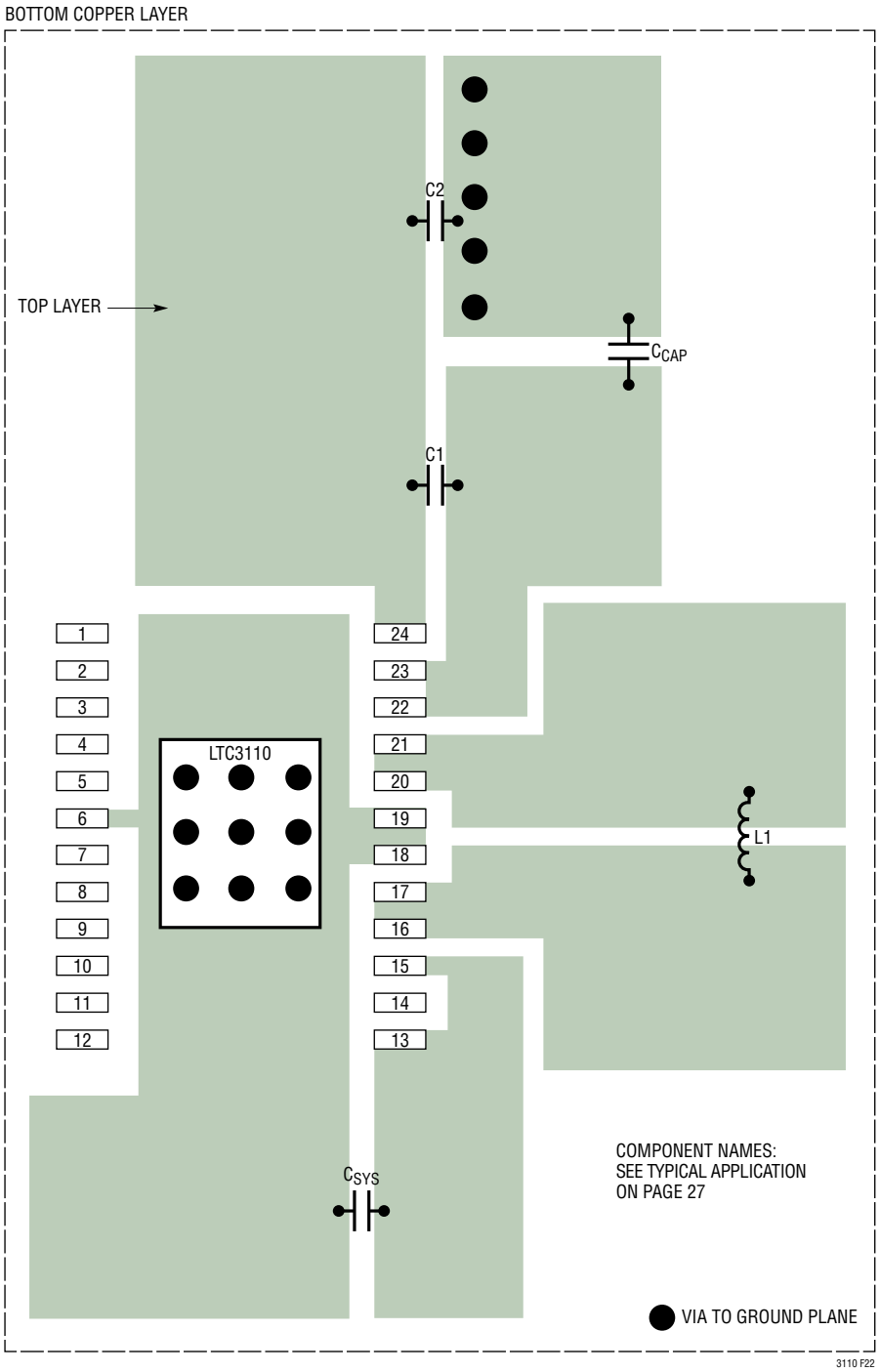


Figure 19. PCB Component Placement of the TSSOP Package

APPLICATIONS INFORMATION

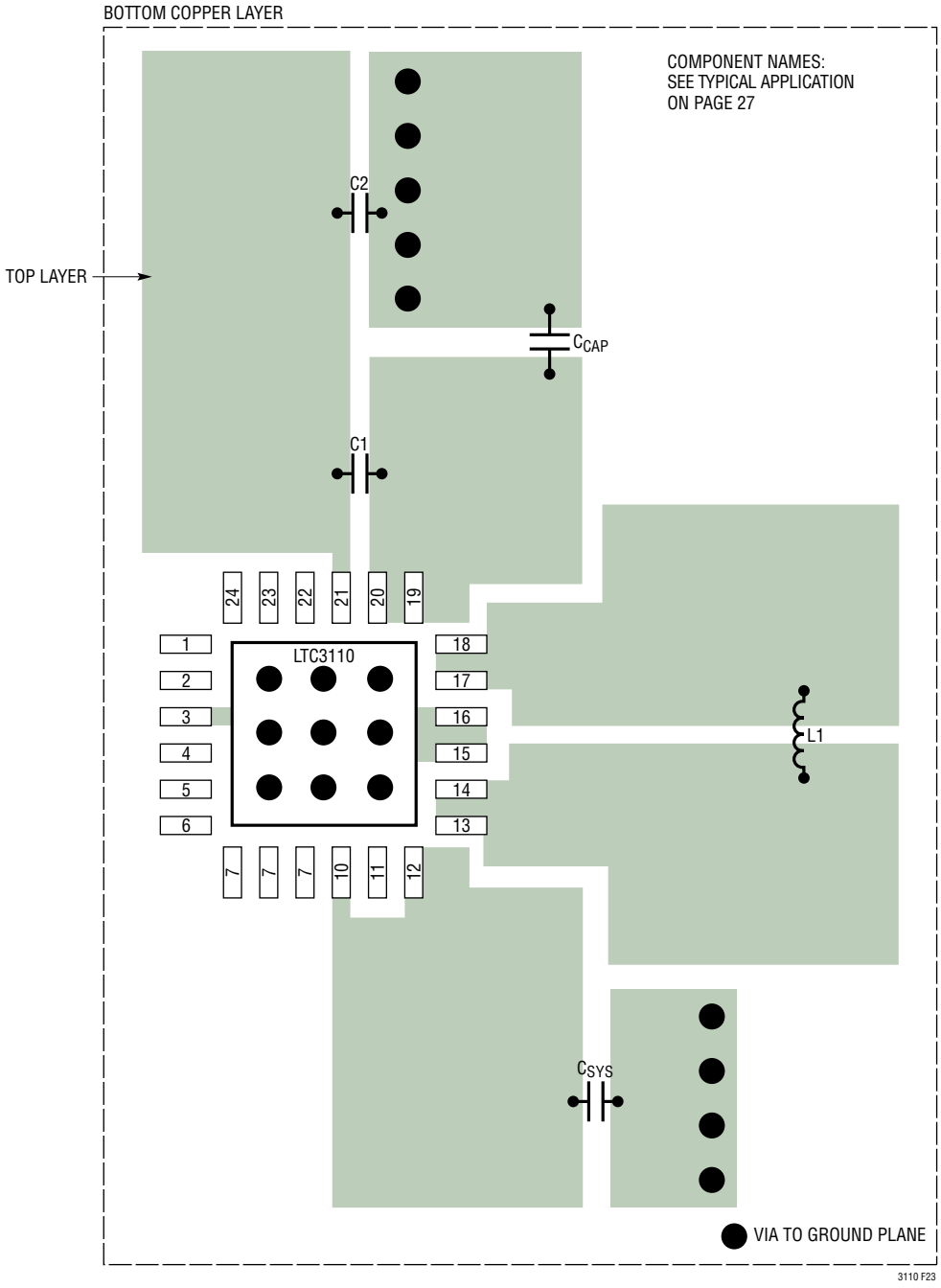
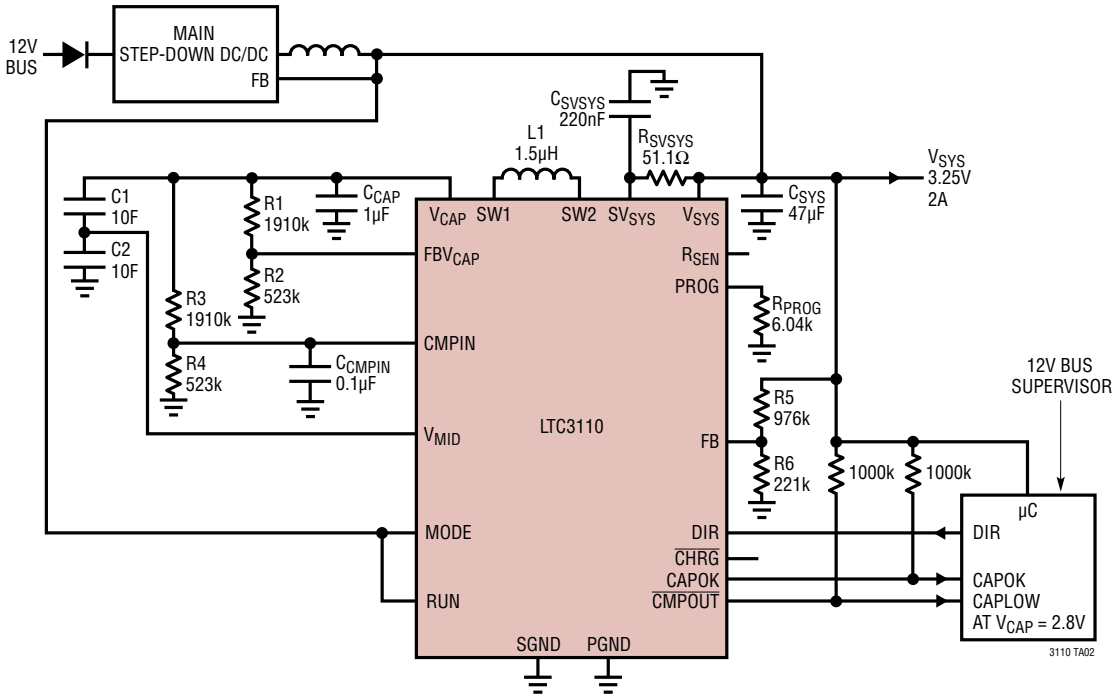


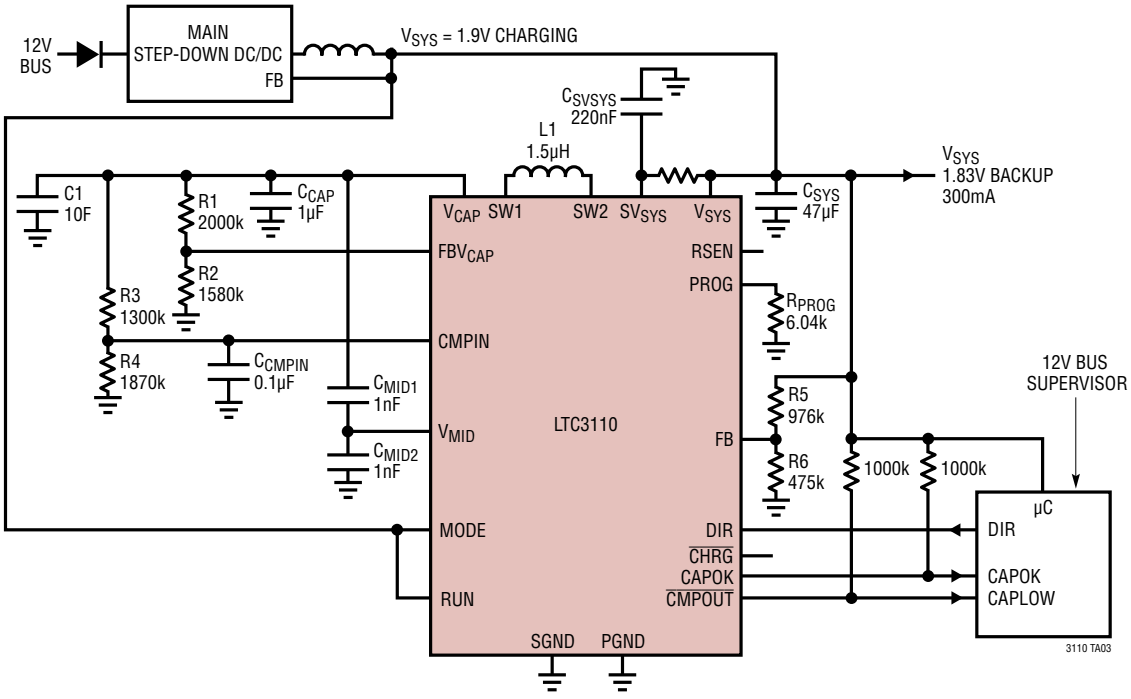
Figure 20. PCB Component Placement of the QFN Package

TYPICAL APPLICATIONS

3.3V/2A Output from Stack of Supercapacitors Backup/Recharge Application with Active Voltage Balancing

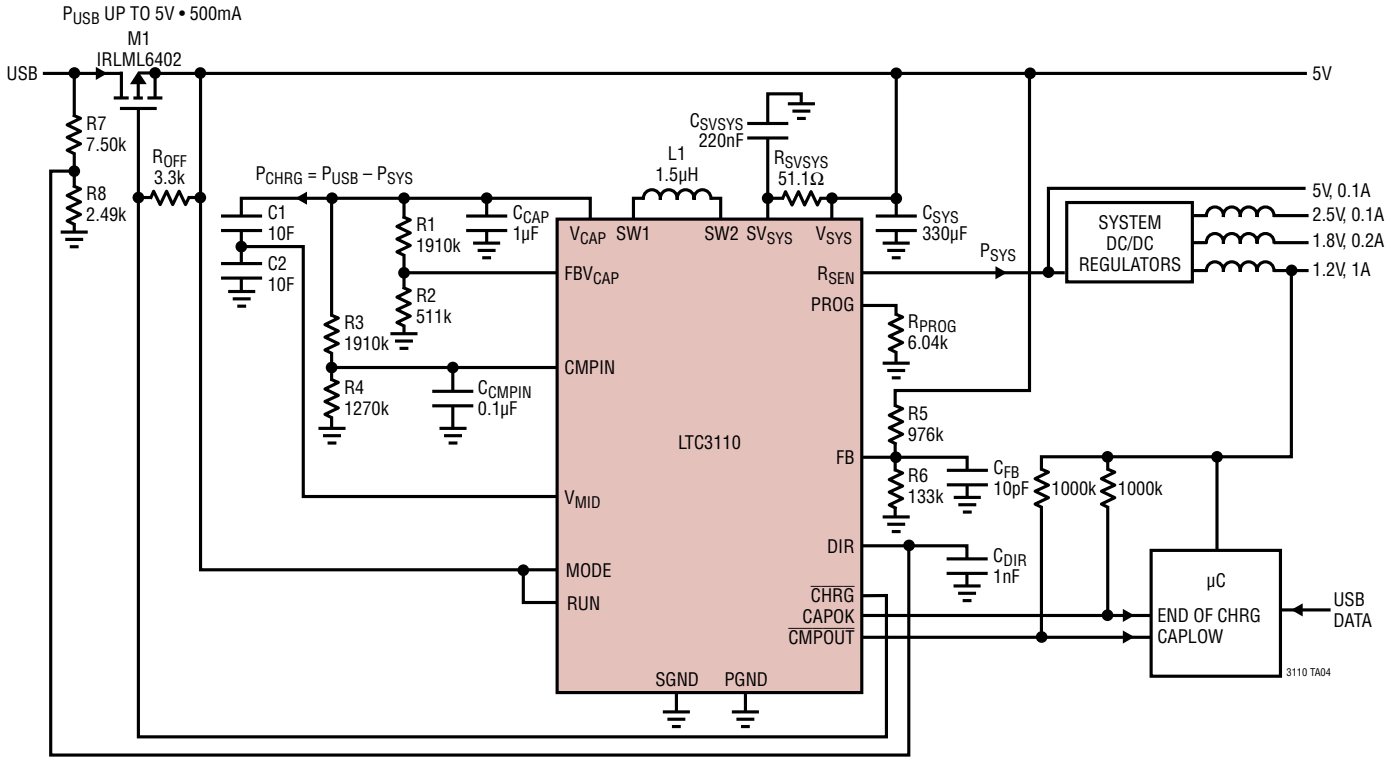


1.8V/300mA Output from Single Capacitor Discharged from 2.5V to 1V and with Reserve Available Down to 0.3V

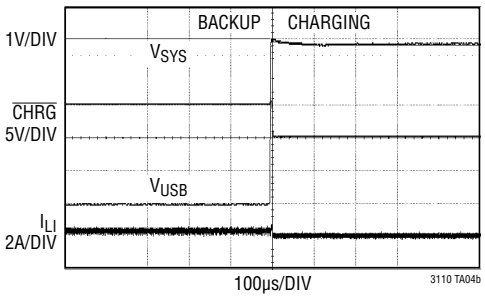


TYPICAL APPLICATIONS

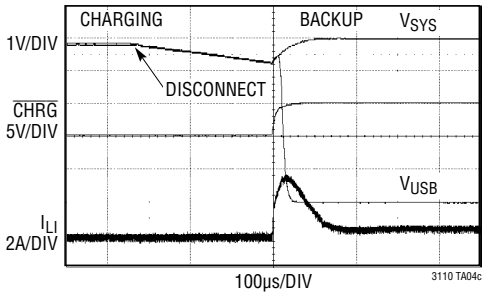
500mA USB Charge/Backup Application with Variable Charging Power, P_{CHRG}, Depending on System Load



USB Connect Transition

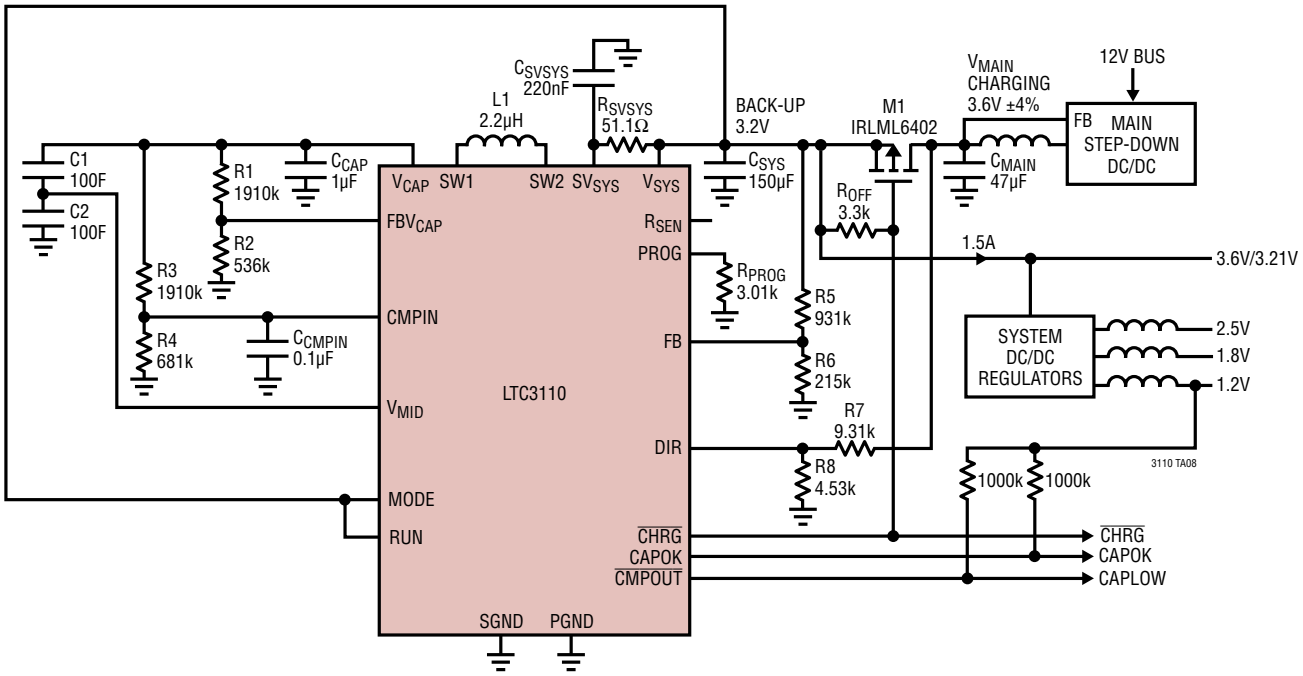


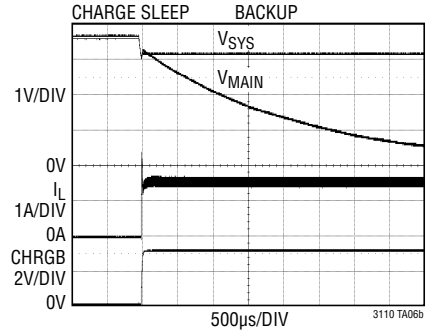
USB Disconnect Transition



TYPICAL APPLICATIONS

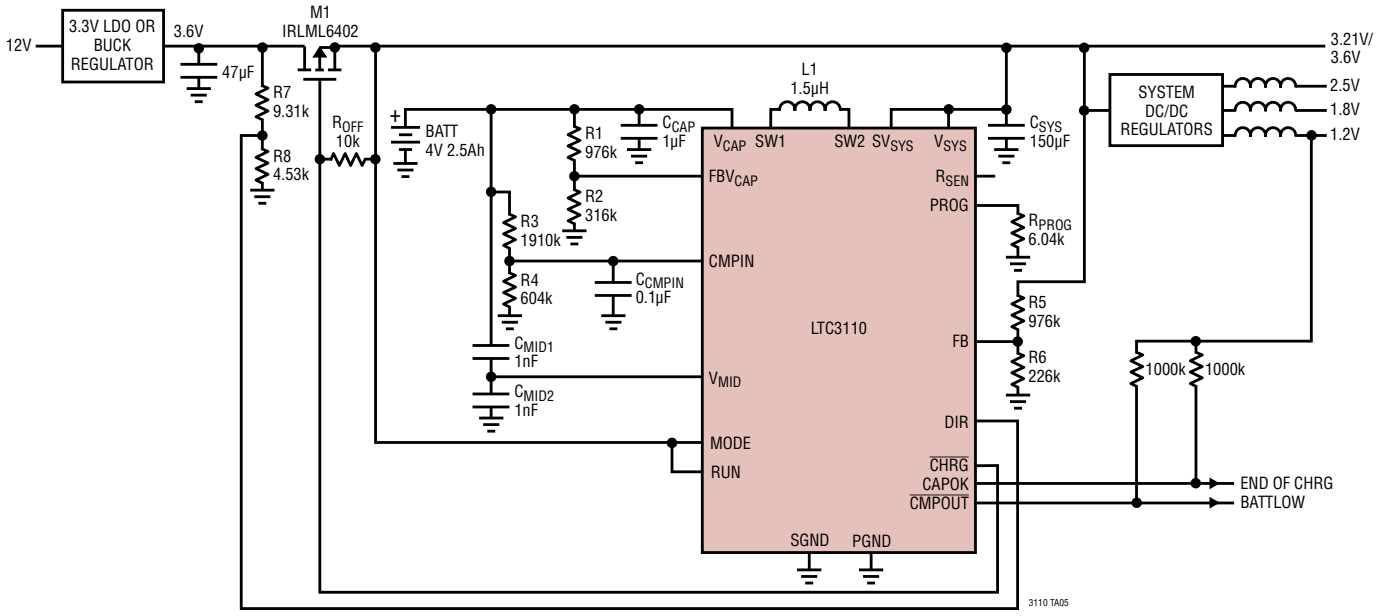
Autonomous Backup and Recharge Application with Input Isolation Switch





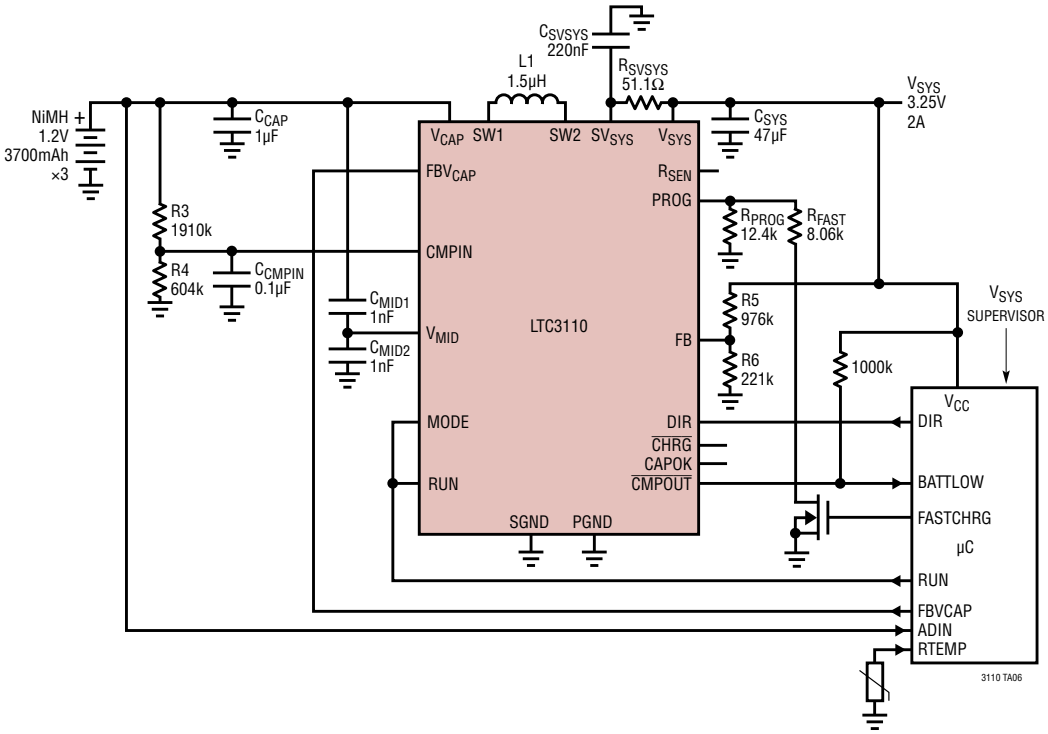
TYPICAL APPLICATIONS

Lead Acid Battery Backup/Recharge Application



TYPICAL APPLICATIONS

NiMH Battery Backup/Recharge Application

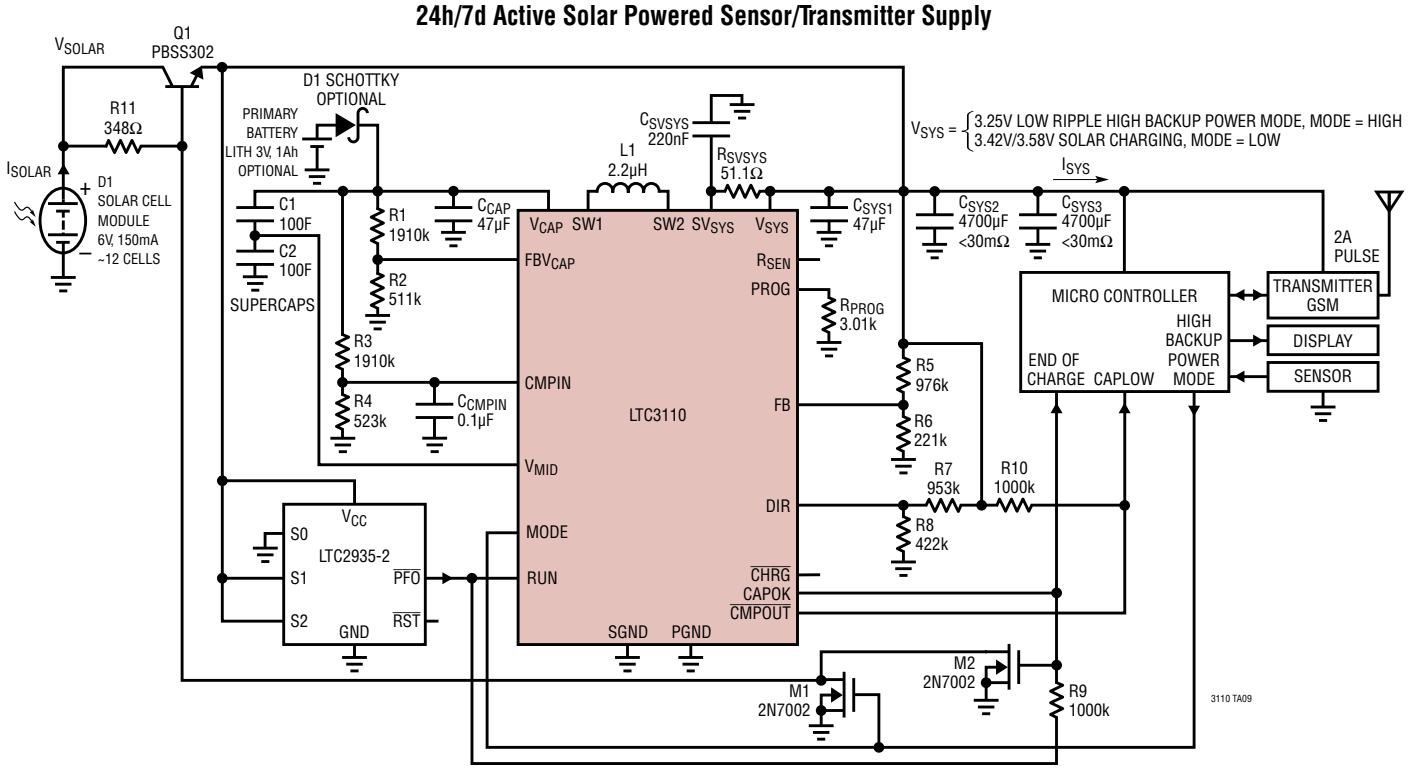


NOTE ON DIGITAL CONTROL SIGNALS IN NiMH BACKUP/RECHARGE APPLICATION:
CHARGING IS INITIATED BY PULLING DIR = HIGH AND FBV_{CAP} = LOW.
CHARGING IS TERMINATED BY PULLING DIR = HIGH AND FBV_{CAP} = HIGH (FBV_{CAP} MUST BE ≥ 1.2V).
SYSTEM BACK-UP IS INITIATED BY FORCING FBVCAP = LOW, WAITING 5µs, THEN FORCING DIR = LOW.

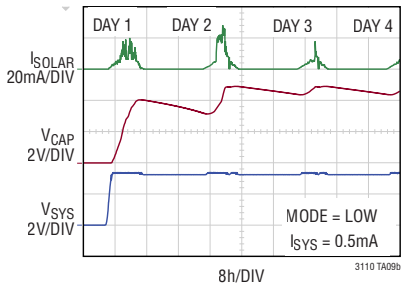
GENERAL SAFETY NOTE: CHARGING MUST BE TERMINATED IF THE BATTERY VOLTAGE OR CHARGE TIME HAVE REACHED THEIR MAXIMUM VALUES OR IF THE BATTERY TEMPERATURE IS ABOVE OR BELOW THE SAVE OPERATING REGION OF THE BATTERY, SEE DATA SHEET OF THE BATTERY.
THE THERMISTOR, USED FOR MEASURING THE TEMPERATURE, MUST HAVE GOOD THERMAL CONNECTION TO THE BATTERY PACK.

TYPICAL APPLICATIONS

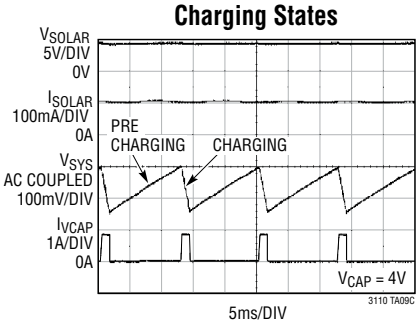
24h/7d Active Solar Powered Sensor/Transmitter Supply



Charging with Solar Current and 24/7 Backup



Charging States



CHARGING WITH SOLAR CURRENT AND 24/7 BACKUP:

IF DAYLIGHT IS PRESENT, THE SUPERCAPACITORS ARE CHARGED UP WITH THE OUTPUT CURRENT OF THE SOLAR CELLS. WHEN DAYLIGHT IS NOT PRESENT, THE SUPERCAPS PARTIALLY DISCHARGE AND PROVIDE THE BACKUP POWER TO MAINTAIN V_{SYS}.

HIGH BACKUP POWER MODE (NO WAVEFORM): IF MODE = HIGH AND WITH THE SUPERCAPACITORS CHARGED, THE APPLICATION CAN PROVIDE THE V_{SYS} BACKUP VOLTAGE WITH LOW RIPPLE AND FULL OUTPUT CURRENT CAPABILITIES. MODE = HIGH STOPS FURTHER CHARGING.

CHARGING STATES:

IF MODE = LOW: THE V_{SYS} VOLTAGE IS FED WITH CURRENT FROM THE SOLAR MODULE OR IS REGULATED FROM THE LTC3110 IN BURST MODE IF SUNLIGHT IS MISSING. IF SUNLIGHT IS PRESENT, V_{SYS} IS REGULATED WITH A TWO POINT VOLTAGE REGULATION DEFINED BY DIR RISING AND DIR FALLING THRESHOLDS.

THE APPLICATION HAS THREE STATES OF OPERATION:

1. C_{SYS} PRE-CHARGING STATE: THE SOLAR PANEL OUTPUT CURRENT PRE-CHARGES THE CAPACITOR C_{SYS} UNTIL THE DIR VOLTAGE RISES ABOVE THE DIR RISING THRESHOLD AND THE SUPERCAPACITOR CHARGING STATE IS ENTERED.
2. SUPERCAPACITOR CHARGING STATE: THE LTC3110 CHARGES THE SUPERCAPACITORS BY DRAWING CURRENT FROM CAPACITOR C_{SYS} UNTIL THE V_{SYS} VOLTAGE FALLS BELOW THE DIR FALLING THRESHOLD AND THE V_{SYS} PRE-CHARGING STATE IS RE-ENTERED.

   THE LTC3110 TOGGLES BETWEEN THE PRE-CHARGING STATE AND THE CHARGING STATE UNTIL FBV_{CAP} IS ABOVE THE FBV_{CAP} RISING THRESHOLD AND THE CHARGE SLEEP STATE IS ENTERED.
3. CHARGE SLEEP STATE (NO WAVEFORM): V_{CAP} IS FULLY CHARGED AND FBV_{CAP} IS ABOVE THE FBV_{CAP} FALLING THRESHOLD WHILE THE V_{SYS} VOLTAGE IS REGULATED WITH LTC3110's BURST MODE BACKUP OPERATION. IN THE CHARGE SLEEP STATE, THE SOLAR MODULE IS ISOLATED FROM V_{SYS}.

STARTUP WITH DISCHARGED SUPERCAPS:

THE V_{SYS} VOLTAGE IS MONITORED WITH THE LTC2935-2 SUPERVISOR ENABLING THE LTC3110 ONLY AT A VOLTAGE ABOVE 2.7V.

IF POWERED FROM HIGH IMPEDANCE SOURCES (E. G. SOLAR CELLS). V_{SYS} MUST BE INITIALLY HIGH ENOUGH TO SKIP THE SOFT START FUNCTION OF THE LTC3110, SEE SOFT START (BACKUP MODE) IN THE OPERATION SECTION.

NOTES: THE REQUIRED PANEL SIZE AND THE NUMBER OF SOLAR CELLS IN SERIES OR IN PARALLEL STRONGLY DEPENDS ON THE LOCAL SUNLIGHT CONDITIONS. V_{SOLAR} MUST BE ONE V_{BE} HIGHER THAN V_{SYS} (3.58V + 0.7V = 4.3V) IN THE LOWEST LIGHT CONDITION TO DELIVER SOLAR CURRENT.

TO PREVENT OVERVOLTAGING OF V_{SYS}, THE I_{VSYS} AVERAGE CURRENT LIMIT MUST BE AT LEAST FOUR TIMES LARGER THAN THE MAXIMUM SOLAR CURRENT ($I_{VSYS\_PROG} > 4 \times I_{SOLAR\_MAX}$). ALTERNATIVELY, OUTPUT $\overline{CHRG}$ CAN BE ADDITIONALLY CONNECTED TO THE BASE OF Q1 TO ISOLATE THE SOLAR PANEL DURING CHARGING.

THE ABSOLUTE MAXIMUM OF V_{SOLAR} IS DEFINED FROM THE V_{CEO} VALUE OF Q1 (E.G. 20V) WHICH ALLOWS THE CONNECTION OF MODULES WITH OPEN CIRCUIT VOLTAGES OF $V_{OC} > 5.25V$.

OPTIONALLY A PRIMARY BATTERY CAN BE ADDED AS RESERVE TO COVER POOR LIGHT CONDITIONS.

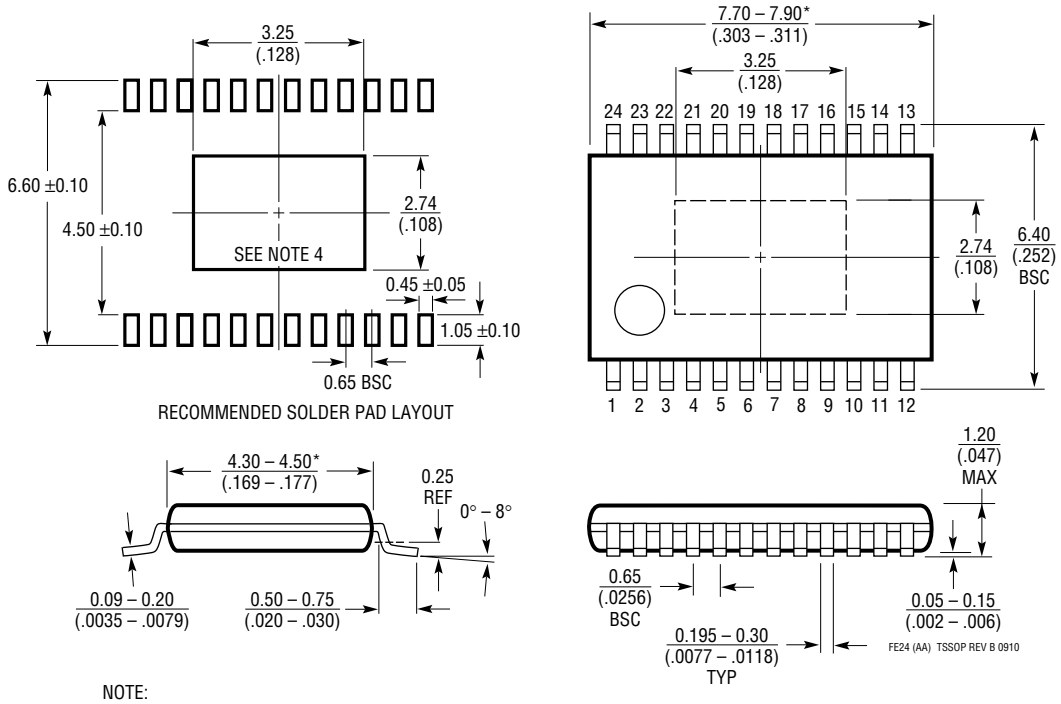
EXAMPLE SOLAR MODULE MANUFACTURERS:

SHARP, PANASONIC, POWERFILM

Rev C

PACKAGE DESCRIPTION

FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1771 Rev B)
Exposed Pad Variation AA

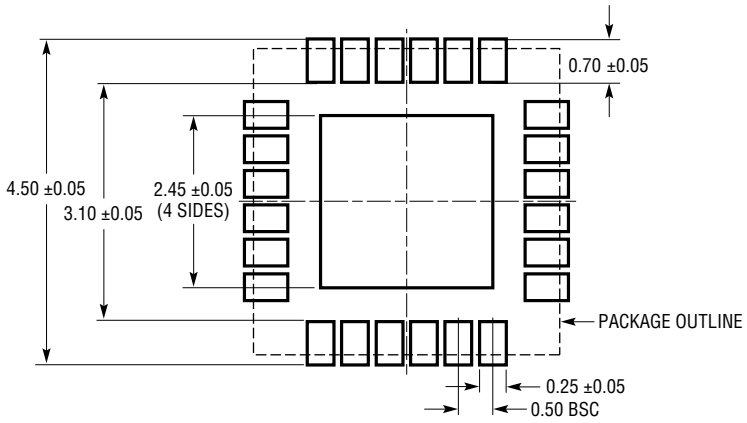


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

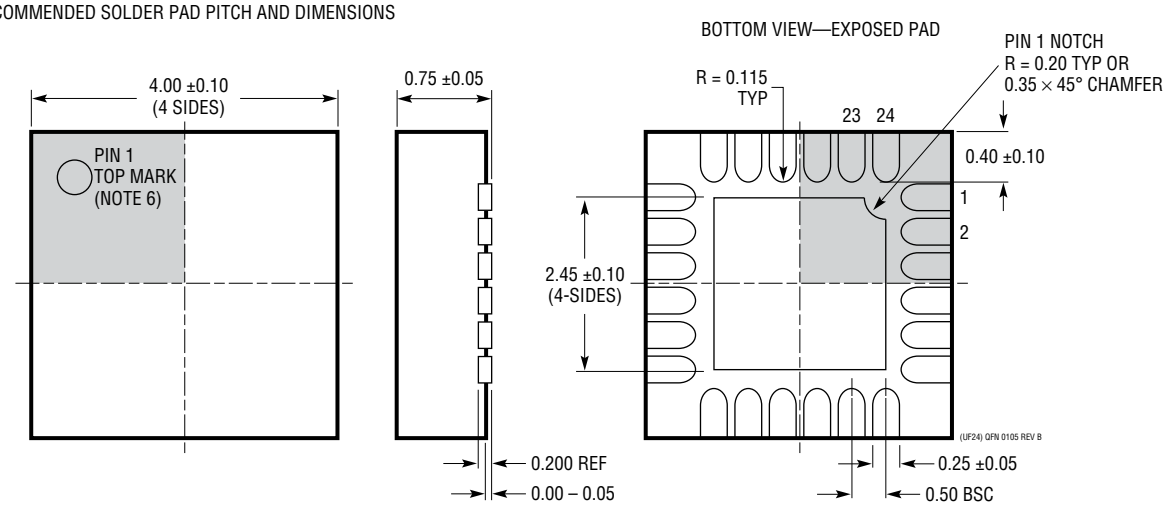
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



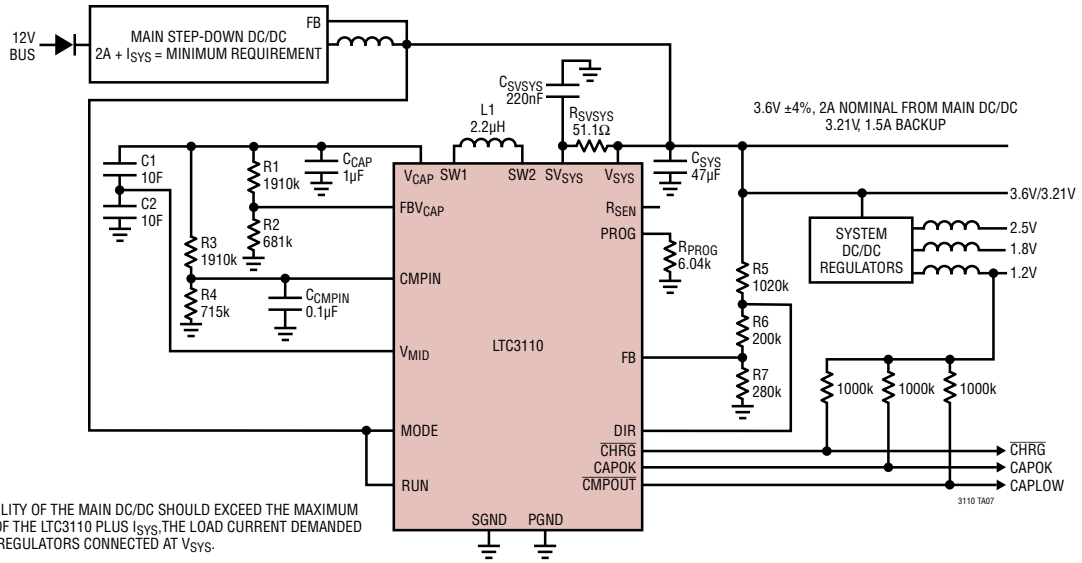
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Add H-grade option.	2, 4
		Clarified conditions and Note 9 for Input Current Limit.	4
		Changed axis labels V_{MID} Buffer Current, Backup Time, Charge Balancer curves.	8, 9
		Enhanced 1.8V/300mA output circuit.	27
B	11/16	Changed reference page number in Preventing V_{CAP} Overcharge Failure section	15
C	8/18	Changed capacitor value	19

TYPICAL APPLICATION

Autonomous Backup and Recharge Application (3.6V Nominal, 3.2V Backup Voltage)



NOTE: THE DRIVING CAPABILITY OF THE MAIN DC/DC SHOULD EXCEED THE MAXIMUM REVERSE CURRENT LIMIT OF THE LTC3110 PLUS I_{SYS}.THE LOAD CURRENT DEMANDED FROM THE SYSTEM DC/DC REGULATORS CONNECTED AT V_{SYS}.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4040	2.5A Battery Backup Power Manager	Step-Up Backup Supply and Step-Down Battery Charger, 6.5A Switches for 2.5A, Automatic Seamless Switchover to Backup Mode Backup from 3.2V Battery
LTC3226	2-Cell Supercapacitor Charger with Backup PowerPath™ Controller	1×/2× Multimode Charge Pump Supercapacitor Charger with Automatic Cell Balancing. Internal 2A LDO Backup Supply (CPO to V_{OUT}). Automatic Main/Backup Switchover, 3mm × 3mm QFN-16 Package
LTC3625/LTC3625-1	1A High Efficiency 2-Cell Supercapacitor Charger with Automatic Cell Balancing	High Efficiency Step-Up/Step-Down Charging of Two Series Supercapacitors, Automatic Cell Balancing. Programmable Charging Current Up to 500mA (Single Inductor), 1A (Dual Inductor), 3mm × 4mm DFN-12 Package
LTC3128	3A Monolithic Buck-Boost Supercapacitor Charger and Balancer with Accurate Input Current Limit	±2% Accurate Average Input Current Limit Programmable to 3A, Active Charge Balancing, Charges 1 or 2 Capacitors, V_{IN}: 1.73V to 5.5V, V_{OUT}: 1.8V to 5.5V
LTC3350	High Current Supercapacitor Backup Controller and System Monitor	Synchronous Step-Down CC/CV Charging up to Four Series Supercapacitors V_{IN}: 4.5V to 35V, 14-Bit ADC for Monitoring System Voltages/Currents, Capacitance and ESR, Internal Active Balancers, 38-Lead 5mm × 7mm QFN Package
LTC4425	Linear SuperCap Charger with Current-Limited Ideal Diode and V/I Monitor	Constant-Current/Constant-Voltage Linear Charger for 2-cell Series Supercapacitor Stack, 2A Charge Current, Auto Cell Balancing, 20µA Quiescent Current
LTC3127	1A Buck-Boost DC/DC Converter with Programmable Input Current Limit	Programmable (0.2A to 1A) ±4% Accurate Average Input Current Limit, 1.8V to 5.5V (Input) and 1.8V to 5.25V (Output) Voltage Range
LTC3125	1.2A I_{OUT}, 1.6MHz, Synchronous Boost DC/DC Converter With Adjustable Input Current Limit	94% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 15µA, I_{SD} < 1µA, 2mm × 3mm DFN-8 Package
LTC3441/LTC3441-2/ LTC3441-3	1.2A I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V, I_Q = 50µA, I_{SD} < 1µA, 3mm × 4mm DFN-12 Package
LTC3113	3A Low Noise Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.5V, I_Q = 40µA, I_{SD} < 1µA, 4mm × 5mm DFN-16 and 20-Lead TSSOP Packages
LTC3355	20V 1A Buck DC/DC with Integrated SCAP Charger and Backup Regulator	V_{IN} Voltage Range: 3V to 20V, V_{OUT} Voltage Range: 2.7V to 5V, 1A Current Mode Buck Main Regulator, 5A Boost Backup Regulator Powered from Single Supercapacitor Down to 0.5V, Overvoltage Protection
LTC3643	2A Bidirectional Power Backup Supply	Bidirectional Synchronous Boost Capacitor Charger/Buck Regulator for System Backup, Wide V_{IN} Voltage Range: 3V to 17V, Up to 40V Capacitor Voltage, 2A Maximum CAP Charge Current, Low Profile 24-Lead 3mm × 5mm QFN Package

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- Alternative Solution
- Excess Inventory Management