THE DATASHEET OF

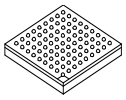
MIMXRT1165CVM5A

NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMXRT1160IEC
Rev. 3, 06/2023

MIMXRT1166CVM5A **MIMXRT1165CVM5A**

i.MX RT1160 Crossover Processors Data Sheet for Industrial Products



Package Information
Plastic Package
289-pin MAPBGA, 14 x 14 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 6

1 i.MX RT1160 introduction

The i.MX RT1160 is a new high-end processor of the i.MX RT family, which features NXP's advanced implementation of a high performance Arm Cortex®-M7 core operating at speeds up to 500 MHz and a power efficient Cortex®-M4 core up to 240 MHz.

The i.MX RT1160 processor has 1 MB on-chip RAM in total, including a 768 KB RAM which can be flexibly configured as TCM (512 KB RAM shared with M7 TCM and 256 KB RAM shared with M4 TCM) or general-purpose on-chip RAM. The i.MX RT1160 integrates advanced power management module with DCDC and LDO regulators that reduce complexity of external power supply and simplifies power sequencing. The i.MX RT1160 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad/Octal SPI, Hyper RAM/Flash, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™,

GPS, displays, and camera sensors. The i.MX RT1160 also has rich audio and video features, including MIPI CSI/DSI, LCD display, graphic accelerator, camera interface, SPDIF, and I2S audio interface.

The i.MX RT1160 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance
- High-end Audio Appliance
- Low-end Instrument Cluster
- Point-of-Sale (PoS)

1.1 Features

The i.MX RT1160 processors are based on Arm Cortex®-M7 Core™ Platform, which has the following features:

- The Arm Cortex-M7 Core Platform:
  - 32 KB L1 Instruction Cache and 32 KB L1 Data Cache
  - Floating Point Unit (FPU) with single-precision and double-precision support of Armv7-M Architecture FPv5
  - Support the Arm®v7-M Thumb instruction set, defined in the Armv7-M architecture
  - Integrated Memory Protection Unit (MPU), up to 16 individual protection regions
  - Up to 512 KB I-TCM and D-TCM in total
  - Frequency of 500 MHz
  - ECC support for both cache and TCM
  - Frequency of the core, as per Table 11, "Operating ranges," on page 27.
- The Arm Cortex®-M4 Core platform:
  - Cortex-M4 processor with single-precision FPU defined by Armv7-M architecture FPv4-SP
  - Integrated MPU with 8 individual protection regions
  - 16 KB Instruction Cache, 16 KB Data Cache, and 256 KB TCM
  - Frequency of 240 MHz
  - ECC support for TCM and parity check support for cache

The SoC-level memory system consists of the following additional components:

  - Boot ROM (256 KB)
  - On-chip RAM (1 MB in total)
    - Configurable 512 KB RAM shared with M7 TCM
    - 256 KB RAM shared with M4 TCM
    - Dedicated 256 KB OCRAM
  - Secure always-on RAM (4 KB)
- External memory interfaces:

  - 8/16/32-bit SDRAM, up to SDRAM-133/SDRAM-166/SDRAM-200
  - 8/16-bit SLC NAND FLASH
  - SD/eMMC
  - SPI NOR/NAND FLASH
  - Parallel NOR FLASH with XIP support
  - Single/Dual channel Quad SPI FLASH with XIP support
  - Hyper RAM/FLASH
  - OCT FLASH
  - Synchronization mode for all devices
- Timers and PWMs:
  - Six General Programmable Timer (GPT) modules
    - 4-channel generic 32-bit resolution timer for each
    - Each supports standard capture and compare operation
  - Two Periodical Interrupt Timer (PIT) modules
    - Four timers for each module
    - Generic 32-bit resolution timer
    - Periodical interrupt generation
  - Four Quad Timer (QTimer) modules
    - 4-channel generic 16-bit resolution timer for each
    - Each supports standard capture and compare operation
    - Quadrature decoder integrated
  - Four FlexPWMs
    - Up to 8 individual PWM channels for each
    - 16-bit resolution PWM suitable for Motor Control applications
  - Four Quadrature Decoders
  - Four Watch Dog (WDOG) modules

Each i.MX RT1160 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
  - Parallel RGB LCD interface (eLCDIF)
    - Support 8/16/24-bit interface
    - Support up to WXGA resolution @60fps
    - Support Index color with 256 entry x 24-bit color LUT
  - Parallel RGB LCD Interface Version 2 (LCDIFv2)
    - Enhanced based on LCDIF version
    - Support up to 8 layers of alpha blending
  - MIPI Display Serial Interface (MIPI DSI)

  - PHY integrated
  - 2 data lanes interface with up to 1.5 GHz bit rate clock
- Smart LCD Display with 8080 interface through SEMC

- Audio:
  - SPDIF input and output
  - Four Synchronous Audio Interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
  - Medium Quality Sound (MQS) interface via GPIO pads
  - PDM microphone interface with 4 pairs of inputs
  - Asynchronous Sample Rate Converter (ASRC)
- Graphics engine:
  - Generic 2D (PXP)
    - BitBlit
    - Flexible image composition options—alpha, chroma key
    - Porter-duff blending
    - Image rotation (90˚, 180˚, 270˚)
    - Image resize
    - Color space conversion
    - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
    - Standard 2D-DMA operation
  - Vector Graphics Processing
    - Real-time hardware curve tessellation of lines, quadratic, and cubic Bezier curves
    - 16x Line Anti-aliasing
    - OpenVG 1.1 support
    - Vector Drawing
- Camera Interface:
  - Parallel Camera Sensor Interface (CSI)
    - Support 24-bit, 16-bit, and 8-bit input
    - Barcode binarization and histogram statistics
  - MIPI Camera Serial Interface (MIPI CSI)
    - PHY integrated
    - 2 data lanes interface with up to 1.5 GHz bit rate clock
- Connectivity:
  - Two USB 2.0 OTG controllers with integrated PHY interfaces
  - Two Ultra Secure Digital Host Controller (uSDHC) interfaces
    - eMMC 5.0 compliance with HS400 support up to 400 MB/sec
    - SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec

  - Support for SDXC (extended capacity)
  - One 10M/100M Ethernet controller with support for IEEE1588
  - One Gigabit Ethernet controller with support for AVB
  - Twelve universal asynchronous receiver/transmitter (UARTs) modules
  - Six I2C modules
  - Six SPI modules
  - Three FlexCAN (with Flexible Data-rate supported) modules
  - Two EMV SIM modules
- Analog:
  - Two Analog-Digital-Converters (ADC), which supports both differential and single-end inputs
  - One Digital-Analog-Converter (DAC)
  - Four Analog Comparators (ACMP)
- GPIO and Pin Multiplexing:
  - General-purpose input/output (GPIO) modules with interrupt capability
  - Input/output multiplexing controller (IOMUXC) to provide centralized pad control
  - Two FlexIO modules
  - 8 x 8 keypad

The i.MX RT1160 processors integrate advanced power management unit and controllers:

- Full PMIC integration, including on-chip DCDC and LDOs
- Temperature sensor with programmable trim points
- Hardware power management controller (GPC)

The i.MX RT1160 processors support the following system debug:

- Arm CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) and SWD debug interfaces

Security functions are enabled and accelerated by the following hardware:

- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance (CAAM) module:
  - Public Key Cryptography Engine (PKHA)
  - Symmetric Engines
  - Cryptographic Hash Engine
  - Random Number Generation (RNG4)
  - Four Job Rings for use by processors
  - Secure Hardware-Only Cryptographic Key Management
  - Encrypted Boot
  - Revision control check based on fuse values

  - DEK includes IV
  - Side channel attack countermeasures
  - 64 KB secure RAM
- Inline Encryption Engine (IEE):
  - External memory encryption/decryption
  - I/O direct encrypted storage and retrieval (Stream Support)
  - FlexSPI decryption only
- On-the-Fly AES Decryption (OTFAD):
  - AES-128 Counter Mode On-the-Fly Decryption
  - Hardware support for unwrapping “key blobs”
  - Functionally acts as a slave sub-module to the FlexSPI
- Secure Non-Volatile Storage (SNVS):
  - Secure real-time clock (SRTC)
  - Zero Master Key (ZMK)
- Secure always-on RAM (4 KB)
- Secure key management and protection
  - Physical Unclonable Function (PUF)
  - UnDocumented Function (UDF)
  - Built-in Manufacturing Protection Hardware
- Secure and trusted access control

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions such as display interfaces, camera interfaces, and connectivity interfaces are not offered on all derivatives.

1.2 Ordering information

Table 1 provide examples of orderable part numbers covered by this Data Sheet.

Table 1. Ordering information

	MIMXRT1166CVM5A	MIMXRT1165CVM5A
Qualification tier	Industrial	
M7 core	500 MHz	
M4 core	240 MHz	
SRAM	1 MB without ECC or 896 KB with ECC	
Parallel LCD and CSI	Yes	—
MIPI DSI and CSI	Yes	—

	MIMXRT1166CVM5A	MIMXRT1165CVM5A
GPU2D	Yes	—
PXP	Yes	—
ADC	x2	
ACMP	x4	
DAC	x1	
CAN-FD	x3	
1 Gb ENET with AVB	x1	
10/100 Mb ENET with 1588	x1	
USB OTG	x2	
eMMC 5.0 / SD 3.0	x2	
EMV SIM	x2	
SAI	x4	
DMIC	x8	
FlexSPI	x2	
UART	x12	
I2C	x6	
SPI	x6	
FlexIO	x2	
GPT	x6	
PIT	x2	
QTimer	x4	
FlexPWM	x4	
Security	Yes	
Package	289 MAPBGA, 14 mm x14 mm, 0.8 mm pitch	
Junction temperature T_j (°C)	-40 to 105	

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX RT1160 Crossover Processors for Industrial Products Data Sheet (IMXRT1160IEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/IMXRT or contact an NXP representative for details.

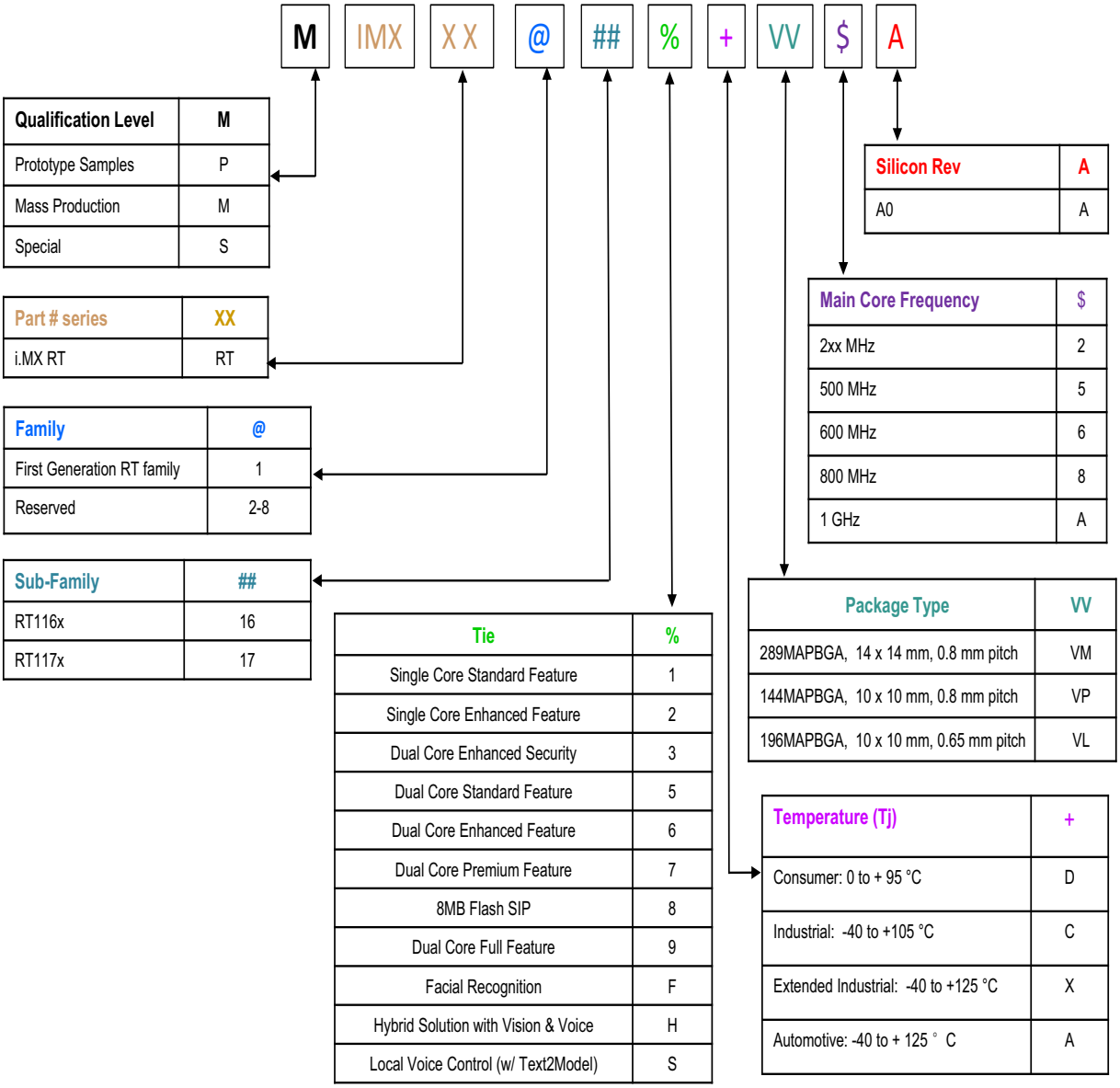


Figure 1. Part number nomenclature—i.MX RT11XX family

1.3 Package marking information

Figure 2 describes the package marking format about the i.MX RT1160 Crossover Processors.

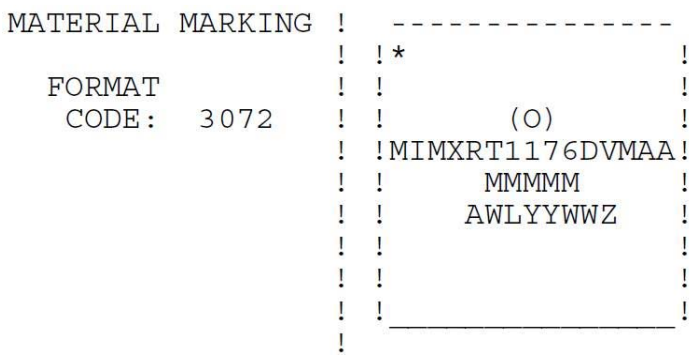


Figure 2. MAPBGA289 14 x 14 mm package marking format

The 14 x 14 mm of i.MX RT1160 MAPBGA289 package has the following top-side marking:

- First line: aaaaaaaaaaaaaa
- Second line: mmmmm
- Third line: xxxyywwx

Table 2 lists the identifier decoder.

Table 2. Identifier decoder

Identifier	Description
a	Part number code, refer to Section 1.2, Ordering information
m	Mask set
y	Year
w	Work week
x	NXP internal use

2 Architectural overview

The following subsections provide an architectural overview of the i.MX RT1160 processor system.

2.1 Block diagram

Figure 3 shows the functional modules in the i.MX RT1160 processor system[1].

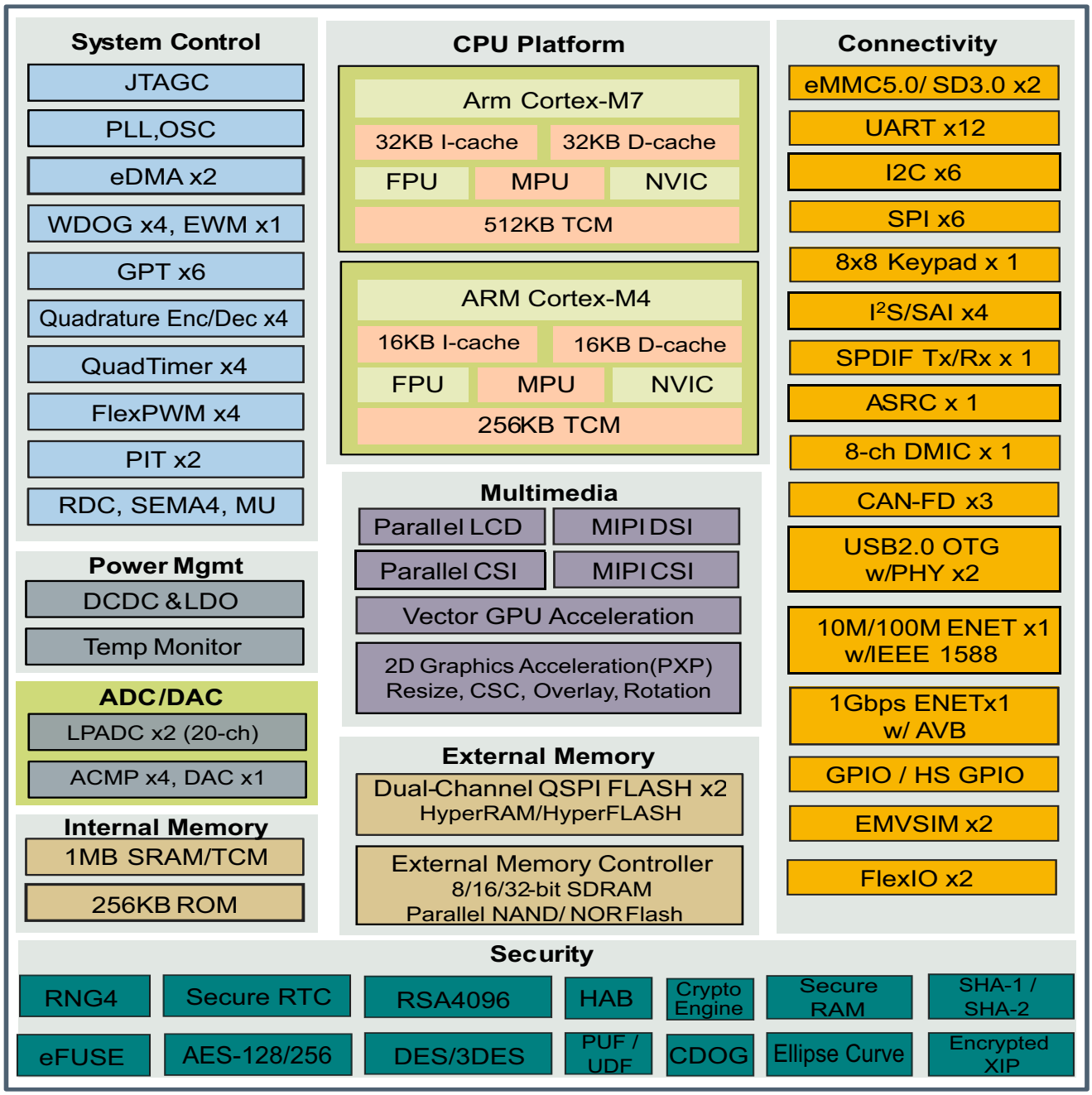


Figure 3. i.MX RT1160 system block diagram

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 1 for details.

3 Modules list

The i.MX RT1160 processors contain a variety of digital and analog modules. Table 3 describes these modules in alphabetical order.

Table 3. i.MX RT1160 modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ACMP1 ACMP2 ACMP3 ACMP4	Analog Comparator	Analog	The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).
ADC_ETC	ADC External Trigger Control	Analog	ADC_ETC enables multiple users shares a ADC module in a Time-Division-Multiplexing (TDM).
ADC1 ADC2	Analog to Digital Converter	Analog	The ADC is a 12-bit general purpose analog to digital converter.
AOI	And-Or-Inverter	Cross Trigger	The AOI provides a universal boolean function generator using a four-term sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).
Arm	Arm Platform	Arm	The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules. The Cortex-M4 platform has following features: • Cortex-M4 processor with FPU • Local memory – 16 KB instruction cache and 16 KB data cache – 256 KB TCM – TCM memories support ECC – Cache memories support Parity Check
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The ASRC can process groups of audio channels with an independent time-based simultaneously.
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM supports a set of standard hardware accelerators, boot time acceleration of the hashing function, crypto key protection, HDCP 2.x authentication and protected video path support, manufacturing protection and public key cryptographic acceleration, and inter-operate with TrustZone, Resource Domain, and system virtualization access controls.
CANFD1 CANFD2 CANFD3	Flexible Controller Area Network	Connectivity Peripherals	The CAN with Flexible Data rate (CAN FD) module is a communication controller implementing the CAN protocol according to the ISO11898-1 and CAN 2.0B protocol specification.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC PGMC PMU SRC	Clock Control Module, General Power Controller, Power Manage Unit, Power Gating and Memory Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit/24-bit Bayer data input.
CWT	Code Watchdog Timer	Timer peripherals	The CWT provides mechanisms for detecting side-channel attacks and the execution of unexpected instruction sequences.
DAC	Digital-Analog-Converter	Analog	The DAC is a 12-bit general purpose digital to analog converter.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform.
DCDC	DCDC Converter	Analog	The DCDC module is used for generating power supply for core logic. Main features are: • Adjustable high efficiency regulator • Two outputs: 1.0 V and 1.8 V • Over current and over voltage detection
eDMA eDMA_LPSR	enhanced Direct Memory Access	System Control Peripherals	There are two enhanced DMAs (eDMA). • The eDMA is a 32-channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor. • The DMA_MUX is capable of multiplexing up to 128 DMA request sources to the 32 DMA channels of eDMA.
eLCDIF	LCD interface	Multimedia Peripherals	The enhanced LCD controller provides flexible display options and to drive a wide range of display devices varying in size and capability. Major features are: • Up to WXGA 60 Hz • 8/16/18/24 bit LCD data bus support available depending on I/O mux options. • Programmable timing and parameters for LCD interfaces to support a wide variety of displays. • Index color with 256 entry x 24-bit color LUT
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity Peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
ENET 1G	Ethernet Controller	Connectivity Peripherals	One 1G Ethernet is also integrated, which has following features: • RGMII/RMII/MII operation • Support IEEE1588 • Support AVB
EWM	External Watchdog Monitor	Timer Peripherals	The EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode.
FlexIO1 FlexIO2	Flexible Input/output	Connectivity and Communications	The FlexIO is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active.
FlexPWM1 FlexPWM2 FlexPWM3 FlexPWM4	Pulse Width Modulation	Timer Peripherals	The pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms.
FlexRAM	RAM	Memories	The i.MX RT1160 has 512 KB of on-chip RAM which could be flexible allocated to I-TCM, D-TCM, and on-chip RAM (OCRAM) in a 32 KB granularity. The FlexRAM is the manager of the 512 KB on-chip RAM array. Major functions of this blocks are: interfacing to I-TCM and D-TCM of CM7 and OCRAM controller; dynamic RAM arrays allocation for I-TCM, D-TCM, and OCRAM.
FlexSPI1 FlexSPI2	Flexible Serial Peripheral Interface	Connectivity and Communications	FlexSPI acts as an interface to one or two external serial memory devices, FlexSPI2 has 8 bi-directional data lines.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O. **Note:** GPIO13 register access takes a long time (about 50μs due to clocked by 32 KHz clock source). During the period of registers access, the LPSR domain bus would be on hold.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics Processing	Multimedia Peripherals	The vector graphics processing supports following features: • Real-time hardware curve tessellation of lines, quadratic, and cubic Bezier curves • 16x line anti-aliasing • OpenVG 1.1 support • Vector drawing
IOMUXC	IOMUX Control	Mux control	This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.
JTAGC	JTAG Controller	System Control Peripherals	The JTAG interface complies with JTAG TAP standards to internal logic. The i.MX RT1160 processors use JTAG port for production, testing, and system debugging. In addition, the JTAG provides BSR (Boundary Scan Register) standard support, which complies with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX RT1160 JTAG incorporates two security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
KPP	Keypad Port	Human Machine Interfaces	The KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: • Multiple-key detection • Long key-press detection • Standby key-press detection • Supports a 2-point and 3-point contact key matrix
LCDIFv2	Parallel RGB LCD interface version 2	Multimedia Peripherals	The LCDIFv2 is an enhanced version of LCDIF. Main features are: • Eight layers of alpha blending • CRC check for configurable region on the final display output after alpha blending • Write-back channel to save the final output into memory
LPI2C1 LPI2C2 LPI2C3 LPI2C4 LPI2C5 LPI2C6	Low Power Inter-integrated Circuit	Connectivity and Communications	The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master. The I2C provides a method of communication between a number of external devices. More detailed information, see Section 4.9.2, LPI2C module timing parameters.
LPSPI1 LPSPI2 LPSPI3 LPSPI4 LPSPI5 LPSPI6	Low Power Serial Peripheral Interface	Connectivity and Communications	The LPSPI is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. • It can continue operating while the chip is in stop modes, if an appropriate clock is available • Designed for low CPU overhead, with DMA off loading of FIFO register access
LPUART1 LPUART2 LPUART3 LPUART4 LPUART5 LPUART6 LPUART7 LPUART8 LPUART9 LPUART10 LPUART11 LPUART12	UART Interface	Connectivity Peripherals	Each of the UART modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 20 Mbps.
MECC64	Error Correcting Code	Memories and Memory Controllers	MECC64 module supports Single Error Correction and Double Error Detection (SECDED) ECC function to provide reliability for 4 banks On-Chip RAM (OCRAM) access. When ECC function is disabled, ECC OCRAM can be also used to store data.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
MIPI-CSI	MIPI CSI Interface	Multimedia Peripherals	Key features of MIPI CSI controller are listed as following: • Implements all three MIPI CSI-2 layers • Supports CSI-2 Unidirectional Master operation • Virtual Channel support • Flexible pixel-based user interface
MIPI-DSI	MIPI DSI Interface	Multimedia Peripherals	Key features of MIPI DSI controller are listed as following: • Implements all three DSI layers • Supports Command and Video Modes • Virtual Channel support • Flexible packet based user interface
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
MU	Messaging Unit	System Control	The Messaging Unit module enables two processors within the SoC to communicate and coordinate by passing messages (e.g. data, status, and control) through the MU interface. The MU also provides the ability for one processor to signal the other processor using interrupts.
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility.
OCRAM	On-Chip Memory controller	Memories and Memory Controllers	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module.
PDM	Pulse Density Modulation	Multimedia Peripherals	The PDM supports up to 8-channels (4 lanes) digital MIC inputs.
PIT1 PIT2	Periodical Interrupt Timer	Timer Peripherals	The PIT features 32-bit counter timer, programmable count modules, clock division features, interrupt generation, and a slave mode to synchronize count enable for multiple PITs.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	Pixel Processing Pipeline	Multimedia Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications.
Quadrature DEC1 Quadrature DEC2 Quadrature DEC3 Quadrature DEC4	Quadrature Decoder	Timer Peripherals	The enhanced quadrature decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed.
QuadTimer1 QuadTimer2 QuadTimer3 QuadTimer4	QuadTimer	Timer Peripherals	The quad-timer provides four time channels with a variety of controls affecting both individual and multi-channel features.Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization.
RDC	Resource Domain Controller	Security	The RDC provides robust support for the isolation of processing domain to prevent one core from accessing another's peripherals, to control access rights to common memory and provide hardware enforcement of semaphore based locking of shared peripherals. For single system use case, RDC can be disabled and AIPS-TZ/DEXSC can be bypassed. For dual system case, RDC can be configured and locked each core starts their own image.
ROMCP	ROM Controller with Patch	Memories and Memory Controllers	The ROMCP acts as an interface between the Arm advanced high-performance bus and the ROM. The on-chip ROM is only used by the Cortex-M7 core during boot up. Size of the ROM is 256 KB.
RTC OSC	Real Time Clock Oscillator	Clock Sources and Control	The RTC OSC provides the clock source for the Real-Time Clock module and low speed clock source for CCM/SRC/GPC modules. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock.
SAI1 SAI2 SAI3 SAI4	Synchronous Audio Interface	Multimedia Peripherals	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SEMA4	Semaphores	System Control	The SEMA4 module implements hardware-enforced semaphores as an IPS-mapped slave peripheral device and provides 16 hardware-enforced gates in a dual-processor configuration.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SEMC	Smart External Memory Controller	Memory and Memory Controller	The SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The interface supported includes SDRAM, NOR Flash, SRAM, and NAND Flash, as well as 8080 display interface.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine and Master Key Control.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSARC	State Save and Restore Controller	Memories and Memory Controllers	The SSARC saves the registers of functional modules in memory before power down, and restores registers from memory after the module is powered up.
SYS OSC	System Clock Oscillator	Clock Sources and Control	The SYS OSC provides the primary clock source for all the PLLs to generate the clock for CPU, BUS, and high-speed interfaces. The SYS OSC module, in conjunction with an external crystal, generates a 24 MHz reference clock.
TEMP SENSE	Temperature Sensor	Analog	The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.
USB1 USB2	Universal Serial Bus 2.0	Connectivity Peripherals	USB 2.0 OTG modules (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX RT1160 specific SoC characteristics: All four MMC/SD/SDIO controllers are identical and are based on the uSDHC. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
VIDMUX	Video mux	Mux control	Video mux are mux control for Parallel CSI (IO PADs), MIPI CSI-2, MIPI DSI, Parallel LCDIF (IO PADs) and CSI, LCDIF-V2, eLCDIF control. It also includes the DCIC of MIPI DSI and Parallel DSI.
WDOG1 WDOG2 WDOG3 WDOG4	Watch Dog	Timer Peripherals	WDOG1 and WDOG2 Timer support two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line. WDOG3 and WDOG4 modules are high reliability independent timers that are available for system to use. They provide a safety feature to ensure software is executing as planned and the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU. Windowed refresh mode is supported as well.
XBARA XBARB	Cross BAR	Cross Trigger	Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.

Table 3. i.MX RT1160 modules list (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
XECC	External ECC Controller	Memories and Memory Controllers	XECC can be used as a gasket module on AXI bus to support ECC function for external memory.
XRDC	Extended Resource Domain Controller	Security	The XRDC provides an integrated, scalable architectural framework for access control, system memory protection, and peripheral isolation. It allows software to assign chip resources including processor cores, non-core bus masters, memory regions, and slave peripherals to processing domains to support enforcement of robust operational environments.

3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX RT1160 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, Package information and contact assignments." Signal descriptions are provided in the *i.MX RT1160 Reference Manual* (IMXRT1160RM).

Table 4. Special signal considerations

Signal Name	Remarks
GPIO_LPSR_02, GPIO_LPSR_03, GPIO_DISP_B1_06, GPIO_DISP_B1_07, GPIO_DISP_B1_08, GPIO_DISP_B1_09, GPIO_DISP_B1_10, GPIO_DISP_B1_11, GPIO_DISP_B2_00, GPIO_DISP_B2_01, GPIO_DISP_B2_02, GPIO_DISP_B2_03, GPIO_DISP_B2_04, GPIO_DISP_B2_05	If not using eFuse setting, these I/Os level determine the boot mode and boot device configuration. In case of boot mode pins immediately change state after POR_B released, user must ensure POR_B remains asserted until the last power rail reach its working voltage.
CLK1_P/ CLK1_N	This differential output is reserved for NXP internal use. For users, this output must be a no connect.
DCDC_PSWITCH	PAD is in DCDC_IN domain and connected to ground to bypass DCDC. To enable DCDC function, assert DCDC_IN with at least 1ms delay for DCDC_IN rising edge.

Table 4. Special signal considerations (continued)

Signal Name	Remarks
RTC_XTALI/RTC_XTALO	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (> 100 M). This de-biases the amplifier and reduces the start-up margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_SNVS_ANA level and the frequency shall be < 100 kHz under the typical conditions. It is recommended to tie RTC_XTALI to GND if external crystal is not used. When a high-accuracy real-time clock is not required, the system may use the on-chip 32 kHz oscillator. The tolerance is ±25%. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI.
XTALI/XTALO	The SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, refer to section of Bypass Configuration (24 MHz) from the reference manual. There are three configurations that can be utilized, but configuration 2 is recommended. The logic level of this forcing clock must not exceed the VDD_LPSR_ANA level. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See Section 4.2.6, On-chip oscillators and relevant interface specifications chapters for details.
JTAG_*nnnn*	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 5 for a summary of the JTAG interface.
	JTAG_TDO is configured with an on-chip keeper circuit, such that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental. See Table 5 for a summary of the JTAG interface.
	When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain. When JTAG_MOD is high, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 standard.
NC	These signals are No Connect (NC) and should not be connected by the user.
POR_B	See the System Boot chapter in the reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence. POR_B signal has internal 100 kΩ pull up to SNVS domain, should pull up to VDD_SNVS_ANA if need to add external pull up resistor, otherwise it will cause additional leakage during SNVS mode. It is recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, please refer to the EVK design for details. Note: • As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power down. • For power on reset, on any conditions ones need to make sure the voltage on DCDC_PSWITCH pin is below 0.5 V before power up.
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF. Both boot mode inputs can be disconnected.
TEST_MODE	This input is reserved for NXP manufacturing use. The user must tie this pin directly to GND.

Table 4. Special signal considerations (continued)

Signal Name	Remarks
WAKEUP	A GPIO powered by SNVS domain power supply which can be configured as wakeup source in SNVS mode.

Table 5. JTAG controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	20–50 kΩ pull-down
JTAG_TMS	Input	20–50 kΩ pull-up
JTAG_TDI	Input	20–50 kΩ pull-up
JTAG_TDO	3-state output	None
JTAG_TRSTB	Input	20–50 kΩ pull-up
JTAG_MOD	Input	20–50 kΩ pull-down

3.2 Recommended connections for unused analog interfaces

Table 6 shows the recommended connections for unused analog interfaces.

Table 6. Recommended connections for unused analog interfaces

Module	Pad Name	Recommendations if Unused
32 kHz OSC	RTC_XTALI, RTC_XTALO	Not connected It is recommended that RTC_XTALI ties to GND if external crystal is not connected.
ADC	ADC_VREFH	10 KΩ resistor to ground
	VDDA_ADC_1P8	10 KΩ resistor to ground
	VDDA_ADC_3P3	10 KΩ resistor to ground
CCM	CLK1_N, CLK1_P	Not connected
DAC	DAC_OUT	Not connected
MIPI	VDD_MIPI_1P0	10 KΩ resistor to ground
	VDD_MIPI_1P8	10 KΩ resistor to ground
	MIPI_DSI_CKN, MIPI_DSI_CKP, MIPI_DSI_DN0, MIPI_DSI_DP0, MIPI_DSI_DN1, MIPI_DSI_DP1	Not connected
	MIPI_CSI_CKN, MIPI_CSI_CKP, MIPI_CSI_DN0, MIPI_CSI_DP0, MIPI_CSI_DN1, MIPI_CSI_DP1	Not connected
DCDC	DCDC_IN, DCDC_IN_Q, DCDC_DIG, DCDC_ANA	Not connected
	DCDC_DIG_SENSE, DCDC_ANA_SENSE, DCDC_LP, DCDC_LN	Not connected
	DCDC_PSWITCH, DCDC_MODE	To ground

Table 6. Recommended connections for unused analog interfaces (continued)

Module	Pad Name	Recommendations if Unused
USB	USB1_DN, USB1_DP, USB1_VBUS, USB2_DN, USB2_DP, USB2_VBUS	Not connected
	VDD_USB_1P8	Powered with 1.8 V
	VDD_USB_3P3	Powered with 3.3 V
SYS OSC	XTALI, XTALO	Not connected

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT1160 processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 7 for a quick reference to the individual tables and sections.

Table 7. i.MX RT1160 chip-Level conditions

For these characteristics	Topic appears
Absolute maximum ratings	on page 24
Thermal characteristics	on page 26
Operating ranges	on page 26
Maximum supply currents	on page 29
Typical power mode supply currents	on page 30
System power and clocks	on page 33

4.1.1 Absolute maximum ratings

CAUTION

Stress beyond those listed under Table 8 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 8 shows the absolute maximum operating ratings.

Table 8. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
Core supplies input voltage	VDD_SOC_IN	-0.3	1.2	V
Power for LPSR domain	VDD_LPSR_IN	-0.3	3.96	V
Power for DCDC	DCDC_IN	-0.3	3.96	V
Power for PLL, OSC, and LDOs	VDDA_1P8_IN	-0.3	1.98	V
Supply input voltage to Secure Non-Volatile Storage and Real Time Clock	VDD_SNVS_IN	-0.3	3.96	V
USB VBUS supply	USB1_VBUS USB2_VBUS	-0.3	5.6	V

Table 8. Absolute maximum ratings (continued)

Power for USB OTG PHYs	VDD_USB_1P8	-0.3	1.98	V
	VDD_USB_3P3	-0.3	3.96	V
Power for ADC, DAC, and ACMP	VDDA_ADC_1P8	-0.3	1.98	V
	VDDA_ADC_3P3	-0.3	3.96	V
Power for MIPI CSI/DSI PHY	VDD_MIPI_1P8	-0.3	1.98	V
	VDD_MIPI_1P0	-0.3	1.2	V
IO supply for GPIO in SDIO1 bank (3.3 V mode)	NVCC_SD1	-0.3	3.96	V
IO supply for GPIO in SDIO1 bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in SDIO2 bank (3.3 V mode)	NVCC_SD2	-0.3	3.96	V
IO supply for GPIO in SDIO2 bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in EMC bank1 (3.3 V mode)	NVCC_EMC1	-0.3	3.96	V
IO supply for GPIO in EMC bank1 (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in EMC bank2 (3.3 V mode)	NVCC_EMC2	-0.3	3.96	V
IO supply for GPIO in EMC bank2 (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in GPIO AD bank (3.3 V mode)	NVCC_GPIO	-0.3	3.96	V
IO power for GPIO in GPIO AD bank (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in DISP1 bank (3.3 V mode)	NVCC_DISP1	-0.3	3.96	V
IO supply for GPIO in DISP1 bank1 (1.8 V mode)		-0.3	1.98	V
IO supply for GPIO in DISP2 bank (3.3 V mode)	NVCC_DISP2	-0.3	3.96	V
IO supply for GPIO in DISP2 bank1 (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in LPSR bank (3.3 V mode)	NVCC_LPSR	-0.3	3.96	V
IO power for GPIO in LPSR bank (1.8 V mode)		-0.3	1.98	V
IO power for GPIO in SNVS bank (1.8 V mode)	NVCC_SNVS	-0.3	1.98	V
Input/Output Voltage range	V_{in}/V_{out}	-0.5	NVCC + 0.3[1]	V
Storage Temperature range	$T_{STORAGE}$	-40	150	°C

1 NVCC is the I/O supply voltage.

Table 9. Electrostatic discharge and latch-up characteristics

Symbol	Description	Min	Max	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1

Table 9. Electrostatic discharge and latch-up characteristics (continued)

Symbol	Description	Min	Max	Unit	Notes
V_{ESD}	Electrostatic discharge voltage, charged-device model				
	All pins except the corner pins	-500	+500	V	2
	Corner pins only	-750	+750	V	
I_{LAT}	Immunity level • Class II @105 °C ambient temperature	100	100	mA	3

1 Determined according to JEDEC Standard JS001, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).*

2 Determined according to JEDEC Standard JS002, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.*

3 Determined according o JEDEC Standard JESD78, *IC Latch-up Test*.

4.1.2 Thermal characteristics

Table 10 displays the 14 x 14 mm package thermal characteristics.

Table 10. 14 x 14 mm thermal characteristics

Rating	Board Type[1]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$[3]	31.6	°C/W
Junction to Top of Package Thermal Characterization Parameter[2]	JESD51-9, 2s2p	Ψ_{JT}[4]	1.4	°C/W
Junction to Case Thermal Resistance[5]	JESD51-9, 1s	$R_{\theta JC}$[6]	10	°C/W

1 Thermal test board meets JEDEC specification for this package (JESD51-9).

2 Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

3 $R_{\theta JA} = (T_j - T_a)/P$ [unit: °C/W], where T_j = junction temperature, T_a = ambient temperature, P = device power.

4 $\Psi_{JT} = (T_j - T_t)/P$ [unit: °C/W], where T_j = junction temperature, T_t = temperature at top of package, P = device power.

5 Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature is taken at the package top side centre surface temperature.

6 $R_{\theta JC} = (T_j - T_c)/P$ [unit: °C/W], where T_j = junction temperature, Tc = case temperature, P = device power.

4.1.3 Operating ranges

Table 11 provides the operating ranges of the i.MX RT1160 processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX RT1160 Reference Manual* (IMXRT1160RM).

Table 11. Operating ranges

Parameter Description	Symbol	Operating Conditions	Min	Max[1]	Unit	Comment
Run Mode	VDD_SOC_IN	M7 core at 500 MHz	1.0	1.15	V	—
		M7 core at 240 MHz	0.9	1.15	V	—
	VDD_LPSR_DIG	M4 core at 240 MHz	1.0	1.15	V	—
		M4 core at 120 MHz	0.9	1.15	V	—
STANDBY Mode	VDD_SOC_IN	M7 core	0.8	1.15	V	—
	VDD_LPSR_DIG	M4 core	0.8	1.15	V	—
Power for DCDC	DCDC_IN	—	3.0	3.6	V	—
Power for PLL, OSC, and LDOs	VDDA_1P8_IN	—	1.71	1.89	V	—
Power for LPSR domain	VDD_LPSR_IN	—	3.0	3.6	V	—
Power for SNVS and RTC	VDD_SNVS_IN	—	2.4	3.6	V	—
Power for USB OTG PHYs	VDD_USB_1P8	—	1.65	1.95	V	—
	VDD_USB_3P3	—	3.0	3.6	V	—
USB VBUS supply	USB1_VBUS USB2_VBUS	—	2.4	5.5	V	—
Power for ADC, DAC, and ACMP	VDDA_ADC_1P8	—	1.65	1.95	V	—
	VDDA_ADC_3P3	—	3.0	3.6	V	—
	ADC_VREFH	—	1.0	1.89	V	—
Power for MIPI CSI/DSI PHY	VDD_MIPI_1P8	—	1.65	1.95	V	—
	VDD_MIPI_1P0	—	0.9	1.1	V	—

Table 11. Operating ranges (continued)

GPIO supplies	NVCC_SD1	—	3.0	3.6	V	IO power for GPIO in SDIO1 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in SDIO1 bank (1.8 V mode)
	NVCC_SD2	—	3.0	3.6	V	IO power for GPIO in SDIO2 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in SDIO2 bank (1.8 V mode)
	NVCC_EMC1	—	3.0	3.6	V	IO power for GPIO in EMC bank1 (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in EMC bank1 (1.8 V mode)
	NVCC_EMC2	—	3.0	3.6	V	IO power for GPIO in EMC bank2 (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in EMC bank2 (1.8 V mode)
	NVCC_GPIO	—	3.0	3.6	V	IO power for GPIO in GPIO AD bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in GPIO AD bank (1.8 V mode)
	NVCC_DISP1	—	3.0	3.6	V	IO power for GPIO in DISP1 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in DISP1 bank (1.8 V mode)
	NVCC_DISP2	—	3.0	3.6	V	IO power for GPIO in DISP2 bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in DISP2 bank (1.8 V mode)
	NVCC_LPSR	—	3.0	3.6	V	IO power for GPIO in LPSR bank (3.3 V mode)
		—	1.65	1.95	V	IO power for GPIO in LPSR bank (1.8 V mode)
	NVCC_SNVS	—	1.65	1.95	V	IO power for GPIO in SNVS bank (1.8 V mode)
Temperature Operating Ranges						
Junction temperature	Tj	Standard Industrial	-40	105	°C	See the application note, i.MX RT1160 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor.

[1] Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This results in an optimized power/speed ratio.

4.1.4 Maximum supply currents

The data shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

Table 12. Maximum supply currents

Power Rail	Comments	Max Current	Unit
DCDC_IN	Max current for chip at 105 °C	1000	mA
VDDA_1P8_IN	1.8 V power supply for PLL, OSC, and LDOs	100	mA
VDD_SOC_IN	Power supply for digital logic	850	mA
VDD_LPSR_IN	3.3 V power supply for LPSR domain	75	mA
VDD_SNVS_IN	Power supply for SNVS domain	1	mA
VDD_USB_1P8	1.8 V power supply for USB OTG PHYs	50	mA
VDD_USB_3P3	3.3 V power supply for USB OTG PHYs	60	mA
VDDA_ADC_1P8	1.8 V power supply for ADC, DAC, and ACMP	10	mA
VDDA_ADC_3P3 ADC_VREFH	3.3 V power supply for ADC, DAC, and ACMP	2	mA
VDD_MIPI_1P8	1.8 V power supply for MIPI CSI/DSI PHY	4	mA
VDD_MIPI_1P0	1.0 V power supply for MIPI CSI/DSI PHY	30	mA
NVCC_SD1 NVCC_SD2 NVCC_EMC1 NVCC_EMC2 NVCC_GPIO NVCC_DISP1 NVCC_DISP2 NVCC_LPSR NVCC_SNVS	Imax = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F) In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.		

4.1.5 Typical power mode supply currents

Table 13 shows the current and power consumption (not including I/O) of i.MX RT1160 processors in selected power modes.

Table 13. Typical power modes current and power consumption (Dual core)

Modes	Test conditions	Power supplies at 3.3 V (Typical)[1]			Units
			25 °C Tj	105 °C Tj	
Set Point #0 Active	• CM7 runs at 500 MHz, drive voltage to 1.0 V; CM4 runs at 240 MHz, drive voltage to 1.0 V • CM7 domain bus frequency at 200 MHz; CM4 domain bus frequency at 120 MHz • Enables ECC for cache, TCM, and OCRAM • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • 16 MHz, 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under normal drive mode	DCDC_IN	83.4	137.6	mA
		VDD_LPSR_IN	28.1	30.8	µA
		VDD_SNVS_IN	4	12	µA
		Total	275.326	454.221	mW
Set Point #5 Active	• CM7 runs at 240 MHz, lower voltage to 0.9 V; CM4 runs at 120 MHz, lower voltage to 0.9 V • CM7 domain bus frequency at 100 MHz; CM4 domain bus frequency at 60 MHz • Enables ECC for cache, TCM, and OCRAM • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • 16 MHz, 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled • All PLLs are enabled • All peripherals are enabled and run at their maximum clock root frequency under underdrive mode	DCDC_IN	43.3	74.1	mA
		VDD_LPSR_IN	28.1	30.5	µA
		VDD_SNVS_IN	3.9	11.4	µA
		Total	142.996	244.668	mW
Set Point #7 Active	• CM7 runs at 200 MHz, lower voltage to 0.9 V; CM4 is clock gated, lower voltage to 0.9 V • CM7 domain bus frequency at 100 MHz • Enables ECC for cache, TCM, and OCRAM • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • 16 MHz, 400 MHz, and external 32 kHz crystal are enabled • All PLLs are power gated • All peripherals controlled by CM4 core are clock gated, but remain powered	DCDC_IN	24.9	52.6	mA
		VDD_LPSR_IN	28.1	30.3	µA
		VDD_SNVS_IN	3.9	11.1	µA
		Total	82.276	173.717	mW

Table 13. Typical power modes current and power consumption (Dual core) (continued)

Set Point #9 Active	• CM7 is clock gated, lower voltage to 0.9 V; CM4 runs at 100 MHz, lower voltage to 0.9 V • CM4 domain bus frequency at 50 MHz • Enables ECC for cache, TCM, and OCRAM • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • 16 MHz, 400 MHz, and external 32 kHz crystal are enabled • All PLLs are power gated • All peripherals controlled by CM7 core are clock gated, but remain powered	DCDC_IN	14.5	39.5	mA
		VDD_LPSR_IN	28.2	30.2	μA
		VDD_SNVS_IN	3.9	11	μA
		Total	47.956	130.486	mW
Set Point #11 Active	• CM7 is power off; CM4 runs at 200 MHz, drive voltage to 1.0 V • CM4 domain bus frequency at 100 MHz • Enables ECC for CM4 TCM and OCRAM • DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active • 16 MHz, 400 MHz, and external 32 kHz crystal are enabled • All PLLs are power gated • The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated • All peripherals in LPSRMIX domain are clocked	DCDC_IN	26.5	41.8	μA
		VDD_LPSR_IN	38.2	46.9	mA
		VDD_SNVS_IN	3.9	11.3	μA
		Total	126.160	154.945	mW
Set Point #12 Active	• CM7 is power off; CM4 runs at 100 MHz, lower voltage to 0.9 V • CM4 domain bus frequency at 50 MHz • Enables ECC for CM4 TCM and OCRAM • DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active • 16 MHz, 400 MHz, and external 32 kHz crystal are enabled • All PLLs are power gated • The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated • All peripherals in LPSRMIX domain are clocked	DCDC_IN	26.2	41.1	μA
		VDD_LPSR_IN	22.9	28.9	mA
		VDD_SNVS_IN	3.9	11	μA
		Total	75.669	95.542	mW
Set Point #0 Standby Suspend	• System is on STANDBY mode • Both CM7 and CM4 are on SUSPEND mode • TCM with ECC is on retention • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • All peripherals are clock gated, but remain powered	DCDC_IN	3	19.4	mA
		VDD_LPSR_IN	29.9	41.1	μA
		VDD_SNVS_IN	3.9	10.8	μA
		Total	10.012	64.191	mW

Table 13. Typical power modes current and power consumption (Dual core) (continued)

Set Point #5 Standby Suspend	• System is on STANDBY mode • Both CM7 and CM4 are on SUSPEND mode • TCM with ECC is on retention • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • All peripherals are clock gated, but remain powered	DCDC_IN	2.3	14.6	mA
		VDD_LPSR_IN	29.8	41.3	μA
		VDD_SNVS_IN	3.8	10.7	μA
		Total	7.701	48.352	mW
Set Point #7 Standby Suspend	• System is on STANDBY mode • Both CM7 and CM4 are on SUSPEND mode • TCM with ECC is on retention • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • All peripherals are clock gated, but remain powered	DCDC_IN	2.3	14.6	mA
		VDD_LPSR_IN	29.8	41.3	μA
		VDD_SNVS_IN	3.8	10.7	μA
		Total	7.701	48.352	mW
Set Point #10 Standby Suspend	• Lower voltage to 0.8 V with RBB mode for both SOC and LPSR domains • System is on STANDBY mode • Both CM7 and CM4 are on SUSPEND mode • TCM with ECC is on retention • LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • All peripherals are clock gated, but remain powered	DCDC_IN	1.8	11	mA
		VDD_LPSR_IN	29.7	41.2	μA
		VDD_SNVS_IN	3.8	10.7	μA
		Total	6.051	36.471	mW
Set Point #11 Standby Suspend	• System is on STANDBY mode • CM7 is power off, CM4 is on SUSPEND mode • CM4 TCM with ECC is on retention • DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated • All peripherals in LPSRMIX domain are clock gated, but remain powered	DCDC_IN	26.1	40.8	μA
		VDD_LPSR_IN	0.893	7.1	mA
		VDD_SNVS_IN	3.8	10.6	μA
		Total	3.046	23.600	mW

Table 13. Typical power modes current and power consumption (Dual core) (continued)

Set Point #15 Standby Suspend	• Lower voltage to 0.8 V with RBB mode for LPSR domain • System is on STANDBY mode • CM7 is power off, CM4 is on SUSPEND mode • CM4 TCM with ECC is on retention • DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active • All clock sources are turned off except for 32 kHz RTC • All PLLs are power gated • The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated • All peripherals in LPSRMIX domain are clock gated, but remain powered	DCDC_IN	26.1	40.6	µA
		VDD_LPSR_IN	0.503	4.6	mA
		VDD_SNVS_IN	3.8	10.6	µA
		Total	1.759	15.349	mW
SNVS	• Only SNVS domain is powered • 32 kHz RTC is alive • DCDC_IN and VDD_LPSR_IN are power gated	DCDC_IN	0	0	µA
		VDD_LPSR_IN	0	0	µA
		VDD_SNVS_IN	3.8	10.7	µA
		Total	12.54	35.31	µW

1 Code runs in the ITCM; typical values are the average values on typical process wafers.

Table 14 shows the typical wakeup time.

Table 14. Typical wakeup time[1]

Description	Typical wakeup time	Unit
From Set Point #0 Standby Suspend to Set Point #0 normal drive RUN	4.13	ms
From Set Point #5 Standby Suspend to Set Point #0 normal drive RUN	4.79	ms
From Set Point #10 Standby Suspend to Set Point #0 normal drive RUN	5.47	ms
From Set Point #15 Standby Stop to Set Point #0 normal drive RUN	7.6	ms
From SNVS mode to ROM exit	8.54	ms

1 Please refer to Table 13 for Set Point modes definition, and the only difference between Set Point #15 Standby Suspend mode and Set Point #15 Standby Stop mode is the Suspend mode versus Stop mode on CM4 core.

4.2 System power and clocks

This section provides the information about the system power and clocks.

4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting

- Irreversible damage to the processor (worst-case scenario)

Figure 4 shows the power sequence.

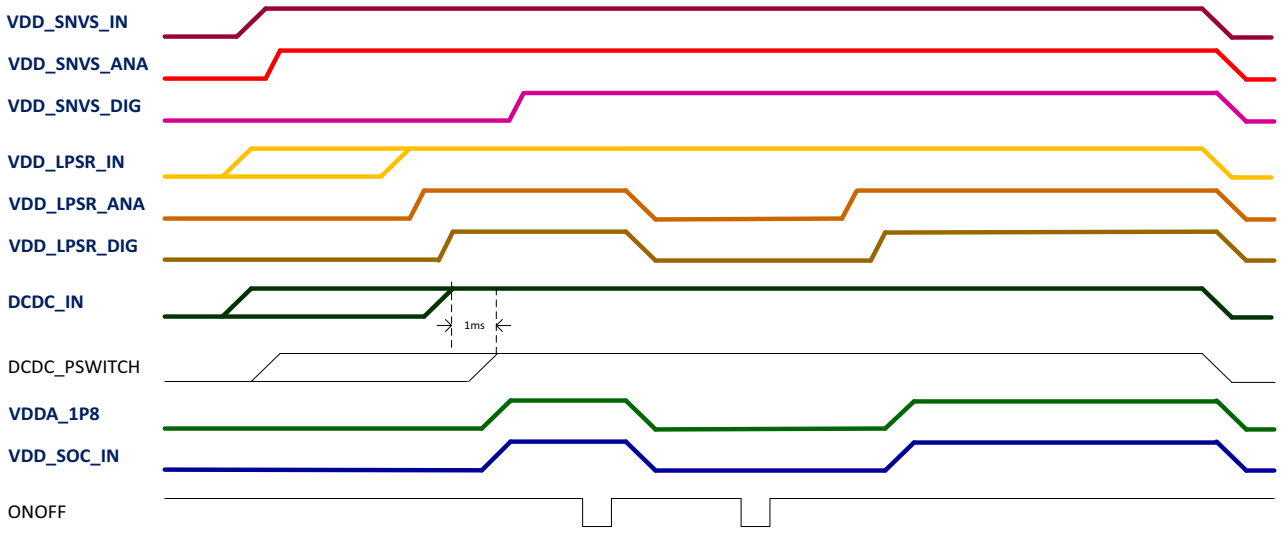


Figure 4. Power sequence

4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_LPSR_IN and DCDC_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- An RC delay circuit is recommended for providing the delay between DCDC_IN stable and DCDC_PSWITCH. The total RC delay should be 5 – 40 ms.
- DCDC_IN must reach a minimum 3.0 V within 0.3 x RC.
- Delay from DCDC_IN stable at 3.0 V min to DCDC_PSWITCH reaching 0.5 x DCDC_IN (1.5 V) must be at least 1 ms.
- Power up slew rate specification for other power domains is 360 V/s – 36 KV/s.
- Ensure VDD_LPSR_DIG powered prior to VDD_SOC_IN.

NOTE

If expect to release MCU by POR_B signal, the POR_B input must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for further details and to ensure that all necessary requirements are being met.

NOTE

The voltage on DCDC_PSWITCH pin should be below 0.5 V before ramping up the voltage on DCDC_PSWITCH.

NOTE

The power rail VDD_SNVS_DIG is controlled by software.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB1_VBUS, USB2_VBUS, and VDDA_ADC_3P3 are not part of the power supply sequence and may be powered at any time.

4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_LPSR_IN and DCDC_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off.

4.2.1.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, Package information and contact assignments.”

4.2.2 Internal POR and power detect

Internal detector monitors VDD_SOC_IN and VDD_LPSR_DIG. Internal POR will be asserted whenever VDD_SOC_IN or VDD_LPSR_DIG are lower than the valid voltage values shown in the Table 15.

Table 15. Internal POR and power detect

Symbol	Description	Value	Unit
$V_{detlpsr1p0\_H}$	1.0 V supply valid	0.75	V
$V_{detsoc1p0\_H}$	1.0 V supply valid	0.75	V
$Hyst_{det1p0}$	The detector hysteresis	100	mV

4.2.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. The on-chip LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for details on the power tree scheme.

4.2.3.1 LDO_SNVS_ANA

Table 16 shows the parameters of LDO_SNVS_ANA.

Table 16. LDO_SNVS_ANA specification

Specification	Min	Typ	Max	Unit
VDD_SNVS_IN	2.4	3	3.6	V
VDD_SNVS_ANA	1.65	1.75	1.95	V
I_out	—	—	1	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.2 LDO_SNVS_DIG

Table 17 shows the parameters of LDO_SNVS_DIG.

Table 17. LDO_SNVS_DIG specification

Specification	Min	Typ	Max	Unit
VDD_SNVS_ANA	1.65	1.75	1.95	V
VDD_SNVS_DIG	0.65	0.85	0.95	V
I_out	—	—	1	mA
External decoupling capacitor	—	0.22	—	μF

4.2.3.3 LDO_PLL

Table 18 shows the parameters of LDO_PLL.

Table 18. LDO_PLL specification

Specification	Min	Typ	Max	Unit
VDDA_1P8_IN	1.71	1.8	1.89	V
VDDA_1P0	0.9	1	1.2	V
I_out	—	—	70	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.4 LPSR_LDO_DIG

LPSR_LDO_DIG provides 1.0 V power source (VDD_LPSR_DIG) from 1.8V power domain (VDD_LPSR_ANA). The trim voltage range of LDO output is from 0.7 V to 1.15 V. There are two work modes: Low Power mode and High Power mode. In typical PVT case, the static current consumption is less than 3 μA in Low Power mode. The maximum drive strength of this LDO regulator is 50 mA in High Power mode.

Table 19. LPSR_LDO_DIG specification

Specification	Min	Typ	Max	Unit
VDD_LPSR_ANA	1.71	1.8	1.89	V
VDD_LPSR_DIG	0.7	1	1.15	V
I_out	—	—	50	mA
External decoupling capacitor	—	2.2	—	μF

4.2.3.5 LPSR_LDO_ANA

LPSR_LDO_ANA provides 1.8 V power source (VDD_LPSR_ANA) from 3.3 V power domain (VDD_LPSR_IN). Its default output value is 1.8 V. Two work modes are supported by this LDO: Low Power mode and High Power mode. In Low Power mode, the LDO provides 2 mA (maximum value) by consuming only 4 μA current. In High Power mode, the LDO provides 75 mA current capacity with 40 μA static power dissipation.

Table 20. LPSR_LDO_ANA specification

Specification	Min	Typ	Max	Unit
VDD_LPSR_IN	3	3.3	3.6	V
VDD_LPSR_ANA	—	1.8	—	V
I_out	—	—	75	mA
External decoupling capacitor	—	4.7	—	μF

4.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.

On-chip regulators are designed to power on-chip load only. Do not use on-chip regulators to power external loads. DCDC_DIG is used to power VDD_SOC_IN. DCDC_ANA is a low-noise power rail used to power on-chip analog loads only.

Table 21 shows DCDC characteristics.

Input voltage refers to DCDC_IN balls. 1.0 V output refers to DCDC_DIG balls. 1.8 V output refers to DCDC_ANA balls.

Table 21. DCDC characteristics[1]

Description	Min	Typ	Max	Unit	Comments
Input voltage	3	3.3	3.6	V	—
Output voltage					
• 1.0 V output	0.6	1	1.375	V	25 mV per step
• 1.8 V output	1.5	1.8	2.275	V	25 mV per step
Loading					
• 1.0 V output	—	150	850	mA	—
• 1.8 V output	—	80	150	mA	Consider 1.8 V supply currents in Table 12 to ensure no DCDC overload. Add currents for active modules per use case.
Efficiency					
• DCDC run mode	—	80%	—	—	150 mA@vdd1p0 80 mA@vdd1p8
• DCDC low power mode	—	80%	—	—	300 μA@vdd1p0 300 μA@vdd1p8
Output voltage accuracy					

Table 21. DCDC characteristics[1]

Description	Min	Typ	Max	Unit	Comments
• DCDC Run mode	-2.5%	—	2.5%	—	Maximum 50 mV Vp-p@vdd1p0
• DCDC Low power mode	-6%	—	6%	—	—
Over current detection	—	1.5	—	A	The typical value can be configured as 1.5 A and 2 A by register.
Over voltage detection					
• Output 1.8 V	—	2.5	2.75	V	—
• Output 1.0 V	—	1.5	1.65	V	—
• Low DCDC_IN detection	—	2.6	2.8	V	—
Leakage current	—	3	—	μA	DCDC off
Quiescent current					
• DCDC Run mode	—	150	—	μA	—
• DCDC Low power mode	—	5	—	μA	—
Capacitor value	—	33 (DCDC_ANA) 66 (DCDC_DIG)	—	μF	High frequency capacitor are also required.
Inductor value	—	4.7	—	μH	—
• Saturation current	—	1	—	A	—

[1] Values in this table are based on CZ test with limited matrix samples in lab environment.

For additional information, see the *i.MX RT1160 Reference Manual* (IMXRT1160RM).

4.2.5 PLL's electrical characteristics

This section provides PLL electrical characteristics.

4.2.5.1 Audio/Video PLL's electrical parameters

Table 22. Audio/Video PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range	650	—	1300	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles

Table 22. Audio/Video PLL's electrical parameters (continued)

Parameter	Min	Typ	Max	Unit
Period jitter (p2p)	—	50	—	ps
Duty cycle	48.5	—	51.5	%

4.2.5.2 528 MHz PLL

Table 23. 528 MHz PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range	—	—	528	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles
Period jitter (p2p)	—	50	—	ps
PFD period jitter (p2p)	—	100	—	ps
Duty cycle	45	—	55	%

4.2.5.3 Ethernet PLL

Table 24. Ethernet PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range	—	—	1000	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	11250	reference cycles
Period jitter (p2p)	—	50	—	ps
Duty cycle	47.5	—	52.5	%

4.2.5.4 480 MHz PLL

Table 25. 480 MHz PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range	—	—	480	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	383	reference cycles
Period jitter (p2p)	—	40	—	ps

Table 25. 480 MHz PLL's electrical parameters (continued)

Parameter	Min	Typ	Max	Unit
PFD period jitter (p2p)	—	125	—	ps
Duty cycle	45	—	55	%

4.2.5.5 Arm PLL

Table 26. Arm PLL's electrical parameters

Parameter	Min	Typ	Max	Unit
Clock output range	156	—	2496	MHz
Reference clock	—	24	—	MHz
Lock time	—	—	2250	reference cycles
Period jitter (p2p)	—	15	—	ps
Duty cycle	45	—	55	%

4.2.6 On-chip oscillators

The system oscillator (SYS OSC) is a crystal oscillator. The SYS OSC, in conjunction with an external crystal or resonator, generates a reference clock for this chip. It also provides the option for an external input clock to XTALI signal directly.

Table 27. 24 MHz system oscillator frequency specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDA} (Low power mode)	Analog supply current	24 MHz	—	0.5	—	mA
I_{VDDA} (High gain mode)	Analog supply current	24 MHz	—	1.3	—	mA
R_F	Feedback resistor	Low-power mode	No need			
		High-gain mode	—	1	—	MΩ
R_S	Series resistor[1]	—	—	0	—	kΩ
C_XC_Y	XTALI/XTALO load capacitance	See crystal or resonator manufacture's recommendation				
C_{para}	Parasitically capacitance of XTALI and XTALO	—	—	1.5	2.0	pF
Clock output						
F_{OSC}	Oscillator crystal or resonator frequency	—	—	24	—	MHz
t_{dcy}	Duty-cycle of the output clock	—	40	50	60	%
Dynamic parameters						

Table 27. 24 MHz system oscillator frequency specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PP}	Peak-peak amplitude of oscillation	Low-power mode	—	0.8	—	V
		High gain mode	0.75x VDDA_1P8_IN	0.8 x VDDA_1P8_IN	—	V
t_{start}	Start-up time from OSC_24M_CNTL[OSC_EN] set to oscillator stable[2]	24 MHz low-power mode	—	250	—	µs
		24 MHz high-gain mode	—	250	—	µs

1 Depends on the drive level of external crystal device

2 Oscillator hardware default is OFF at power-up, so requires firmware or software to enable.

Each i.MX RT1160 processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the clock source from RTC_XTALI. The internal ring oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP recommends using an external crystal as the clock source for RTC_XTALI. If the internal clock oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 28. 32 kHz oscillator specifications

Symbol	Description	Min	Typ	Max	Unit	Note
C_{para}	Parasitically capacitance of RTC_XTALI and RTC_XTALO	—	1.5	2.0	pF	—
V_{pp}	Peak-to-peak amplitude of oscillator	—	0.6	—	V	1
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	—
t_{start}	Crystal startup time from VDD_SNVS_ANA ramp-up to minimum operating voltage to oscillator stable	—	500	—	ms	1
$V_{ec\_extal32}$	Externally provided input clock amplitude	0.7	—	VDD_SNVS_ANA	V	2,3

1 Proper PCB layout procedures must be followed to achieve specifications.

2 This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.

[3] The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to VDD_SNVS_ANA.

The RTC OSC module provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.

Table 29. RC oscillator with 16 MHz internal reference frequency

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock output						
F_{clkout_16M}	Clock frequency	—	15.1	16	16.9	MHz
Dynamic parameters						
T_{start_16M}	Start-up time from VDD_LPSR_ANA ramp-up to minimum operating voltage to oscillator stable	—	—	50	—	μs
Power-down mode						
I_{VDDA}	Supply current in power-down	—	1	2	95	nA

Table 30. RC oscillator with 48 MHz internal reference frequency

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General						
I_{VDDA}	Analog supply current	—	—	350	500	μA
Clock output						
F_{clkout}	Clock frequency	—	—	48	—	MHz
Dynamic parameters						
T_{start}	Start-up time from VDD_LPSR_ANA ramp-up to minimum operating voltage to oscillator stable	—	—	2.5	—	μs
Accuracy						
T_{target}	Trimmed	—	-2	—	2	%

Table 31. RC oscillator with 400 MHz internal reference frequency

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General						
$I_{VDD\_1P8V\_ON}$	Analog supply current	—	—	60	—	μA
I_{VDD_ON}	Digital supply current	—	—	80	—	μA
Clock output						

Table 31. RC oscillator with 400 MHz internal reference frequency (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_tuned	Tuned clock frequency	—	—	400	—	MHz
ΔF/F	Frequency error after tuning	—	—	0.1	—	%
Dynamic parameters						
J_{PP-CC}	Peak-peak, period jitter	—	—	50	—	ps
t_{start}	Start-up time from OSC_400M_CTRL1[PWD] is cleared to oscillator stable[1]	—	—	1	—	μs
t_{tune}	Tuning time	—	1	—	256	μs

1 Oscillator hardware default is OFF at power-up, so requires firmware or software to enable.

Table 32. RC oscillator with 32 kHz internal reference frequency

Symbol	Description	Min	Typ	Max	Unit	Note
f_{irc32k}	Internal reference frequency	—	32	—	kHz	—
Δf_{irc32k}	Deviation of IRC32K frequency	-25%	—	25%	$\%f_{irc32k}$	—

4.3 I/O parameters

This section provides parameters on I/O interfaces.

4.3.1 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (Clock Inputs) DC Parameters
- General Purpose I/O (GPIO)

NOTE

The term ‘NVCC_XXXX’ in this section refers to the associated supply rail of an input or output.

NOTE

When enable the open drain for I/O pad, the external pull-up voltage cannot exceed the associated supply rail.

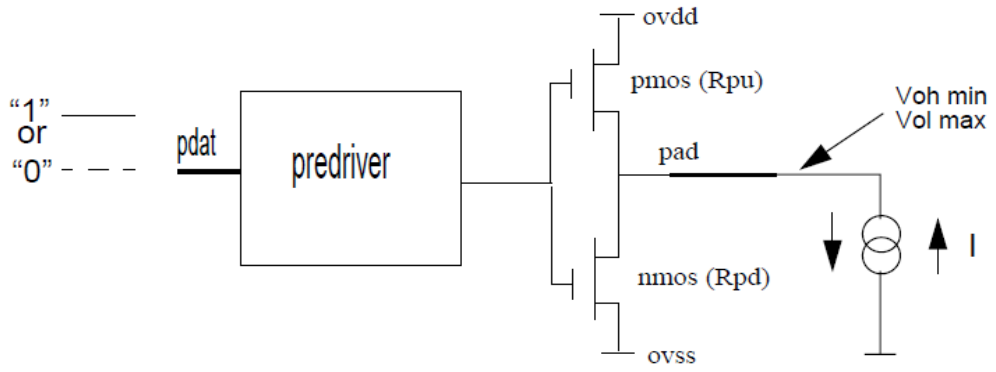


Figure 5. Circuit for parameters Voh and Vol for I/O cells

4.3.1.1 XTALI and RTC_XTALI (clock inputs) DC parameters

Table 33 shows the DC parameters for the clock inputs.

Table 33. XTALI and RTC_XTALI DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Unit
XTALI high-level DC input voltage	Vih	—	VDDA_1P8_IN - 0.5	VDDA_1P8_IN	V
XTALI low-level DC input voltage	Vil	—	0	0.5	V
RTC_XTALI high-level DC input voltage	Vih	—	VDD_SNVS_ANA - 0.5	VDD_SNVS_ANA	V
RTC_XTALI low-level DC input voltage	Vil	—	0	0.5	V

[1] The DC parameters are for external clock input only.

4.3.1.2 General purpose I/O (GPIO) DC parameters

Following section introduces the GPIO DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 11 unless otherwise noted.

Table 34. DC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1 bank

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Receiver 3.3 V						
High level input voltage	V_{IH}	0.625 x NVCC	—	NVCC + 0.3	V	—
Low level input voltage	V_{IL}	-0.3	—	0.25 x NVCC	V	—
Receiver 1.8 V						
High level input voltage	V_{IH}	0.65 x NVCC	—	NVCC + 0.3	V	—
Low level input voltage	V_{IL}	-0.3	—	0.35 x NVCC	V	—
Driver 3.3 V and driver 1.8 V for PDRV = L and PDRV = H						

Table 34. DC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1 bank (continued)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Output high current	I_{OH}	-6	—	—	mA	V_{OH} = 0.8 x NVCC
Output low current	I_{OL}	6	—	—	mA	V_{OL} = 0.2 x NVCC
Output low/high current total for each IO bank	I_{OCT}	—	—	100	mA	—
Weak pull-up and pull-down						
Pull-up / pull-down resistance	R_{High}	10	—	100	kΩ	High voltage range (2.7 V - 3.6 V)
Pull-up / pull-down resistance	R_{Low}	20	—	50	kΩ	Low voltage range (1.65 V - 1.95 V)

Table 35. DC specification for GPIO_SNVS bank[1]

Parameter	Symbol	Min	Typ[2]	Max	Unit	Condition
High level input voltage	V_{IH}	0.7 x NVCC_SNVS	—	NVCC_SNVS + 0.1	V	—
Low level input voltage	V_{IL}	-0.3	—	0.3 x NVCC_SNVS	V	—
Output high current	I_{OH}	—	-45	—	μA	V_{OH} = NVCC_SNVS - 0.3
Output low current	I_{OL}	—	50	—	μA	V_{OL} = 0.3
Output low/high current total for GPIO_SNVS bank	I_{OCT}	—	—	1	mA	—
Weak pull-up and pull-down						
Pull-up and pull-down resistance	R_{High}/ R_{Low}	100	200	600	kΩ	—

1 By default, functionality of GPIO_SNVS_XX port is determined by the part number. Tamper function is available only on tamper-enabled parts, and GPIO is the only available function on parts which do not support tamper.

2 Typical numbers are not guaranteed.

Table 36. DC specification for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank

NO.	Characteristics	Test Conditions	Min	Max	Units
1	Input high voltage (V_{IH})	Normal voltage range	0.7 x NVCC	NVCC + 0.1	V
		Derated voltage range	0.75 x NVCC	NVCC + 0.1	V
		Derated2 voltage range	0.75 x NVCC	NVCC + 0.1	V
		Low voltage range	0.7 x NVCC	NVCC + 0.1	V
		High voltage range	0.7 x NVCC	NVCC + 0.1	V

Table 36. DC specification for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank (continued)

NO.	Characteristics	Test Conditions	Min	Max	Units
2	Input low voltage (V_{IL})	Normal voltage range	- 0.3	0.3 x NVCC	V
		Derated voltage range	- 0.3	0.25 x NVCC	V
		Derated2 voltage range	- 0.3	0.25 x NVCC	V
		Low voltage range	- 0.3	0.3 x NVCC	V
		High voltage range	- 0.3	0.3 x NVCC	V
3	Input Hysteresis (VHYSN)	All voltage range	0.06 x NVCC	—	V
4	Output high voltage (V_{OH}) DSE = 1	Normal voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
		Derated voltage range I_{OH} = -6 mA	NVCC - 0.5	—	V
		Derated2 voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		Low voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
		High voltage range I_{OH} = -10 mA	NVCC - 0.5	—	V
5	Output high voltage (V_{OH}) DSE = 0	Normal voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		Derated voltage range I_{OH} = -3 mA	NVCC - 0.5	—	V
		Derated2 voltage range I_{OH} = -2.5 mA	NVCC - 0.5	—	V
		Low voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
		High voltage range I_{OH} = -5 mA	NVCC - 0.5	—	V
6	Output low voltage (V_{OL}) DSE = 1	Normal voltage range I_{OL} = 10 mA	—	0.5	V
		Derated voltage range I_{OL} = 6 mA	—	0.5	V
		Derated2 voltage range I_{OL} = 5 mA	—	0.5	V
		Low voltage range I_{OL} = 10 mA	—	0.5	V
		High voltage range I_{OL} = 10 mA	—	0.5	V

Table 36. DC specification for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank (continued)

NO.	Characteristics	Test Conditions	Min	Max	Units
7	Output low voltage (V_{OL}) DSE = 0	Normal voltage range I_{OL} = 5 mA	—	0.5	V
		Derated voltage range I_{OL} = 3 mA	—	0.5	V
		Derated2 voltage range I_{OL} = 2.5 mA	—	0.5	V
		Low voltage range I_{OL} = 5 mA	—	0.5	V
		High voltage range I_{OL} = 5 mA	—	0.5	V
8	NVCC	Normal voltage range	2.7	3.6	V
		Derated voltage range	1.98	2.7	V
		Derated2 voltage range	1.71	1.98	V
		Low voltage range	1.71	1.98	V
		High voltage range	3	3.6	V
11	Pull-up resistor range (R_{PU}) Measure @V_{DD}	All voltage range	25	50	kΩ
12	Pull-down resistor range (R_{PD}) Measure @V_{SS}	All voltage range	25	50	kΩ
13	Input leakage current	All voltage range	—	400	nA
14	Output capacitance (CL)	All voltage range	—	15	pF
15	Input capacitance (Cin)	All voltage range	—	5	pF
16	Output low/high current total for each IO bank (I_{OCT})	All voltage range	—	100	mA

4.3.2 I/O AC parameters

The GPIO and DDR I/O load circuit and output transition time waveform are shown in Figure 6 and Figure 7.

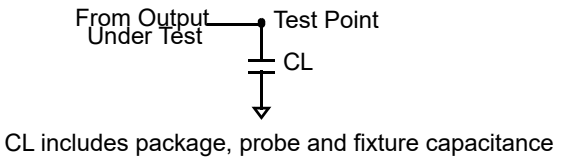


Figure 6. Load circuit for output

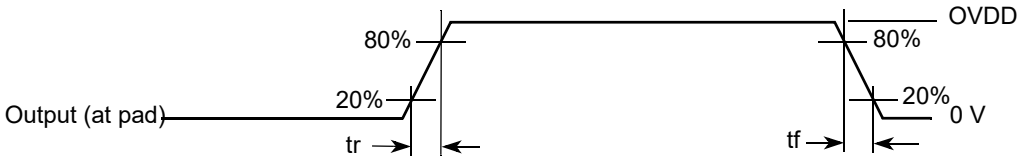


Figure 7. Output transition time waveform

4.3.2.1 General purpose I/O (GPIO) AC parameters

The I/O AC parameters for GPIO are presented in the Table 37 and Table 38, respectively.

Table 37. AC specification for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1 bank

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Driver 1.8 V application						
f_{max}	Maximum frequency	Load = 21 pF (PDRV = L, high drive, 33 Ω)	—	—	208	MHz
		Load = 15 pF (PDRV = H, low drive, 50 Ω)				
tr	Rise time	Measured between V_{OL} and V_{OH}	0.4	—	1.32	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	0.4	—	1.32	ns
Driver 3.3 V application						
f_{max}	Maximum frequency	Load = 20 pF	—	—	200	MHz
tr	Rise time	Measured between V_{OL} and V_{OH}	—	—	3	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	—	—	3	ns

Table 38. Dynamic input characteristics for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1 bank

Symbol	Parameter	Test Condition[1, 2]	Min	Max	Unit
Dynamic Input Characteristics for 3.3 V Application					
f_{op}	Input frequency of operation	—	—	200	MHz
Dynamic Input Characteristics for 1.8 V Application					
f_{op}	Input frequency of operation	—	—	208	MHz

1 For all supply ranges of operation.

2 The dynamic input characteristic specifications are applicable for the digital bidirectional cells.

Table 39. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank

NO.	Characteristic	Condition	Min	Max	Unit
1	f_{max}	Cload = 15 pF	—	104	MHz
2	Pad rise/fall time (DSE = 0, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	3	ns
		Derated voltage range (Cload = 15 pF)	—	5	ns
		Derated2 voltage range (Cload = 15 pF)	—	6	ns
		Low voltage range (Cload = 15 pF)	—	3	ns
		High voltage range (Cload = 15 pF)	—	3	ns
3	Pad rise/fall time (DSE = 0, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	6	ns
		Derated voltage range (Cload = 15 pF)	—	10	ns
		Derated2 voltage range (Cload = 15 pF)	—	12	ns
		Low voltage range (Cload = 15 pF)	—	6	ns
		High voltage range (Cload = 15 pF)	—	6	ns
4	Pad rise/fall time (DSE = 1, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2.5	ns
		Derated voltage range (Cload = 15 pF)	—	4.5	ns
		Derated2 voltage range (Cload = 15 pF)	—	5	ns
		Low voltage range (Cload = 15 pF)	—	2.5	ns
		High voltage range (Cload = 15 pF)	—	2.5	ns

Table 39. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank (continued)

NO.	Characteristic	Condition	Min	Max	Unit
5	Pad rise/fall time (DSE = 1, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	5	ns
		Derated voltage range (Cload = 15 pF)	—	9	ns
		Derated2 voltage range (Cload = 15 pF)	—	10	ns
		Low voltage range (Cload = 15 pF)	—	5	ns
		High voltage range (Cload = 15 pF)	—	5	ns
6	IPP_DO to pad propagation delay: (DSE = 0, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2.5	ns
		Derated voltage range (Cload = 15 pF)	—	4.5	ns
		Derated2 voltage range (Cload = 15 pF)	—	5	ns
		Low voltage range (Cload = 15 pF)	—	2.5	ns
		High voltage range (Cload = 15 pF)	—	4	ns
7	IPP_DO to pad propagation delay: (DSE = 0, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	7	ns
		Derated voltage range (Cload = 15 pF)	—	12	ns
		Derated2 voltage range (Cload = 15 pF)	—	14	ns
		Low voltage range (Cload = 15 pF)	—	7	ns
		High voltage range (Cload = 15 pF)	—	8.5	ns
8	IPP_DO to pad propagation delay: (DSE = 1, SRE = 0)	Normal voltage range (Cload = 15 pF)	—	2	ns
		Derated voltage range (Cload = 15 pF)	—	3.6	ns
		Derated2 voltage range (Cload = 15 pF)	—	4	ns
		Low voltage range (Cload = 15 pF)	—	2	ns
		High voltage range (Cload = 15 pF)	—	4	ns

Table 39. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank (continued)

NO.	Characteristic	Condition	Min	Max	Unit
9	IPP_DO to pad propagation delay: (DSE = 1, SRE = 1)	Normal voltage range (Cload = 15 pF)	—	6	ns
		Derated voltage range (Cload = 15 pF)	—	11	ns
		Derated2 voltage range (Cload = 15 pF)	—	12	ns
		Low voltage range (Cload = 15 pF)	—	6	ns
		High voltage range (Cload = 15 pF)	—	7.5	ns

Figure 8 is the GPIO block diagram.

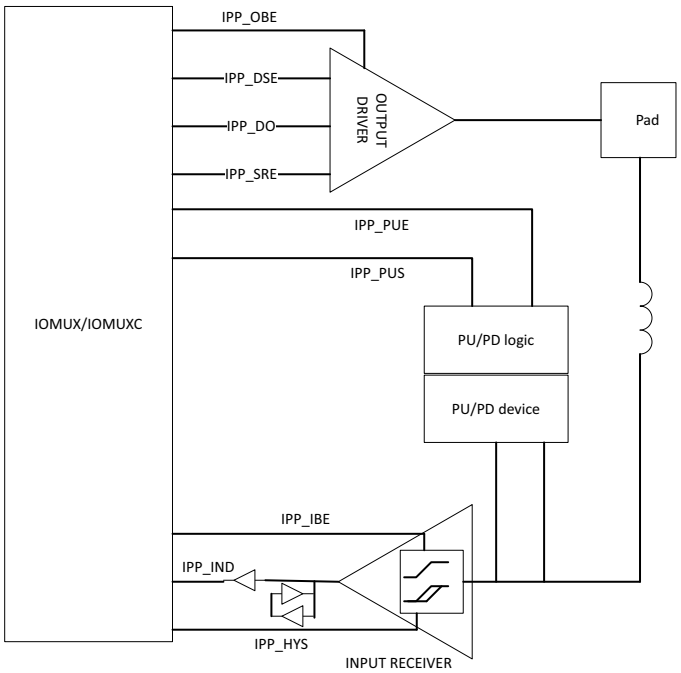


Figure 8. GPIO block diagram

4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1160 processor.

4.4.1 Reset timing parameters

Figure 9 shows the POR reset timing and Table 40 lists the timing parameters.

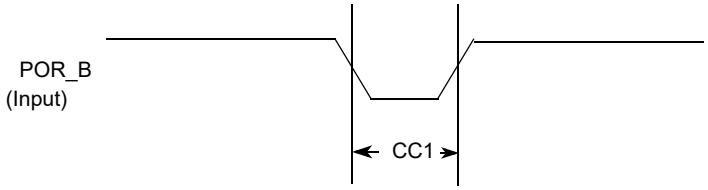


Figure 9. POR reset timing diagram

Table 40. POR reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.4.2 WDOG reset timing parameters

Figure 10 shows the WDOG reset timing and Table 41 lists the timing parameters.

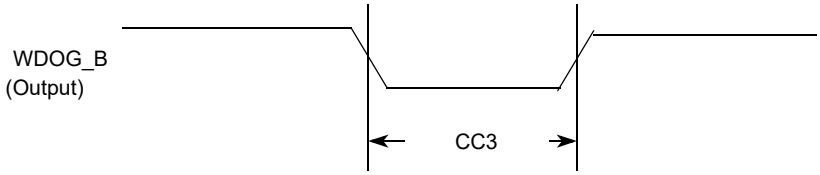


Figure 10. WDOG_B timing diagram

Table 41. WDOG_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.4.3 JTAG Controller timing parameters

Figure 11 depicts the JTAG controller timing. Figure 12 depicts the JTAG TRST_B timing.

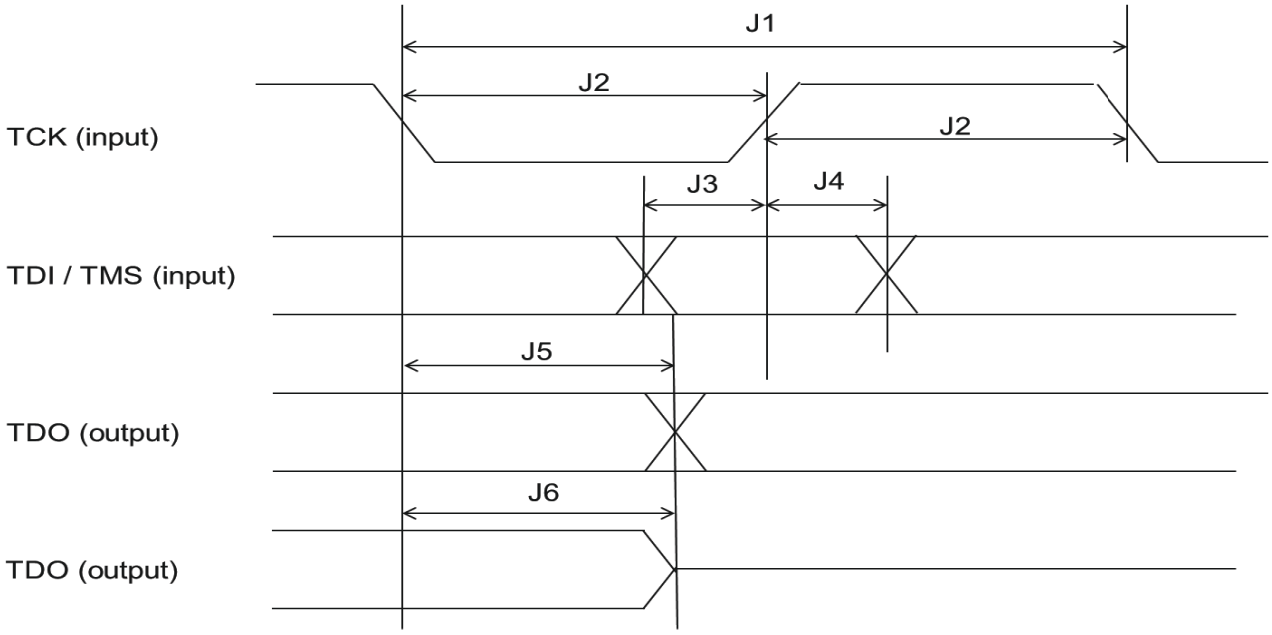


Figure 11. JTAG controller timing

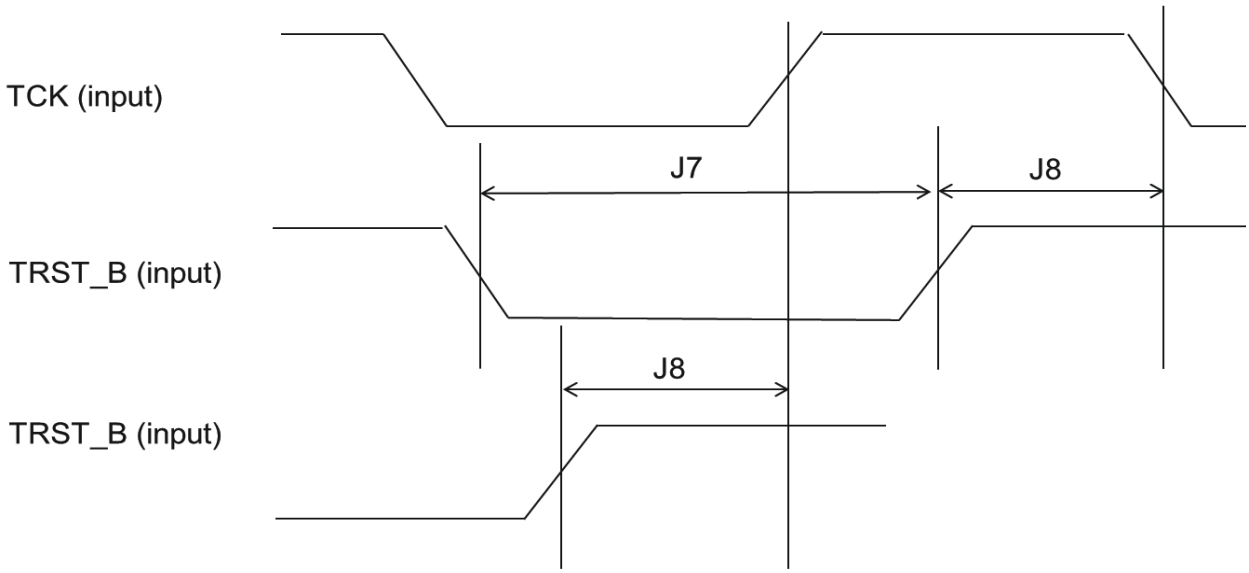


Figure 12. JTAG_TRST_B timing

Table 42. JTAG timing parameters

ID	Parameter	Value		Unit
		Min	Max	
J0	TCK frequency	—	25	MHz
J1	TCK cycle time	40	—	ns
J2	TCK pulse width	20	—	ns
J3	Input data setup time	5	—	ns
J4	Input data hold time	5	—	ns
J5	Output data valid time	—	15.2	ns
J6	Output high impedance time	—	15.2	ns
J7	TRST_B assert time	100	—	ns
J8	TRST_B setup time to TCK edge	18	—	ns

4.4.4 SWD timing parameters

Figure 13 depicts the SWD timing.

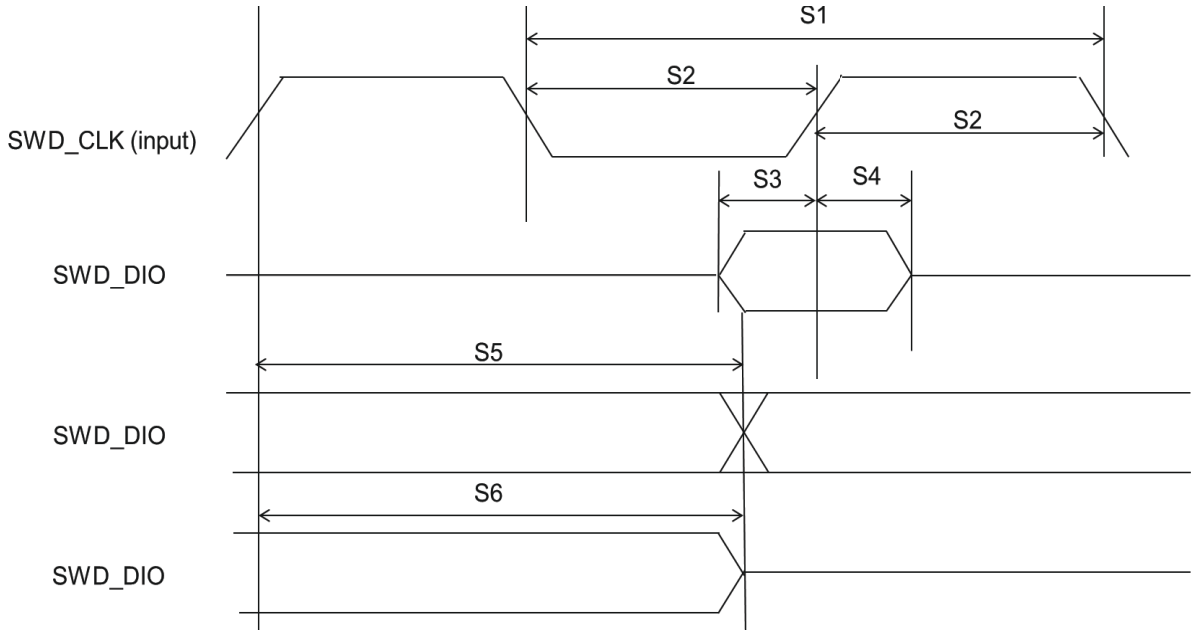


Figure 13. SWD timing

Table 43. SWD timing parameters

Symbol	Description	Min	Max	Unit
S0	SWD_CLK frequency	—	50	MHz
S1	SWD_CLK cycle time	20	—	ns
S2	SWD_CLK pulse width	10	—	ns
S3	Input data setup time	5	—	ns
S4	Input data hold time	1	—	ns
S5	Output data valid time	—	14.4	ns
S6	Output high impedance time	—	14.4	ns

4.4.5 Trace timing parameters

Figure 14 depicts the trace timing.

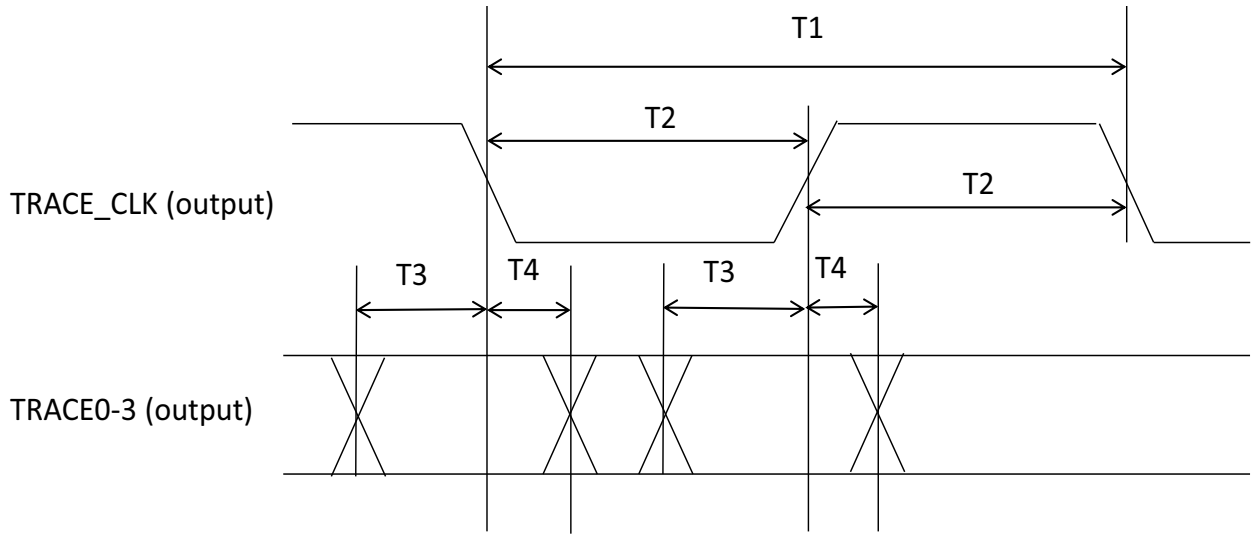


Figure 14. Trace timing

Table 44. Trace timing parameters

Symbol	Description	Min	Max	Unit
T0	TRACE_CLK frequency	—	70	MHz
T1	TRACE_CLK cycle time	1/T0	—	ns
T2	TRACE_CLK pulse width	6	—	ns

Table 44. Trace timing parameters (continued)

Symbol	Description	Min	Max	Unit
T3	TRACE data setup time	2	—	ns
T4	TRACE data hold time	0.7	—	ns

4.5 External memory interface

The following sections provide information about external memory interfaces.

4.5.1 SEMC specifications

The following sections provide information on SEMC interface.

Measurements are with a load of 15 pf and an input slew rate of 1 V/ns.

4.5.1.1 SEMC output timing

There are ASYNC and SYNC modes for SEMC output timing.

4.5.1.1.1 SEMC output timing in ASYNC mode

Table 45 shows SEMC output timing in ASYNC mode.

Table 45. SEMC output timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	200	MHz	
T_{CK}	Internal clock period	5	—	ns	
T_{AVO}	Address output valid time	—	2	ns	These timing parameters apply to Address and ADV# for NOR/PSRAM in ASYNC mode.
T_{AHO}	Address output hold time	(TCK - 2) [1]	—	ns	
T_{ADVL}	Active low time	(TCK - 1) [2]			
T_{DVO}	Data output valid time	—	2	ns	These timing parameters apply to Data/CLE/ALE and WE# for NAND, apply to Data/DM/CRE for NOR/PSRAM, apply to Data/DCX and WRX for DBI interface.
T_{DHO}	Data output hold time	(TCK - 2) [3]	—	ns	
T_{WEL}	WE# low time	(TCK - 1) [4]		ns	

1 Address output hold time is configurable by SEMC_*CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N, T_{AHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for more detail about SEMC_*CR0.AH register field.

2 ADV# low time is configurable by SEMC_*CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N, T_{ADL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for more detail about SEMC_*CR0.AS register field.

3 Data output hold time is configurable by SEMC_*CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N, T_{DHO} min time should be ((N + 1) x T_{CK}). See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for more detail about SEMC_*CR0.WEH register field.

4 WE# low time is configurable by SEMC_*CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N, T_{WEL} min time should be ((N + 1) x T_{CK} - 1). See the *i.MX RT1160 Reference Manual* (IMXRT1160RM) for more detail about SEMC_*CR0.WEL register field.

Figure 15 shows the output timing in ASYNC mode.

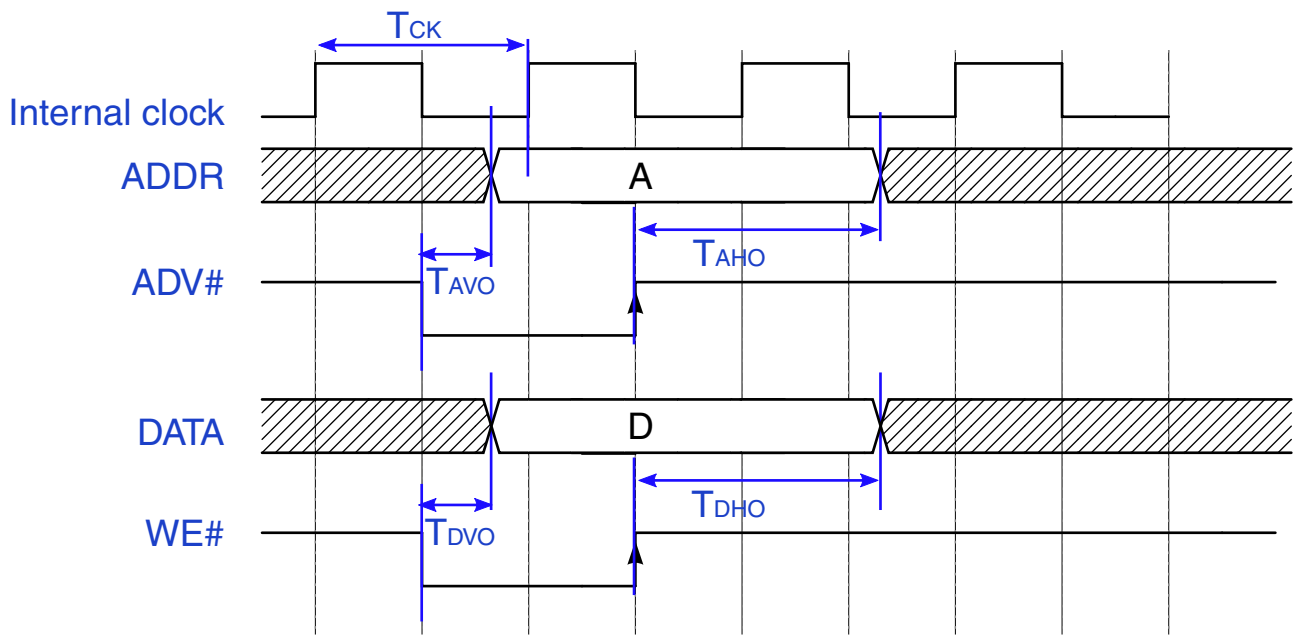


Figure 15. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 46 shows SEMC output timing in SYNC mode.

Table 46. SEMC output timing in SYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
	Frequency of operation	—	200	MHz	—
T_{CK}	Internal clock period	5	—	ns	—
T_{DVO}	Data output valid time	—	0.6	ns	These timing parameters apply to Address/Data/DM/CKE/control signals with SEMC_CLK for SDRAM.
T_{DHO}	Data output hold time	-0.7	—	ns	

Figure 16 shows the output timing in SYNC mode.

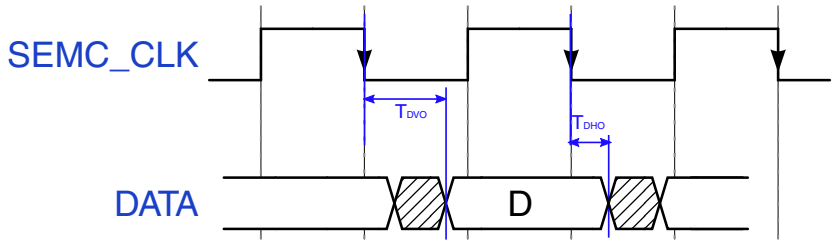


Figure 16. SEMC output timing in SYNC mode

4.5.1.2 SEMC input timing

There are ASYNC and SYNC modes for SEMC input timing.

4.5.1.2.1 SEMC input timing in ASYNC mode

Table 47 shows SEMC input timing in ASYNC mode.

Table 47. SEMC input timing in ASYNC mode

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	7.1	—	ns	For NAND/NOR/PSRAM/DBI, these timing parameters apply to RE# and Read Data.
T_{IH}	Data input hold	0	—	ns	

Figure 17 shows the input timing in ASYNC mode.

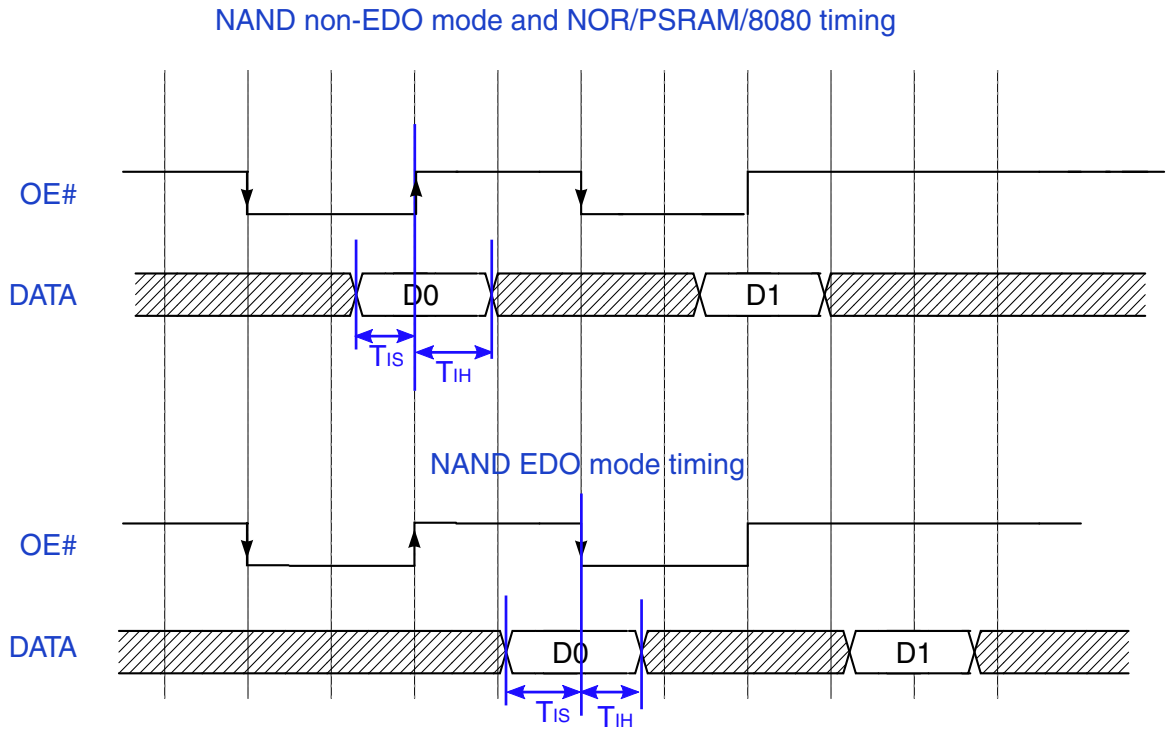


Figure 17. SEMC input timing in ASYNC mode

4.5.1.2.2 SEMC input timing in SYNC mode

Table 48 and Table 49 show SEMC input timing in SYNC mode.

Table 48. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x0)

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	8.67	—	ns	—
T_{IH}	Data input hold	0	—	ns	

Table 49. SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x1)

Symbol	Parameter	Min.	Max.	Unit	Comment
T_{IS}	Data input setup	0.6	—	ns	—
T_{IH}	Data input hold	1	—	ns	

Figure 18 shows the input timing in SYNC mode.

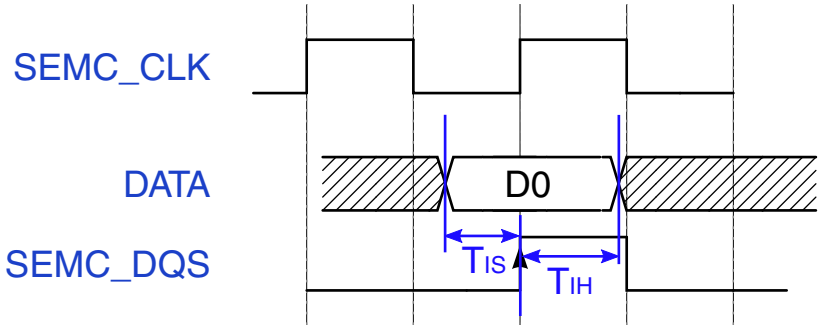


Figure 18. SEMC input timing in SYNC mode

4.5.2 FlexSPI parameters

Measurements are with a load 15 pf and input slew rate of 1 V/ns.

4.5.2.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these three internal sample clock sources.

4.5.2.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

Table 50. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	60	MHz
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 51. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X1

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	133	MHz
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time for incoming data	1	—	ns

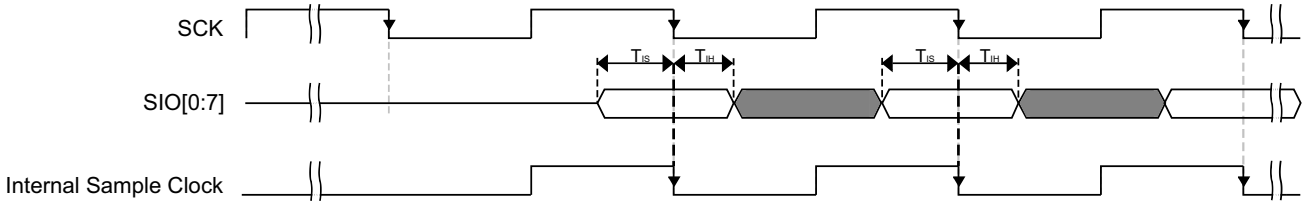


Figure 19. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0, 0X1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.5.2.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1–Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2–Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 52. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A1)

Symbol	Parameter	Value		Unit
		Min	Max	
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

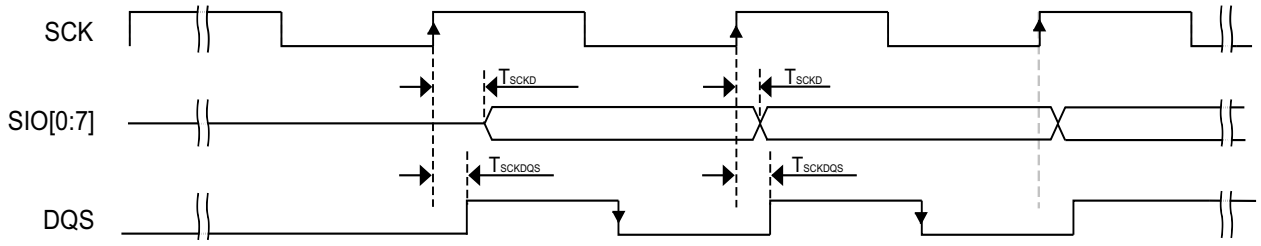


Figure 20. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X3 (case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 53. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A2)

Symbol	Parameter	Value		Unit
		Min	Max	
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

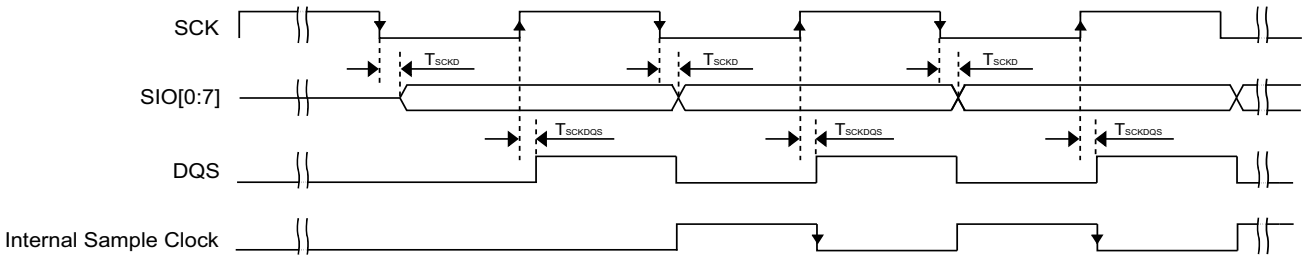


Figure 21. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X3 (case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half cycle delayed DQS falling edge.

4.5.2.1.3 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

Table 54. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	30	MHz
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time for incoming data	0	—	ns

Table 55. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	66	MHz
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time for incoming data	1	—	ns

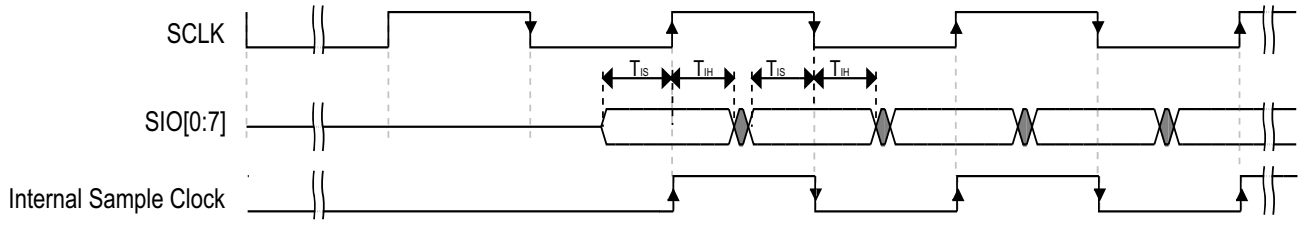


Figure 22. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1

4.5.2.1.4 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in DDR mode:

- B1—Memory generates both read data and read strobe on SCK edges
- B2—Memory generates read data on SCK edges and generates read strobe on SCK2 edges

Table 56. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-1	1	ns

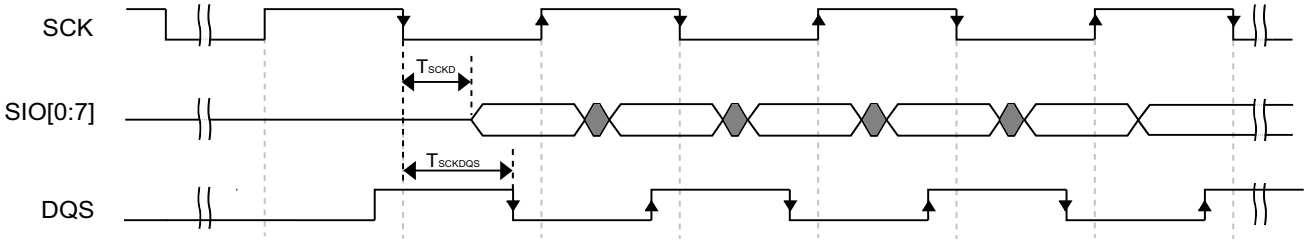


Figure 23. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B1)

Table 57. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166	MHz
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-1	1	ns

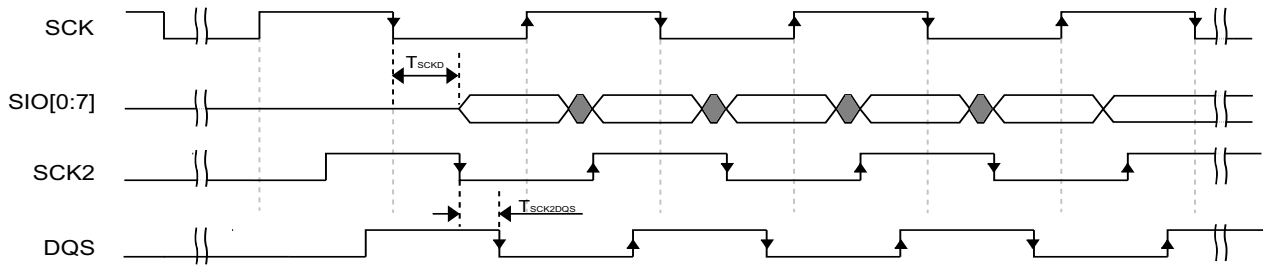


Figure 24. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case B2)

4.5.2.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.5.2.2.1 SDR mode

Table 58. FlexSPI output timing in SDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation	—	166[1]	MHz
T_{ck}	SCK clock period	6.0	—	ns
T_{DVO}	Output data valid time	—	4	ns
T_{DHO}	Output data hold time	2	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} + 2	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1 register, the default values are shown above. Please refer to the *i.MXRT1160 Reference Manual* (IMXRT1160RM) for more details.

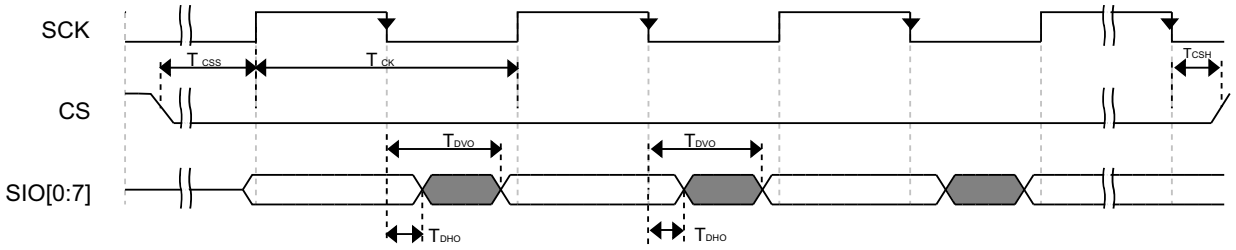


Figure 25. FlexSPI output timing in SDR mode

4.5.2.2.2 DDR mode

Table 59. FlexSPI output timing in DDR mode

Symbol	Parameter	Min	Max	Unit
	Frequency of operation[1]	—	166	MHz
T_{ck}	SCK clock period (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)	6.0	—	ns
T_{DVO}	Output data valid time	—	2.2	ns
T_{DHO}	Output data hold time	0.8	—	ns
T_{CSS}	Chip select output setup time	3 x T_{CK} / 2 - 0.7	—	ns
T_{CSH}	Chip select output hold time	3 x T_{CK} / 2 + 0.8	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHA*x*CR1 register, the default values are shown above. Please refer to the *i.MXRT1160 Reference Manual* (IMXRT1160RM) for more details.

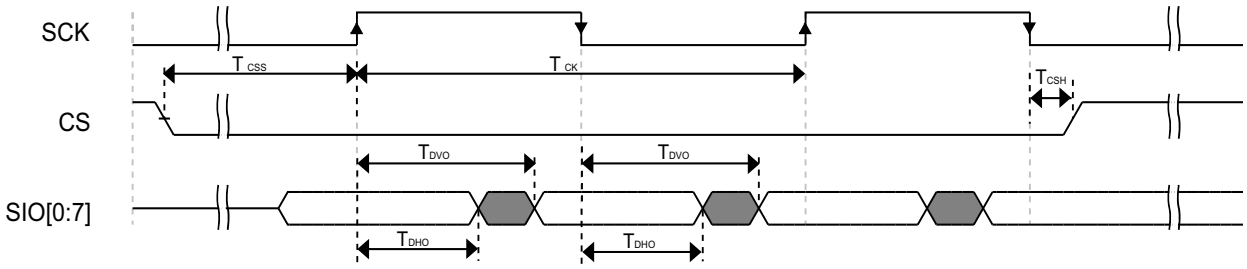


Figure 26. FlexSPI output timing in DDR mode

4.6 Display and graphics

The following sections provide information about display and graphic interfaces.

4.6.1 MIPI D-PHY electrical characteristics

The i.MX RT1160 conforms to the MIPI CSI-2 and D-PHY standards for protocol and electrical specifications.

Compliant with standards:

- *MIPI Alliance Specification for Display Serial Interface Version 1.1* (MIPI DSI controller)
- *MIPI Standard 1.1 for D-PHY* (MIPI DSI D-PHY)
- Compatible with *MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1*

4.6.1.1 MIPI HS-TX specifications

Table 60. MIPI high-speed transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}[1]	High Speed Transmit Static Common Mode Voltage	150	200	250	mV
$\|\Delta V_{CMTX}\|_{(1,0)}$	V_{CMTX} mismatch when Output is Differential-1 or Differential-0	—	—	5	mV
$\|V_{OD}\|$[1]	High Speed Transmit Differential Voltage	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when Output is Differential-1 or Differential-0	—	—	14	mV
V_{OHHS}[1]	High Speed Output High Voltage	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single Ended Output Impedance Mismatch	—	—	10	%

1 Value when driving into load impedance anywhere in the Z_{ID} (Differential input impedance) range.

Table 61. MIPI high-speed transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	—	—	15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	—	—	25	mV_{PEAK}
t_R and t_F[1]	Rise Time and Fall Time (20% to 80%)	150	—	0.3 x UI	ps

1 UI is the long-term average unit interval.

4.6.1.2 MIPI LP-TX specifications

Table 62. MIPI low-power transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}[1]	Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	Thevenin Output Low Level	-50	—	50	mV
Z_{OLP}[2]	Output Impedance of Low Power Transmitter	110	—	—	Ω

1 This specification can only be met when limiting the core supply variation from 1.1 V to 1.3 V.

2 Though there is no specified maximum for Z_{OLP}, the LP transmitter output impedance ensures the T_{RLP}/T_{FLP} specification is met.

Table 63. MIPI low-power transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}[1]	15% to 85% Rise Time and Fall Time	—	—	25	ns
T_{REOT}[1,2,3]	30% to 85% Rise Time and Fall Time	—	—	35	ns
$T_{LP-PULSE-TX}$[4]	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	—	—	ns
	Pulse width of the LP exclusive-OR clock: All other pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	—	—	ns
$\delta V/\delta t_{SR}$[1,5,6,7]	Slew Rate @ C_{LOAD} = 0 pF	30	—	500	mV/ns
	Slew Rate @ C_{LOAD} = 5 pF	30	—	200	mV/ns
	Slew Rate @ C_{LOAD} = 20 pF	30	—	150	mV/ns
	Slew Rate @ C_{LOAD} = 70 pF	30	—	100	mV/ns
C_{LOAD}[1]	Load Capacitance	0	—	70	pF

1 C_{LOAD} includes the low equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.

2 The rise-time of T_{REOT} starts from the HS common-level at the moment of the differential amplitude drops below 70 mV, due to stopping of the differential drive.

3 With an additional load capacitance C_{CM} between 0 to 60 pF on the termination center tap at RX side of the lane.

4 This parameter value can be lower than T_{LPX} (MIPI D-PHY low power states), due to differences in rise vs. fall signal slopes, trip levels, and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.

5 When the output voltage is between 15% and 85% of the fully settled LP signal levels.

6 Measured as average across any 50 mV segment of the output signal transition.

7 This value represents a corner point in a piecewise linear curve.

4.6.1.3 MIPI LP-RX specifications

Table 64. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	—	1300	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 65. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE}[1,2]	Input pulse rejection	—	—	300	V.ps

Table 65. MIPI low power receiver AC specifications (continued)

T_{MIN-RX}[3]	Minimum pulse width response	20	—	—	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1 Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state.

2 An impulse below this value will not change the receiver state.

3 An input pulse greater than this value will toggle the output.

4.6.1.4 MIPI LP-CD specifications

Table 66. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

4.6.1.5 MIPI DC specifications

Table 67. MIPI input characteristics DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pad signal voltage range	-50	—	1350	mV
I_{LEAK}[1]	Pin leakage current	-10	—	10	μA
V_{GNDSH}	Ground shift	-50	—	50	mV
$V_{PIN(absmax)}$[2]	Maximum pin voltage level	-0.15	—	1.45	V
$T_{VPIN(absmax)}$[3]	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	—	—	20	ns

1 When the pad voltage is within the signal voltage range between $V_{GNDSH(min)}$ to V_{OH} + $V_{GNDSH(max)}$ and the Lane Module is in LP receive mode.

2 This value includes ground shift.

3 The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20 ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

4.6.2 CMOS Sensor Interface (CSI) timing parameters

The following sections describe the CSI timing in gated and ungated clock modes.

4.6.2.1 Gated clock mode timing

Figure 27 and Figure 28 shows the gated clock mode timings for CSI, and Table 68 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

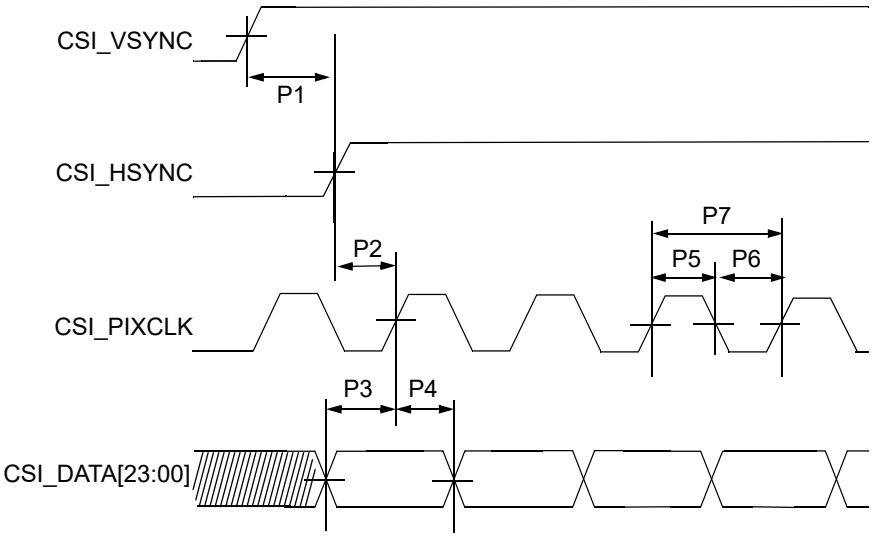


Figure 27. CSI Gated clock mode—sensor data at falling edge, latch data at rising edge

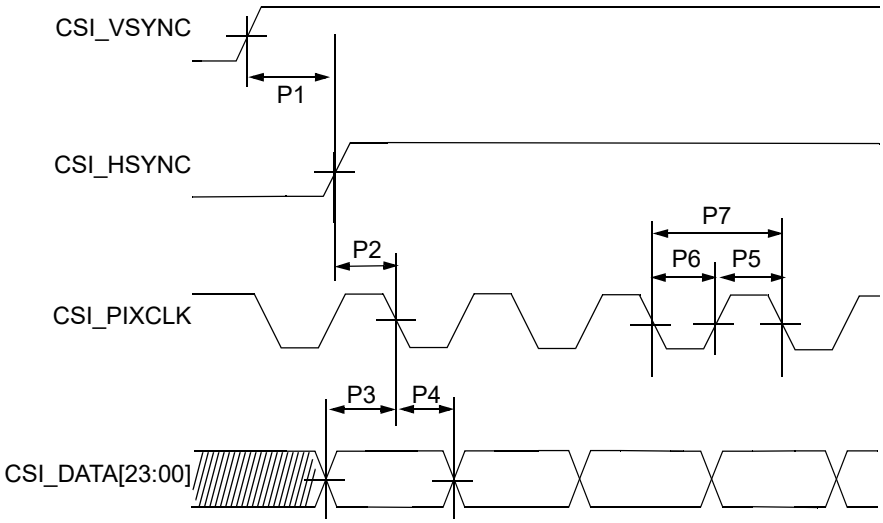


Figure 28. CSI Gated clock mode—sensor data at rising edge, latch data at falling edge

Table 68. CSI gated clock mode timing parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	2.6	—	ns
P3	CSI DATA setup time	tDsu	2.6	—	ns

Table 68. CSI gated clock mode timing parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P4	CSI DATA hold time	tDh	0	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	80	MHz

4.6.2.2 Ungated clock mode timing

Figure 29 shows the ungated clock mode timings of CSI, and Table 69 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

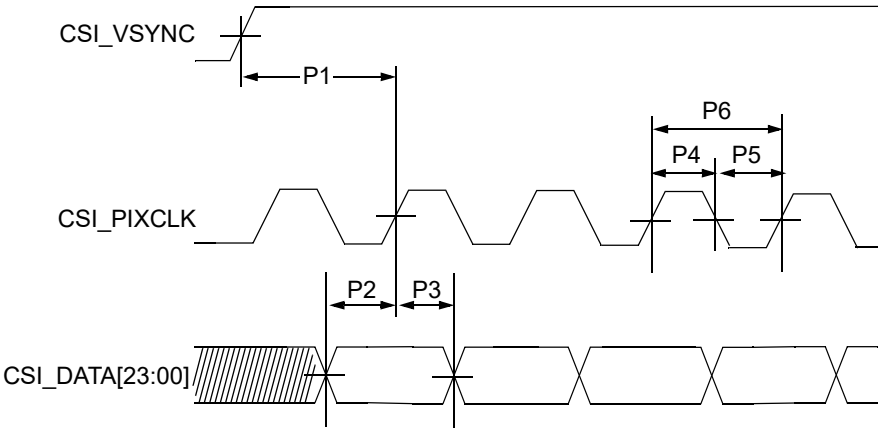


Figure 29. CSI ungated clock mode—sensor data at falling edge, latch data at rising edge

Table 69. CSI ungated clock mode timing parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	2.6	—	ns
P3	CSI DATA hold time	tDh	0	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	80	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

4.6.3 LCD Controller timing parameters

Figure 30 shows the LCD timing and Table 70 lists the timing parameters.

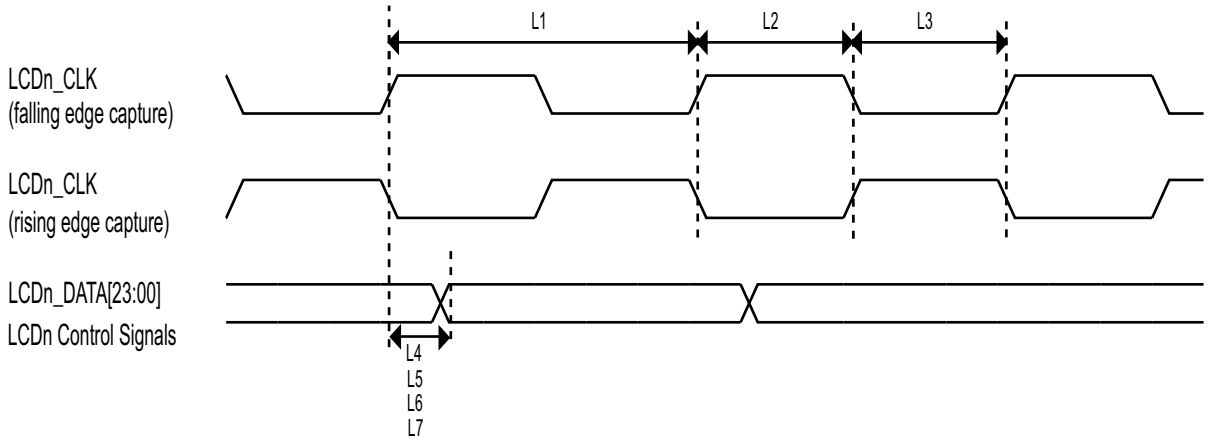


Figure 30. LCD timing

Table 70. LCD timing parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	75/150[1]	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

[1] For eLCDIF or LCDIFv2, the maximum pixel clock frequency of parallel IO interface is 75 MHz, while it is 150 MHz for MIPI DSI interface.

4.7 Audio

This section provides information about SAI/I2S.

4.7.1 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 71. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	15	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	8.4	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	10	ns
S8	SAI_BCLK to SAI_TXD invalid	1	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	14	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

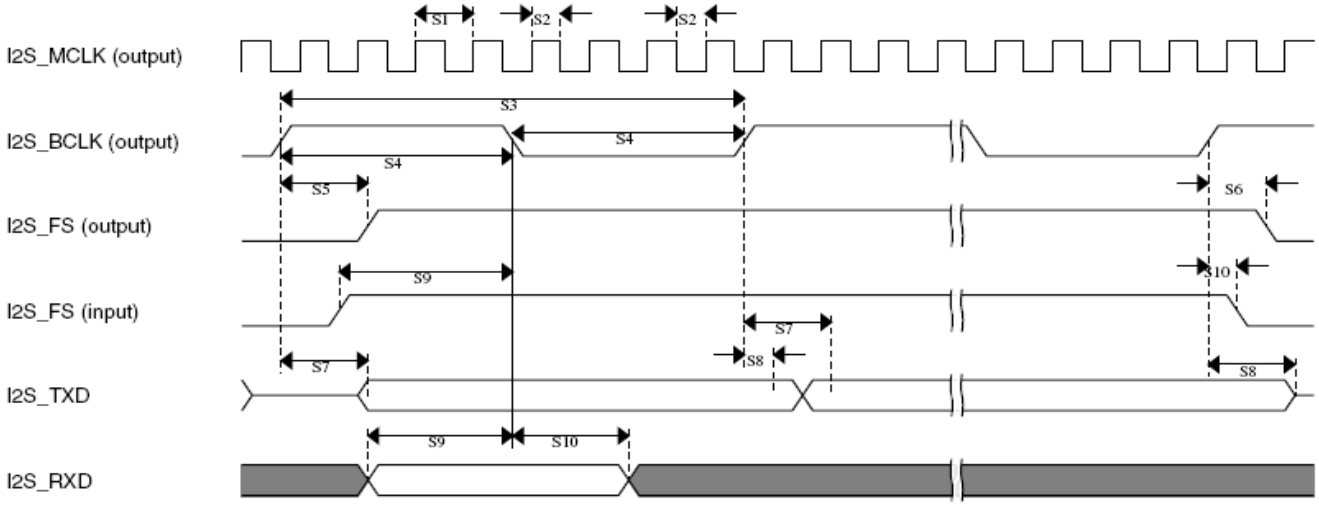


Figure 31. SAI timing—Master modes

Table 72. Slave mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	6	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	-1.5	—	ns

Table 72. Slave mode SAI timing

Num	Characteristic	Min	Max	Unit
S17	SAI_RXD setup before SAI_BCLK	6	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

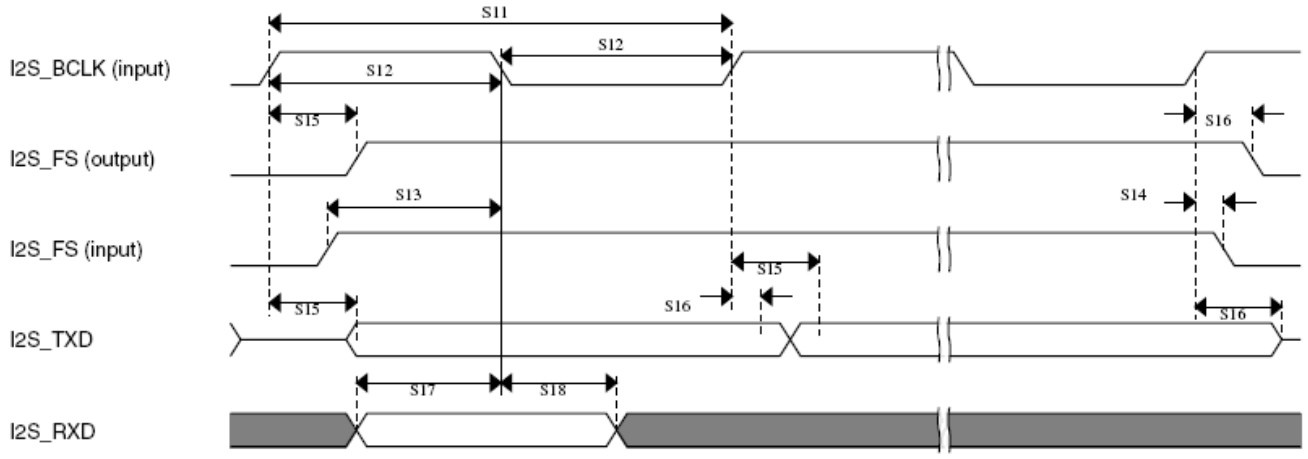


Figure 32. SAI timing—Slave mode

4.8 Analog

The following sections provide information about analog interfaces.

4.8.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8[1] and $VADIN_{max}$ ≤ VREFH)[2]

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{ADIN}	Input voltage	V_{REFL}	—	V_{REFH}	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input resistance	—	500	—	Ω	—
R_{AS}	Analog source resistance	—	—	5	KΩ	3
f_{ADCK}	ADC conversion clock frequency	8	—	88	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	Cycles	4
$C_{compare}$	Fixed compare cycles	—	17.5	—	Cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			Cycles	—
DNL	Differential nonlinearity	—	±0.7	±1	LSB	5,6,7
INL	Integral nonlinearity	—	±0.8	±1	LSB	5,6,7

Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8[1] and $VADIN_{max}$ ≤ VREFH)[2] (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
ENOB	Effective number of bits					8,9,10
	Single-ended mode					
	Avg = 1	10.0	10.4	—	—	
	Avg = 2	10.4	10.6	—	—	
	Avg = 16	11.2	11.3	—	—	
	Differential mode					
	Avg = 1	11.0	11.2	—	—	
	Avg = 2	—	—	—	—	
	Avg = 16	—	—	—	—	
SINAD	Signal to noise plus distortion	SINAD = 6.02 x ENOB + 1.76			dB	—
E_G	Gain error[11]	—	-0.16	-0.56	%FSV	12
E_O	Offset error	—	±0.01	±0.02	%FSV	13
Iin_ext_leak	External channel leakage current	—	30	500	nA	—
EIL	Input leakage error	R_{AS} * $I_{in\_ext\_leak}$			mV	—
tADCSTUP	Setup time	—	5	—	μs	—

1 The range is from 1.71 V to 1.89 V.

2 Values in this table are based on test with limited matrix samples in lab environment.

3 This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance.

4 See Figure 33, "Sample time VS. RAS".

5 1 LSB = (VREFH - VREFL) / 2^N, N = 12

6 ADC conversion clock at max frequency and using linear histogram.

7 No missing code

8 Input data used for test is 1 kHz sine wave.

9 Measured at VREFH = 1.8 V and pwrsel = 2.

10 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

11 Gain error is FSE-ZSE (same as FSE-E_O).

12 Error measured at full scale at 1.8 V.

13 Offset error is same as ZSE, error measured at 0 V with zero scale.

Table 74. ADC electrical specifications (VREFH = 1.68 V and $VADIN_{max}$ ≤ $NVCC\_GPIO_{max}$)[1]

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
V_{ADIN}	Input voltage	V_{REFL}	—	$NVCC\_GPIO_{max}$	V	—
C_{ADIN}	Input capacitance	—	2.25	—	pF	—
R_{ADIN}	Input resistance	—	1	—	KΩ	—

Table 74. ADC electrical specifications (VREFH = 1.68 V and $VADIN_{max} \leq NVCC\_GPIO_{max}$)[1] (continued)

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
R_{AS}	Analog source resistance	—	—	5	KΩ	3
f_{ADCK}	ADC conversion clock frequency	8	—	88	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	Cycles	4
$C_{compare}$	Fixed compare cycles	—	17.5	—	Cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			Cycles	—
DNL	Differential nonlinearity	—	±0.7	±1	LSB	5,6,7
INL	Integral nonlinearity	—	±0.8	±1	LSB	5,6,7
ENOB	Effective number of bits					8,9,10
	Single-ended mode					
	Avg = 1	10.0	10.3	—	—	
	Avg = 2	10.4	10.6	—	—	
	Avg = 16	11.2	11.3	—	—	
	Differential mode					
	Avg = 1	11.0	11.2	—	—	
	Avg = 2	—	—	—	—	
	Avg = 16	—	—	—	—	
SINAD	Signal to noise plus distortion	SINAD = 6.02 x ENOB + 1.76			dB	—
E_G	Gain error[11]	—	-0.16	-0.56	%FSV	12
E_O	Offset error	—	±0.01	±0.02	%FSV	13
Iin_ext_leak	External channel leakage current	—	30	500	nA	—
EIL	Input leakage error	$R_{AS} * I_{in\_ext\_leak}$			mV	—
tADCSTUP	Setup time	—	5	—	μs	—

1 Values in this table are based on test with limited matrix samples in lab environment.

2 Typical values assume Temp = 25 °C and f_{ACLK} = Max, unless otherwise stated. Typical values are for reference only, and are not tested in production.

3 This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance.

4 See Figure 33, "Sample time VS. RAS".

5 1 LSB = (VREFH - VREFL) / 2^N, N = 12

6 ADC conversion clock at max frequency and using linear histogram.

7 No missing code

8 Input data used for test is 1 kHz sine wave.

9 Measured at VREFH = 1.68 V and pwrsel = 2.

10 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

[11] Gain error is FSE-ZSE (same as FSE-E_O).

[12] Error measured at full scale at 3.6 V.

[13] Offset error is same as ZSE, error measured at 0 V with zero scale.

Table 75. ADC electrical specifications (1 V ≤ VREFH < 1.71 V and $VADIN_{max}$ ≤ VREFH)[1]

Symbol	Description	Min	Typ[2]	Max	Unit	Notes
V_{ADIN}	Input voltage	V_{REFL}	—	V_{REFH}	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input resistance	—	500	—	Ω	—
R_{AS}	Analog source resistance	—	—	5	KΩ	[3]
f_{ADCK}	ADC conversion clock frequency	8	—	88	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	Cycles	[4]
$C_{compare}$	Fixed compare cycles	—	17.5	—	Cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			Cycles	—
DNL	Differential nonlinearity	—	±0.7	±1	LSB	[5,6,7]
INL	Integral nonlinearity	—	±0.8	±1	LSB	[5,6,7]
ENOB	Effective number of bits					[8,9,10]
	Single-ended mode					
	Avg = 1	10.0	10.3	—	—	
	Avg = 2	10.4	10.6	—	—	
	Avg = 16	11.2	11.3	—	—	
	Differential mode					
	Avg = 1	11.0	11.2	—	—	
	Avg = 2	—	—	—	—	
	Avg = 16	—	—	—	—	
SINAD	Signal to noise plus distortion	SINAD = 6.02 x ENOB + 1.76			dB	—
E_G	Gain error[11]	—	-0.16	-0.56	%FSV	[12]
E_O	Offset error	—	±0.01	±0.02	%FSV	[13]
Iin_ext_leak	External channel leakage current	—	30	500	nA	—
EIL	Input leakage error	$R_{AS} * I_{in\_ext\_leak}$			mV	—
tADCSTUP	Setup time	—	5	—	μs	—

[1] Values in this table are based on test with limited matrix samples in lab environment.

[2] Typical values assume Temp = 25 °C and f_{ACLK} = Max, unless otherwise stated. Typical values are for reference only, and are not tested in production.

[3] This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance.

[4] See Figure 33, "Sample time VS. RAS".
[5] 1 LSB = (VREFH - VREFL) / 2^N, N = 12
[6] ADC conversion clock at max frequency and using linear histogram.
[7] No missing code
[8] Input data used for test is 1 kHz sine wave.
[9] Measured at VREFH = 1.0 V and pwrsel = 2.
[10] ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.
[11] Gain error is FSE-ZSE (same as FSE-E_O).
[12] Error measured at full scale at 1.0 V.
[13] Offset error is same as ZSE, error measured at 0 V with zero scale.

The following figure shows a plot of the ADC sample time versus R_{AS}.

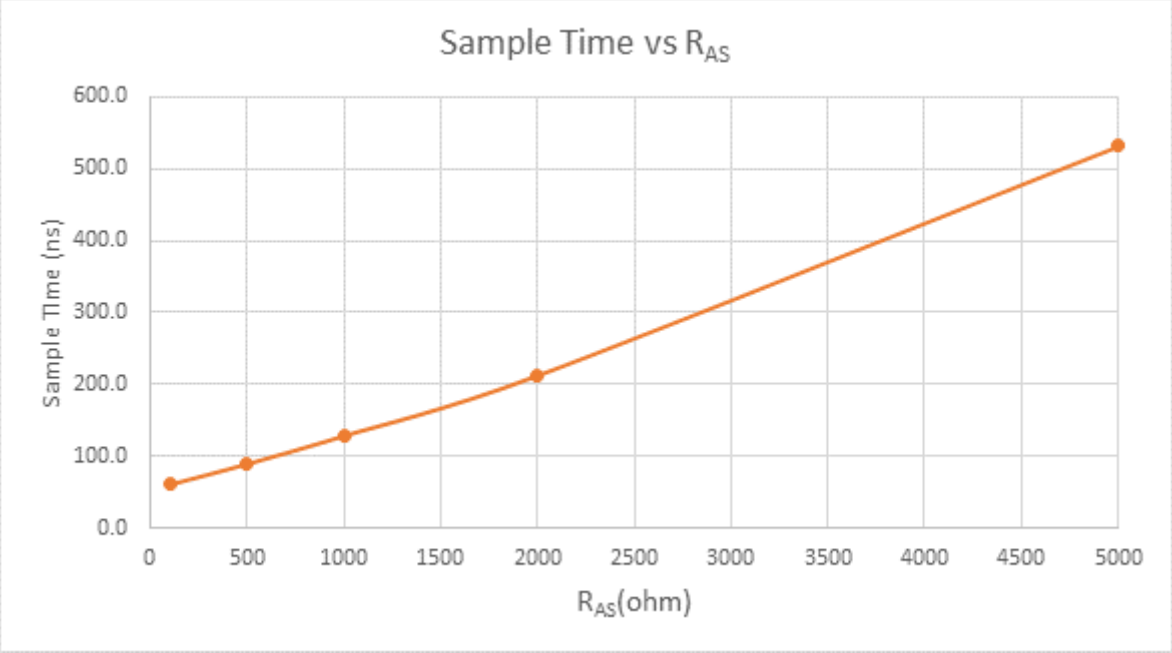


Figure 33. Sample time VS. R_{AS}

4.8.1.1 12-bit ADC input impedance equivalent circuit diagram

There is an additional R_{IOMUX} of 350 Ω (from 295 Ω to 405 Ω) resistance if an input goes through the MUX inside the IO and C_P of 2.5 pF as shown in Figure 34.

To calculate the sample request time, using the following equation where $R_{ADCtotal} = R_{ADIN} + R_{IOMUX}$, R_{IOMUX} = 350 Ω, C_P = 2.5 pF and B = 11 for 1/4 LSB settling.

$$T_{smp\_req} = B\,[R_{AS}\,(C_{AS} + C_P + C_{ADIN}) + (R_{AS} + R_{ADCtotal})\,C_{ADIN}]$$

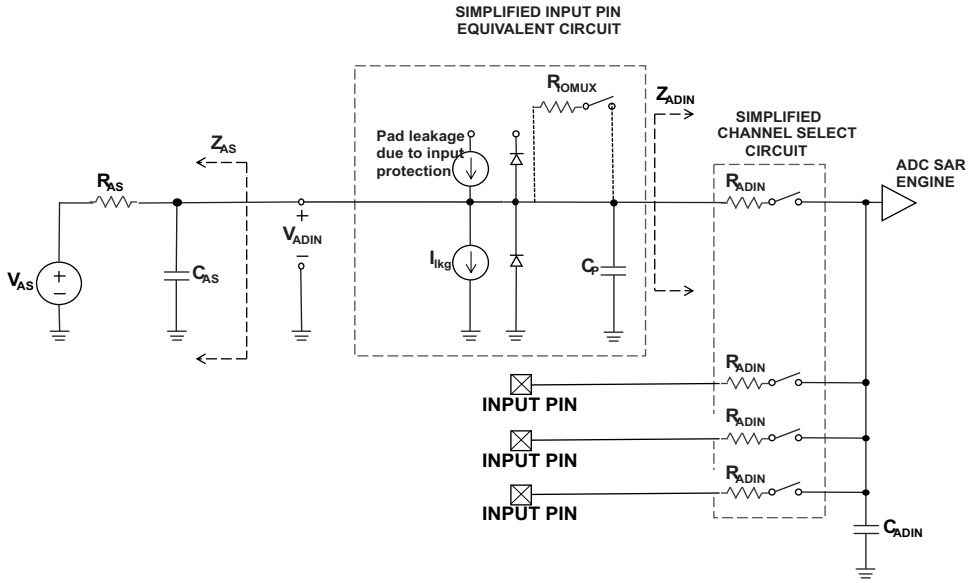


Figure 34. ADC input impedance equivalent circuit diagram

4.8.2 12-bit DAC electrical characteristics

4.8.2.1 12-bit DAC operating requirements

Table 76. 12-bit DAC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Notes
C_L	Output load capacitance	—	50	100	pF	1
I_L	Output load current	—	—	1	mA	2

1 The DAC output can drive R and C loading. The user should consider both DC and dynamic application requirements. 50 pF C_L provides the best dynamic performance, while 100 pF provides the best DC performance.

2 Sink or source current ability.

Table 77. DAC characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
VDACOUTL	DAC low level output voltage	ADC_VREFH selected, Rload = 18 kΩ, Cload = 50 pF	VSS	—	0.15	V	1
VDACOUTH	DAC high level output voltage		VDDA_ADC_1P8 - 0.15	—	VDDA_ADC_1P8	V	
DNL	Differential nonlinearity error	Code 100h — F00h best fit curve	—	±0.5	±1	LSB	—

Table 77. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
INL	Integral nonlinearity error	Code 100h — F00h best fit curve	—	±1	—	LSB	[2]
			—	±2	—	LSB	[3]
EO	Offset error	Code 100h	—	±0.6	—	%FSR (Full-scale range)	—
TEO	Offset error temperature coefficient	Code 100h	—	±30	—	μV/°C	—
EG	Gain error	Code F00h	—	±0.4	—	%FSR	—
TEG	Gain error temperature coefficient	Code F00h	—	±10	—	ppm of FSR/°C	—

Table 77. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
TFS_LS	Full scale setting time in Low Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	5	—	μs	4
		Code 100h — F00h or F00h —100h @PTAT current	—	5	—		
TFS_MS	Full scale setting time in Middle Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	1	—		
		Code 100h — F00h or F00h — 100h @PTAT current	—	1	—		
TFS_HS	Full scale setting time in High Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	0.5	—		
		Code 100h — F00h or F00h — 100h @PTAT current	—	0.5	—		
TCC_LS	Code to code setting time in Low Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	1	—		
		Code 7F7h — 807h or 807h — 7F7h @PTAT current	—	1	—		
TCC_MS	Code to code setting time in Middle Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	0.5	—		
		Code 7F7h — 807h or 807h — 7F7h @PTAT current	—	0.5	—		
TCC_HS	Code to code setting time in Middle Speed mode	Code 7F7h — 807h or 807h — 7F7h @ZTC current	—	0.3	—		
		Code 7F7h — 807h or 807h — 7F7h @PTAT current	—	0.3	—		

Table 77. DAC characteristics (continued)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit	Notes
SR_LS	Slew rate in Low Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	0.24	—	V/μs	5
		Code 100h — F00h or F00h —100h @PTAT current	—	0.24	—		
SR_MS	Slew rate in Middle Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	1.2	—		
		Code 100h — F00h or F00h —100h @PTAT current	—	1.2	—		
SR_HS	Slew rate in High Speed mode	Code 100h — F00h or F00h — 100h @ZTC current	—	2.4	—		
		Code 100h — F00h or F00h —100h @PTAT current	—	2.4	—		
PSRR	Power supply rejection ratio	Code 800h, ∆ VDD_ANA18 = 100 mV, VREFH_ANA12 selected	—	70	—	dB	6
Glitch	Glitch energy	Code 100h — F00h — 100h	—	30	—	nV-s	—
		Code 7FFh — 800h — 7FFh	—	30	—		
CT	Channel to channel crosstalk	—	—	—	-80	dB	7
ROP	Output resistance	Code 100h — F00h and Rload = 18 kΩ	—	200	—	Ω	8

1 It is recommended to operate the DAC in the output voltage range between 0.15 V and (VDDA_ADC_1P8 - 0.15 V) for best accuracy. Linearity of the output voltage outside this range will be affected as current load increases.

2 When ADC_VREFH is selected as the reference (DAC_CR[DACRFS] = 0b).

3 When the internal 1.2 V source is selected as the reference (DAC_CR[DACRFS] = 1b).

4 The DAC output remains within ±0.5 LSB of the final measured value for digital input code change. Noise on the power supply can cause this performance to degrade to ±1 LSB. This parameter represents both rising edge and falling edge settling time.

5 Time for the DAC output to transition from 10% to 90% signal amplitude (rising edge or falling edge).

6 PSRR = 20 x log{ΔVDD_ANA18 /ΔVDAC_OUT}

7 If two DACs are used and sharing the same VREFH.

8 Based on design simulation.

4.8.3 ACMP electrical specifications

Table 78. ACMP operating conditions

Symbol	Description	Min	Typ	Max	Unit
VREFH_EXT	External reference voltage	1	—	1.98	V
VREFH_INT[1]	Internal reference voltage	—	1.3	—	V

1 This is an internal reference voltage generated by PMC0.

Table 79. ACMP characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
VAIN	Analog input voltage	—	0	—	NVCC_GPIO[1]	V
VAIO	Analog input offset voltage	—	—	—	20	mV
VH	Analog comparator hysteresis	Hystrl[1:0] = 00	—	5	—	mV
		Hystrl[1:0] = 01	—	10	—	mV
		Hystrl[1:0] = 10	—	20	—	mV
		Hystrl[1:0] = 11	—	30	—	mV
TDHS	Propagation delay, high-speed mode	Normal supply	—	—	50	ns
TDHS	Propagation delay, low-speed mode	—	—	—	5	μs
—	Analog comparator initialization delay	—	—	—	20	μs
INL	8-bit DAC integral non-linearity	—	-1	—	1	LSB
DNL	8-bit DAC differential non-linearity	—	-1	—	1	LSB

1 The maximum input voltage for CMP analog inputs associated with GPIO_AD bank is NVCC_GPIO.

4.8.4 Temperature sensor

Table 80 lists the parameters of temperature sensor.

Table 80. Temperature sensor parameters

Parameter	Min	Max	Unit
Temperature range[1]	-40	125	°C

1 Accuracy of measurement: ± 5°C for 25°C and above, while ± 10°C for below 25°C.

4.9 Communication interfaces

The following sections provide the information about communication interfaces.

4.9.1 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

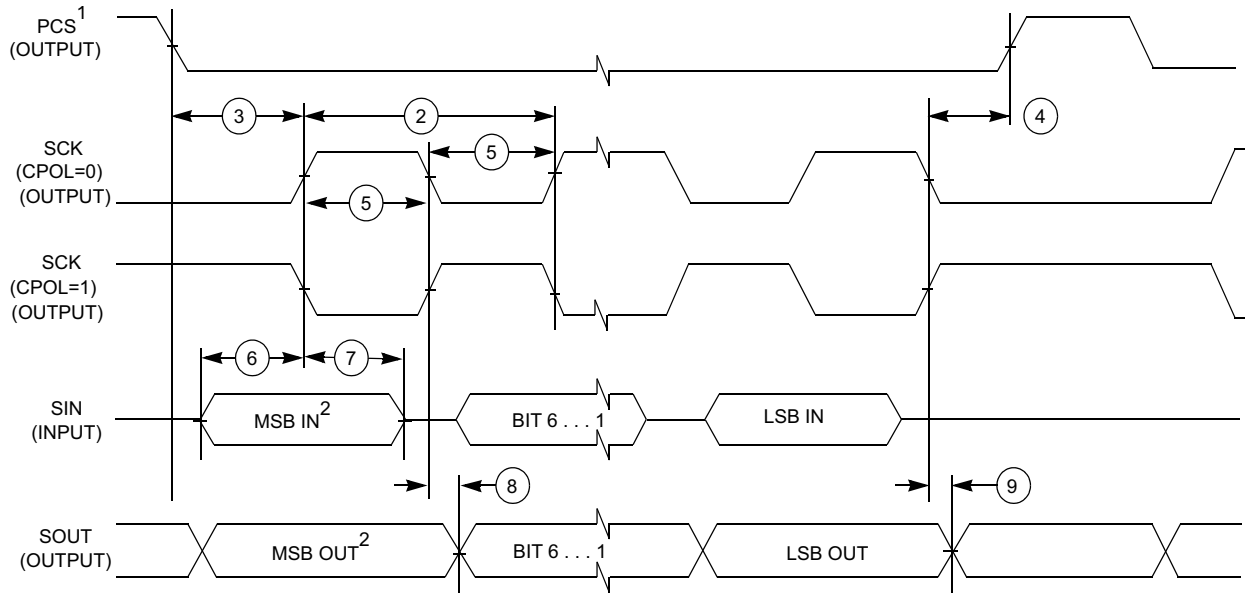
All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 81. LPSPI Master mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of operation	—	f_{periph} / 2	MHz	1
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 3	—	ns	—
6	t_{SU}	Data setup time (inputs)	10	—	ns	—
7	t_{HI}	Data hold time (inputs)	2	—	ns	—
8	t_{V}	Data valid (after SCK edge)	—	8	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—

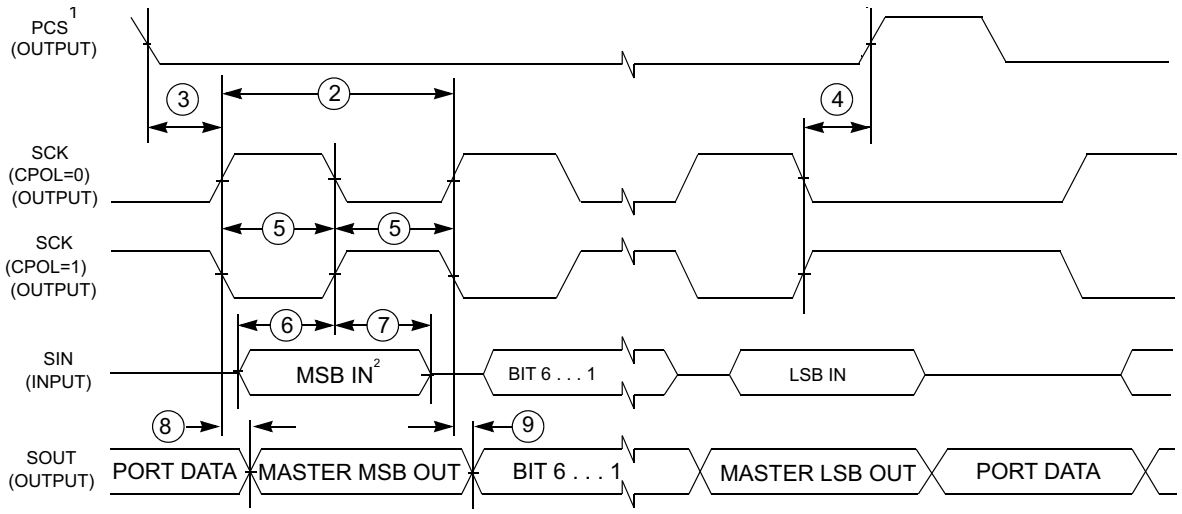
1 Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must guaranteed this limit is not exceeded.

2 $t_{periph} = 1000 / f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI Master mode timing (CPHA = 1)

Table 82. LPSPI Slave mode timing

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of operation	0	f_{periph} / 2	MHz	1
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 5	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.7	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.8	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_V	Data valid (after SCK edge)	—	14.5	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—

1 Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for f_{periph} must be guaranteed this limit is not exceeded.

2 t_{periph} = 1000 / f_{periph}

3 Time to data active from high-impedance state

4 Hold time to high-impedance state

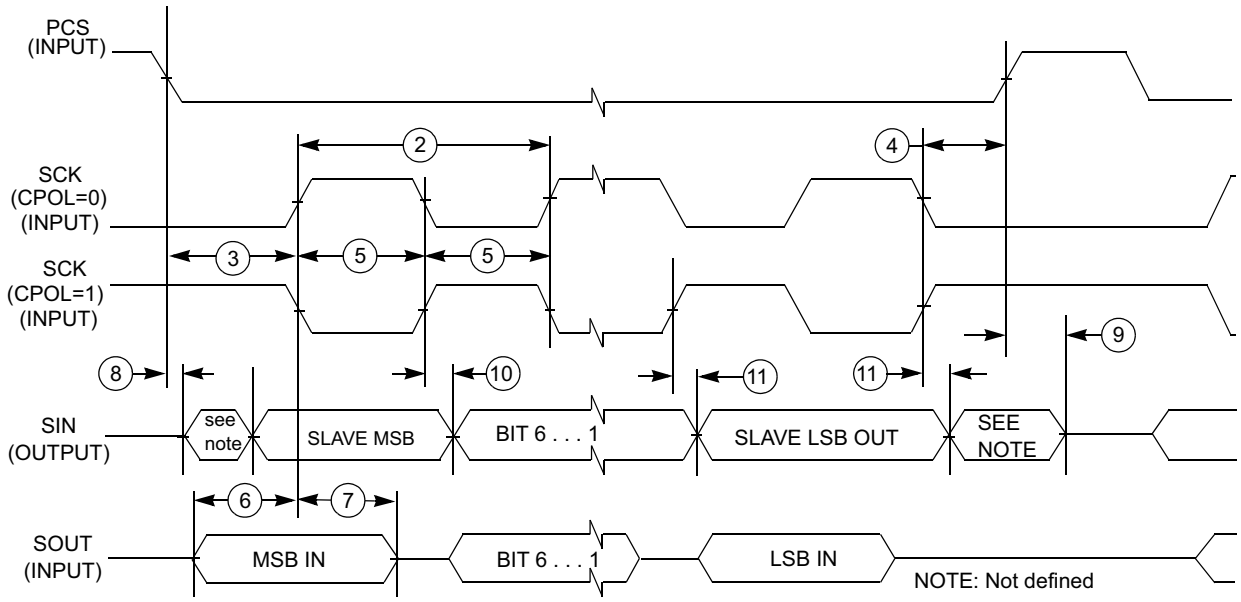


Figure 37. LPSPI Slave mode timing (CPHA = 0)

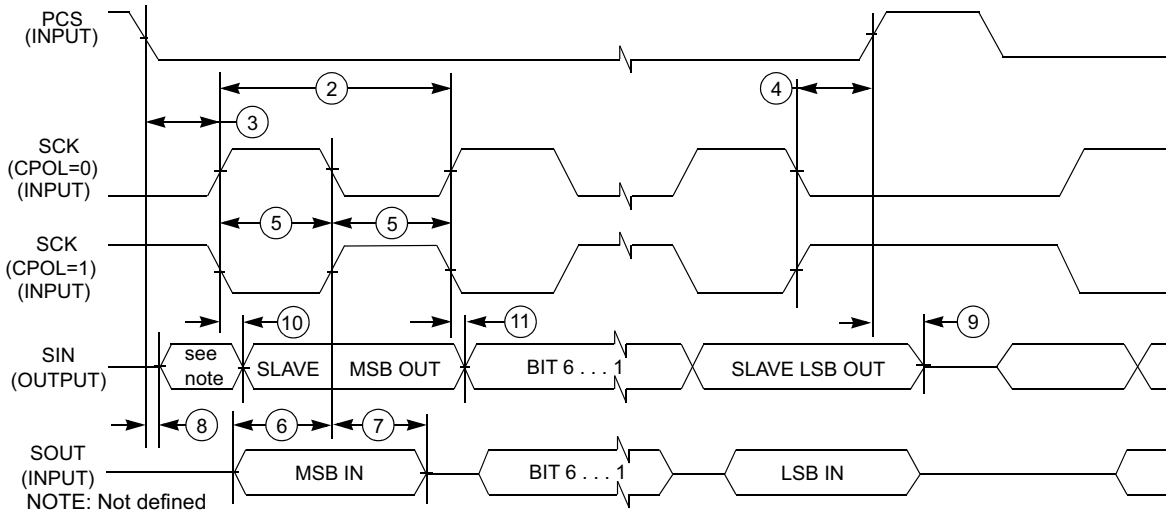


Figure 38. LPSPI Slave mode timing (CPHA = 1)

4.9.2 LPI2C module timing parameters

This section describes the timing parameters of the LPI2C module.

Table 83. LPI2C module timing parameters

Symbol	Description		Min	Max	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	[1]
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		High speed mode (Hs-mode)	0	3400		
		Ultra Fast mode (UFm)	0	5000		

[1] Hs-mode and Ultra Fast mode are supported in slave mode.

4.9.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD3.0 (Single Data Rate) timing and eMMC5.0 (up to 200 MHz) timing.

4.9.3.1 SD3.0/eMMC4.3 (Single Data Rate) specifications

Figure 39 depicts the timing of SD3.0/eMMC4.3, and Table 84 lists the SD/eMMC4.3 timing characteristics.

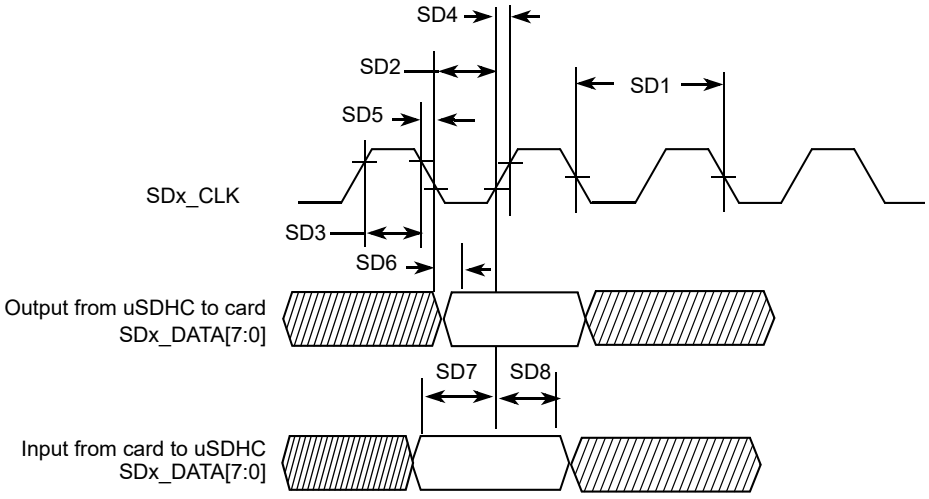


Figure 39. SD/eMMC4.3 timing

Table 84. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.9.3.2 eMMC4.4/4.41/SD3.0 (Dual Data Rate) AC timing)

Figure 40 depicts the timing of eMMC4.4/4.41/SD3.0. Table 85 lists the eMMC4.4/4.41/SD3.0 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

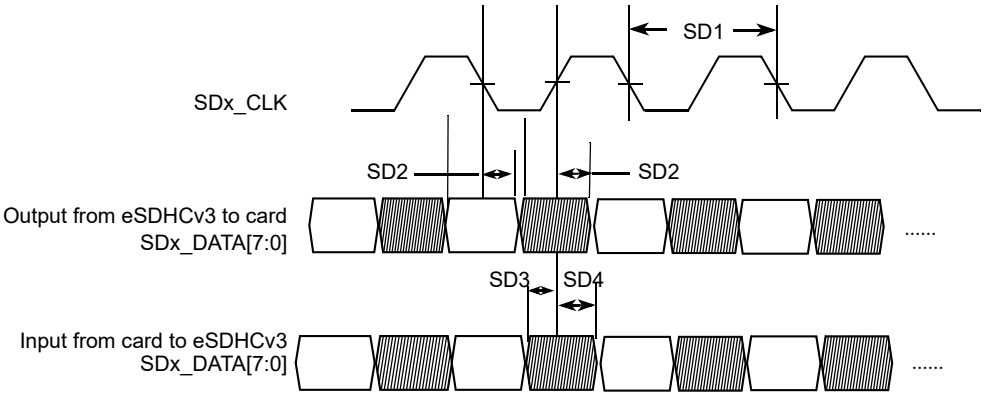


Figure 40. eMMC4.4/4.41/SD3.0 timing

Table 85. eMMC4.4/4.41/SD3.0 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.2	—	ns

4.9.3.3 SDR50/SDR104 AC timing

Figure 41 depicts the timing of SDR50/SDR104, and Table 86 lists the SDR50/SDR104 timing characteristics.

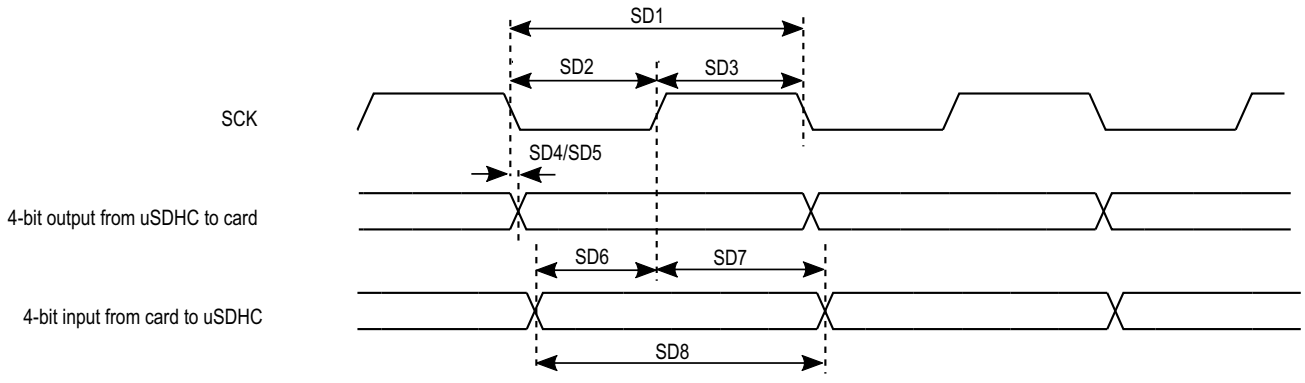


Figure 41. SDR50/SDR104 timing

Table 86. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.9.3.4 HS200 mode timing

Figure 42 depicts the timing of HS200 mode, and Table 87 lists the HS200 timing characteristics.

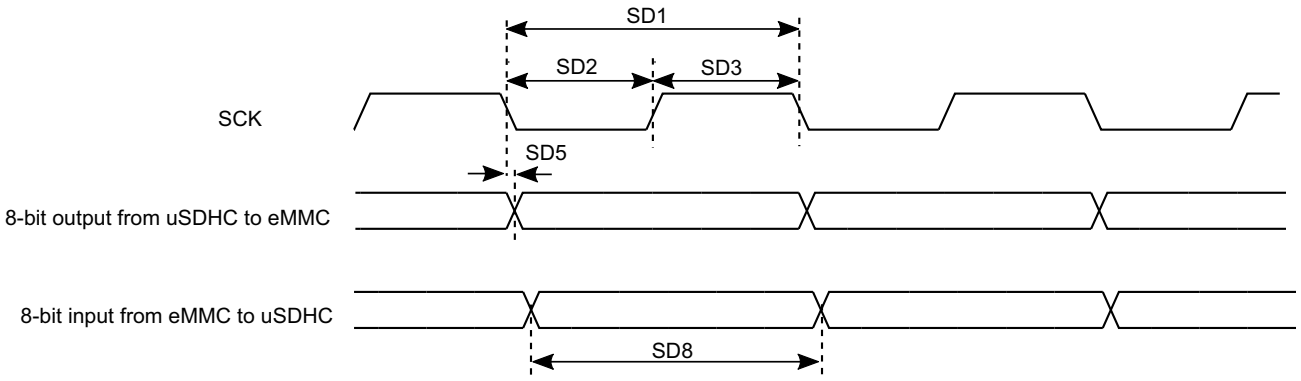


Figure 42. HS200 mode timing

Table 87. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.9.3.5 HS400 specifications - eMMC 5.0 only

Be aware that only data are sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for HS200 mode. Check SD5 and SD8 parameters in the HS200 interface timing specifications table for CMD input/output timing of HS400 mode.

Table 87 lists the HS400 timing characteristics.

Table 88. HS400 interface timing specification

Symbol	Description	Min	Max	Unit
	Operating voltage	1.71	1.95	V
Card input clock				
	Clock frequency	0	200	MHz
SD1	Clock period	5.0	—	ns
SD2	Clock Low time	0.46 x SD1	0.54 x SD1	ns
SD3	Clock High time	0.46 x SD1	0.54 x SD1	ns
SDHC output / card Inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)				
SD4	Output skew from data to edge of SCK	0.45	—	ns
SD5	Output skew from edge of SCK to data	0.45	—	ns
SDHC input / card outputs (reference to strobe)				
SD6	SDHC input skew	—	0.45	ns
SD7	SDHC hold skew	—	0.45	ns

Figure 42 depicts the timing of HS400.

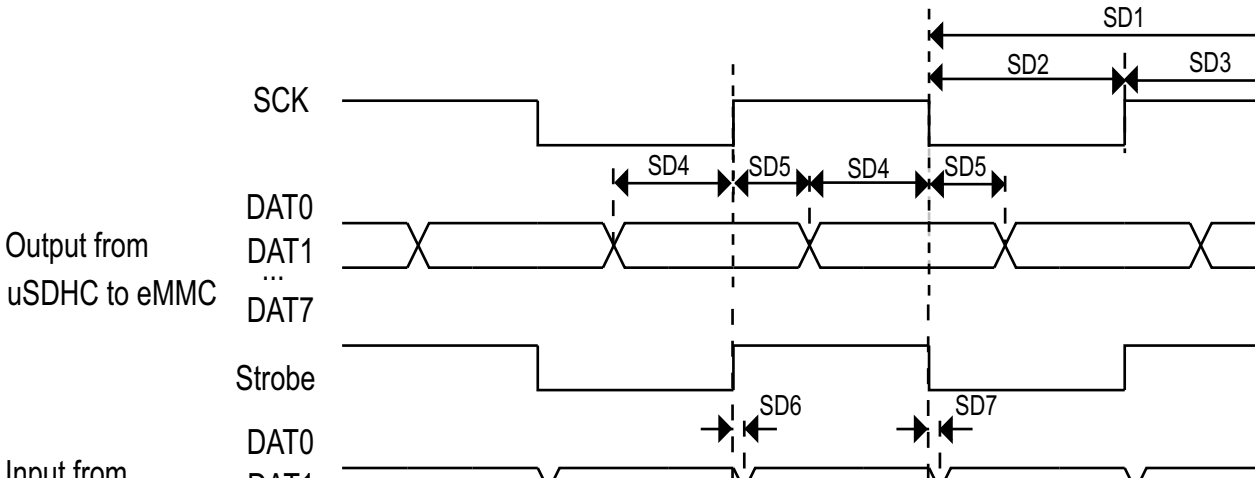


Figure 43. HS400 timing

4.9.3.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50/HS200/HS400 mode is 1.8 V.

4.9.4 Ethernet controller (ENET) AC electrical specifications

4.9.4.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.9.4.1.1 MII receive signal timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Figure 44 shows MII receive signal timings. Table 89 describes the timing parameters (M1–M4) shown in the figure.

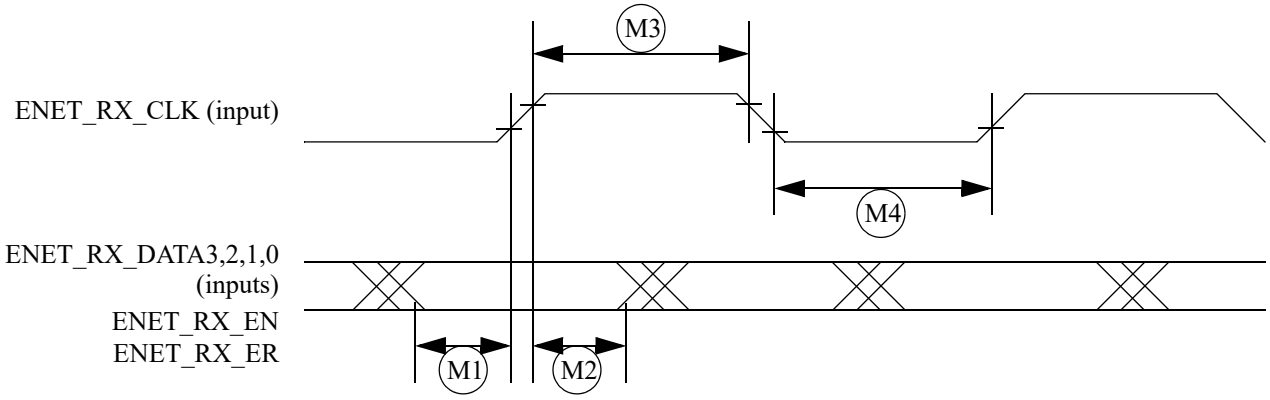


Figure 44. MII receive signal timing diagram

Table 89. MII receive signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.9.4.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 45 shows MII transmit signal timings. Table 90 describes the timing parameters (M5–M8) shown in the figure.

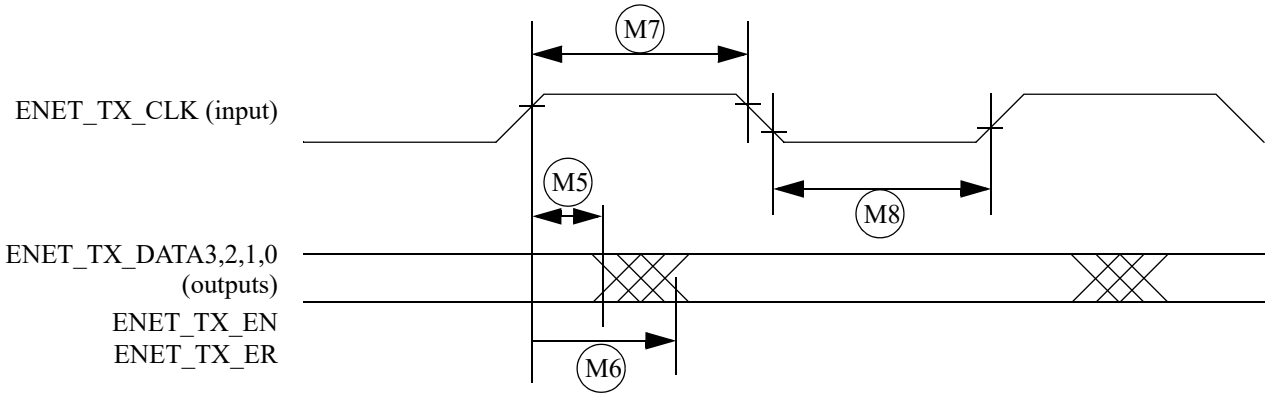


Figure 45. MII transmit signal timing diagram

Table 90. MII transmit signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.9.4.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 46 shows MII asynchronous input timings. Table 91 describes the timing parameter (M9) shown in the figure.

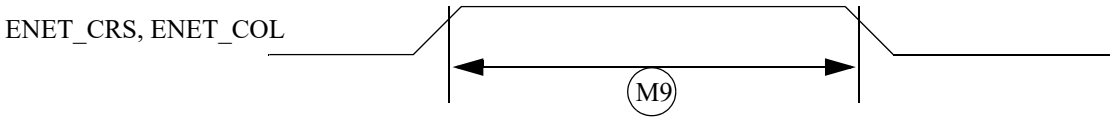


Figure 46. MII asynchronous inputs timing diagram

Table 91. MII asynchronous inputs signal timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.9.4.1.4 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 47 shows MII asynchronous input timings. Table 92 describes the timing parameters (M10–M15) shown in the figure.

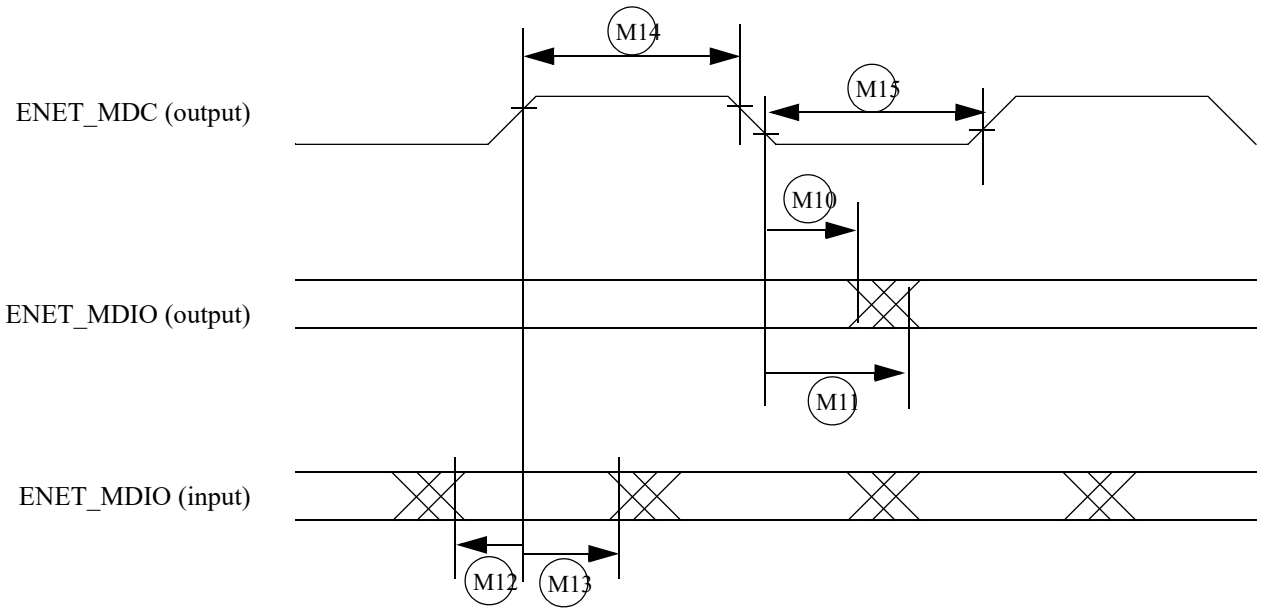


Figure 47. MII serial management channel timing diagram

Table 92. MII serial management channel timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.9.4.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock.

Figure 48 shows RMII mode timings. Table 93 describes the timing parameters (M16–M21) shown in the figure.

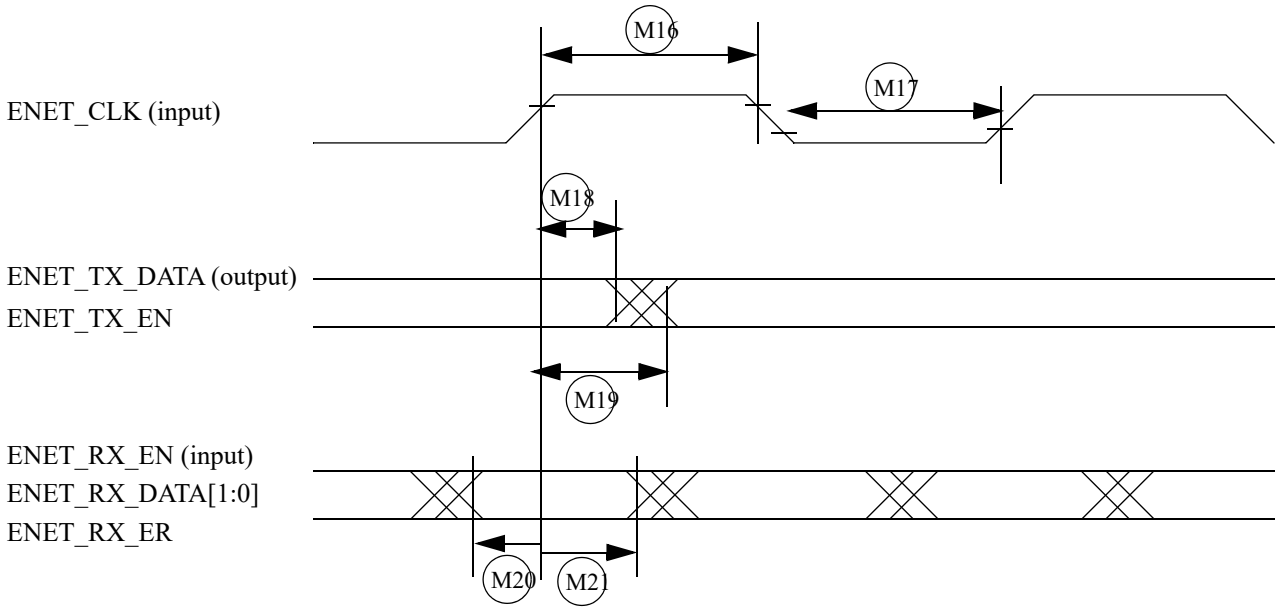


Figure 48. RMII mode signal timing diagram

Table 93. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	13	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	2	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.9.4.3 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 94. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps

Table 94. RGMII signal switching specifications[1] (continued)

Symbol	Description	Min.	Max.	Unit
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	85	%
Duty_T[4]	Duty cycle for 10/100T	40	90	%
Tr/Tf	Rise/fall time (20–80%)	—	0.98	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

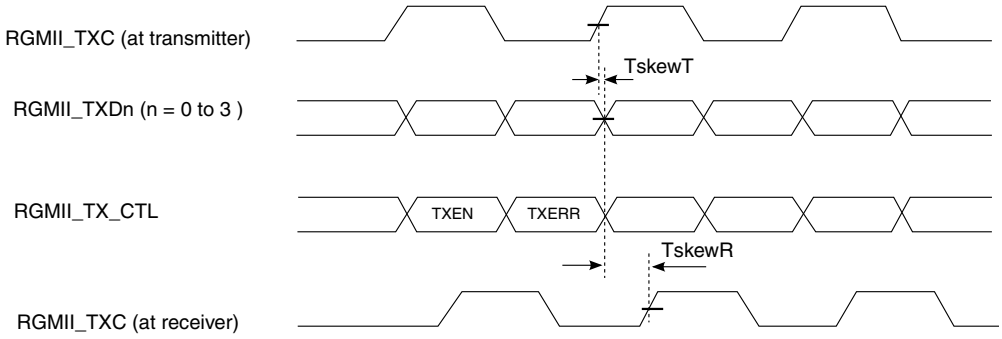


Figure 49. RGMII transmit signal timing diagram

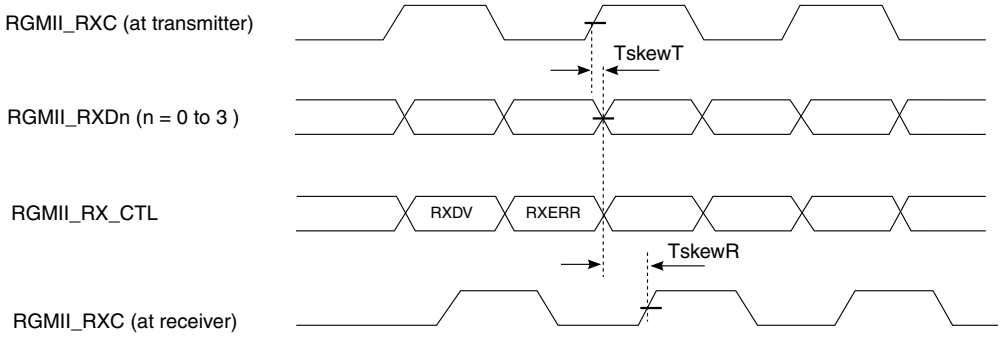


Figure 50. RGMII receive signal timing diagram

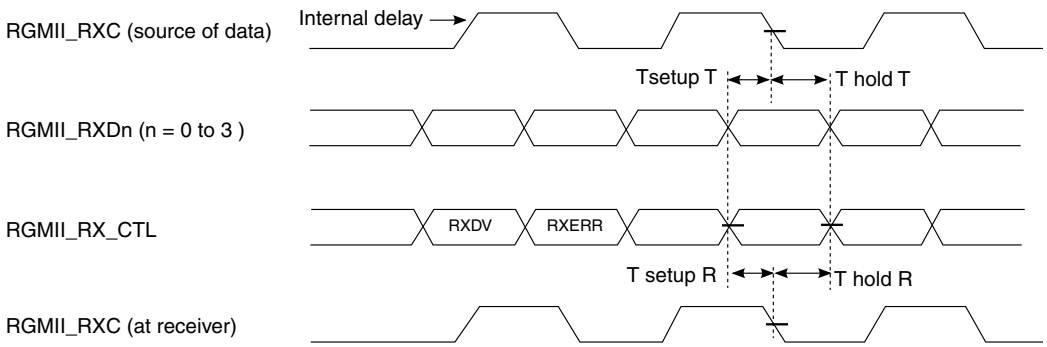


Figure 51. RGMII receive signal timing diagram with internal delay

4.9.5 Controller Area Network (CAN) AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has three CAN modules available. Tx and Rx ports are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

Please refer to Section 4.3.2.1, General purpose I/O (GPIO) AC parameters.

4.9.6 LPUART electrical specifications

Please refer to Section 4.3.2.1, General purpose I/O (GPIO) AC parameters.

4.9.7 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE

  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

4.10 Timers

This section provides information on timers.

4.10.1 Pulse Width Modulator (PWM) characteristics

This section describes the electrical information of the PWM.

Table 95. PWM timing parameters

Parameter	Symbol	Typ	Max	Unit
PWM Clock Frequency	—	—	240	MHz
Output skew	—	—	2	ns

4.10.2 Quad timer timing

Table 96 lists the quad timer parameters.

Table 96. Quad timer timing

Characteristic	Symbo	Min[1]	Max	Unit	See Figure
Timer input period	T_{IN}	2T + 6	—	ns	
Timer input high/low period	T_{INHL}	1T + 3	—	ns	
Timer output period	T_{OUT}	33	—	ns	
Timer output high/low period	T_{OUTHL}	16.7	—	ns	

[1] T = clock cycle. For 60 MHz operation, T = 16.7 ns.

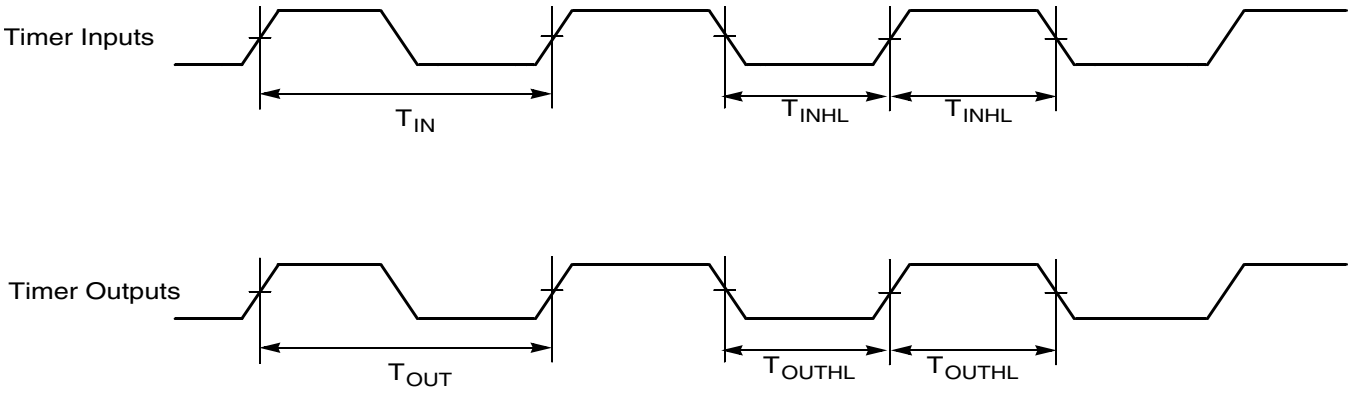


Figure 52. Quad timer timing

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 97 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX RT1160 Fuse Map and the System Boot chapter in *i.MX RT1160 Reference Manual (IMXRT1160RM)*.

Table 97. Fuses and associated pins used for boot

Pad	Default setting on reset	eFuse name	Details
GPIO_LPSR_02	35 K pull-down	BOOT_MODE[0]	
GPIO_LPSR_03	35 K pull-down	BOOT_MODE[1]	
GPIO_DISP_B1_06	HighZ	BT_CFG[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
GPIO_DISP_B1_07	HighZ	BT_CFG[1]	
GPIO_DISP_B1_08	HighZ	BT_CFG[2]	
GPIO_DISP_B1_09	HighZ	BT_CFG[3]	
GPIO_DISP_B1_10	HighZ	BT_CFG[4]	
GPIO_DISP_B1_11	HighZ	BT_CFG[5]	
GPIO_DISP_B2_00	HighZ	BT_CFG[6]	
GPIO_DISP_B2_01	HighZ	BT_CFG[7]	
GPIO_DISP_B2_02	HighZ	BT_CFG[8]	
GPIO_DISP_B2_03	HighZ	BT_CFG[9]	
GPIO_DISP_B2_04	HighZ	BT_CFG[10]	
GPIO_DISP_B2_05	HighZ	BT_CFG[11]	

5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 98. Boot through NAND

PAD Name	IO Function	ALT	Comments
GPIO_EMC_B1_00	semc.DATA[0]	ALT 0	—
GPIO_EMC_B1_01	semc.DATA[1]	ALT 0	—
GPIO_EMC_B2_02	semc.DATA[2]	ALT 0	—

Table 98. Boot through NAND

GPIO_EMC_B1_03	semc.DATA[3]	ALT 0	—
GPIO_EMC_B1_04	semc.DATA[4]	ALT 0	—
GPIO_EMC_B1_05	semc.DATA[5]	ALT 0	—
GPIO_EMC_B1_06	semc.DATA[6]	ALT 0	—
GPIO_EMC_B1_07	semc.DATA[7]	ALT 0	—
GPIO_EMC_B1_30	semc.DATA[8]	ALT 0	—
GPIO_EMC_B1_31	semc.DATA[9]	ALT 0	—
GPIO_EMC_B1_32	semc.DATA[10]	ALT 0	—
GPIO_EMC_B1_33	semc.DATA[11]	ALT 0	—
GPIO_EMC_B1_34	semc.DATA[12]	ALT 0	—
GPIO_EMC_B1_35	semc.DATA[13]	ALT 0	—
GPIO_EMC_B1_36	semc.DATA[14]	ALT 0	—
GPIO_EMC_B1_37	semc.DATA[15]	ALT 0	—
GPIO_EMC_B1_18	semc.ADDR[9]	ALT 0	—
GPIO_EMC_B1_19	semc.ADDR[11]	ALT 0	—
GPIO_EMC_B1_20	semc.ADDR[12]	ALT 0	—
GPIO_EMC_B1_22	semc.BA1	ALT 0	—
GPIO_EMC_B1_41	semc.CSX[0]	ALT 0	—

Table 99. Boot through FlexSPI1

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B2_00	flexspi1.B_DATA[3]	ALT 1	—
GPIO_SD_B2_01	flexspi1.B_DATA[2]	ALT 1	—
GPIO_SD_B2_02	flexspi1.B_DATA[1]	ALT 1	—
GPIO_SD_B2_03	flexspi1.B_DATA[0]	ALT 1	—
GPIO_SD_B2_04	flexspi1.B_SCLK	ALT 1	—
GPIO_SD_B1_05	flexspi1.B_DQS	ALT 8	—
GPIO_SD_B1_04	flexspi1.B_SS0_B	ALT 8	—
GPIO_SD_B1_03	flexspi1.B_SS1_B	ALT 9	—
GPIO_SD_B2_05	flexspi1.A_DQS	ALT 1	—
GPIO_EMC_B2_18	flexspi1.A_DQS	ALT 6	Secondary option for DQS
GPIO_SD_B2_06	flexspi1.A_SS0_B	ALT 1	—
GPIO_SD_B1_02	flexspi1.A_SS1_B	ALT 9	—

Table 99. Boot through FlexSPI1 (continued)

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B2_07	flexspi1.A_SCLK	ALT 1	—
GPIO_SD_B2_08	flexspi1.A_DATA[0]	ALT 1	—
GPIO_SD_B2_09	flexspi1.A_DATA[1]	ALT 1	—
GPIO_SD_B2_10	flexspi1.A_DATA[2]	ALT 1	—
GPIO_SD_B2_11	flexspi1.A_DATA[3]	ALT 1	—

Table 100. Boot through FlexSPI2 (QSPI/HyperFLASH)

PAD Name	IO Function	ALT	Comments
GPIO_EMC_B1_41	flexspi2.B_DATA[7]	ALT 4	—
GPIO_EMC_B2_00	flexspi2.B_DATA[6]	ALT 4	—
GPIO_EMC_B2_01	flexspi2.B_DATA[5]	ALT 4	—
GPIO_EMC_B2_02	flexspi2.B_DATA[4]	ALT 4	—
GPIO_EMC_B2_03	flexspi2.B_DATA[3]	ALT 4	—
GPIO_EMC_B2_04	flexspi2.B_DATA[2]	ALT 4	—
GPIO_EMC_B2_05	flexspi2.B_DATA[1]	ALT 4	—
GPIO_EMC_B2_06	flexspi2.B_DATA[0]	ALT 4	—
GPIO_EMC_B2_07	flexspi2.B_DQS	ALT 4	—
GPIO_EMC_B2_08	flexspi2.B_SS0_B	ALT 4	—
GPIO_EMC_B2_09	flexspi2.B_SCLK	ALT 4	—
GPIO_EMC_B2_10	flexspi2.A_SCLK	ALT 4	—
GPIO_EMC_B2_11	flexspi2.A_SS0_B	ALT 4	—
GPIO_EMC_B2_12	flexspi2.A_DQS	ALT 4	—
GPIO_EMC_B2_13	flexspi2.A_DATA[0]	ALT 4	—
GPIO_EMC_B2_14	flexspi2.A_DATA[1]	ALT 4	—
GPIO_EMC_B2_15	flexspi2.A_DATA[2]	ALT 4	—
GPIO_EMC_B2_16	flexspi2.A_DATA[3]	ALT 4	—
GPIO_EMC_B2_17	flexspi2.A_DATA[4]	ALT 4	—
GPIO_EMC_B2_18	flexspi2.A_DATA[5]	ALT 4	—
GPIO_EMC_B2_19	flexspi2.A_DATA[6]	ALT 4	—
GPIO_EMC_B2_20	flexspi2.A_DATA[7]	ALT 4	—

Table 101. FlexSPI reset

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B1_00	gpio_mux4.IO[3]	ALT 5	—
GPIO_EMC_B1_40	gpio_mux2.IO[8]	ALT 5	Secondary option

Table 102. Boot through SAI1

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_17	sai1.MCLK	ALT 0	—
GPIO_AD_18	sai1.RX_SYNC	ALT 0	—
GPIO_AD_19	sai1.RX_BCLK	ALT 0	—
GPIO_AD_20	sai1.RX_DATA[0]	ALT 0	—
GPIO_AD_21	sai1.TX_DATA[0]	ALT 0	—
GPIO_AD_22	sai1.TX_BCLK	ALT 0	—
GPIO_AD_23	sai1.TX_SYNC	ALT 0	—

Table 103. Boot through SD1

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_32	usdhc1.CD_B	ALT 4	—
GPIO_AD_33	usdhc1.WP	ALT 4	—
GPIO_AD_34	usdhc1.VSELECT	ALT 4	—
GPIO_AD_35	usdhc1.RESET_B	ALT 4	—
GPIO_SD_B1_00	usdhc1.CMD	ALT 0	—
GPIO_SD_B1_01	usdhc1.CLK	ALT 0	—
GPIO_SD_B1_02	usdhc1.DATA0	ALT 0	—
GPIO_SD_B1_03	usdhc1.DATA1	ALT 0	—
GPIO_SD_B1_04	usdhc1.DATA2	ALT 0	—
GPIO_SD_B1_05	usdhc1.DATA3	ALT 0	—

Table 104. Boot through SD2

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_26	usdhc2.CD_B	ALT 11	—
GPIO_AD_27	usdhc2.WP	ALT 11	—
GPIO_AD_28	usdhc2.VSELECT	ALT 11	—
GPIO_SD_B2_00	usdhc2.DATA3	ALT 0	—
GPIO_SD_B2_01	usdhc2.DATA2	ALT 0	—

Table 104. Boot through SD2 (continued)

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B2_02	usdhc2.DATA1	ALT 0	—
GPIO_SD_B2_03	usdhc2.DATA0	ALT 0	—
GPIO_SD_B2_04	usdhc2.CLK	ALT 0	—
GPIO_SD_B2_05	usdhc2.CMD	ALT 0	—
GPIO_SD_B2_06	usdhc2.RESET_B	ALT 0	—
GPIO_SD_B2_08	usdhc2.DATA4	ALT 0	—
GPIO_SD_B2_09	usdhc2.DATA5	ALT 0	—
GPIO_SD_B2_10	usdhc2.DATA6	ALT 0	—
GPIO_SD_B2_11	usdhc2.DATA7	ALT 0	—

Table 105. Boot through SPI1

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_28	lpspi1.SCK	ALT 0	—
GPIO_AD_29	lpspi1.PCS0	ALT 0	—
GPIO_AD_30	lpspi1.SDO	ALT 0	—
GPIO_AD_31	lpspi1.SDI	ALT 0	—

Table 106. Boot through SPI2

PAD Name	IO Function	Mux Mode	Comments
GPIO_SD_B2_07	lpspi2.SCK	ALT 6	—
GPIO_SD_B2_08	lpspi2.PCS0	ALT 6	—
GPIO_SD_B2_09	lpspi2.SDO	ALT 6	—
GPIO_SD_B2_10	lpspi2.SDI	ALT 6	—

Table 107. Boot through SPI3

PAD Name	IO Function	Mux Mode	Comments
GPIO_DISP_B1_04	lpspi3.SCK	ALT 9	—
GPIO_DISP_B1_07	lpspi3.PCS0	ALT 9	—
GPIO_DISP_B1_06	lpspi3.SDO	ALT 9	—
GPIO_DISP_B1_05	lpspi3.SDI	ALT 9	—

Table 108. Boot through SPI4

PAD Name	IO Function	Mux Mode	Comments
GPIO_DISP_B2_12	lpspi4.SCK	ALT 9	—
GPIO_DISP_B2_15	lpspi4.PCS0	ALT 9	—
GPIO_DISP_B2_14	lpspi4.SDO	ALT 9	—
GPIO_DISP_B2_13	lpspi4.SDI	ALT 9	—

Table 109. Boot through UART1

PAD Name	IO Function	Mux Mode	Comments
GPIO_AD_24	lpuart1.TX	ALT 0	—
GPIO_AD_25	lpuart1.RX	ALT 0	—
GPIO_AD_26	lpuart1.CTS_B	ALT 0	—
GPIO_AD_27	lpuart1.RTS_B	ALT 0	—

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14 x 14 mm package information

6.1.1 14 x 14 mm, 0.8 mm pitch, ball matrix

Figure 53 shows the top, bottom, and side views of the 14 x 14 mm MAPBGA package.

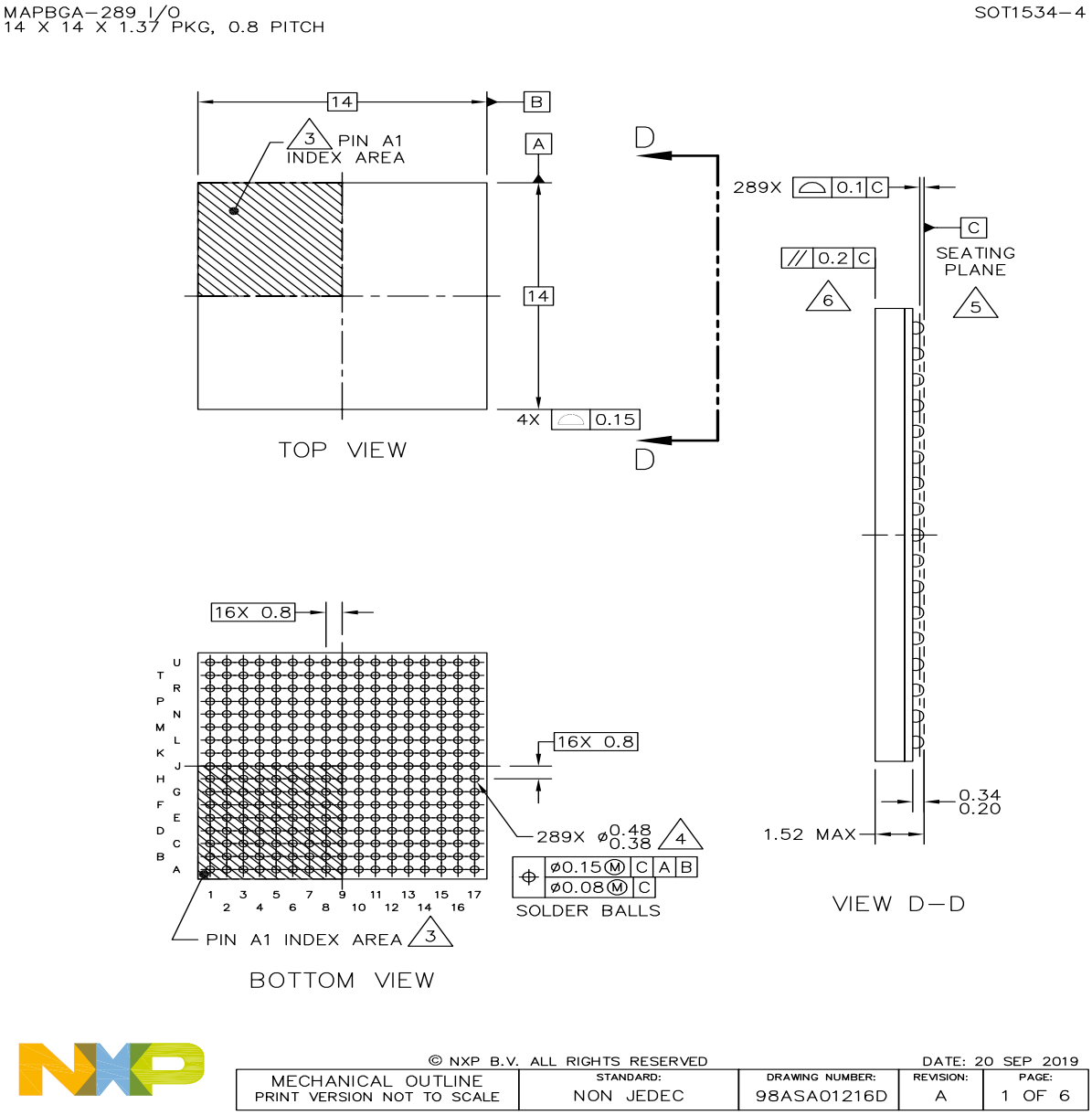


Figure 53. 14 x 14 mm BGA, case x package top, bottom, and side Views

6.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 110 shows the device connection list for ground, sense, and reference contact signals.

Table 110. 14 x 14 mm supplies contact assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	G16	—
DAC_OUT	H16	—
DCDC_ANA	M7, M8	—
DCDC_ANA_SENSE	M6	—
DCDC_DIG	K8, K9, L8	—
DCDC_DIG_SENSE	L7	—
DCDC_GND	K6, K7, L6	—
DCDC_IN	M5, N5	—
DCDC_IN_Q	L5	—
DCDC_LN	T4, U4	—
DCDC_LP	T3, U3	—
DCDC_MODE	N4	—
DCDC_PSWITCH	P3	—
NVCC_DISP1	D12	—
NVCC_DISP2	E7	—
NVCC_EMC1	F6, F7, G6	—
NVCC_EMC2	H6, J6	—
NVCC_GPIO	M12	—
NVCC_LPSR	P7	—
NVCC_SNVS	U11	—
NVCC_SD1	D14	—
NVCC_SD2	G13	—
VDD_LPSR_ANA	P12	—
VDD_LPSR_DIG	P11	—
VDD_LPSR_IN	R12	—
VDD_MIPI_1P0	F10	—
VDD_MIPI_1P8	F9	—
VDD_USB_1P8	H12	—
VDD_USB_3P3	G12	—

Table 110. 14 x 14 mm supplies contact assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SOC_IN	H8, H9, H10, J8, J9, J10, K10	
VDD_SNVS_ANA	U14	—
VDD_SNVS_DIG	T14	—
VDD_SNVS_IN	U12	—
VDDA_1P0	N11	—
VDDA_1P8_IN	M11	—
VDDA_ADC_1P8	K15	
VDDA_ADC_3P3	J13	—
VSS	A1, A17, B7, C8, C10, C12, C14, D4, F11, F12, F13, G3, G7, G8, G9, G10, G11, G15, H7, H11, J7, J11, K11, L3, L10, L11, L15, P4, P14, R4, R7, T12, U1, U17	—

Table 111 shows an alpha-sorted list of functional contact assignments of the 14 x 14 mm package.

Table 111. 14 x 14 mm functional contact assignment

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
CLK1_N	T15	—	—	—		—	—
CLK1_P	U15	—	—	—		—	—
GPIO_AD_00	N12	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX2_IO31	Input	35K PU[1]
GPIO_AD_01	R14	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO0	Input	35K PU
GPIO_AD_02	R13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO1	Input	35K PD[2]
GPIO_AD_03	P15	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO2	Input	35K PD
GPIO_AD_04	M13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO3	Input	35K PD
GPIO_AD_05	P13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO4	Input	35K PD
GPIO_AD_06	N13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO5	Input	35K PD
GPIO_AD_07	T17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO6	Input	35K PD
GPIO_AD_08	R15	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO7	Input	35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_AD_09	R16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO8	Input	35K PD
GPIO_AD_10	R17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO9	Input	35K PD
GPIO_AD_11	P16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO10	Input	35K PD
GPIO_AD_12	P17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO11	Input	35K PD
GPIO_AD_13	L12	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO12	Input	35K PD
GPIO_AD_14	N14	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO13	Input	35K PD
GPIO_AD_15	M14	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO14	Input	35K PD
GPIO_AD_16	N17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO15	Input	35K PD
GPIO_AD_17	N15	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO16	Input	35K PD
GPIO_AD_18	M16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO17	Input	35K PU
GPIO_AD_19	L16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO18	Input	35K PD
GPIO_AD_20	K13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO19	Input	35K PD
GPIO_AD_21	K14	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO20	Input	35K PD
GPIO_AD_22	K12	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO21	Input	35K PD
GPIO_AD_23	J12	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO22	Input	35K PD
GPIO_AD_24	L13	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO23	Input	35K PD
GPIO_AD_25	M15	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO24	Input	35K PD
GPIO_AD_26	L14	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO25	Input	35K PU
GPIO_AD_27	N16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO26	Input	35K PU

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_AD_28	L17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO27	Input	35K PD
GPIO_AD_29	M17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO28	Input	35K PD
GPIO_AD_30	K17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO29	Input	35K PD
GPIO_AD_31	J17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO30	Input	35K PD
GPIO_AD_32	K16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX3_IO31	Input	35K PD
GPIO_AD_33	H17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX4_IO0	Input	35K PD
GPIO_AD_34	J16	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX4_IO1	Input	35K PD
GPIO_AD_35	G17	NVCC_GPIO	Digital GPIO	ALT 5	GPIO_MUX4_IO2	Input	35K PU
GPIO_DISP_B1_00	E13	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO21	Input	50/35K PD[3]
GPIO_DISP_B1_01	D13	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO22	Input	50/35K PD
GPIO_DISP_B1_02	D11	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO23	Input	50/35K PD
GPIO_DISP_B1_03	E11	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO24	Input	50/35K PD
GPIO_DISP_B1_04	E10	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO25	Input	50/35K PD
GPIO_DISP_B1_05	C11	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO26	Input	50/35K PD
GPIO_DISP_B1_06	D10	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO27	Input	Highz
GPIO_DISP_B1_07	E12	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO28	Input	Highz
GPIO_DISP_B1_08	A15	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO29	Input	Highz
GPIO_DISP_B1_09	C13	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO30	Input	Highz
GPIO_DISP_B1_10	B14	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX4_IO31	Input	Highz

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_DISP_B1_11	A14	NVCC_DISP1	Digital GPIO	ALT 5	GPIO_MUX5_IO0	Input	Highz
GPIO_DISP_B2_00	E8	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO1	Input	Highz
GPIO_DISP_B2_01	F8	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO2	Input	Highz
GPIO_DISP_B2_02	E9	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO3	Input	Highz
GPIO_DISP_B2_03	D7	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO4	Input	Highz
GPIO_DISP_B2_04	C7	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO5	Input	Highz
GPIO_DISP_B2_05	C9	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO6	Input	Highz
GPIO_DISP_B2_06	C6	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO7	Input	35K PD
GPIO_DISP_B2_07	D6	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO8	Input	35K PD
GPIO_DISP_B2_08	B5	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO9	Input	35K PD
GPIO_DISP_B2_09	D8	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO10	Input	35K PD
GPIO_DISP_B2_10	D9	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO11	Input	35K PD
GPIO_DISP_B2_11	A6	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO12	Input	35K PD
GPIO_DISP_B2_12	B6	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO13	Input	35K PD
GPIO_DISP_B2_13	A5	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO14	Input	35K PD
GPIO_DISP_B2_14	A7	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO15	Input	35K PD
GPIO_DISP_B2_15	A4	NVCC_DISP2	Digital GPIO	ALT 5	GPIO_MUX5_IO16	Input	35K PU
GPIO_EMC_B1_00	F3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO0	Input	50/35K PD
GPIO_EMC_B1_01	F2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO1	Input	50/35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_EMC_B1_02	G4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO2	Input	50/35K PD
GPIO_EMC_B1_03	E4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO3	Input	50/35K PD
GPIO_EMC_B1_04	H5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO4	Input	50/35K PD
GPIO_EMC_B1_05	F4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO5	Input	50/35K PD
GPIO_EMC_B1_06	H4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO6	Input	50/35K PD
GPIO_EMC_B1_07	H3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO7	Input	50/35K PD
GPIO_EMC_B1_08	F5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO8	Input	50/35K PD
GPIO_EMC_B1_09	A3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO9	Input	50/35K PD
GPIO_EMC_B1_10	A2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO10	Input	50/35K PD
GPIO_EMC_B1_11	C2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO11	Input	50/35K PD
GPIO_EMC_B1_12	C5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO12	Input	50/35K PD
GPIO_EMC_B1_13	D5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO13	Input	50/35K PD
GPIO_EMC_B1_14	B1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO14	Input	50/35K PD
GPIO_EMC_B1_15	C1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO15	Input	50/35K PD
GPIO_EMC_B1_16	D3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO16	Input	50/35K PD
GPIO_EMC_B1_17	B3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO17	Input	50/35K PD
GPIO_EMC_B1_18	B4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO18	Input	50/35K PD
GPIO_EMC_B1_19	C4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO19	Input	50/35K PD
GPIO_EMC_B1_20	C3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO20	Input	50/35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_EMC_B1_21	G2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO21	Input	50/35K PD
GPIO_EMC_B1_22	H2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO22	Input	50/35K PD
GPIO_EMC_B1_23	B2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO23	Input	50/35K PD
GPIO_EMC_B1_24	J5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO24	Input	50/35K PD
GPIO_EMC_B1_25	J4	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO25	Input	50/35K PD
GPIO_EMC_B1_26	J3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO26	Input	50/35K PD
GPIO_EMC_B1_27	G5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO27	Input	50/35K PD
GPIO_EMC_B1_28	E5	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO28	Input	50/35K PD
GPIO_EMC_B1_29	E6	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO29	Input	50/35K PD
GPIO_EMC_B1_30	E3	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO30	Input	50/35K PD
GPIO_EMC_B1_31	D2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX1_IO31	Input	50/35K PD
GPIO_EMC_B1_32	D1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO0	Input	50/35K PD
GPIO_EMC_B1_33	E2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO1	Input	50/35K PD
GPIO_EMC_B1_34	E1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO2	Input	50/35K PD
GPIO_EMC_B1_35	F1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO3	Input	50/35K PD
GPIO_EMC_B1_36	G1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO4	Input	50/35K PD
GPIO_EMC_B1_37	H1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO5	Input	50/35K PD
GPIO_EMC_B1_38	J1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO6	Input	50/35K PD
GPIO_EMC_B1_39	J2	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO7	Input	50/35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_EMC_B1_40	K1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO8	Input	50/35K PD
GPIO_EMC_B1_41	L1	NVCC_EMC1	Digital GPIO	ALT 5	GPIO_MUX2_IO9	Input	50/35K PD
GPIO_EMC_B2_00	K2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO10	Input	50/35K PD
GPIO_EMC_B2_01	K4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO11	Input	50/35K PD
GPIO_EMC_B2_02	K3	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO12	Input	50/35K PD
GPIO_EMC_B2_03	R1	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO13	Input	50/35K PD
GPIO_EMC_B2_04	M1	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO14	Input	50/35K PD
GPIO_EMC_B2_05	N1	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO15	Input	50/35K PD
GPIO_EMC_B2_06	T1	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO16	Input	50/35K PD
GPIO_EMC_B2_07	M3	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO17	Input	50/35K PD
GPIO_EMC_B2_08	P1	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO18	Input	50/35K PU
GPIO_EMC_B2_09	N2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO19	Input	50/35K PD
GPIO_EMC_B2_10	R2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO20	Input	50/35K PD
GPIO_EMC_B2_11	L4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO21	Input	50/35K PU
GPIO_EMC_B2_12	M2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO22	Input	50/35K PD
GPIO_EMC_B2_13	K5	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO23	Input	50/35K PD
GPIO_EMC_B2_14	M4	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO24	Input	50/35K PD
GPIO_EMC_B2_15	L2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO25	Input	50/35K PD
GPIO_EMC_B2_16	P2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO26	Input	50/35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_EMC_B2_17	T2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO27	Input	50/35K PD
GPIO_EMC_B2_18	N3	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO28	Input	50/35K PD
GPIO_EMC_B2_19	U2	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO29	Input	50/35K PD
GPIO_EMC_B2_20	R3	NVCC_EMC2	Digital GPIO	ALT 5	GPIO_MUX2_IO30	Input	50/35K PD
GPIO_LPSR_00	N6	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO0	Input	35K PD
GPIO_LPSR_01	R6	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO1	Input	35K PD
GPIO_LPSR_02	P6	NVCC_LPSR	Digital GPIO	ALT 0	BOOT_MODE0	Input	35K PD
GPIO_LPSR_03	T7	NVCC_LPSR	Digital GPIO	ALT 0	BOOT_MODE1	Input	35K PD
GPIO_LPSR_04	N7	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO4	Input	35K PD
GPIO_LPSR_05	N8	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO5	Input	35K PD
GPIO_LPSR_06	P8	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO6	Input	35K PD
GPIO_LPSR_07	R8	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO7	Input	35K PD
GPIO_LPSR_08	U8	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO8	Input	35K PD
GPIO_LPSR_09	P5	NVCC_LPSR	Digital GPIO	ALT 10	GPIO12_IO9	Input	35K PD
GPIO_LPSR_10	R5	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_TRSTB	Input	35K PU
GPIO_LPSR_11	T5	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_TDO	Input	Highz
GPIO_LPSR_12	U5	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_TDI	Input	35K PU
GPIO_LPSR_13	U6	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_MOD	Input	35K PD
GPIO_LPSR_14	T6	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_TCK	Input	35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_LPSR_15	U7	NVCC_LPSR	Digital GPIO	ALT 0	JTAG_MUX_TMS	Input	35K PU
GPIO_SD_B1_00	B16	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO3	Input	50/35K PU
GPIO_SD_B1_01	D15	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO4	Input	50/35K PD
GPIO_SD_B1_02	C15	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO5	Input	50/35K PU
GPIO_SD_B1_03	B17	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO6	Input	50/35K PU
GPIO_SD_B1_04	B15	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO7	Input	50/35K PU
GPIO_SD_B1_05	A16	NVCC_SD1	Digital GPIO	ALT 5	GPIO_MUX4_IO8	Input	50/35K PD
GPIO_SD_B2_00	J15	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO9	Input	50/35K PD
GPIO_SD_B2_01	J14	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO10	Input	50/35K PD
GPIO_SD_B2_02	H13	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO11	Input	50/35K PD
GPIO_SD_B2_03	E15	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO12	Input	50/35K PD
GPIO_SD_B2_04	F14	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO13	Input	50/35K PU
GPIO_SD_B2_05	E14	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO14	Input	50/35K PU
GPIO_SD_B2_06	F17	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO15	Input	50/35K PU
GPIO_SD_B2_07	G14	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO16	Input	50/35K PD
GPIO_SD_B2_08	F15	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO17	Input	50/35K PD
GPIO_SD_B2_09	H15	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO18	Input	50/35K PD
GPIO_SD_B2_10	H14	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO19	Input	50/35K PD
GPIO_SD_B2_11	F16	NVCC_SD2	Digital GPIO	ALT 5	GPIO_MUX4_IO20	Input	50/35K PD

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
GPIO_SNVS_00	R10	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO3	Input	PD
GPIO_SNVS_01	P10	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO4	Input	PD
GPIO_SNVS_02	L9	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO5	Input	PD
GPIO_SNVS_03	M10	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO6	Input	PD
GPIO_SNVS_04	N10	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO7	Input	PD
GPIO_SNVS_05	P9	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO8	Input	PD
GPIO_SNVS_06	M9	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO9	Input	PD
GPIO_SNVS_07	R9	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO10	Input	PD
GPIO_SNVS_08	N9	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO11	Input	PD
GPIO_SNVS_09	R11	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO12	Input	PD
MIPI_CSI_CKP	B12	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_CSI_CKN	A12	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_CSI_DN0	A11	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_CSI_DN1	A13	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_CSI_DP0	B11	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_CSI_DP1	B13	VDD_MIPI_1P8	CSI	—	—	—	—
MIPI_DSI_CKP	B9	VDD_MIPI_1P8	DSI	—	—	—	—
MIPI_DSI_CKN	A9	VDD_MIPI_1P8	DSI	—	—	—	—
MIPI_DSI_DN0	A8	VDD_MIPI_1P8	DSI	—	—	—	—
MIPI_DSI_DN1	A10	VDD_MIPI_1P8	DSI	—	—	—	—
MIPI_DSI_DP0	B8	VDD_MIPI_1P8	DSI	—	—	—	—
MIPI_DSI_DP1	B10	VDD_MIPI_1P8	DSI	—	—	—	—
ONOFF	U10	NVCC_SNVS	ANALOG GPIO	ALT 0	RESET_B	Input	PU
PMIC_ON_REQ	U9	NVCC_SNVS	ANALOG GPIO	ALT 0	SNVS_LP_PMIC_ON _REQ	Output	Output high

Table 111. 14 x 14 mm functional contact assignment (continued)

Ball name	14 x 14 ball	Power group	Ball Types	Default setting			
				Default modes	Default function	Input/ output	Nominal value
PMIC_STBY_REQ	T9	NVCC_SNVS	ANALOG GPIO	ALT 0	CCM_PMIC_VSTBY_ REQ	Output	Output low
POR_B	T10	NVCC_SNVS	ANALOG GPIO	ALT 0	POR_B	—	PU
RTC_XTALI	T13	—	—	—	—	—	—
RTC_XTALO	U13	—	—	—	—	—	—
TEST_MODE	T11	NVCC_SNVS	ANALOG GPIO	ALT 0	TEST_MODE	Input	PD
USB1_DN	E16	—	—	—	—	—	—
USB1_DP	E17	—	—	—	—	—	—
USB2_DN	C16	—	—	—	—	—	—
USB2_DP	C17	—	—	—	—	—	—
USB1_VBUS	D17	—	—	—	—	—	—
USB2_VBUS	D16	—	—	—	—	—	—
XTALI	U16	—	—	—	—	—	—
XTALO	T16	—	—	—	—	—	—
WAKEUP	T8	NVCC_SNVS	ANALOG GPIO	ALT 5	GPIO13_IO0	Input	PU

1 Pull-up

2 Pull-down

3 Typical resistance value is 50 kΩ for 3.3 V and 35 kΩ for 1.8 V. The range is from 10 kΩ to 100 kΩ (3.3 V) and 20 kΩ to 50 kΩ (1.8 V).

6.1.3 14 x 14 mm, 0.8 mm pitch, ball map

Table 112 shows the 14 x 14 mm, 0.8 mm pitch ball map for the i.MX RT1160.

Table 112. 14 x 14 mm, 0.8 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	GPIO_EMC_B1_10	GPIO_EMC_B1_09	GPIO_DISP_B2_15	GPIO_DISP_B2_13	GPIO_DISP_B2_11	GPIO_DISP_B2_14	MIPI_DSI_DN0	MIPI_DSI_CKN	MIPI_DSI_DN1	MIPI_CSI_DN0	MIPI_CSI_CKN	MIPI_CSI_DN1	GPIO_DISP_B1_11	GPIO_DISP_B1_08	GPIO_SD_B1_05	VSS
B	GPIO_EMC_B1_14	GPIO_EMC_B1_23	GPIO_EMC_B1_17	GPIO_EMC_B1_18	GPIO_DISP_B2_08	GPIO_DISP_B2_12	VSS	MIPI_DSI_DP0	MIPI_DSI_CKP	MIPI_DSI_DP1	MIPI_CSI_DP0	MIPI_CSI_CKP	MIPI_CSI_DP1	GPIO_DISP_B1_10	GPIO_SD_B1_04	GPIO_SD_B1_00	GPIO_SD_B1_03
C	GPIO_EMC_B1_15	GPIO_EMC_B1_11	GPIO_EMC_B1_20	GPIO_EMC_B1_19	GPIO_EMC_B1_12	GPIO_DISP_B2_06	GPIO_DISP_B2_04	VSS	GPIO_DISP_B2_05	VSS	GPIO_DISP_B1_05	VSS	GPIO_DISP_B1_09	VSS	GPIO_SD_B1_02	USB2_DN	USB2_DP
D	GPIO_EMC_B1_32	GPIO_EMC_B1_31	GPIO_EMC_B1_16	VSS	GPIO_EMC_B1_13	GPIO_DISP_B2_07	GPIO_DISP_B2_03	GPIO_DISP_B2_09	GPIO_DISP_B2_10	GPIO_DISP_B1_06	GPIO_DISP_B1_02	NVCC_DISP1	GPIO_DISP_B1_01	NVCC_SD1	GPIO_SD_B1_01	USB2_VBUS	USB1_VBUS
E	GPIO_EMC_B1_34	GPIO_EMC_B1_33	GPIO_EMC_B1_30	GPIO_EMC_B1_03	GPIO_EMC_B1_28	GPIO_EMC_B1_29	NVCC_DISP2	GPIO_DISP_B2_00	GPIO_DISP_B2_02	GPIO_DISP_B1_04	GPIO_DISP_B1_03	GPIO_DISP_B1_07	GPIO_DISP_B1_00	GPIO_SD_B2_05	GPIO_SD_B2_03	USB1_DN	USB1_DP
F	GPIO_EMC_B1_35	GPIO_EMC_B1_01	GPIO_EMC_B1_00	GPIO_EMC_B1_05	GPIO_EMC_B1_08	NVCC_EMC1	NVCC_EMC1	GPIO_DISP_B2_01	VDD_MIPI_1P8	VDD_MIPI_1P0	VSS	VSS	VSS	GPIO_SD_B2_04	GPIO_SD_B2_08	GPIO_SD_B2_11	GPIO_SD_B2_06
G	GPIO_EMC_B1_36	GPIO_EMC_B1_21	VSS	GPIO_EMC_B1_02	GPIO_EMC_B1_27	NVCC_EMC1	VSS	VSS	VSS	VSS	VSS	VDD_USB_3P3	NVCC_SD2	GPIO_SD_B2_07	VSS	ADC_VREFH	GPIO_AD_35
H	GPIO_EMC_B1_37	GPIO_EMC_B1_22	GPIO_EMC_B1_07	GPIO_EMC_B1_06	GPIO_EMC_B1_04	NVCC_EMC2	VSS	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VSS	VDD_USB_1P8	GPIO_SD_B2_02	GPIO_SD_B2_10	GPIO_SD_B2_09	DAC_OUT	GPIO_AD_33
J	GPIO_EMC_B1_38	GPIO_EMC_B1_39	GPIO_EMC_B1_26	GPIO_EMC_B1_25	GPIO_EMC_B1_24	NVCC_EMC2	VSS	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VSS	GPIO_AD_23	VDDA_ADC_3P3	GPIO_SD_B2_01	GPIO_SD_B2_00	GPIO_AD_34	GPIO_AD_31

Table 112. 14 x 14 mm, 0.8 mm pitch, ball map (continued)

K	GPIO_EMC_B1_40	GPIO_EMC_B2_00	GPIO_EMC_B2_02	GPIO_EMC_B2_01	GPIO_EMC_B2_13	DCDC_GND	DCDC_GND	DCDC_DIG	DCDC_DIG	VDD_SOC_IN	VSS	GPIO_AD_22	GPIO_AD_20	GPIO_AD_21	VDDA_ADC_1P8	GPIO_AD_32	GPIO_AD_30
L	GPIO_EMC_B1_41	GPIO_EMC_B2_15	VSS	GPIO_EMC_B2_11	DCDC_IN_Q	DCDC_GND	DCDC_DIG_SENSE	DCDC_DIG	GPIO_SNVS_02	VSS	VSS	GPIO_AD_13	GPIO_AD_24	GPIO_AD_26	VSS	GPIO_AD_19	GPIO_AD_28
M	GPIO_EMC_B2_04	GPIO_EMC_B2_12	GPIO_EMC_B2_07	GPIO_EMC_B2_14	DCDC_IN	DCDC_ANA_SENSE	DCDC_ANA	DCDC_ANA	GPIO_SNVS_06	GPIO_SNVS_03	VDDA_1P8_IN	NVCC_GPIO	GPIO_AD_04	GPIO_AD_15	GPIO_AD_25	GPIO_AD_18	GPIO_AD_29
N	GPIO_EMC_B2_05	GPIO_EMC_B2_09	GPIO_EMC_B2_18	DCDC_MODE	DCDC_IN	GPIO_LPSR_00	GPIO_LPSR_04	GPIO_LPSR_05	GPIO_SNVS_08	GPIO_SNVS_04	VDDA_1P0	GPIO_AD_00	GPIO_AD_06	GPIO_AD_14	GPIO_AD_17	GPIO_AD_27	GPIO_AD_16
P	GPIO_EMC_B2_08	GPIO_EMC_B2_16	DCDC_PSWITCH	VSS	GPIO_LPSR_09	GPIO_LPSR_02	NVCC_LPSR	GPIO_LPSR_06	GPIO_SNVS_05	GPIO_SNVS_01	VDD_LPSR_DIG	VDD_LPSR_ANA	GPIO_AD_05	VSS	GPIO_AD_03	GPIO_AD_11	GPIO_AD_12
R	GPIO_EMC_B2_03	GPIO_EMC_B2_10	GPIO_EMC_B2_20	VSS	GPIO_LPSR_10	GPIO_LPSR_01	VSS	GPIO_LPSR_07	GPIO_SNVS_07	GPIO_SNVS_00	GPIO_SNVS_09	VDD_LPSR_IN	GPIO_AD_02	GPIO_AD_01	GPIO_AD_08	GPIO_AD_09	GPIO_AD_10
T	GPIO_EMC_B2_06	GPIO_EMC_B2_17	DCDC_LP	DCDC_LN	GPIO_LPSR_11	GPIO_LPSR_14	GPIO_LPSR_03	WAKEUP	PMIC_STBY_REQ	POR_B	TEST_MODE	VSS	RTC_XTALI	VDD_SNVS_DIG	CLK1_N	XTALO	GPIO_AD_07
U	VSS	GPIO_EMC_B2_19	DCDC_LP	DCDC_LN	GPIO_LPSR_12	GPIO_LPSR_13	GPIO_LPSR_15	GPIO_LPSR_08	PMIC_ON_REQ	ONOFF	NVCC_SNVS	VDD_SNVS_IN	RTC_XTALO	VDD_SNVS_ANA	CLK1_P	XTALI	VSS
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**

7 Revision history

Table 113 provides a revision history for this data sheet.

Table 113. i.MX RT1160 Data Sheet document revision history (continued)

Rev. Number	Date	Substantive Change(s)
Rev 3	06/2023	• From Section 5.2, Boot device interface allocation, removed the table describing UART12 as a boot interface. • In Table 58. FlexSPI output timing in SDR mode, updated the value of TDVO max to 4ns and TDHO min to 2ns. • Removed “Pad to IPP_IND” and “IPP_IND” specs from Table 39, AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank.
Rev 2.1	01/2023	• Updated the Figure 3. • Changed ‘Power’ to Current’ for DCDC_IN in Table 12, Maximum supply currents.
Rev 2	04.2022	• In Table 49, SEMC input timing in SYNC mode (SEMC_MCR.DQSMD = 0x1), changed the T_{IS} Min value from 2 to 0.6. • In Table 4. Special signal considerations, in the signal “RTC_XTALI/RTC_XTALO” changed the tolerance from ±10% to ±25%. • In Table 4. Special signal considerations, for the signal “RTX_XTALI/RTX_XTALO” changed VDD_SNVS_DIG to VDD_SNVS_ANA. • Updated the Figure 3, "i.MX RT1160 system block diagram". • Updated the Table 1. Order information.

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2021	• Updated the note in Section 1.1, Features • Updated the format of Table 1. Ordering information • Updated Figure 3, "i.MX RT1160 system block diagram" • Updated the SYS OSC and RTC OSC in Table 3. i.MX RT1160 modules list • Added Boot_mode/Boot CFG in Table 4. Special signal considerations • Updated the on-chip termination of JTAG_TDO in Table 5. JTAG controller interface summary • Added the USB VBUS supply in Table 11. Operating ranges • Updated the maximum current of DCDC_IN and VDD_MIPI_1P8 in Table 12. Maximum supply currents • Updated Figure 4, "Power sequence" • Updated the restrictions and first note in Section 4.2.1.1, Power-up sequence • Updated the descriptions about on-chip regulators, input voltages, and output voltages in Section 4.2.4, DCDC • Updated the comments of loading 1.8 V supply currents and footnote in Table 21. DCDC characteristics • Updated the clock output range in Table 26. Arm PLL's electrical parameters • Updated the descriptions about the RTC_XTALI in Section 4.2.6, On-chip oscillators • Updated the title and t_{start} descriptions in Table 27. 24 MHz system oscillator frequency specifications • Updated the title and t_{start} descriptions in Table 28. 32 kHz oscillator specifications • Updated the t_{start} descriptions in Table 29. RC oscillator with 16 MHz internal reference frequency • Updated the t_{start} descriptions in Table 30. RC oscillator with 48 MHz internal reference frequency • Updated the t_{start} descriptions and unit of J_{PP-CC} in Table 31. RC oscillator with 400 MHz internal reference frequency • Updated Table 35. DC specification for GPIO_SNVS bank • Removed the INPSL values in Table 38. Dynamic input characteristics for GPIO_EMC_B1/GPIO_EMC_B2/GPIO_SD_B1/GPIO_SD_B2/GPIO_DISP_B1 bank • Added the maximum frequency in Table 39. AC specifications for GPIO_AD/GPIO_LPSR/GPIO_DISP_B2 bank • Changed the WDOGn_B to WDOG_B in Section 4.4.2, WDOG reset timing parameters • Changed the VDD_ANA_18 to VDDA_ADC_1P8 in Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8 and VADINmax ≤ VREFH); removed the values of V_{REFH},TUE, FSE, and ZSE from Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8 and VADINmax ≤ VREFH); added gain error, offset error, and footnote in Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8 and VADINmax ≤ VREFH); updated INL, DNL, ENOB, and footnote in Table 73. ADC electrical specifications (VREFH = VDDA_ADC_1P8 and VADINmax ≤ VREFH) • Removed the values of V_{REFH}, TUE, FSE, and ZSE from Table 74. ADC electrical specifications (VREFH = 1.68 V and VADINmax ≤ NVCC_GPIOmax); updated the typical value of C_{ADIN}, INL, DNL, min values of ENOB, and footnote in Table 74. ADC electrical specifications (VREFH = 1.68 V and VADINmax ≤ NVCC_GPIOmax); added gain error, offset error, and footnote in Table 74. ADC electrical specifications (VREFH = 1.68 V and VADINmax ≤ NVCC_GPIOmax)

Revision history

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2021	• Updated the table title and footnote of Table 75. ADC electrical specifications (1 V ≤ VREFH < 1.71 V and VADINmax ≤ VREFH); removed the values of V_{REFH},TUE, FSE, ZSE, and a footnote from Table 75. ADC electrical specifications (1 V ≤ VREFH < 1.71 V and VADINmax ≤ VREFH); added gain error, offset error, and footnote in Table 75. ADC electrical specifications (1 V ≤ VREFH < 1.71 V and VADINmax ≤ VREFH); updated the min values of ENOB, INL and ENL in Table 75. ADC electrical specifications (1 V ≤ VREFH < 1.71 V and VADINmax ≤ VREFH) • Updated Figure 34. ADC input impedance equivalent circuit diagram and added equations in Section 4.8.1.1, 12-bit ADC input impedance equivalent circuit diagram
Rev. 0	04/2021	• Initial version

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