



**THE DATASHEET OF
PESD5V0U1BLD,315**





PESD5V0U1BLD

Ultra low capacitance bidirectional ESD protection diode

1 April 2023

Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

2. Features and benefits

- Bidirectional ESD protection of one line
- Ultra small SMD plastic package
- Solderable side pads
- Package height typ. 0.37 mm
- Ultra low diode capacitance $C_d = 2.9$ pF
- ESD protection up to 10 kV
- IEC 61000-4-2; level 4 (ESD)
- Ultra low leakage current: $I_{RM} = 5$ nA

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- High-speed data lines
- Communication systems
- Portable electronics

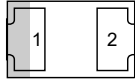
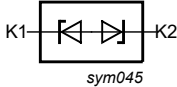
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	5	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	2.9	3.5	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view</p> <p>DFN1006D-2 (SOD882D)</p>	 <p>sym045</p>
2	K2	cathode (diode 2)		

6. Ordering information

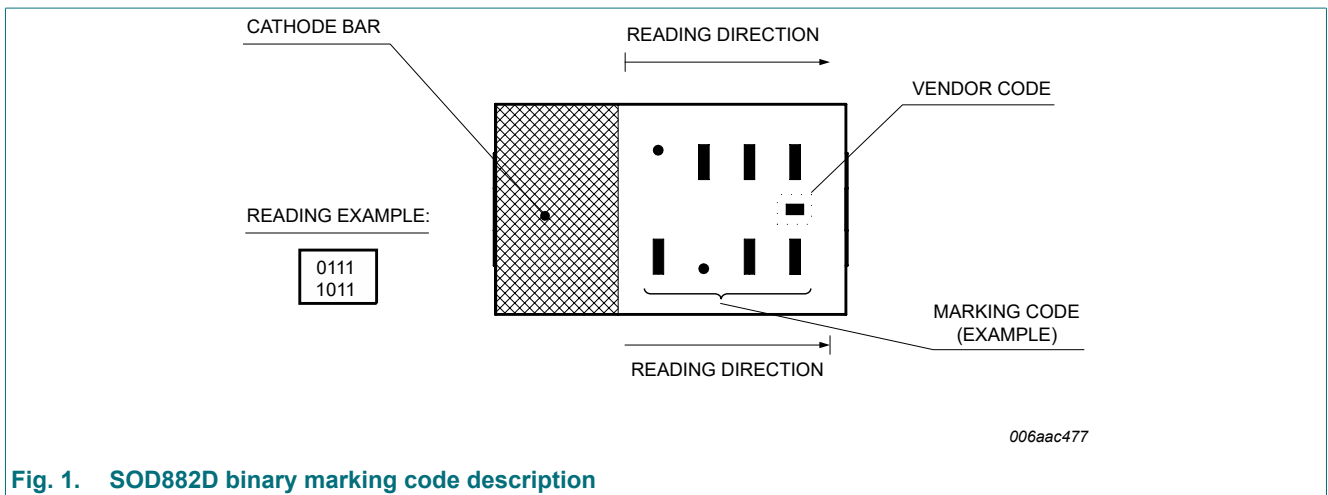
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U1BLD	DFN1006D-2	leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.4 mm body	SOD882D

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0U1BLD	0001 0000



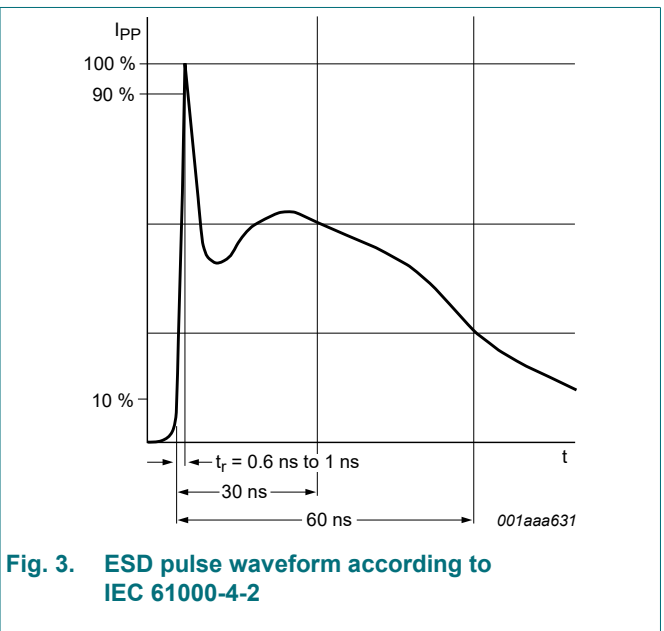
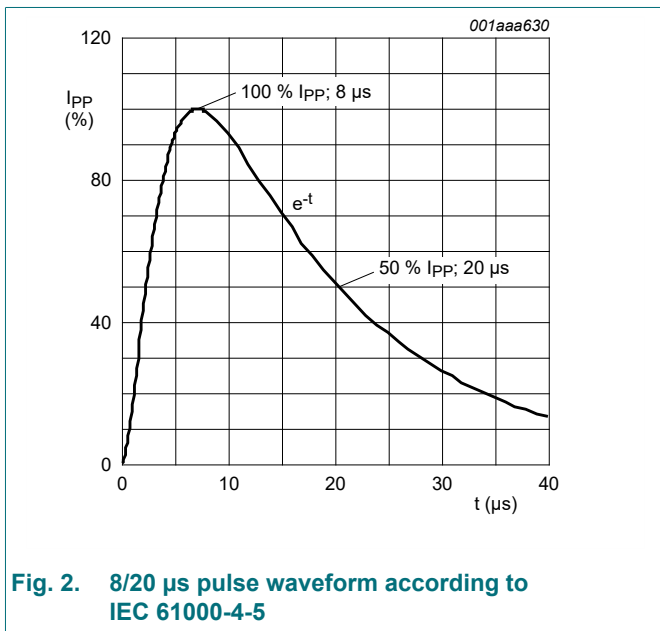
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge), $T_{amb} = 25\text{ °C}$	[1] [2]	-	10	kV
		IEC 61000-4-2 (air discharge), $T_{amb} = 25\text{ °C}$		-	15	kV
		machine model, $T_{amb} = 25\text{ °C}$		-	400	V
		MIL-STD-883 (human body model), $T_{amb} = 25\text{ °C}$		-	10	kV

- [1] Device stressed with ten non-repetitive ESD pulses.
- [2] Measured from pin 1 to pin 2.

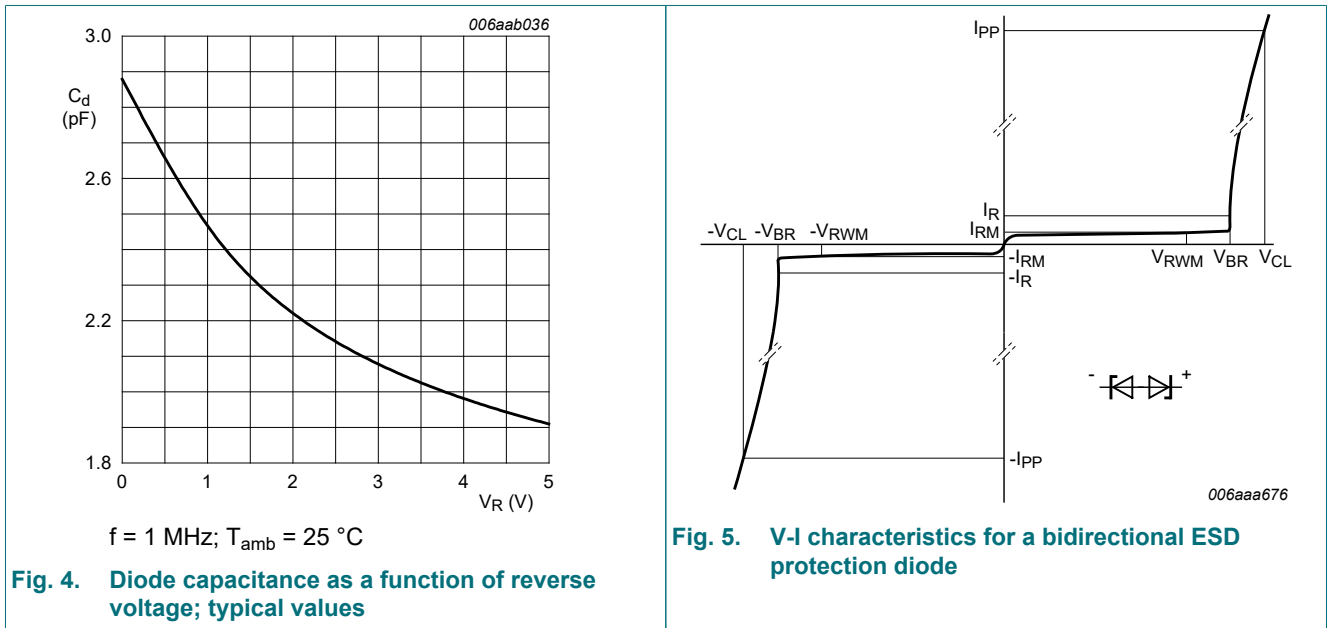


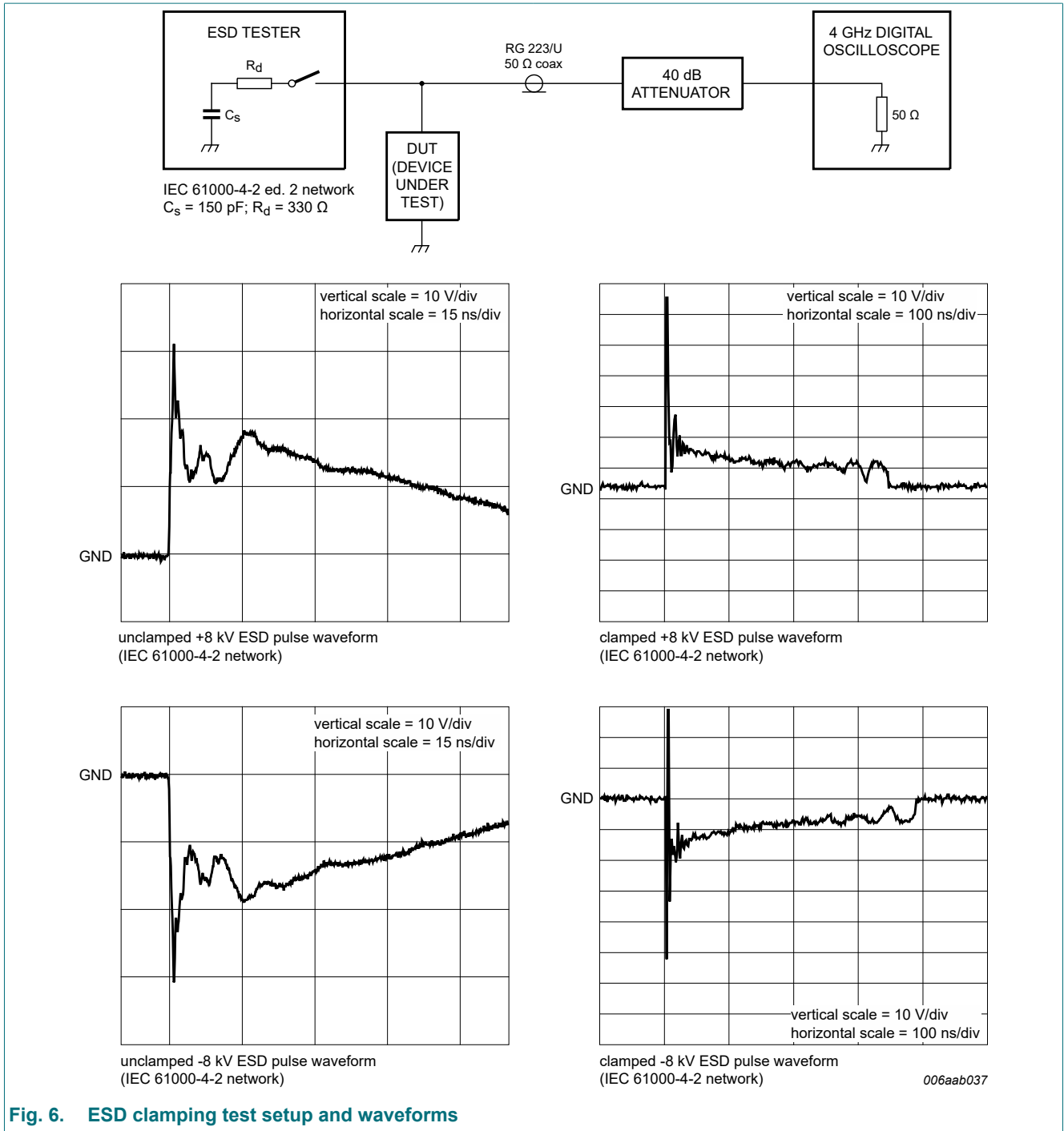
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	5.5	7	9.5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	5	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2.9	3.5	pF
R_{dyn}	dynamic resistance	$I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	0.8	-	Ω

[1] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANSI / ESD STM5.5.1-2008.





10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

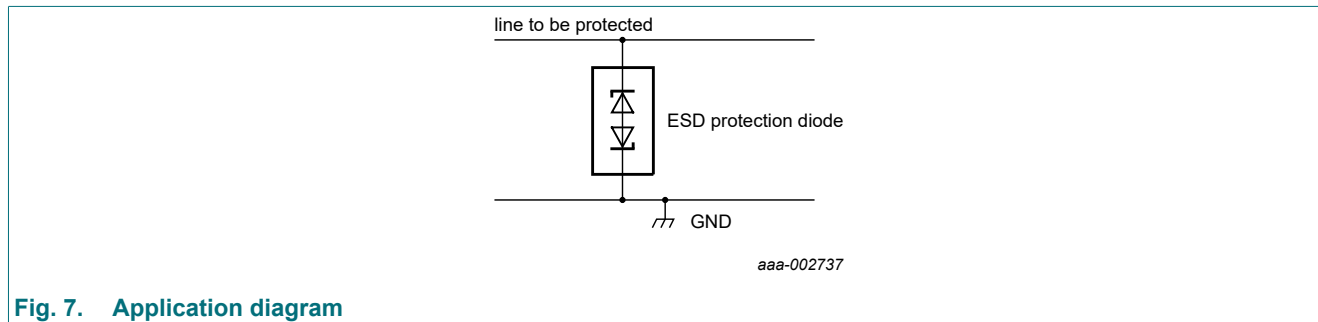


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

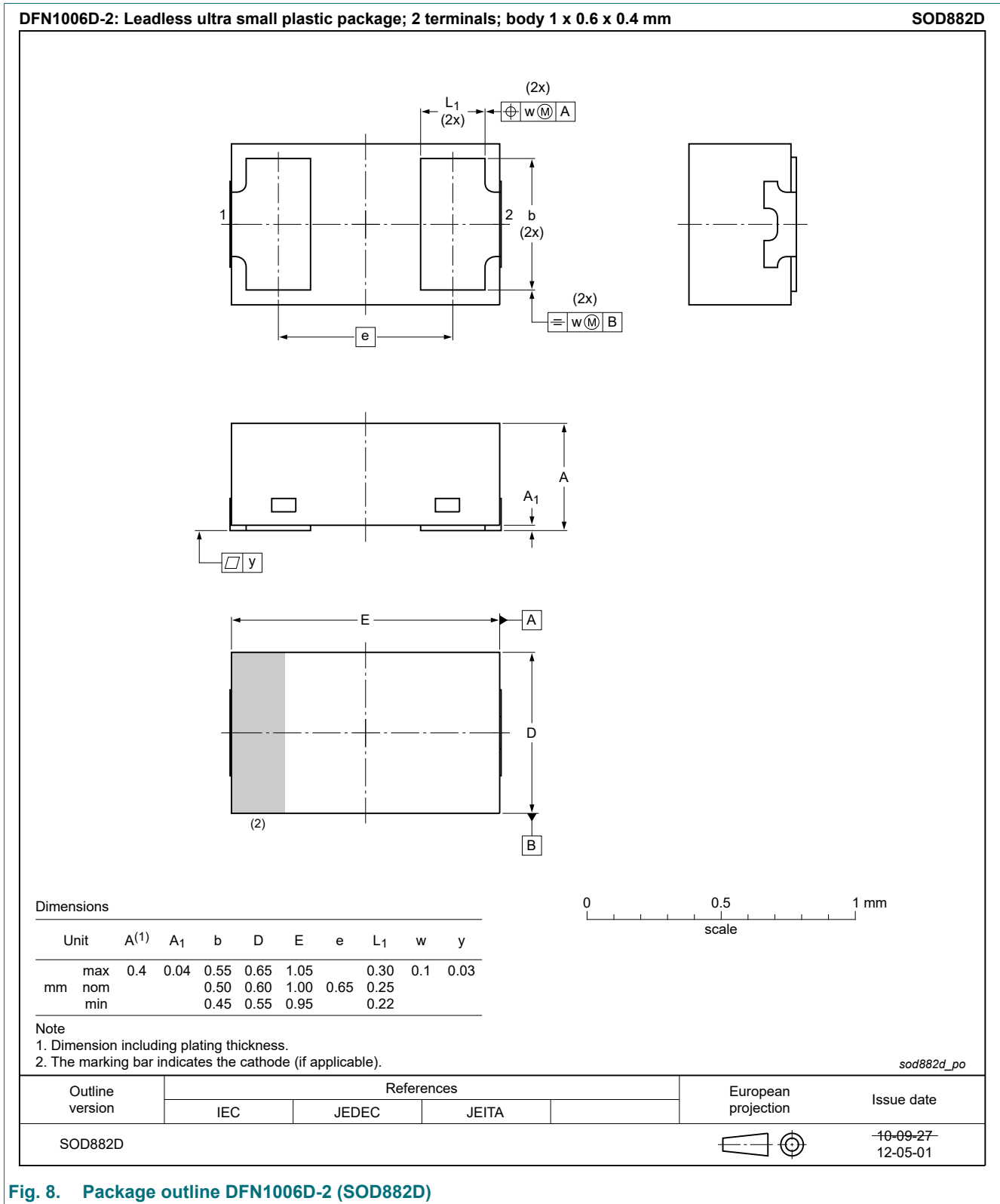


Fig. 8. Package outline DFN1006D-2 (SOD882D)

12. Soldering

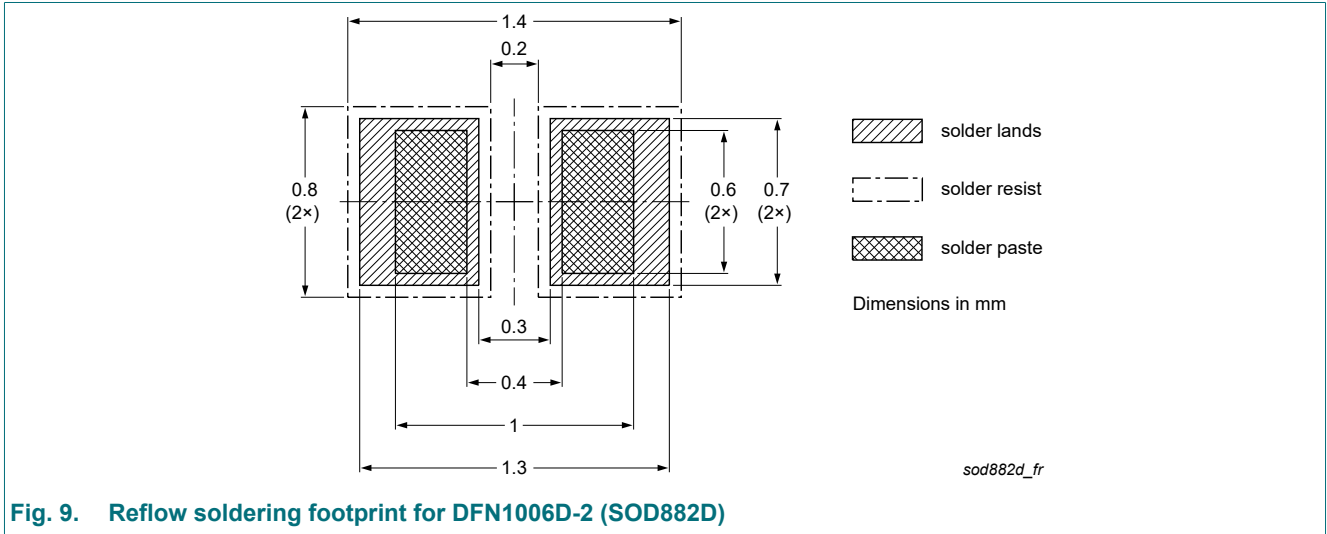


Fig. 9. Reflow soldering footprint for DFN1006D-2 (SOD882D)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U1BLD v.3	20230401	Product data sheet	-	PESD5V0U1BLD v.2
Modifications:	<ul style="list-style-type: none">Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).			
PESD5V0U1BLD v.2	20110727	Product data sheet	-	PESD5V0U1BLD v.1
PESD5V0U1BLD v.1	20110504	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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