



**THE DATASHEET OF
DMS3012SFG-13**



30V N-CHANNEL ENHANCEMENT MODE MOSFET WITH SCHOTTKY DIODE
PowerDI3333-8

Product Summary

BV _{DSS}	R _{DS(ON)}	Package	I _{D MAX} T _A = +25°C
30V	10mΩ @ V _{GS} = 10V	PowerDI® 3333-8	12A
	15mΩ @ V _{GS} = 4.5V		9.5A

Description

This MOSFET is designed to minimize on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

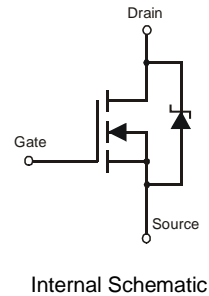
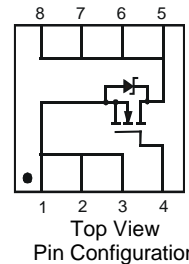
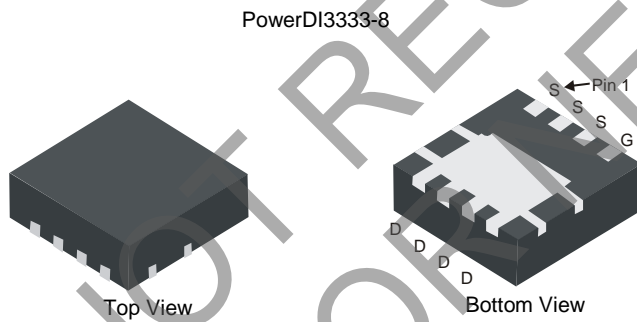
- Backlighting
- Power Management Functions
- DC-DC Converters

Features

- DIOFET Utilizes a Unique Patented Process to Monolithically Integrate a MOSFET and a Schottky in a Single Die to Deliver:
 - Low R_{DS(ON)} – Minimize Conduction Losses
 - Low V_{SD} – Reducing The Losses Due to Body Diode Conduction
 - Low Q_{rr} – Lower Q_{rr} of the Integrated Schottky Reduces Body Diode Switching Losses
 - Low Gate Capacitance (Q_g/Q_{GS}) Ratio – Reduces Risk of Shoot Through or Cross Conduction Currents at High Frequencies
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- Occupies just 33% of the Board Area Occupied by SO-8, Enabling Smaller End Product
- 100% UIS (Avalanche) Rated
- 100% R_g Tested
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: PowerDI3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 Ⓢ
- Weight: 0.072 grams (Approximate)

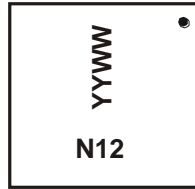


Ordering Information (Note 4)

Part Number	Case	Packaging
DMS3012SFG-7	PowerDI3333-8	2000/Tape & Reel
DMS3012SFG-13	PowerDI3333-8	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



N12 = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 18 = 2018)
 WW = Week Code (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	I _D	12 9.5	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	16.0 12.7	A
Continuous Drain Current (Note 6) V _{GS} = 4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	9.5 7.5	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	13.0 10.3	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	90	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	3.5	A
Avalanche Current (Note 7) L = 0.1mH			I _{AS}	17	A
Avalanche Energy (Note 7) L = 0.1mH			E _{AS}	43	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T _A = +25°C	P _D	0.89	W
	T _A = +70°C		0.55	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{θJA}	145	°C/W
	t < 10s		74	
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	2.2	W
	T _A = +70°C		1.3	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	58	°C/W
	t < 10s		31	
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	11	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 7. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.

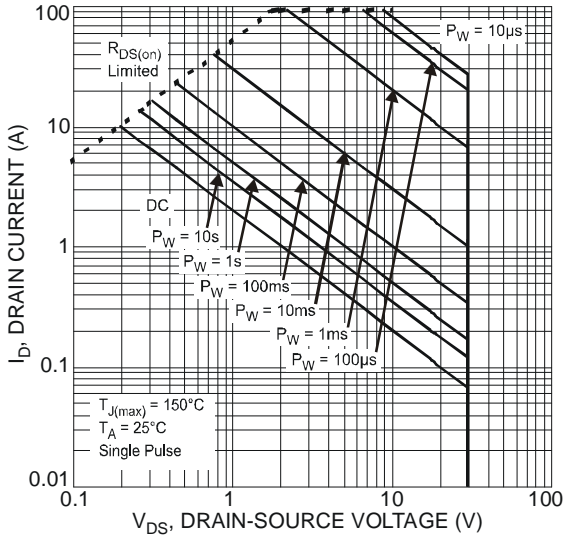


Fig. 1 SOA, Safe Operation Area

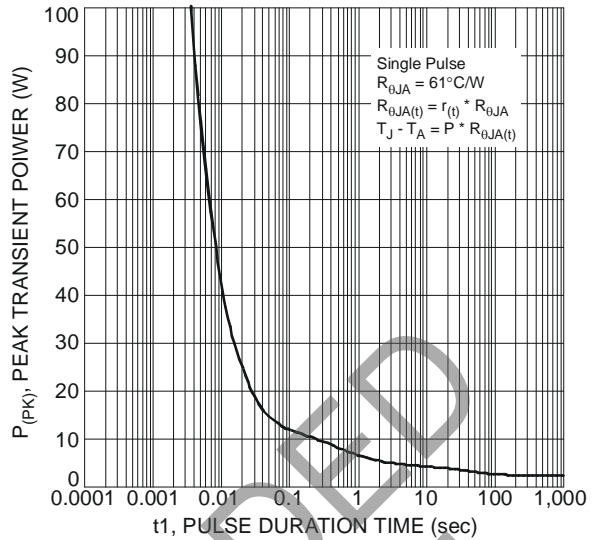


Fig. 2 Single Pulse Maximum Power Dissipation

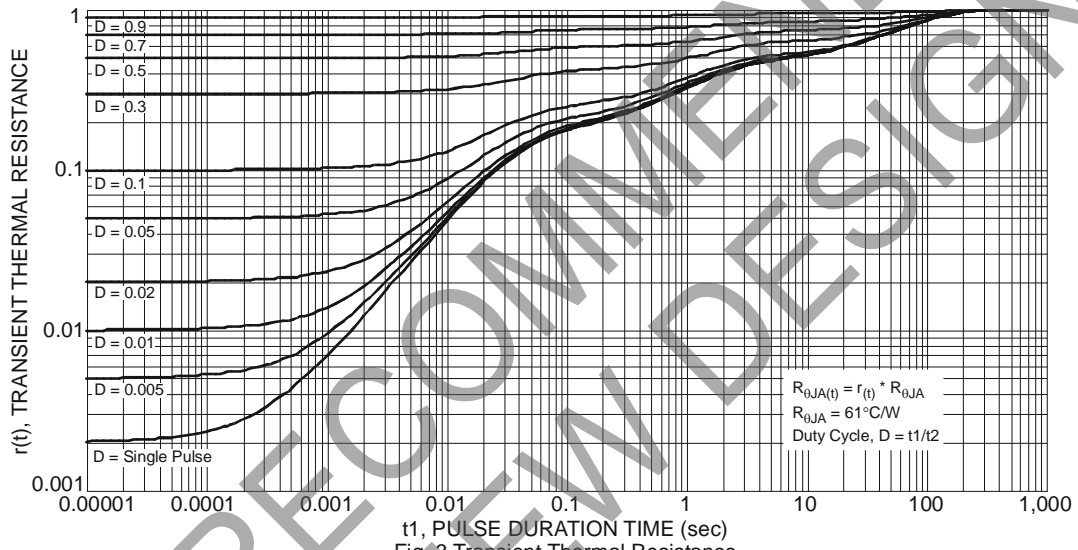


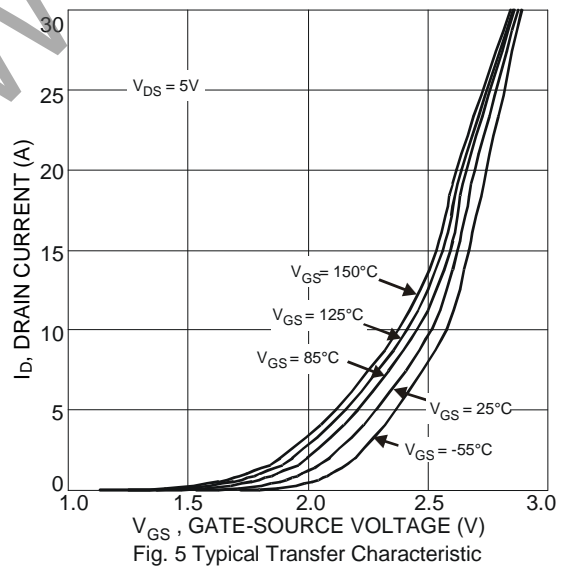
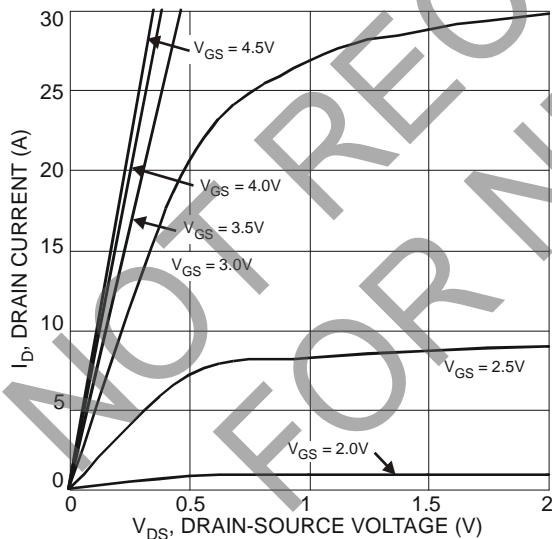
Fig. 3 Transient Thermal Resistance

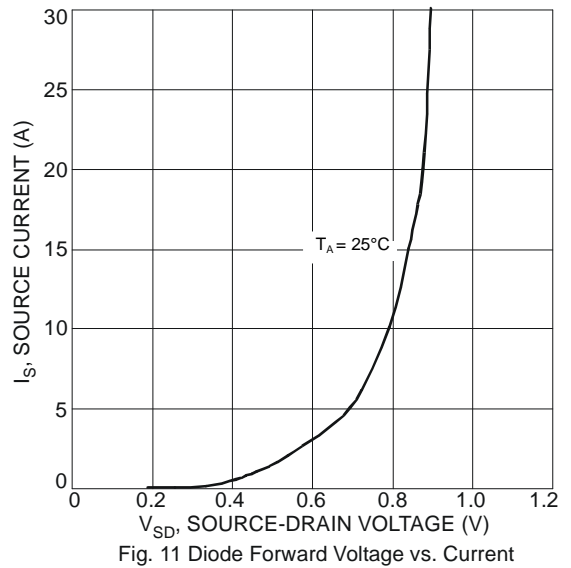
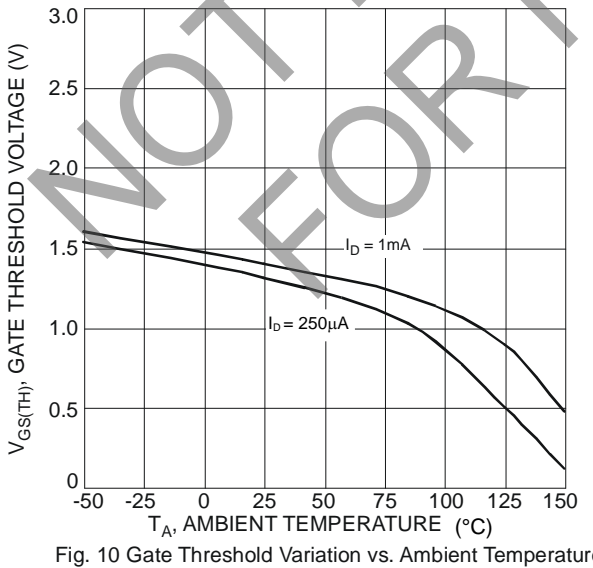
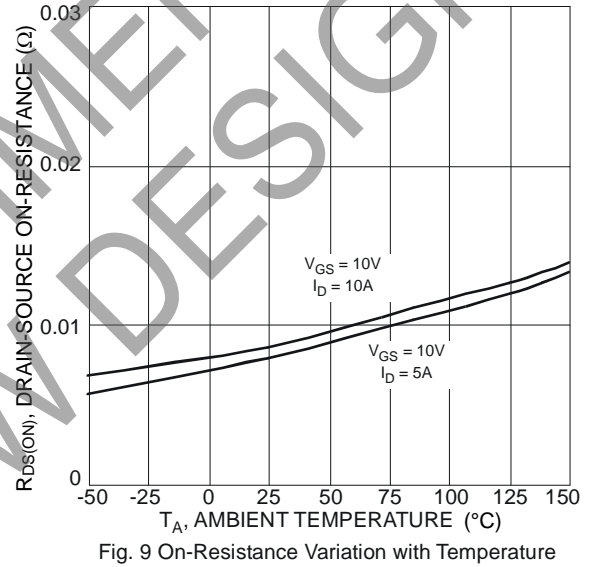
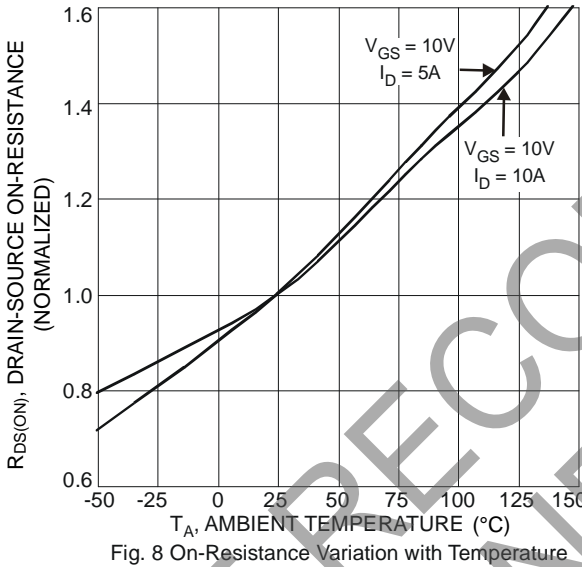
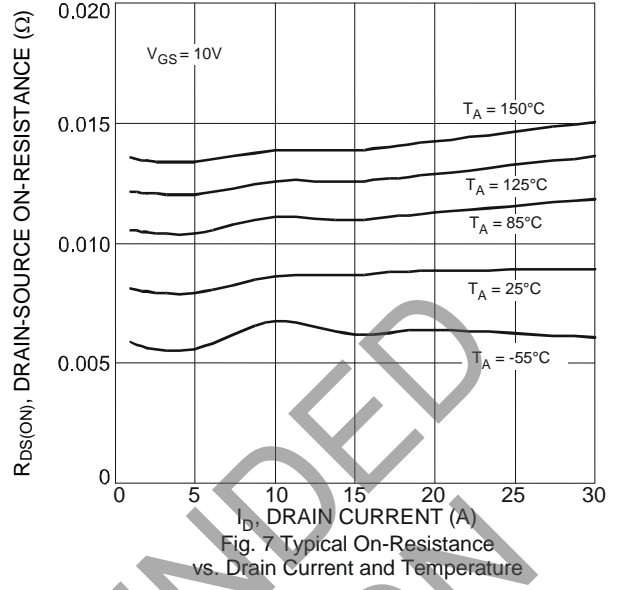
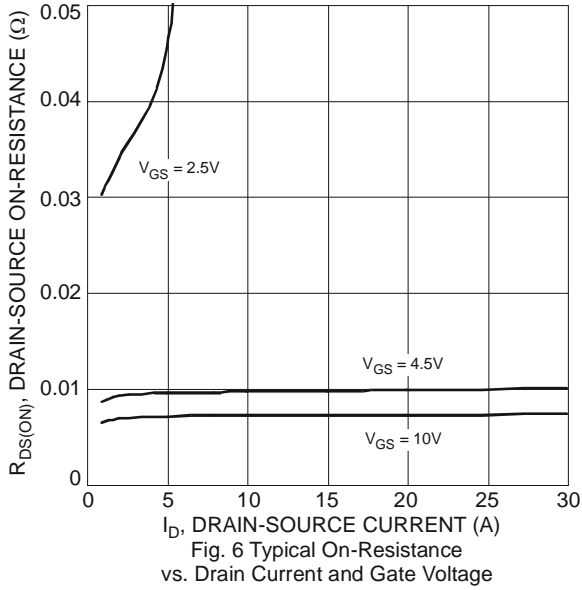
NOT RECOMMENDED FOR NEW DESIGN

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	100	μA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	1.0	1.5	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	7.3	10	mΩ	V _{GS} = 10V, I _D = 13.5A
		—	10	15		V _{GS} = 4.5V, I _D = 11A
Forward Transfer Admittance	Y _{fs}	—	30	—	S	V _{DS} = 5V, I _D = 10.0A
Diode Forward Voltage	V _{SD}	—	0.45	0.55	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}	—	1296	4310	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	415	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	204	—	pF	
Gate Resistance	R _g	0.26	1.6	2.6	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge V _{GS} = 4.5V	Q _g	—	14.7	—	nC	V _{DS} = 15V, V _{GS} = 10V, I _D = 13.5A
Total Gate Charge V _{GS} = 10V	Q _g	—	31.6	—	nC	
Gate-Source Charge	Q _{gs}	—	3.5	—	nC	
Gate-Drain Charge	Q _{gd}	—	5.0	—	nC	
Turn-On Delay Time	t _{D(on)}	—	15.8	—	ns	
Turn-On Rise Time	t _r	—	27.8	—	ns	V _{GS} = 10V, V _{DS} = 15V, R _g = 3Ω, I _D = 8.8A
Turn-Off Delay Time	t _{D(off)}	—	29.7	—	ns	
Turn-Off Fall Time	t _f	—	13.6	—	ns	I _F = 13.5A, di/dt = 100A/μs
Reverse Recovery Time	t _{rr}	—	13.1	—	ns	
Reverse Recovery Charge	Q _{rr}	—	4.3	—	nC	I _F = 13.5A, di/dt = 100A/μs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.





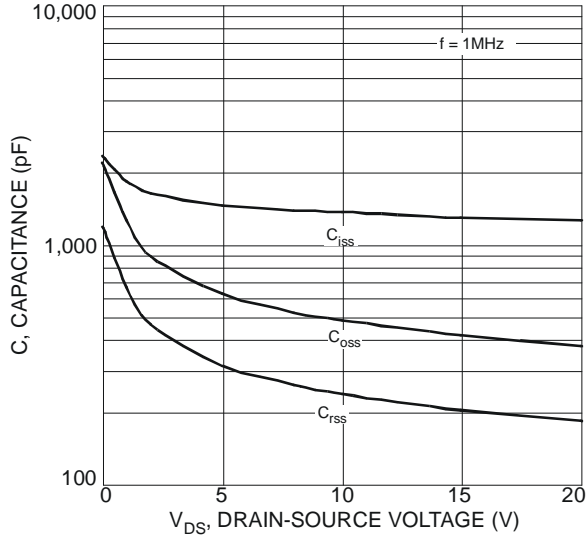


Fig. 12 Typical Total Capacitance

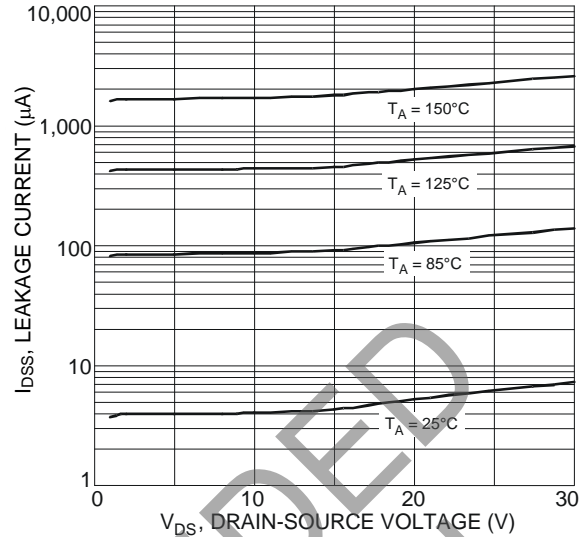


Fig. 13 Typical Leakage Current vs. Drain-Source Voltage

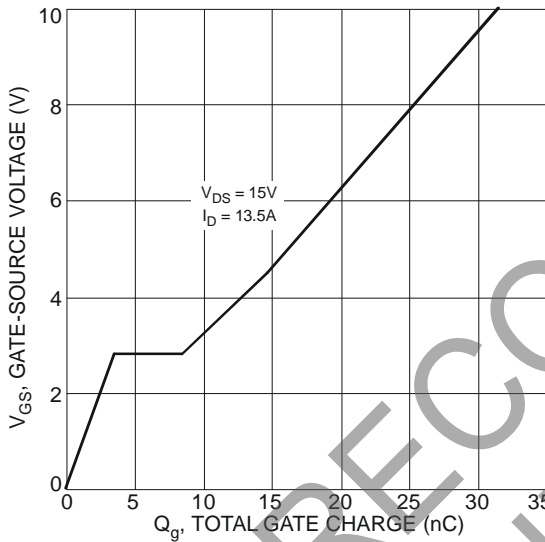


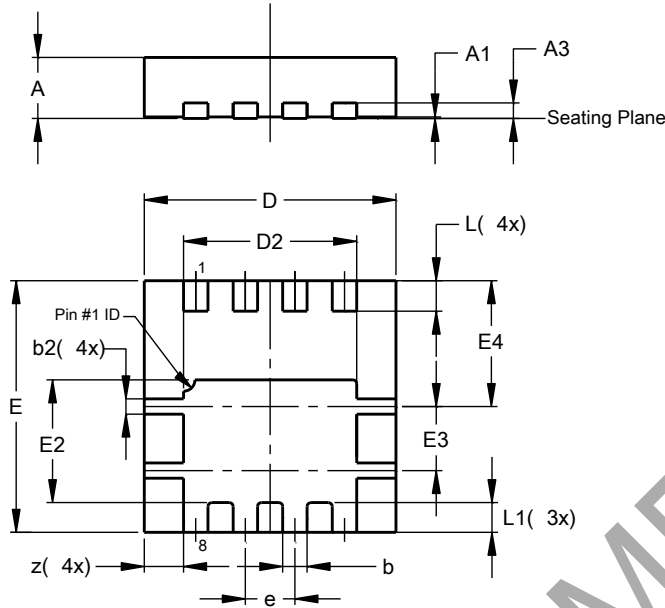
Fig. 14 Gate-Source Voltage vs. Total Gate Charge

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Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI3333-8

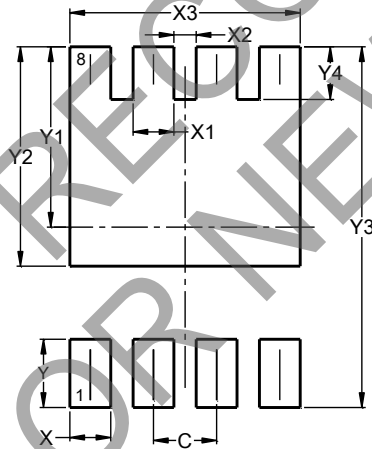


PowerDI3333-8			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.27	0.37	0.32
b2	0.15	0.25	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
E4	1.60	1.70	1.65
e	-	-	0.65
L	0.35	0.45	0.40
L1	-	-	0.39
z	-	-	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI3333-8



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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