THE DATASHEET OF

DMS3019SSD-13

ASYMMETRIC DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

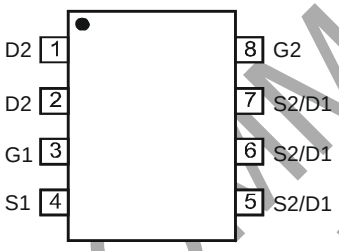
Features

- DIOFET Utilizes a Unique Patented Process to Monolithically Integrate a MOSFET and a Schottky in a Single Die To Deliver:
  - Low $R_{DS(on)}$—Minimizes Conduction Loss
  - Low V_{SD}—Reduces Losses Due to Body Diode Construction
  - Low Q_{rr}—Lower Q_{rr} of Integrated Schottky Reduces Body Diode Switching Losses
  - Low Gate Capacitance (Q_g/Q_{gs}) Ratio—Reduces Risk of Shoot-Through or Cross Conduction Currents at High Frequencies
  - Avalanche Rugged—I_{AR} and E_{AR} Rated
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

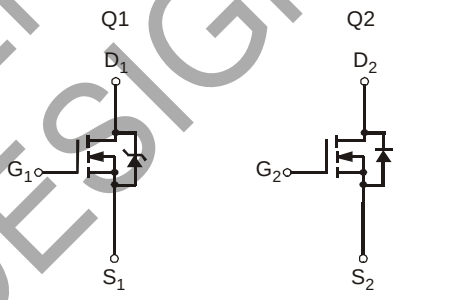
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.072 grams (Approximate)

Top View



Top View
Internal Schematic



N-Channel MOSFET + Integrated Schottky Diode

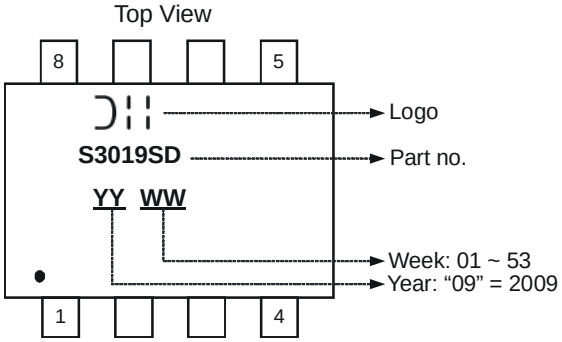
N-Channel MOSFET

Ordering Information (Note 3)

Part Number	Case	Packaging
DMS3019SSD-13	SO-8	2500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds
4. For packaging details, go to our website at http://www.diodes.com/.

Marking Information



Maximum Ratings – Q1 @TA = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±12	V
Continuous Drain Current (Note 4) V_{GS} = 10V	Steady State	T_A = 25°C T_A = 70°C	I_D	7.0 5.6	A
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = 25°C T_A = 70°C	I_D	9.0 7.0	A
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = 25°C T_A = 70°C	I_D	8.0 6.5	A
Pulsed Drain Current (Note 6)			I_{DM}	40	A
Avalanche Current (Notes 6 & 7)			I_{AR}	13	A
Repetitive Avalanche Energy (Notes 6 & 7) L = 0.3mH			E_{AR}	25.4	mJ

Maximum Ratings – Q2 @TA = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 4) V_{GS} = 10V	Steady State	T_A = 25°C T_A = 70°C	I_D	5.7 4.6	A
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T_A = 25°C T_A = 70°C	I_D	7.0 5.6	A
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = 25°C T_A = 70°C	I_D	6.0 4.7	A
Pulsed Drain Current (Note 6)			I_D	40	A
Avalanche Current (Notes 6 & 7)			I_{AR}	16	A
Repetitive Avalanche Energy (Notes 6 & 7) L = 0.1mH			E_{AR}	12.8	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_D	1.19	W
Thermal Resistance, Junction to Ambient @T_A = 25°C (Note 4)	$R_{\theta JA}$	107	°C/W
Power Dissipation (Note 5)	P_D	1.79	W
Thermal Resistance, Junction to Ambient @T_A = 25°C (Note 5)	$R_{\theta JA}$	70	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes:
4. Device mounted on FR-4 substrate PCB, with minimum recommended pad layout. The value in any given application depends on the user's specific board design. Device contains two active die running at equal power.
5. Device mounted on 1 inch × 1 inch FR4 PCB with high coverage of single sided 1oz copper, in still air conditions. Device contains two active die running at equal power.
6. Repetitive rating, pulse width limited by junction temperature.
7. I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep T_J = 25°C

Electrical Characteristics – Q1 @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 1mA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.1	mA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.4	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	10 12	15 18	mΩ	V_{GS} = 10V, I_D = 9A V_{GS} = 4.5V, I_D = 7A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	5	—	S	V_{DS} = 5V, I_D = 9A
Diode Forward Voltage	V_{SD}	—	0.4	1	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1932	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	154	—		
Reverse Transfer Capacitance	C_{rss}	—	121	—		
Gate Resistance	R_g	—	2.7	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	18.1	—	nC	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 9A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	42.0	—		V_{DS} = 15V, V_{GS} = 10V, I_D = 9A
Gate-Source Charge	Q_{gs}	—	4.5	—		
Gate-Drain Charge	Q_{gd}	—	4.0	—		
Turn-On Delay Time	$t_{D(on)}$	—	6.16	—	ns	V_{GS} = 10V, V_{DS} = 15V, R_G = 3Ω, R_L = 1.7Ω
Turn-On Rise Time	t_r	—	7.22	—		
Turn-Off Delay Time	$t_{D(off)}$	—	36.76	—		
Turn-Off Fall Time	t_f	—	5.38	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

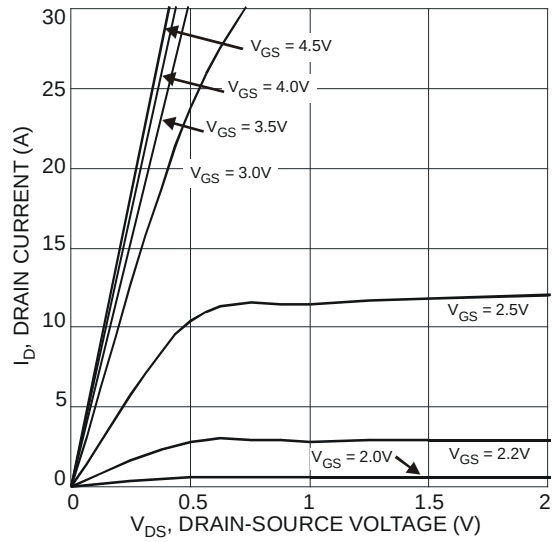


Fig. 1 Typical Output Characteristic

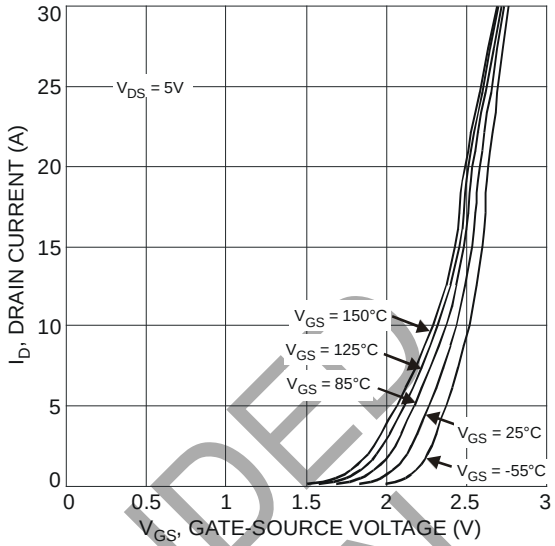


Fig. 2 Typical Transfer Characteristic

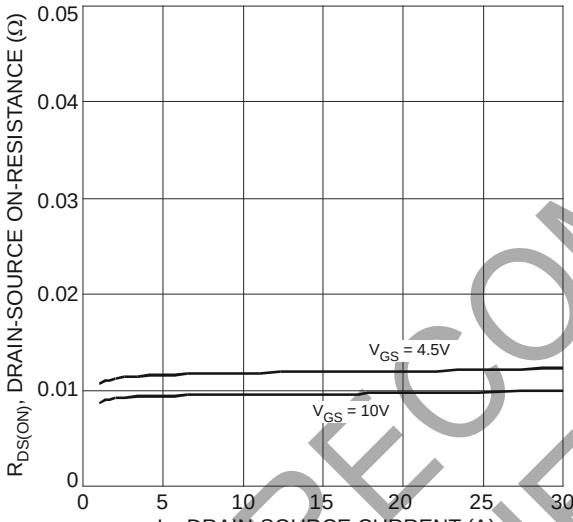


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

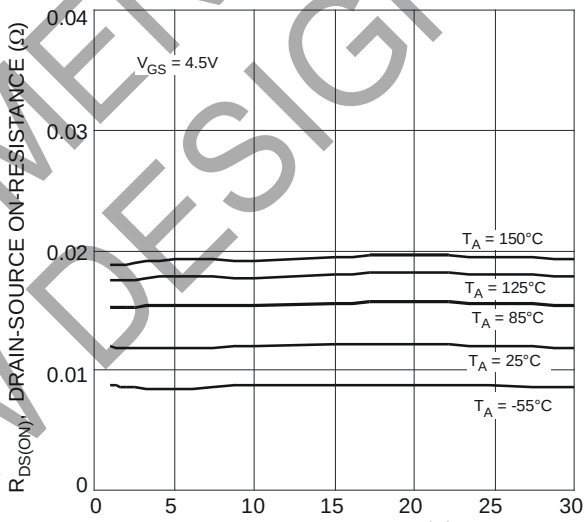


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

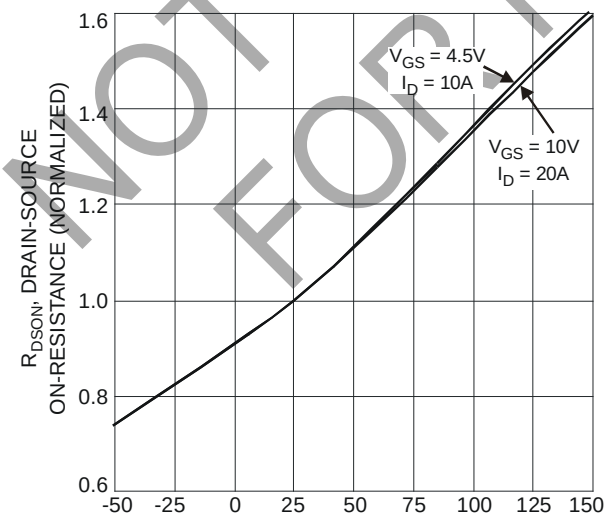


Fig. 5 On-Resistance Variation with Temperature

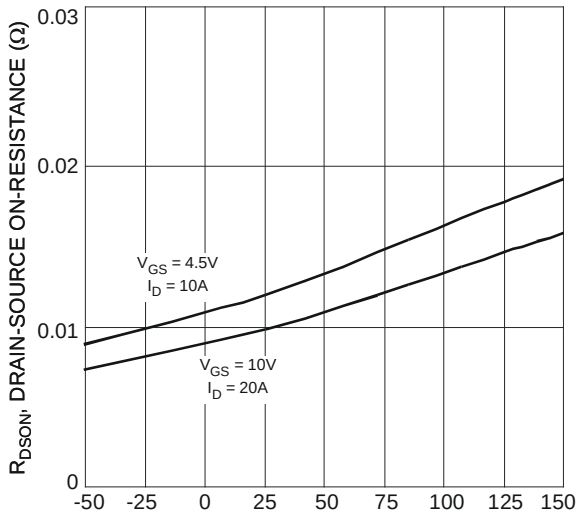


Fig. 6 On-Resistance Variation with Temperature

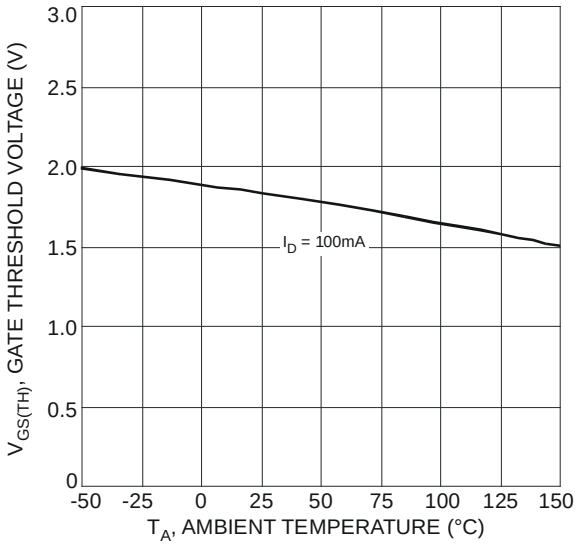


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

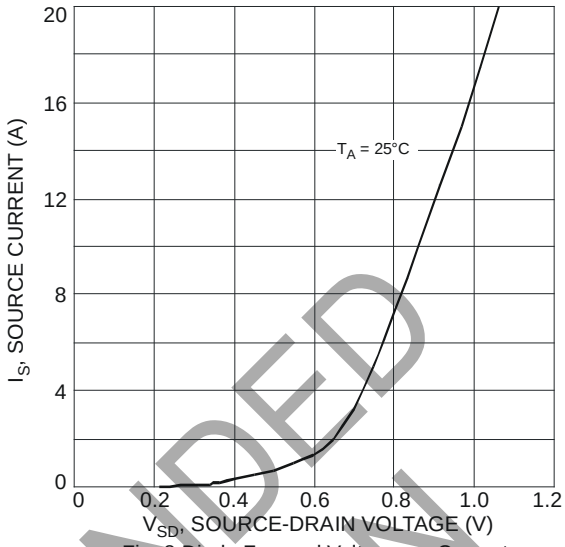


Fig. 8 Diode Forward Voltage vs. Current

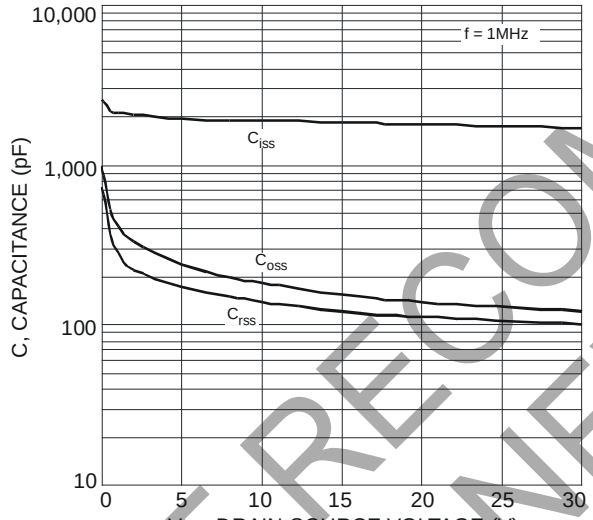


Fig. 9 Typical Total Capacitance

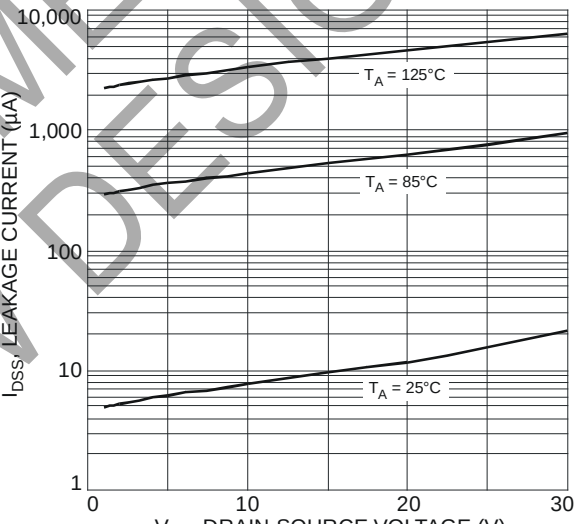


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

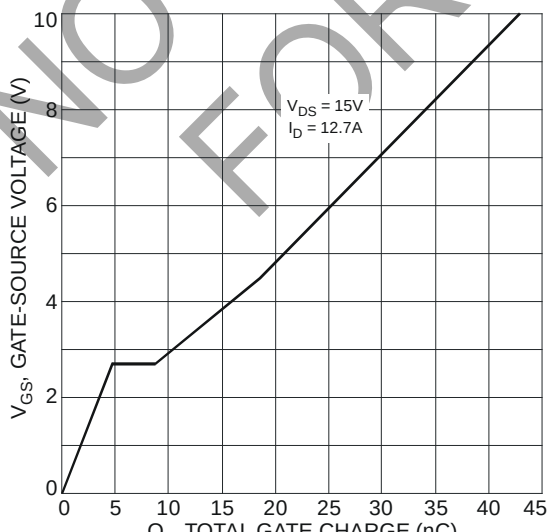


Fig. 11 Gate-Charge Characteristics

Electrical Characteristics – Q2 @ T_A = 25°C unless otherwise stated

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.4	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	15 25	23 33	mΩ	V_{GS} = 10V, I_D = 10A V_{GS} = 4.5V, I_D = 7.5A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	2.5	—	S	V_{DS} = 5V, I_D = 10A
Diode Forward Voltage	V_{SD}	—	0.65	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	478.9	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	96.7	—		
Reverse Transfer Capacitance	C_{rss}	—	61.4	—		
Gate Resistance	R_g	0.4	1.1	1.6	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	5.0	—	nC	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 10A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	10.5	—		V_{DS} = 15V, V_{GS} = 10V, I_D = 10A
Gate-Source Charge	Q_{gs}	—	1.8	—		
Gate-Drain Charge	Q_{gd}	—	1.6	—		
Turn-On Delay Time	$t_{D(on)}$	—	2.9	—	ns	V_{GS} = 10V, V_{DS} = 15V, R_G = 3Ω, R_L = 1.5Ω
Turn-On Rise Time	t_r	—	7.9	—		
Turn-Off Delay Time	$t_{D(off)}$	—	14.6	—		
Turn-Off Fall Time	t_f	—	3.1	—		

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

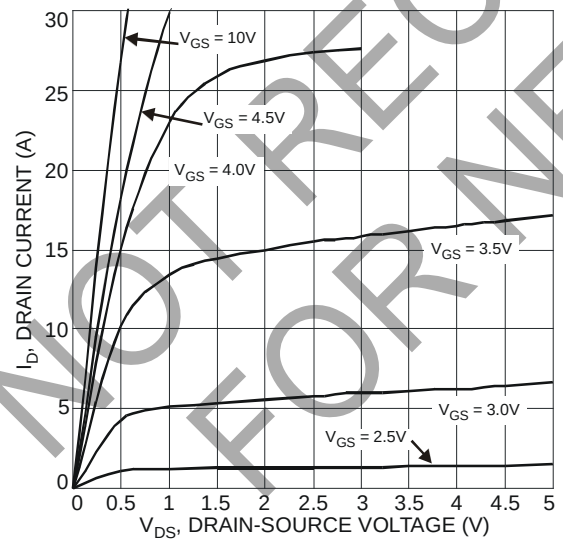


Fig. 12 Typical Output Characteristic

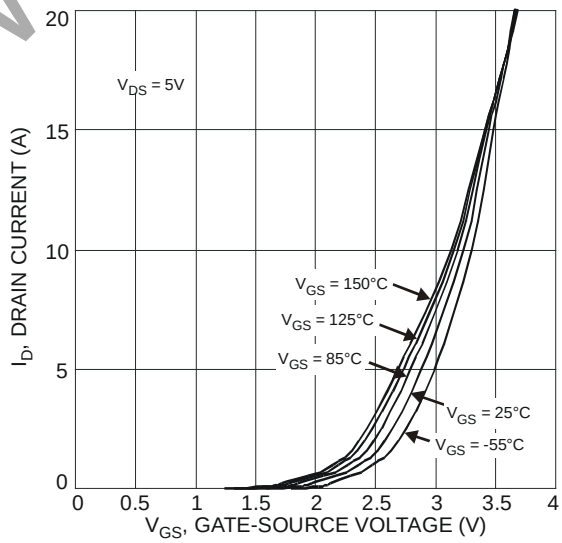


Fig. 13 Typical Transfer Characteristic

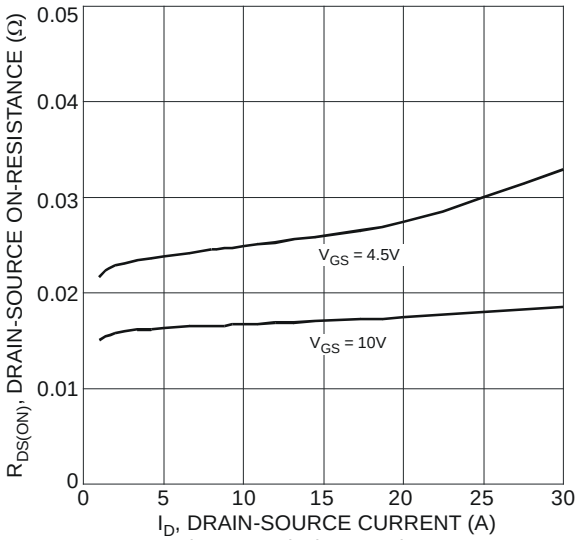


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

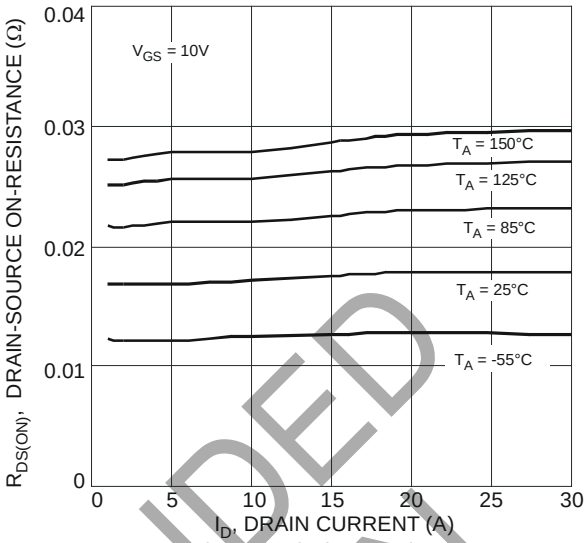


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

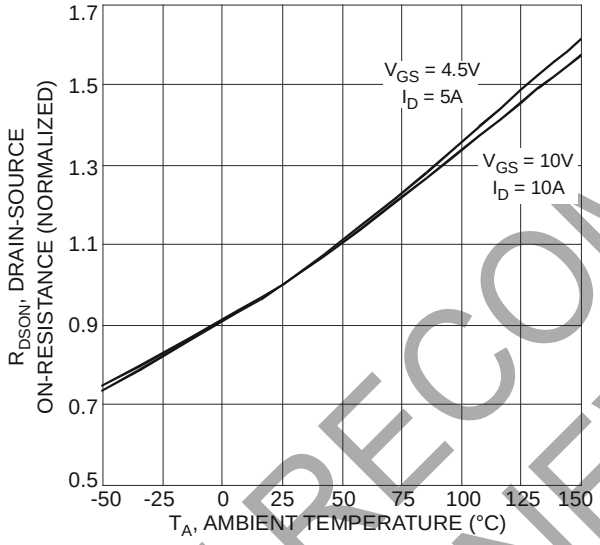


Fig. 16 On-Resistance Variation with Temperature

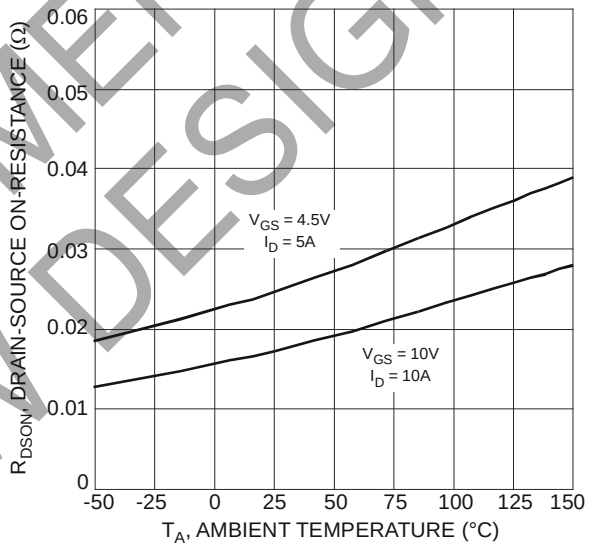


Fig. 17 On-Resistance Variation with Temperature

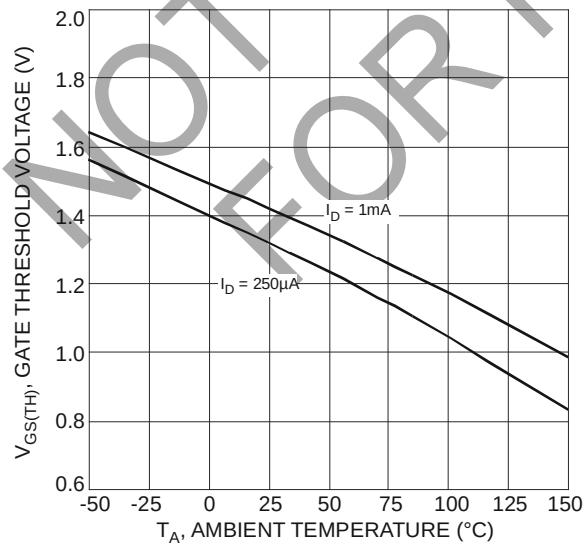


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

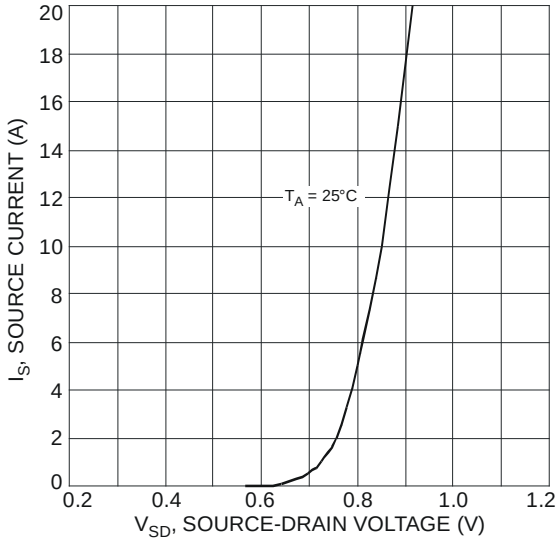


Fig. 19 Diode Forward Voltage vs. Current

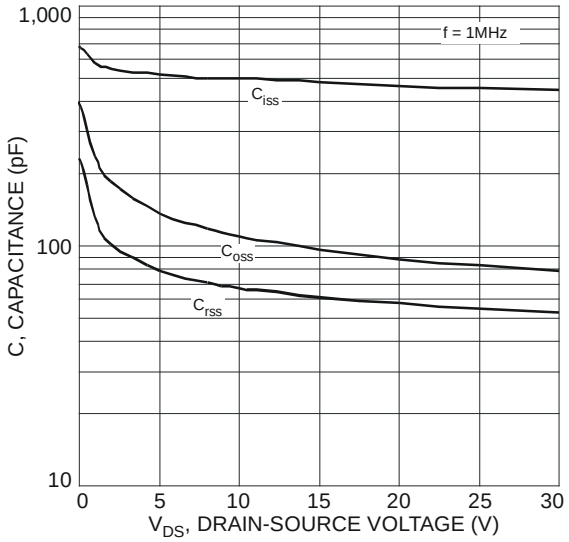


Fig. 20 Typical Total Capacitance

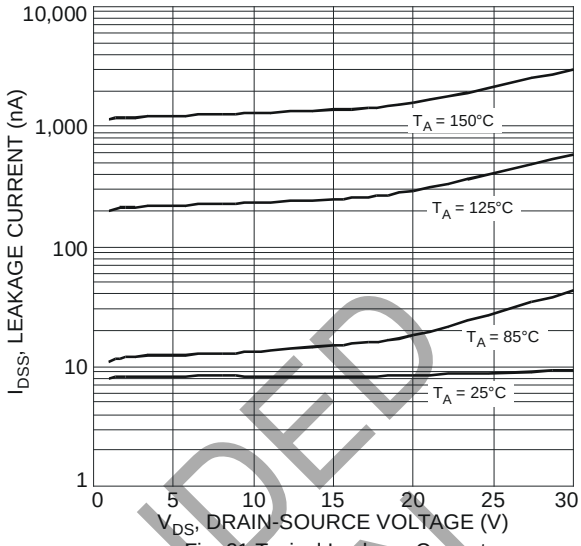


Fig. 21 Typical Leakage Current vs. Drain-Source Voltage

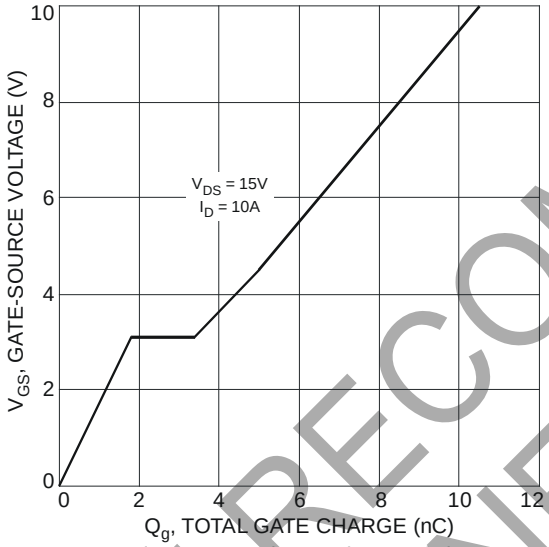


Fig. 22 Gate-Charge Characteristics

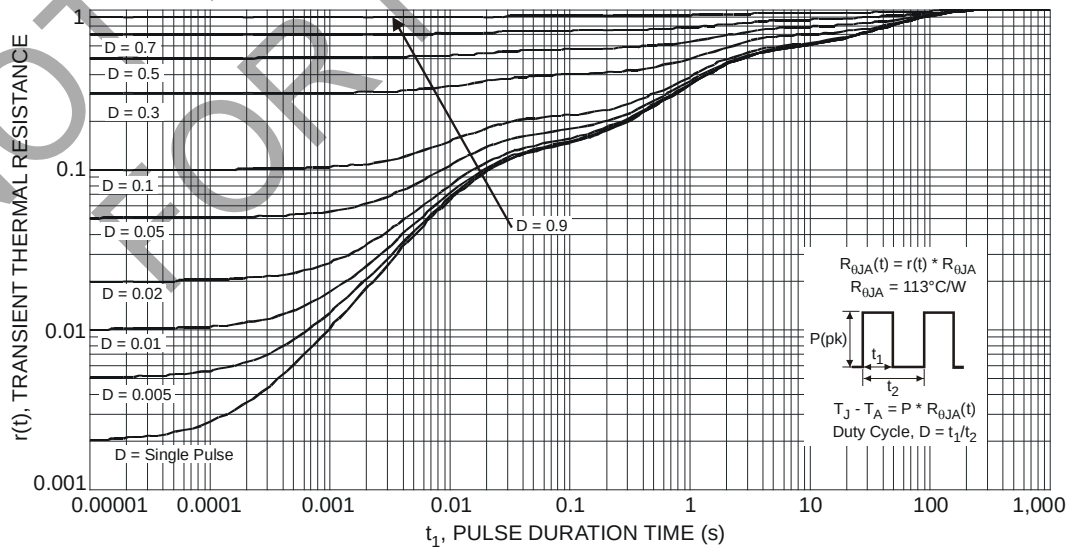
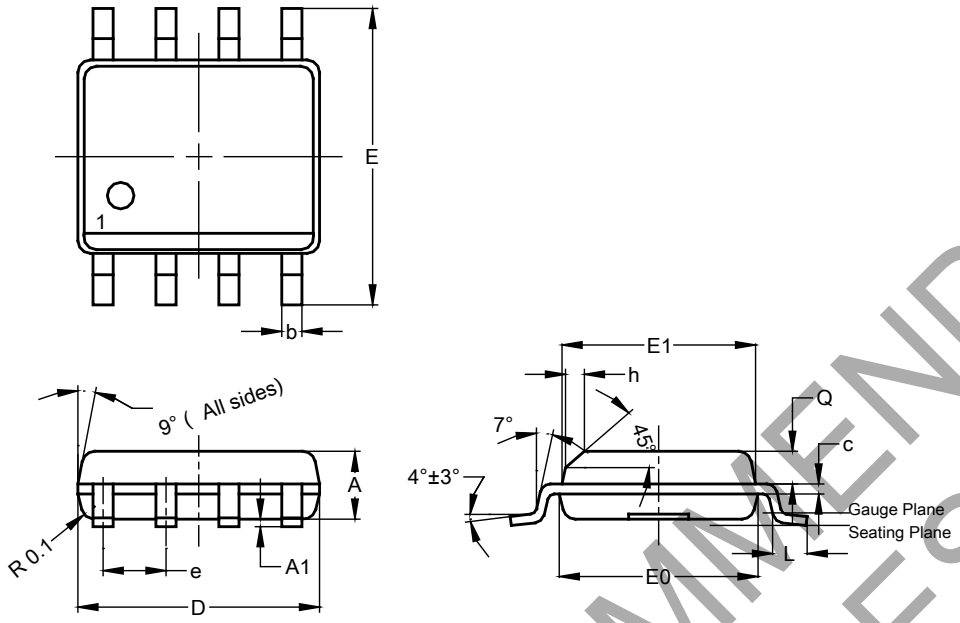


Fig. 23 Transient Thermal Response

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8

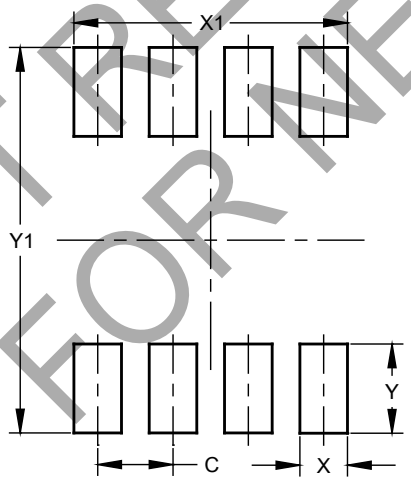


SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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