THE DATASHEET OF

TLV75518PDQNT

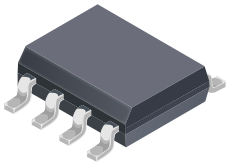
ACS711

Hall-Effect Linear Current Sensor with Overcurrent Fault Output for <100 V Isolation Applications

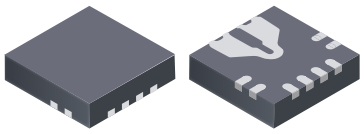
FEATURES AND BENEFITS

- No external sense resistor required; single package solution
- Reduced power loss:
  - □ 0.6 mΩ internal conductor resistance on EX package
  - □ 1.2 mΩ internal conductor resistance on LC package
- Economical low- and high-side current sensing
- Output voltage proportional to AC or DC currents
- ±12.5 A and ±25 A full-scale sensing ranges on LC package
- ±15.5 A and ±31 A full-scale sensing ranges on EX package
- Overcurrent $\overline{\text{FAULT}}$ trips and latches at 100% of full-scale current
- Low-noise analog signal path
- 100 kHz bandwidth
- Small footprint, low-profile SOIC8 and QFN packages
- 3 to 5.5 V single supply operation
- Integrated electrostatic shield for output stability
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Zero magnetic hysteresis
- Ratiometric output from supply voltage

PACKAGES:



8-pin SOICN
with internally fused path
(LC package)



12-contact QFN
3 mm × 3 mm × 0.75 mm
(EX package)

Not to scale

DESCRIPTION

The Allegro™ ACS711 provides economical and precise solutions for AC or DC current sensing in <100 V audio, communications systems, and white goods. The device package allows for easy implementation by the customer. Typical applications include circuit protection, current monitoring, and motor and inverter control.

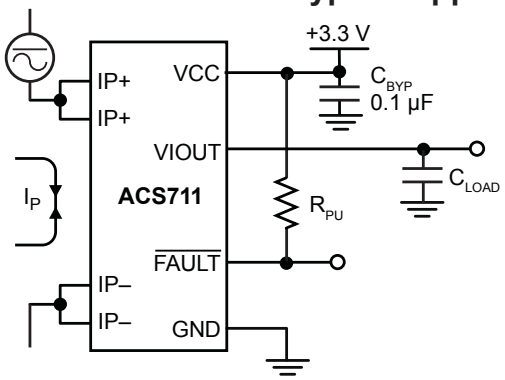
The device consists of a linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer.

The output of the device has a positive slope proportional to the current flow from IP+ to IP– (pins 1 and 2, to pins 3 and 4). The internal resistance of this conductive path is 0.6 mΩ for the EX package, and 1.2 mΩ for the LC package, providing a non-intrusive measurement interface that saves power in applications that require energy efficiency.

The ACS711 is optimized for low-side current sensing applications, although the terminals of the conductive path are electrically isolated from the sensor IC leads, providing sufficient internal creepage and clearance dimensions for a low AC or DC working voltage applications. The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions.

The ACS711 is provided in small, surface-mount packages: SOIC8 and QFN12. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Typical Application



Application 1. The ACS711 outputs an analog signal, V_{IOUT}, that varies linearly with the bi-directional AC or DC primary current, I_P, within the range specified. The $\overline{\text{FAULT}}$ pin trips when I_P reaches ±100% of its full-scale current.

SELECTION GUIDE

Part Number	T_A (°C)	Optimized Accuracy Range, I_P (A)	Sensitivity [1], Sens (Typ) (mV/A)	Package	Packing
ACS711ELCTR-12AB-T	–40 to 85	±12.5	110	8-pin SOICN	3000 pieces/reel
ACS711KLCTR-12AB-T	–40 to 125				
ACS711KLCTR-25AU-T	–40 to 125	25	100		
ACS711ELCTR-25AB-T	–40 to 85	±25	55		
ACS711KLCTR-25AB-T	–40 to 125				
ACS711KEXLT-15AB-T [2]	–40 to 125	±15.5	90	12-contact QFN with fused current loop	1500 pieces/reel
ACS711KEXLT-30AU-T [2]	–40 to 125	30	90		
ACS711KEXLT-31AB-T [2]	–40 to 125	±31	45		

[1] Sensitivity measured with V_{CC} = 3.3 V.

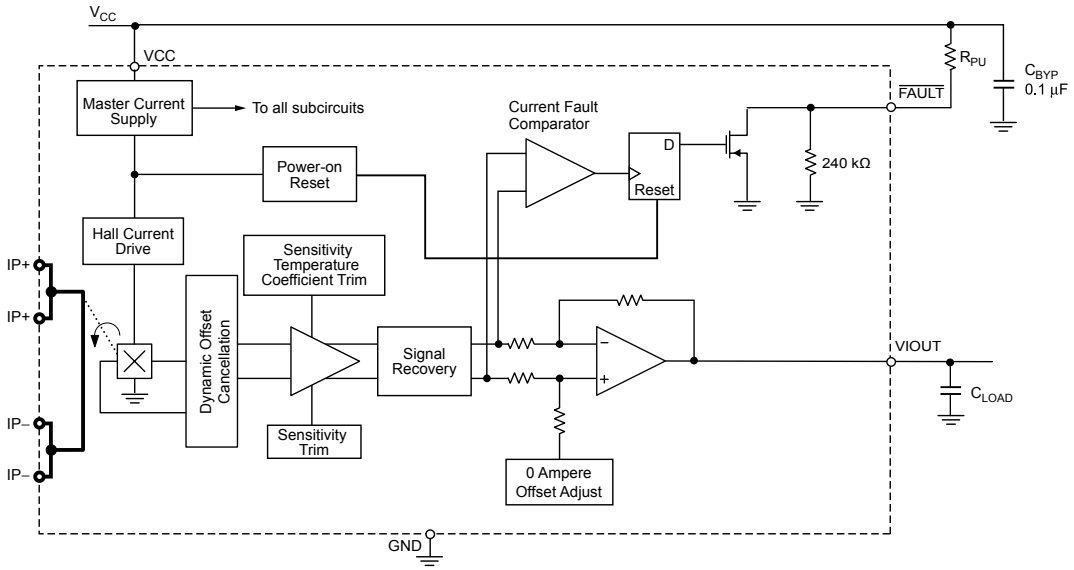
[2] QFN package not qualified for automotive applications.

ABSOLUTE MAXIMUM RATINGS

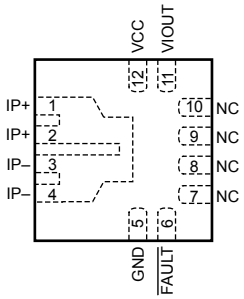
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		7	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Output Voltage	V_{IOUT}		7	V
Reverse Output Voltage	V_{RIOUT}		–0.1	V
Working Voltage for Basic Isolation	$V_{WORKING}$	Voltage applied between pins 1-4 and 5-8	100	VAC peak or VDC
$\overline{\text{FAULT}}$ Pin Voltage	V_{FAULT}		7	V
Overcurrent Transient Tolerance	I_{POC}	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

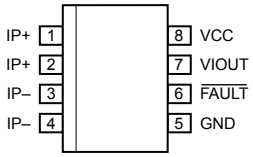
Functional Block Diagram



PINOUT DIAGRAMS



EX Package



LC Package

TERMINAL LIST TABLE

Name	Number		Description
	EX	LC	
GND	5	5	Signal ground terminal
$\overline{\text{FAULT}}$	6	6	Overcurrent fault; active low
IP–	3 and 4	3 and 4	Terminals for current being sensed; fused internally
IP+	1 and 2	1 and 2	Terminals for current being sensed; fused internally
NC	7, 8, 9, 10	–	No connection; connect to GND for optimal ESD performance.
VCC	12	8	Device power supply terminal
VIOUT	11	7	Analog output signal

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

COMMON OPERATING CHARACTERISTICS: Valid across the full range of T_A for the LC package and at T_A = 25°C for the EX package, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		3	3.3	5.5	V
Supply Current	I_{CC}	V_{CC} = 3.3 V, output open	–	4	5.5	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	1	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	15	–	–	kΩ
Primary Conductor Resistance	R_{IP}	EX package	–	0.6	–	mΩ
		LC package, T_A = 25°C	–	1.2	–	mΩ
Primary Conductor Inductance	L_{IP}	T_A = 25°C	–	2	–	nH
VIOUT Rise Time	t_r	$I_P = I_{P(max)}$, T_A = 25°C, C_{LOAD} = 0 nF	–	3.5	–	µs
Propagation Delay Time	t_{PROP}	$I_P = I_{P(max)}$, T_A = 25°C, C_{LOAD} = 0 nF	–	1.2	–	µs
Response Time	$t_{RESPONSE}$	$I_P = I_{P(max)}$, T_A = 25°C, C_{LOAD} = 0 nF	–	4.6	–	µs
Output Slew Rate	SR	T_A = 25°C, C_{LOAD} = 0 nF	–	0.30	–	V/µs
Internal Bandwidth [2]	BW_I	–3 dB, T_A = 25°C	–	100	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	±1	–	%
Symmetry	E_{SYM}	Apply full scale I_P	–	100	–	%
VIOUT Saturation Voltages	V_{IOH}		V_{CC} – 0.3	–	–	V
	V_{IOL}		–	–	0.3	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_A = 25°C, 20 A present on primary conductor	–	35	–	µs
$\overline{\text{FAULT}}$ PIN CHARACTERISTICS						
$\overline{\text{FAULT}}$ Operating Point	I_{FAULT}		–	±1 × I_P	–	A
$\overline{\text{FAULT}}$ Output Pullup Resistor	R_{PU}		1	–	–	kΩ
$\overline{\text{FAULT}}$ Output Voltage	V_{OH}		–	V_{CC} – 0.3	–	V
	V_{OL}	R_{PU} = 1 kΩ	–	0.3	–	V
$\overline{\text{FAULT}}$ Response Time	t_{FAULT}	Measured from | I_P | > | I_{FAULT} | to $V_{FAULT} \le V_{OL}$	–	1.3	–	µs
V_{CC} Off Voltage Level for Fault Reset [3]	V_{CCFR}		–	–	200	mV
V_{CC} Off Duration for Fault Reset [3]	t_{CCFR}		100	–	–	µs

[1] Devices are programmed for maximum accuracy at 3.3 V V_{CC} levels. The device contains ratiometry circuits that accurately alter the 0 A Output Voltage and Sensitivity level of the device in proportion to the applied V_{CC} level. However, as a result of minor nonlinearities in the ratiometry circuit additional output error will result when V_{CC} varies from the 3.3 V V_{CC} level.

[2] Calculated using the formula $BW_I = 0.35 / t_r$.

[3] After the $\overline{\text{FAULT}}$ pin is latched low, the only way to reset it is through a power-off and power-on cycle on the VCC pin. For fault reset, V_{CC} must stay below V_{CCFR} for a period greater than t_{CCFR} before settling to the normal operation voltage (3 to 5.5 V).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

x12AB PERFORMANCE CHARACTERISTICS for LC package and E Temperature Range[1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–12.5	–	12.5	A
Sensitivity	Sens	Over full range of I_P	–	110	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise[2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 85°C	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error[3]	E_{TOT}	I_P = ±12.5 A, T_A = –40°C to 85°C	–	±5	–	%

[1] See Characteristic Performance Data for parameter distributions over temperature.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±12.5 A.

x12AB PERFORMANCE CHARACTERISTICS for LC package and K Temperature Range[1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–12.5	–	12.5	A
Sensitivity	Sens	Over full range of I_P	–	110	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise[2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error[3]	E_{TOT}	I_P = ±12.5 A, T_A = –40°C to 125°C	–	±5	–	%

[1] See Characteristic Performance Data for parameter distributions over temperature.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±12.5 A.

x25AU PERFORMANCE CHARACTERISTICS for LC package and K Temperature Range

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		0	–	25	A
Sensitivity	Sens	Over full range of I_P	–	100	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.1	–	V
Noise[1]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error[2]	E_{TOT}	I_P = 25 A, T_A = –40°C to 125°C	–	±5	–	%

[1] ±3 sigma noise voltage.
[2] Percentage of I_P, with I_P = 25 A.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

x25AB PERFORMANCE CHARACTERISTICS for LC package and E Temperature Range[1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–25	–	25	A
Sensitivity	Sens	Over full range of I_P	–	55	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise[2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	8	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 85°C	–	±30	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±35	–	mV
Total Output Error[3]	E_{TOT}	I_P = ±25 A, T_A = –40°C to 85°C	–	±4	–	%

[1] See Characteristic Performance Data for parameter distributions over temperature.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±25 A.

x25AB PERFORMANCE CHARACTERISTICS for LC package and K Temperature Range[1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–25	–	25	A
Sensitivity	Sens	Over full range of I_P	–	55	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise[2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	8	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±30	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±35	–	mV
Total Output Error[3]	E_{TOT}	I_P = ±25 A, T_A = –40°C to 125°C	–	±4	–	%

[1] See Characteristic Performance Data for parameter distributions over temperature.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±25 A.

x15AB PERFORMANCE CHARACTERISTICS for EX package and K Temperature Range [1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–15.5	–	15.5	A
Sensitivity	Sens	Over full range of I_P	–	90	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise[2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error[3]	E_{TOT}	I_P = ±12.5 A, T_A = –40°C to 125°C	–	±5	–	%

[1] See Characteristic Performance Data for parameter distributions across the full temperature range.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±15.5 A.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

x30AU PERFORMANCE CHARACTERISTICS for EX package and K Temperature Range

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		0	–	30	A
Sensitivity	Sens	Over full range of I_P	–	90	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.1	–	V
Noise [1]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	11	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±10	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±40	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±50	–	mV
Total Output Error [2]	E_{TOT}	I_P = 12.5 A, T_A = –40°C to 125°C	–	±5	–	%

[1] ±3 sigma noise voltage.
[2] Percentage of I_P, with I_P = 30 A.

x31AB PERFORMANCE CHARACTERISTICS for EX package and K Temperature Range [1]

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		–31	–	31	A
Sensitivity	Sens	Over full range of I_P	–	45	–	mV/A
Zero Current Output Voltage	$V_{IOUT(Q)}$	I_P = 0, T_A = 25°C	–	V_{CC} × 0.5	–	V
Noise [2]	V_{NOISE}	T_A = 25°C, no external low pass filter on VIOUT	–	8	–	mV
Electrical Offset Voltage	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±5	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_A = 25°C to 125°C	–	±30	–	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_A = –40°C to 25°C	–	±35	–	mV
Total Output Error [3]	E_{TOT}	I_P = ±12.5 A, T_A = –40°C to 125°C	–	±4	–	%

[1] See Characteristic Performance Data for parameter distributions across the full temperature range.
[2] ±3 sigma noise voltage.
[3] Percentage of I_P, with I_P = ±31 A.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance, Junction to Lead	$R_{\theta JL}$	LC package, mounted on Allegro ASEK 711 evaluation board	5	°C/W
Package Thermal Resistance, Junction to Ambient [2]	$R_{\theta JA}$	LC package, mounted on Allegro 85-0404 evaluation board, includes the power consumed by the board	23	°C/W
		EX package, mounted on Allegro 85-0528 evaluation board, includes the power consumed by the board	24	°C/W

[1] Additional thermal information available on the Allegro website.

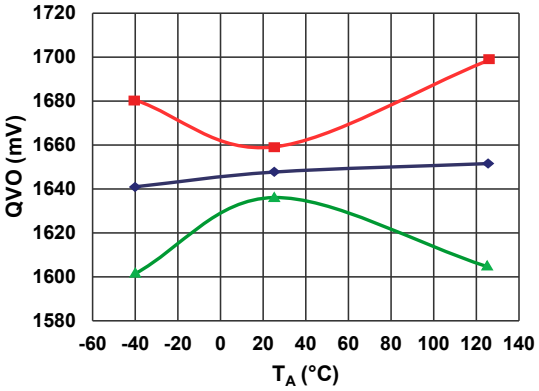
[2] The Allegro evaluation board has 1500 mm^2 of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

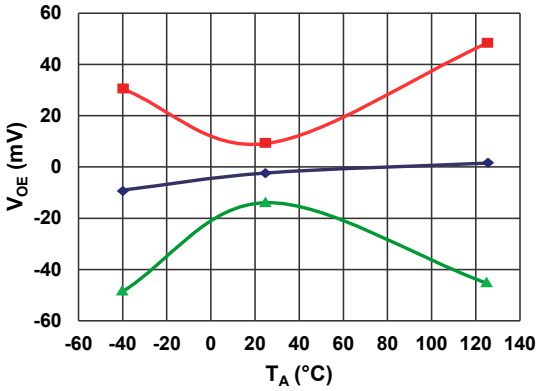
Characteristic Performance Data

Data taken using the ACS711KEX-15A, V_{CC} = 3.3 V

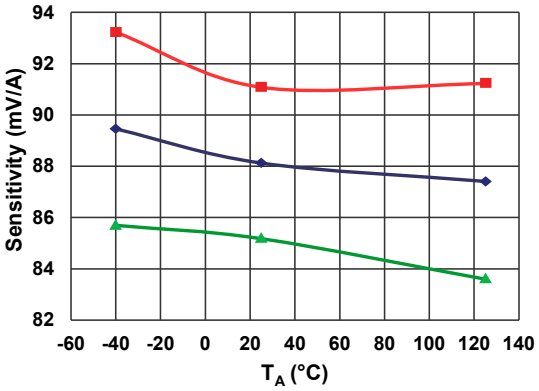
QVO versus Ambient Temperature



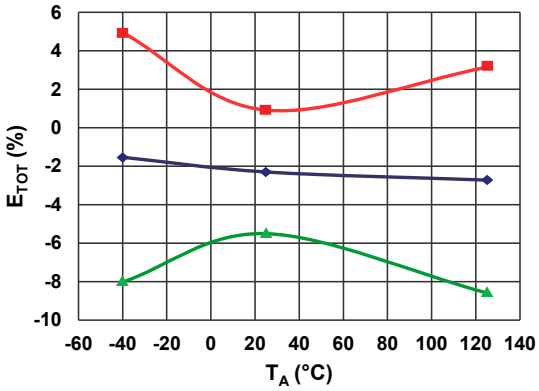
QVO Error versus Ambient Temperature



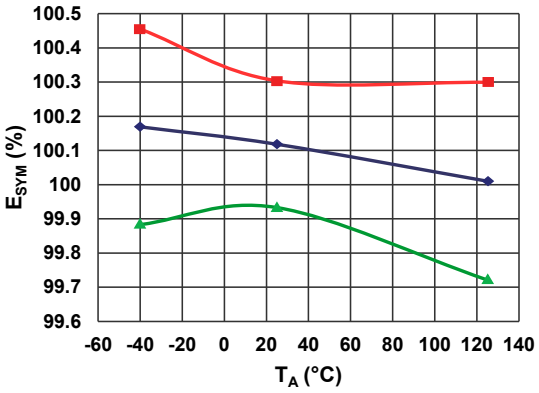
Sensitivity versus Ambient Temperature



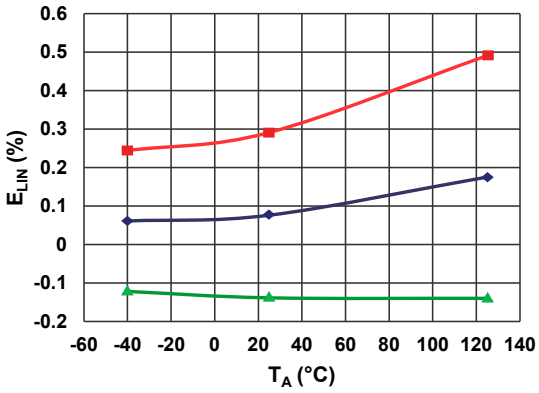
Total Error versus Ambient Temperature

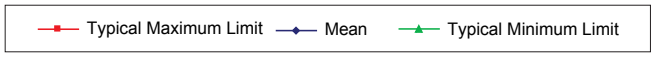


Symmetry versus Ambient Temperature



Nonlinearity versus Ambient Temperature





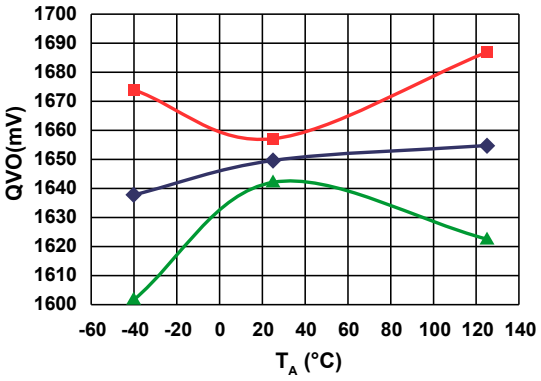
ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

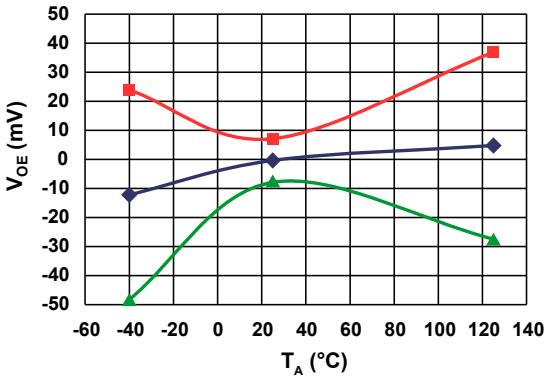
Characteristic Performance Data

Data taken using the ACS711KEX-31AB, V_{CC} = 3.3 V

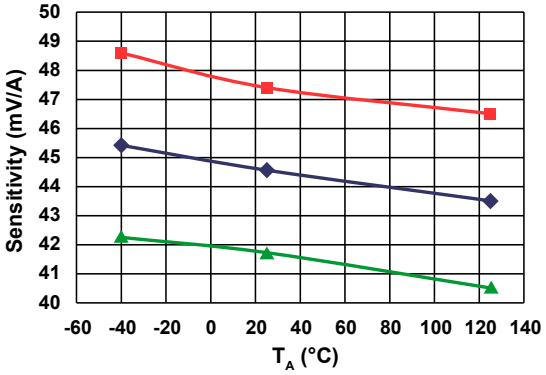
QVO versus Ambient Temperature



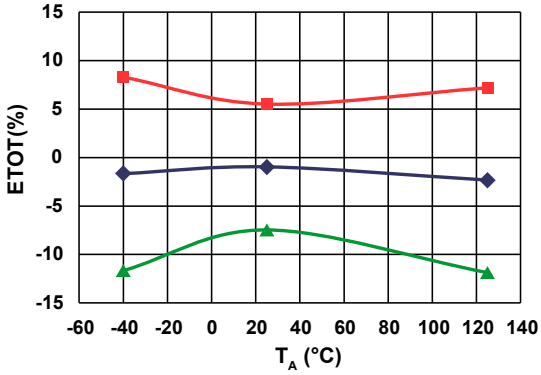
QVO Error versus Ambient Temperature



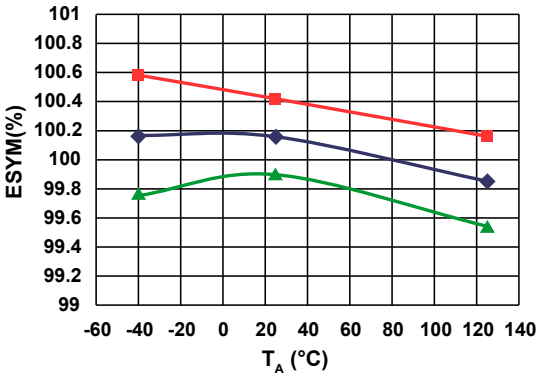
Sensitivity versus Ambient Temperature



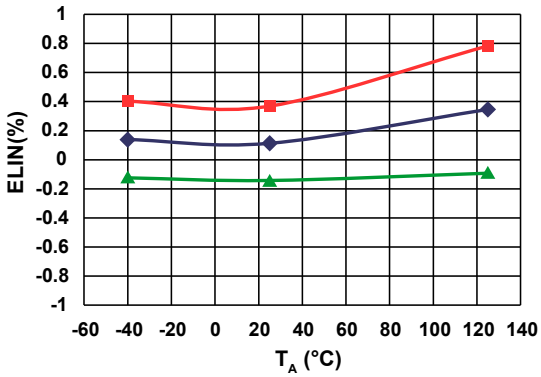
Total Error versus Ambient Temperature

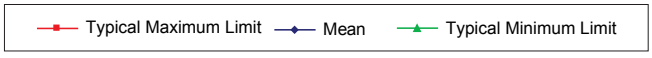


Symmetry versus Ambient Temperature



Nonlinearity versus Ambient Temperature





ALLEGRO microsystems

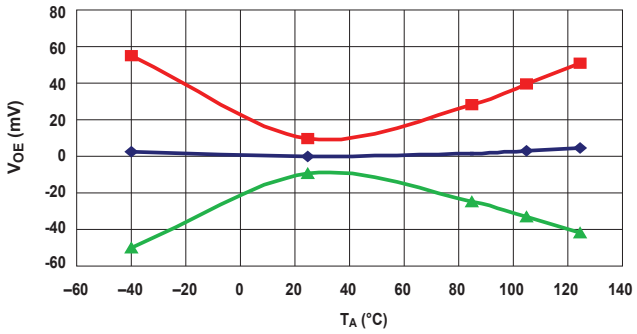
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Characteristic Performance Data

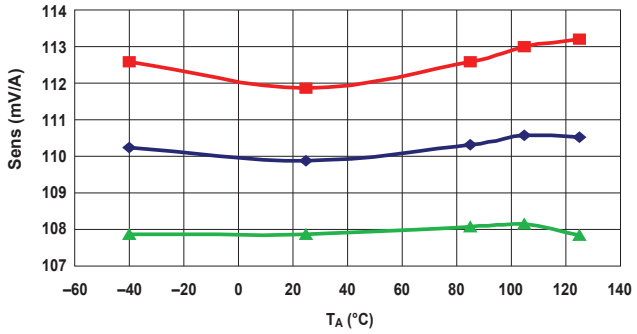
Data taken using the ACS711KLC-12A, V_{CC} = 3.3 V

Accuracy Data

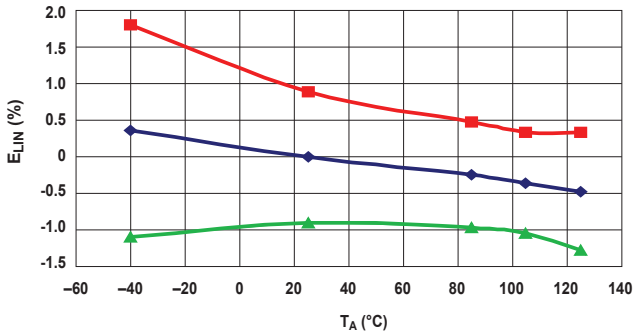
Electrical Offset Voltage versus Ambient Temperature



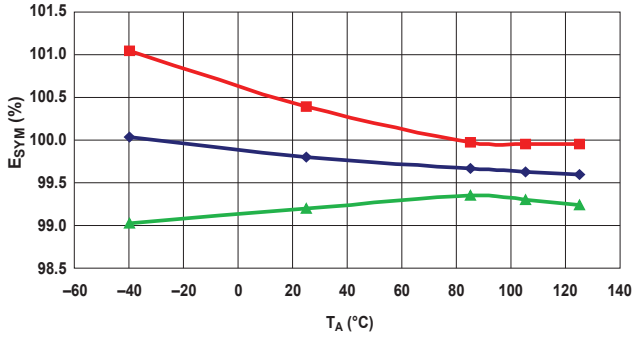
Sensitivity versus Ambient Temperature



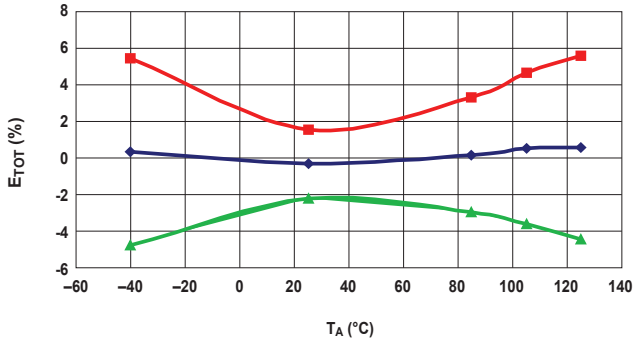
Nonlinearity versus Ambient Temperature



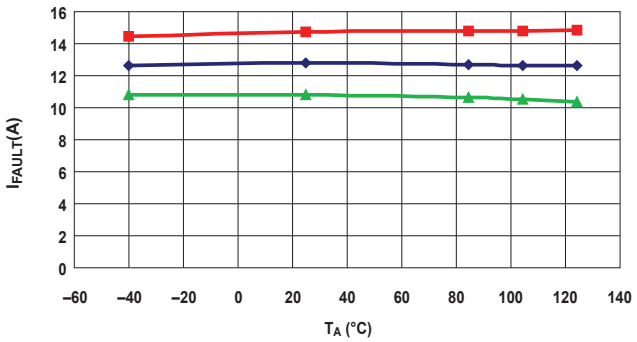
Symmetry versus Ambient Temperature

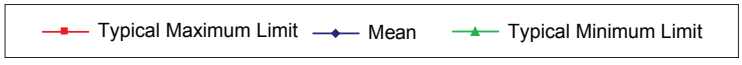


Total Output Error versus Ambient Temperature



Fault Operating Point versus Ambient Temperature





ALLEGRO microsystems

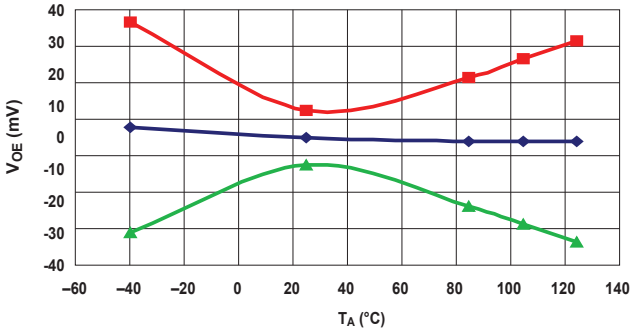
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Characteristic Performance Data

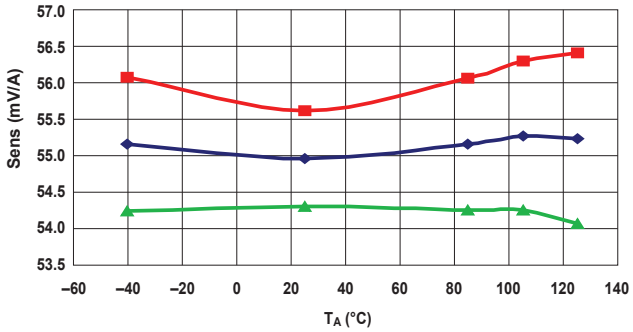
Data taken using the ACS711KLC-25A, V_{CC} = 3.3 V

Accuracy Data

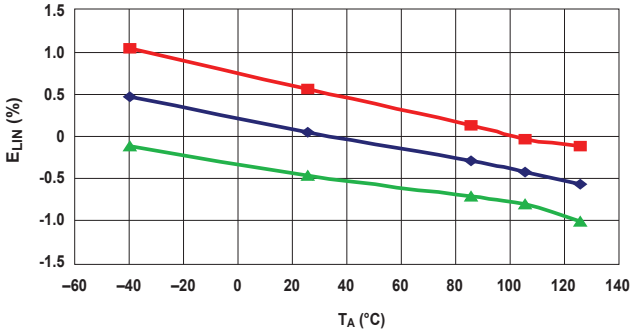
Electrical Offset Voltage versus Ambient Temperature



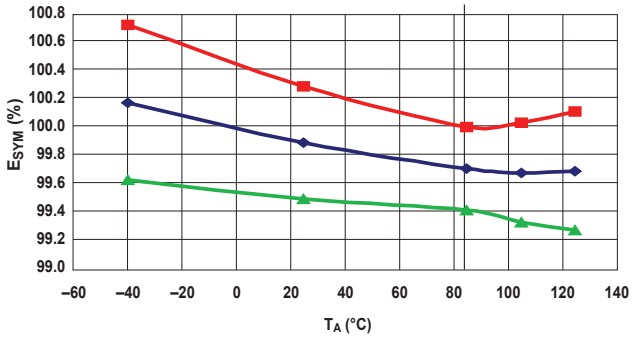
Sensitivity versus Ambient Temperature



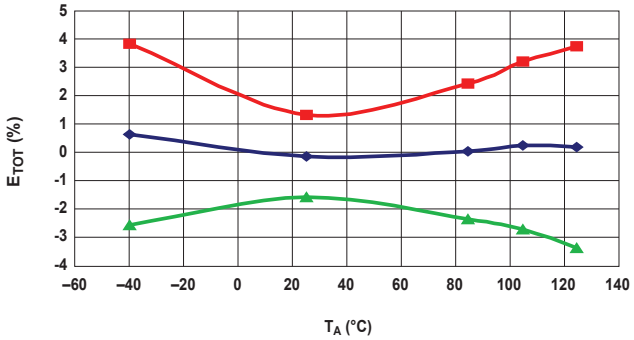
Nonlinearity versus Ambient Temperature



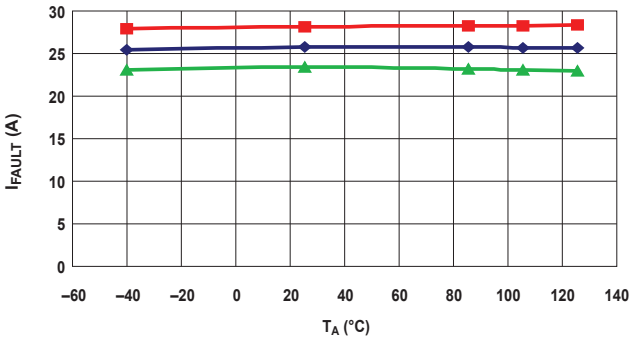
Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



Fault Operating Point versus Ambient Temperature



Typical Maximum Limit — Mean — Typical Minimum Limit

ALLEGRO microsystems

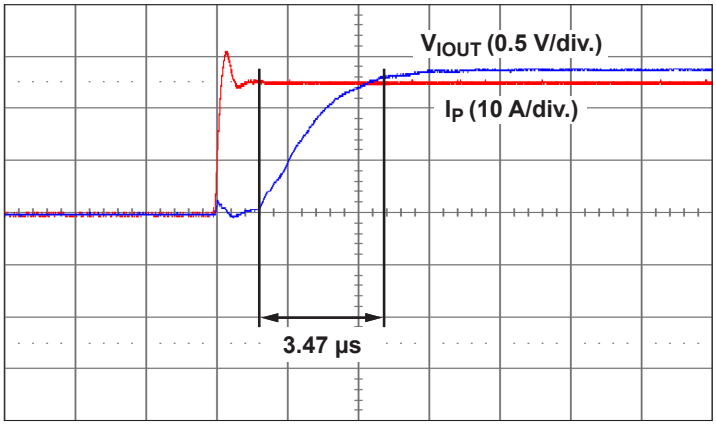
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Characteristic Performance Data

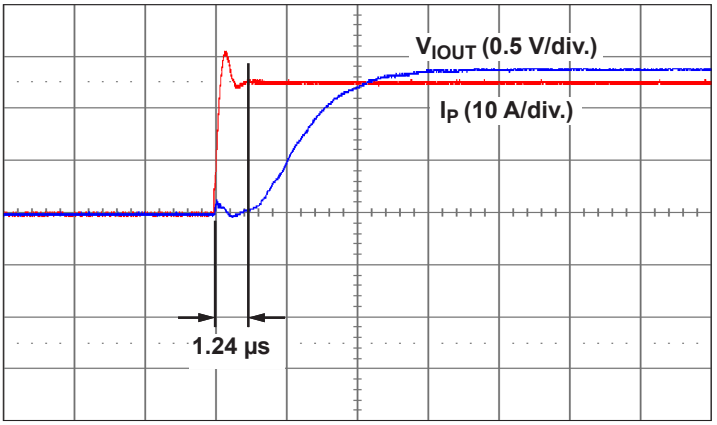
Data taken using the ACS711KLC-25A

Timing Data

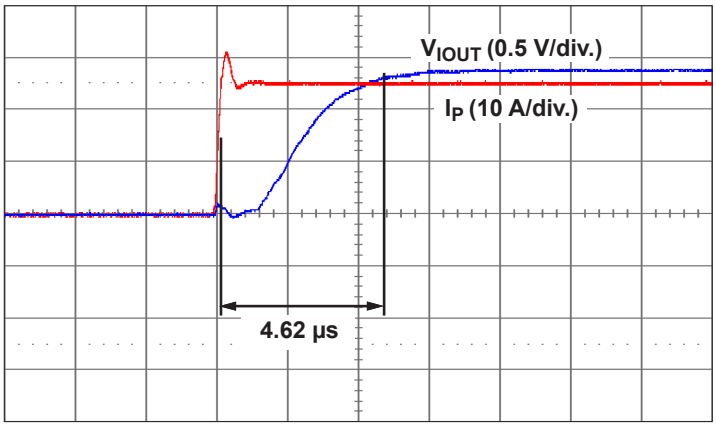
Rise Time



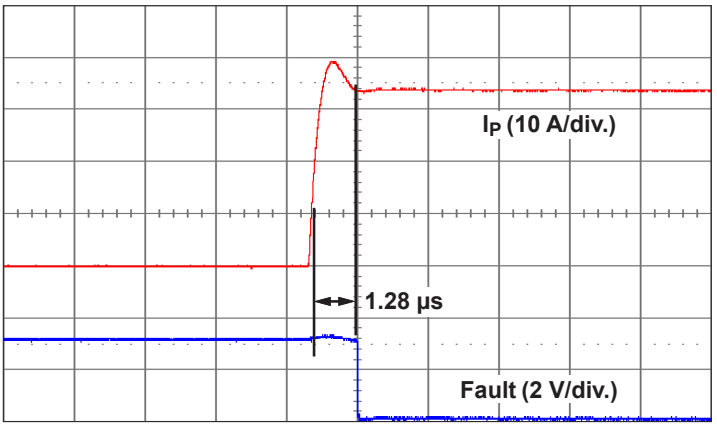
Propagation Delay Time



Response Time

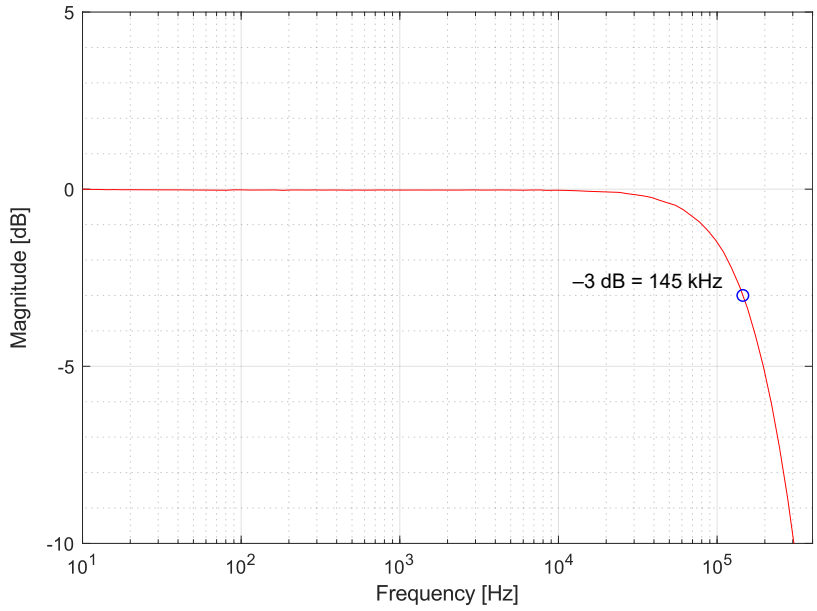


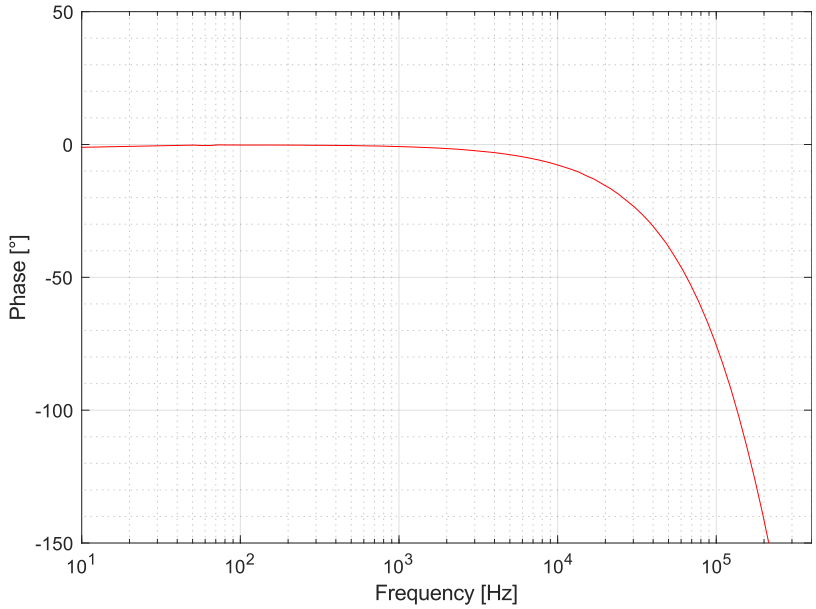
Fault Response



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

CHARACTERISTIC PERFORMANCE
ACS711 TYPICAL FREQUENCY RESPONSE





For information regarding bandwidth characterization methods used for the ACS711, see the “Characterizing System Bandwidth” application note (https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296169-acs720-bandwidth-testing) on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEFINITIONS OF ACCURACY CHARACTERISTICS

Sensitivity (Sens). The change in sensor output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV) and the noise floor for the Allegro Hall effect linear IC. The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the sensor varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta\text{ gain}\times\%\text{ sat}\,(V_{IOUT\_\text{full-scale amperes}}-V_{IOUT(Q)})}{2\,(V_{IOUT\_\text{half-scale amperes}}-V_{IOUT(Q)})}\right]\right\}$$

where $V_{IOUT\_\text{full-scale amperes}}$ = the output voltage (V) when the sensed current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the sensor varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+\text{ full-scale amperes}}-V_{IOUT(Q)}}{V_{IOUT(Q)}-V_{IOUT\_-\text{full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 3.3 V translates into $V_{IOUT(Q)}$ = 1.65 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total ouput error. The accuracy is illustrated graphically in the output voltage versus current chart below.

Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%):

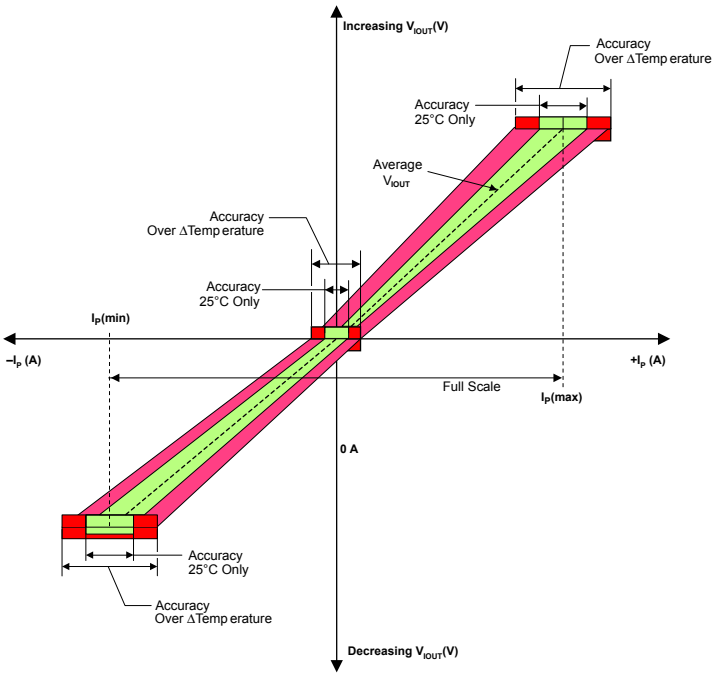
The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{V_{IOUT(Q)VCC}/V_{IOUT(Q)3.3V}}{V_{CC}/3.3\text{ V}}\right)$$

$$100\left(\frac{Sens_{VCC}/Sens_{3.3V}}{V_{CC}/3.3\text{ V}}\right)$$

Output Voltage versus Sensed Current

Accuracy at 0 A and at Full-Scale Current

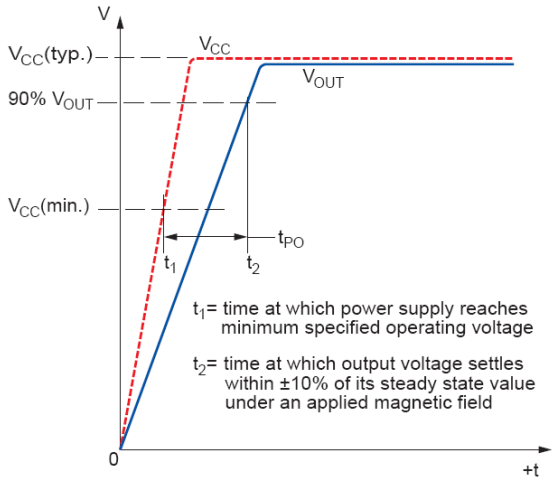


ALLEGRO microsystems

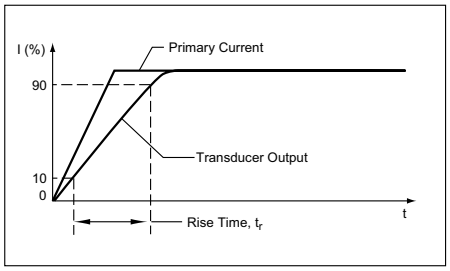
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



Rise time (t_r). The time interval between a) when the sensor reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the current sensor, in which $f(-3\ dB) = 0.35/t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



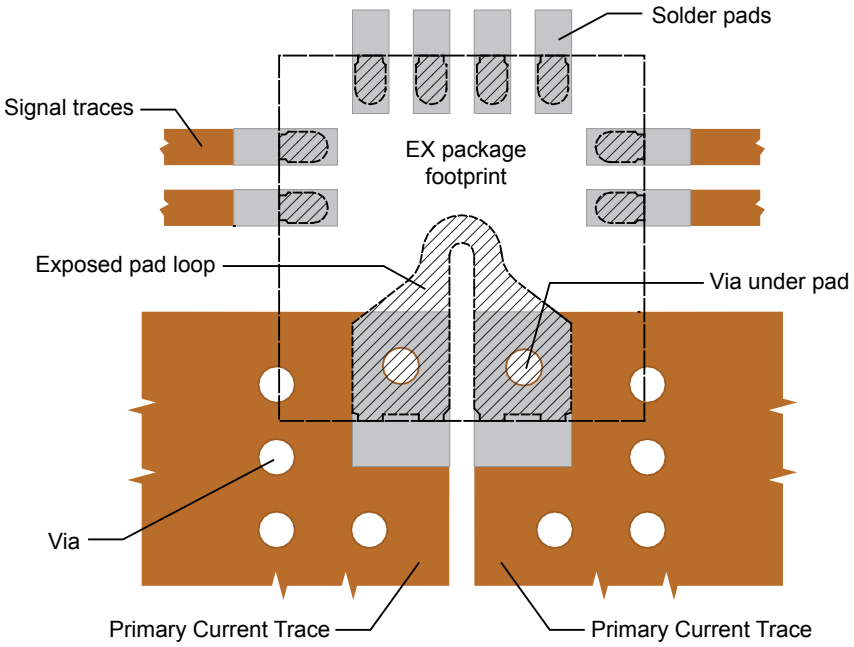
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Layout

To optimize thermal and electrical performance, the following features should be included in the printed circuit board:

- The primary leads should be connected to as much copper area as is available.
- The copper should be 2 oz. or heavier.
- Additional layers of the board should be used for conducting the primary current if possible, and should be connected using the arrangement of vias shown below.
- The two solder pads at the ends of the exposed pad loop should be placed directly on the copper trace that conducts the primary current.
- When using vias under exposed pads, such as with the EX package, using plugged vias prevents wicking of the solder from the pad into the via during reflow. Whether or not to use plugged vias should be evaluated in the application.



Suggested Layout. EX package shown.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Thermal Rise vs. Primary Current

Self-heating due to the flow of current should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current, current "on-time", and duty cycle. While the data presented in this section was collected with direct current (DC), these numbers may be used to approximate thermal response for both AC signals and current pulses.

The plots in Figure 1 and Figure 3 show the measured rise in steady-state die temperature of the ACS711 in the LC package and EX package, respectively, versus continuous current at an ambient temperature, T_A, of 25 °C. The thermal offset curves may be directly applied to other values of T_A. Figure 2 and Figure 4 show the maximum continuous current at a given T_A. Surges beyond the maximum current listed in Figure 2 and Figure 4 are allowed given the maximum junction temperature, $T_{J(MAX)}$ (165°C), is not exceeded.

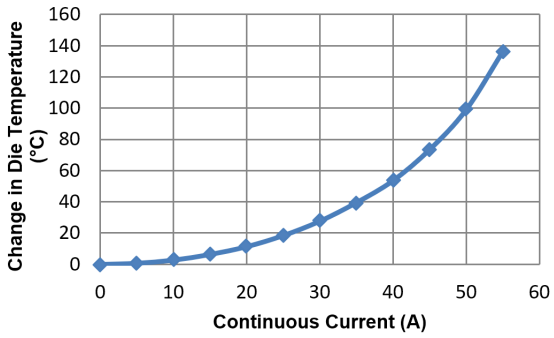


Figure 1: Self-Heating in the LC Package Due to Current Flow

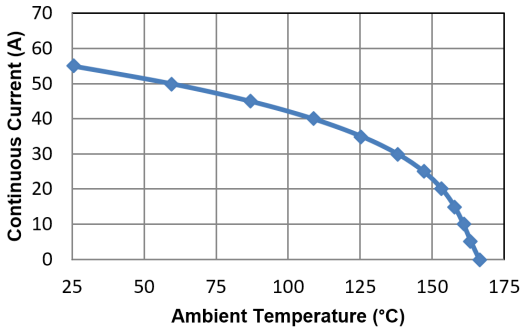


Figure 2: Maximum Continuous Current in the LC Package at a Given T_A

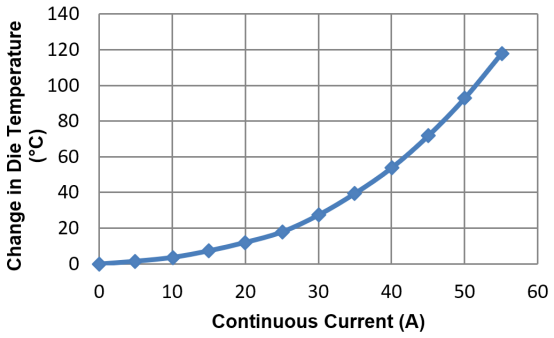


Figure 3: Self-Heating in the EX Package Due to Current Flow

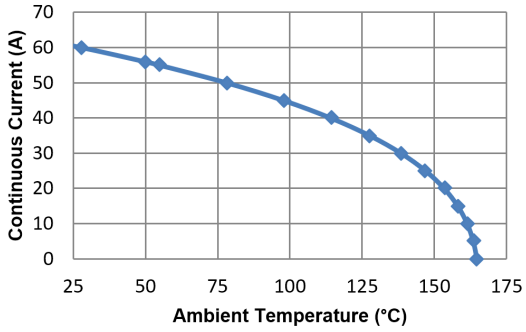


Figure 4: Maximum Continuous Current in the EX Package at a Given T_A

The thermal capacity of the ACS711 should be verified by the end user in the application's specific conditions. The maximum junction temperature, $T_{J(MAX)}$ (165°C), should not be exceeded. Further information on this application testing is available in the DC and Transient Current Capability application note on the Allegro website.

ASEK711 Evaluation Board Layout

Thermal data shown in Figure 1 and Figure 2 was collected using the ASEK711 Evaluation Board (TED-85-0404-001). This board includes 1500 mm^2 of 2 oz. copper (0.0694 mm) connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Top and bottom layers of the PCB are shown below in Figure 5.

Thermal data shown in Figure 3 and Figure 4 was collected using the ASEK711 Evaluation Board (TED-85-0595-001). This board includes 250 mm^2 of 2 oz. copper (0.0694 mm) connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Top and bottom layers of the PCB are shown below in Figure 6.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

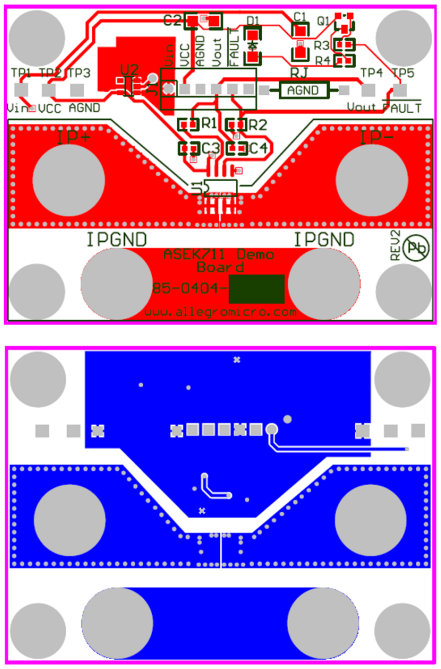


Figure 5: Top and Bottom Layers for ASEK711 Evaluation Board (TED-85-0404-001)

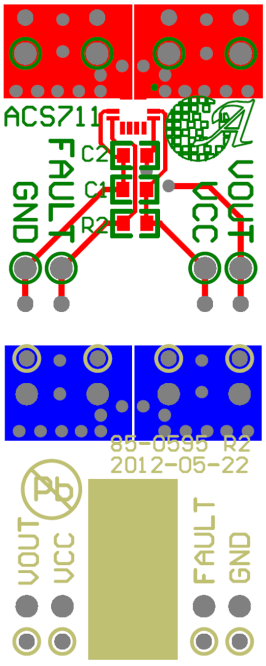


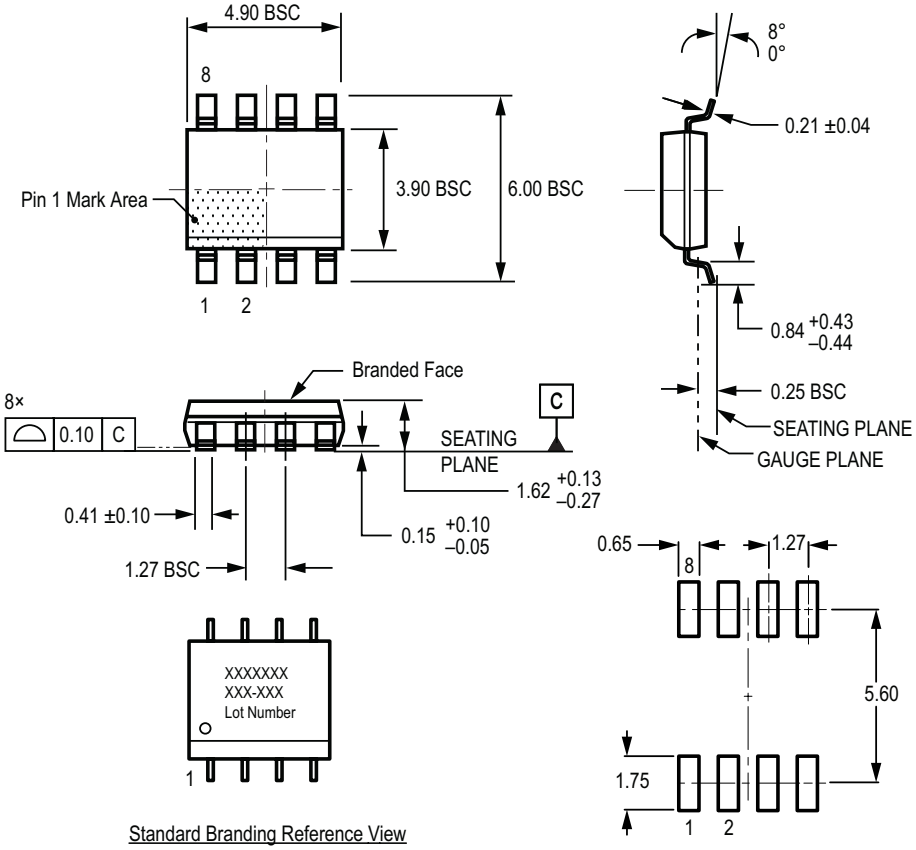
Figure 6: Top and Bottom Layers for ASEK711 Evaluation Board (TED-85-0595-001)

Gerber files for the ASEK711 evaluation board are available for download from the Allegro website. See the technical documents section of the ACS711 device webpage.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package LC, 8-pin SOIC

For Reference Only; not for tooling use
(reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters – Not to scale
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Standard Branding Reference View

Lines 1, 2 = 8 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Temp, Pkg - Amps
Line 3: First 5 Characters of Assembly Lot Number

Belly Brand: Country of Origin, Lot Number

Branding scale and appearance at supplier discretion

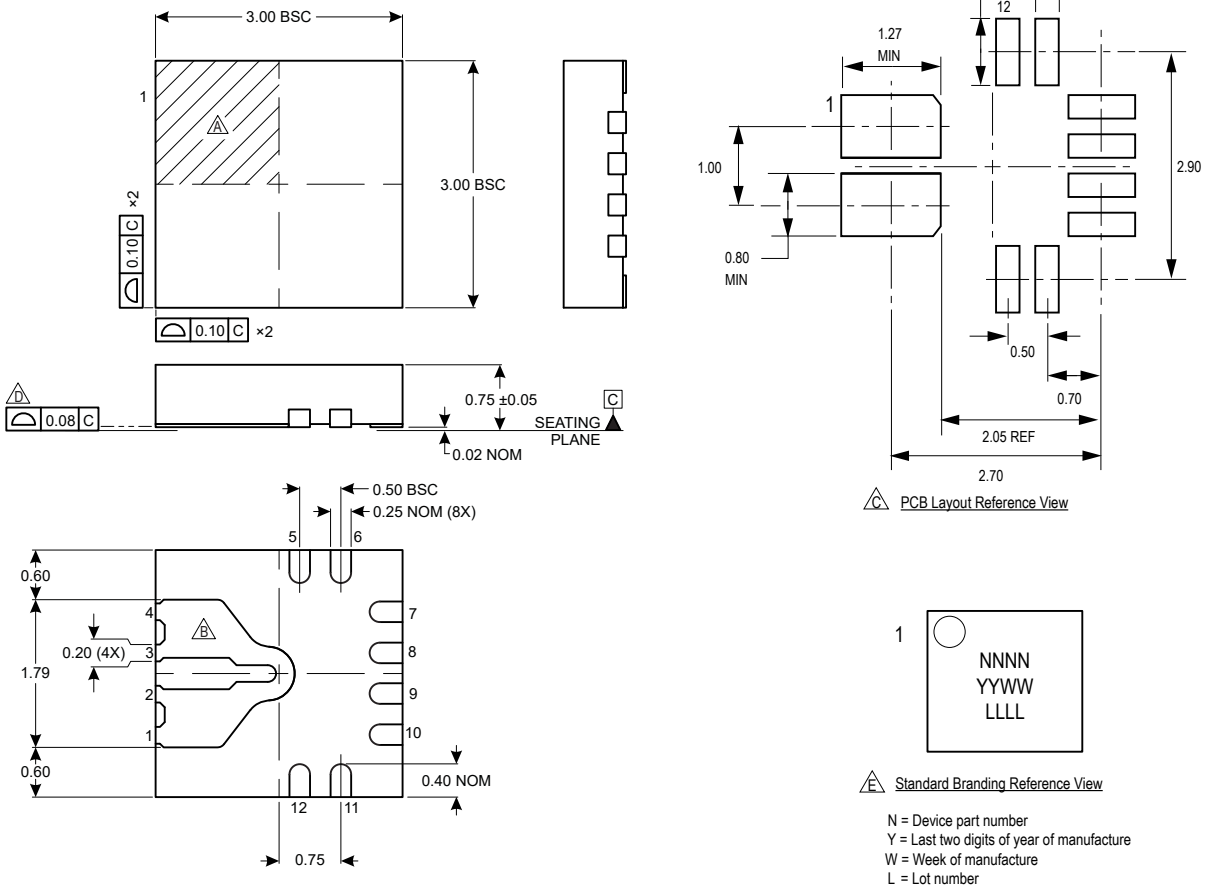
PCB Layout Reference View
Reference land pattern layout
(reference IPC7351 SOIC127P600X175-8M);
all pads a minimum of 0.20 mm from all adjacent pads;
adjust as necessary to meet application process
requirements and PCB layout tolerances.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package EX, 12-Contact QFN
With Fused Sensed Current Loop

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000382, Rev. 2)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

A Terminal #1 mark area

B Fused sensed current path

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed current path and terminals

E Branding scale and appearance at supplier discretion

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
2	July 18, 2013	Update characteristics tables references
3	February 6, 2015	Revised NC description in Terminal List Table
4	June 23, 2017	Added ACS711KEX-15A and ACS711KEX-31AB characteristic performance data plots; Revised product status of ACS711EEXLT-15AB-T and ACS711EEXLT-31AB-T variants to Pre-End-of-Life.
5	January 15, 2021	Added Maximum Continuous Current and ESD Ratings table (page 2), Primary Conductor Inductance and Output Slew Rate (page 4), Frequency Response Plots (page 13), and Thermal Rise vs. Primary Current section (pages 16-17)
6	January 21, 2022	Removed ACS711EEXLT-15AB-T and ACS711EEXLT-31AB-T variants (page 2); added ACS711KLCTR-25AU-T and ACS711KEXLT-30AU-T variants (pages 2, 5, and 7); updated package drawings (pages 20-21), and minor editorial edits (all pages)
7	July 12, 2023	Removed ESD Ratings Table (page 2); removed Maximum Continuous Current from Absolute Maximum Ratings Table (page 2); minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TLV75518PDQNT on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management