THE DATASHEET OF

REF2041QDDCRQ1

TEXAS INSTRUMENTS
REF20-Q1
SBOSA80 – DECEMBER 2021

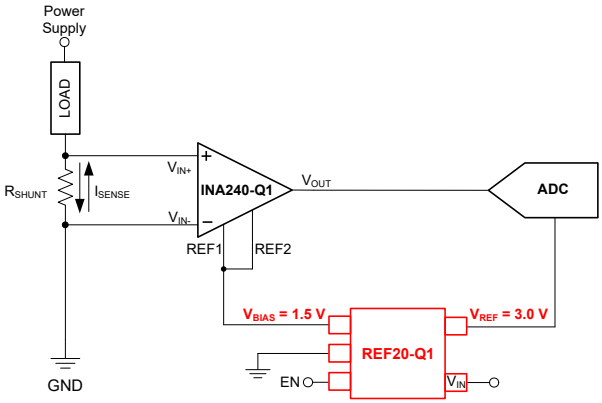
REF20xx-Q1 Low-Drift, Low-Power, Dual-Output, V_{REF} and V_{REF} / 2 Voltage References

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Two Outputs, V_{REF} and V_{REF} / 2, for convenient use in single-supply systems
- Excellent temperature drift performance:
  - 8 ppm/°C (maximum) from –40°C to 125°C
- High initial accuracy: ±0.05% (maximum)
- V_{REF} and V_{BIAS} tracking overtemperature:
  - 7 ppm/°C (maximum) from –40°C to 125°C
- Microsize package: SOT23-5
- Low dropout voltage: 10 mV
- High output current: ±20 mA
- Low quiescent current: 360 µA
- Line regulation: 3 ppm/V
- Load regulation: 8 ppm/mA

2 Applications

- Telematics control
- Battery management systems
- Inverter and motor control
- Automotive gateway
- Power distribution box
- Power steering
- On board chargers



Application Example

3 Description

Applications with only a positive supply voltage often require additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The REF20xx-Q1 provides a reference voltage (V_{REF}) for the ADC and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals.

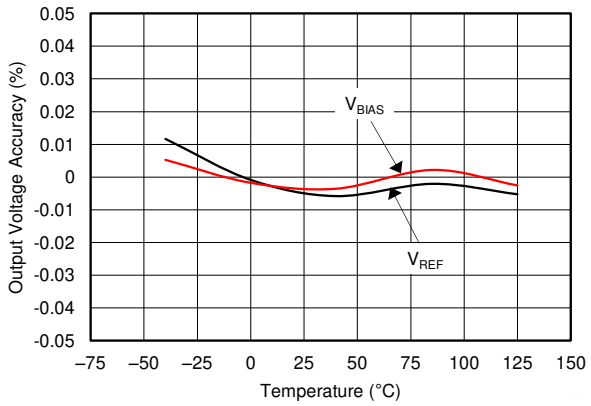
The REF20xx-Q1 offers excellent temperature drift (8 ppm/°C, maximum) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 7 ppm/°C (maximum) across the temperature range of –40°C to 125°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Extremely low dropout voltage of only 10 mV allows operation from very low input voltages, which can be very useful in battery-operated systems.

Both the V_{REF} and V_{BIAS} voltages have the same excellent specifications and can sink and source current equally well. Very good long-term stability and low noise levels make these devices ideally-suited for high-precision applications.

Device Information

PART NAME	PACKAGE (1)	BODY SIZE (NOM)
REF20xx-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



V_{REF} and V_{BIAS} vs Temperature

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2021	*	Initial Release

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5 Device Comparison Table

PRODUCT	V_{REF}	V_{BIAS}
REF2025-Q1	2.5 V	1.25 V
REF2030-Q1	3.0 V	1.5 V
REF2033-Q1	3.3 V	1.65 V
REF2041-Q1	4.096 V	2.048 V

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6 Pin Configuration and Functions

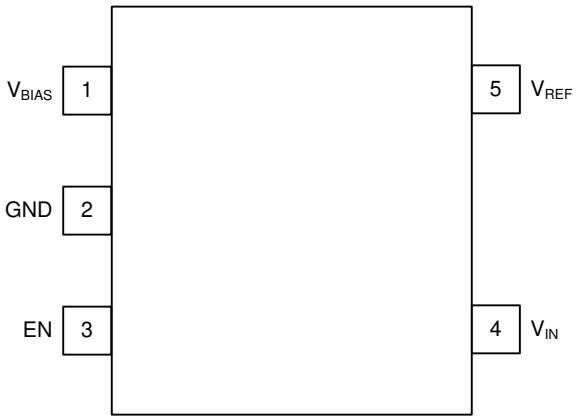

Figure 6-1. DDC Package
SOT23-5
(Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BIAS}	Output	Bias voltage output (V_{REF} / 2)
2	GND	—	Ground
3	EN	Input	Enable (EN ≥ V_{IN} – 0.7 V, device enabled)
4	V_{IN}	Input	Input supply voltage
5	V_{REF}	Output	Reference voltage output (V_{REF})

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
Temperature	Operating	–55	150	°C
	Junction, T_j		150	
	Storage, T_{stg}	–65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range (I_L = 0 mA, T_A = 25°C)	V_{REF} + 0.02 (1)		5.5	V

(1) See Figure 7-27 in Section 7.6 for minimum input voltage at different load currents and temperature

7.4 Thermal Information

THERMAL METRIC (1)		REF20xx-Q1 DDC (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

At T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, unless otherwise noted. Both V_{REF} and V_{BIAS} have the same specifications.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy				–0.05%		0.05%	
	Output voltage temperature coefficient (1)		–40°C ≤ T_A ≤ 125°C			±3	±8	ppm/°C
	V_{REF} and V_{BIAS} tracking over temperature (2)		–40°C ≤ T_A ≤ 125°C			±2	±7	ppm/°C
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta VI)}$	Line regulation		V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			3	35	ppm/V
$\Delta V_{O(\Delta IL)}$	Load regulation	Sourcing	0 mA ≤ I_L ≤ 20 mA , V_{REF} + 0.6 V ≤ V_{IN} ≤ 5.5 V			8	20	ppm/mA
		Sinking	0 mA ≤ I_L ≤ –20 mA, V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			8	20	
POWER SUPPLY								
I_{CC}	Supply current	Active mode				360	430	µA
			–40°C ≤ T_A ≤ 125°C				460	
		Shutdown mode				3.3	5	
			–40°C ≤ T_A ≤ 125°C				9	
	Enable voltage		Device in shutdown mode (EN = 0)		0		0.7	V
			Device in active mode (EN = 1)		V_{IN} – 0.7		V_{IN}	
	Dropout voltage					10	20	mV
			I_L = 20 mA				600	
I_{SC}	Short-circuit current					50		mA
t_{on}	Turn-on time		0.1% settling, C_L = 1 µF			500		µs
NOISE								
	Low-frequency noise (3)		0.1 Hz ≤ f ≤ 10 Hz			12		ppm_{PP}
	Output voltage noise density		f = 100 Hz			0.25		ppm/√ Hz
CAPACITIVE LOAD								
	Stable output capacitor range				0		10	µF
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability (4)		0 to 1000 hours			25		ppm
	Output voltage hysteresis (5)		25°C, –40°C, 125°C, 25°C	Cycle 1		60		ppm
				Cycle 2		35		

(1) Temperature drift is specified according to the box method. See the *Section 9.3* section for more details.
(2) The V_{REF} and V_{BIAS} tracking over temperature specification is explained in more detail in the *Section 9.3* section.
(3) The peak-to-peak noise measurement procedure is explained in more detail in the *Section 8.4* section.
(4) Long-term stability measurement procedure is explained in more in detail in the *Section 8.2* section.
(5) The thermal hysteresis measurement procedure is explained in more detail in the *Section 8.3* section.

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7.6 Typical Characteristics

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.

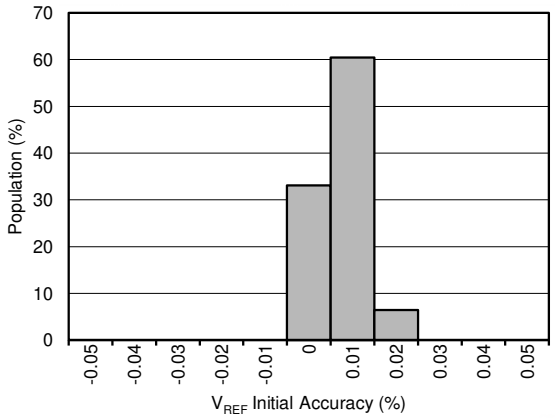
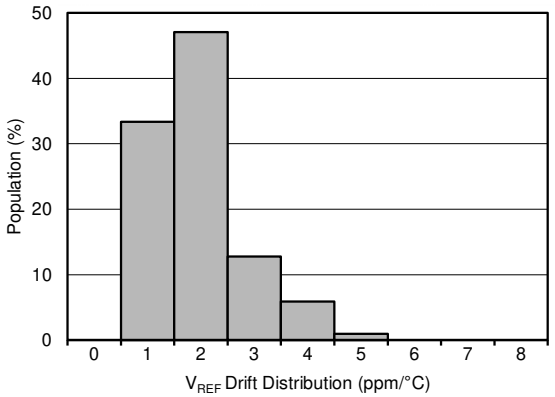


Figure 7-1. Initial Accuracy Distribution (V_{REF})



–40°C ≤ T_A ≤ 125°C

Figure 7-2. Drift Distribution (V_{REF})

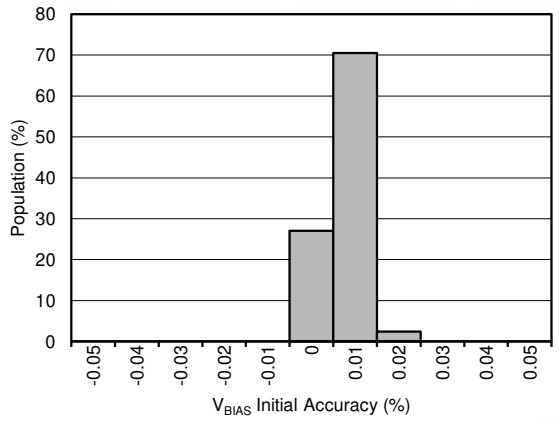
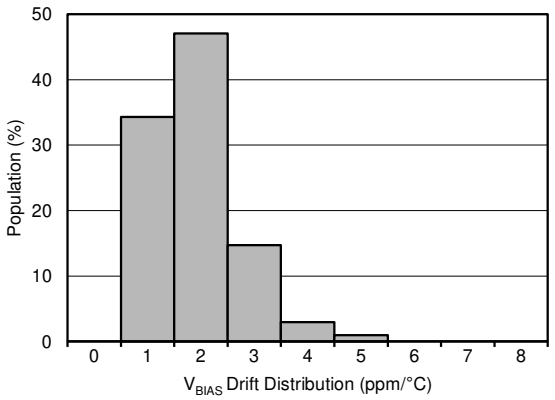


Figure 7-3. Initial Accuracy Distribution (V_{BIAS})



–40°C ≤ T_A ≤ 125°C

Figure 7-4. Drift Distribution (V_{BIAS})

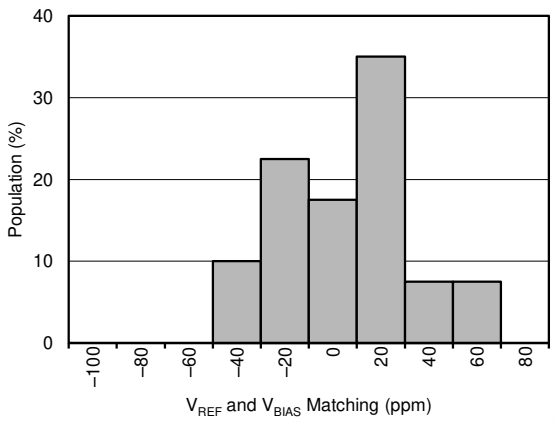
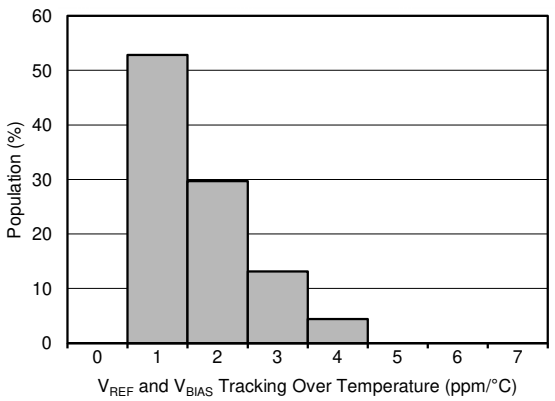


Figure 7-5. V_{REF} – 2 × V_{BIAS} Distribution



–40°C ≤ T_A ≤ 125°C

Figure 7-6. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

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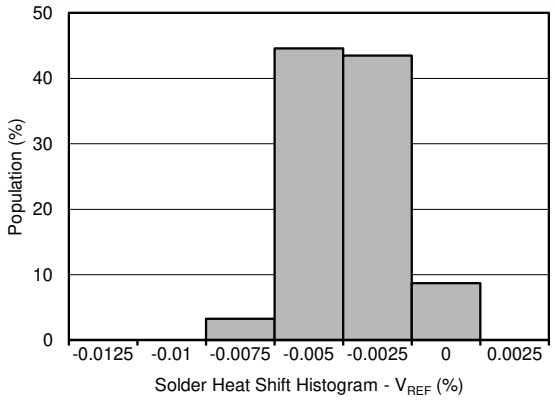
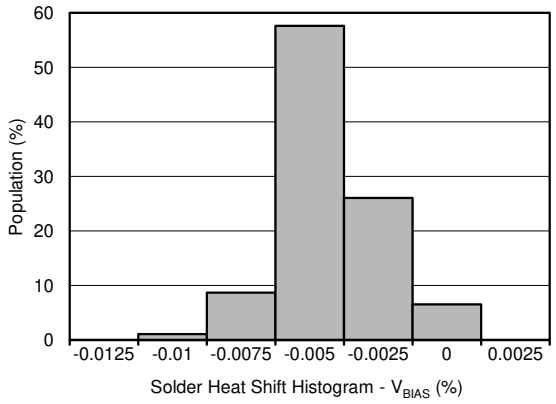
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.



Refer to the *Section 8.1* section for more information.

Figure 7-7. Solder Heat Shift Distribution (V_{REF})



Refer to the *Section 8.1* section for more information.

Figure 7-8. Solder Heat Shift Distribution (V_{BIAS})

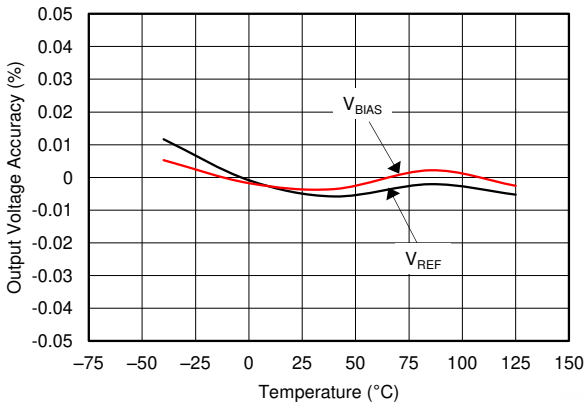


Figure 7-9. Output Voltage Accuracy (V_{REF}) vs Temperature

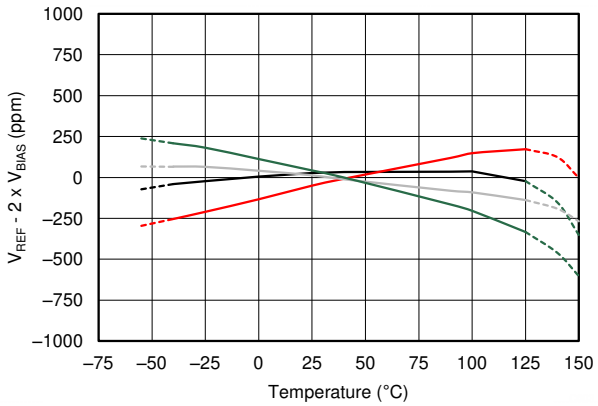
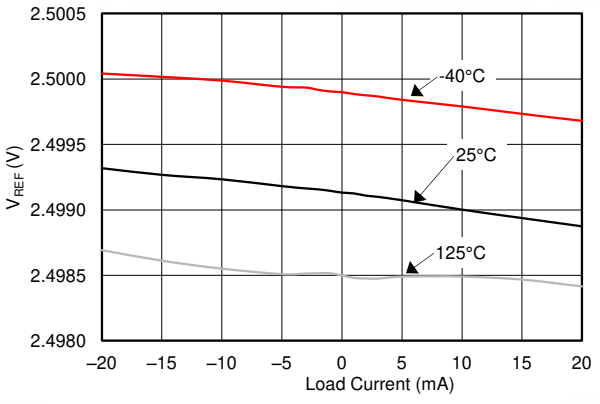
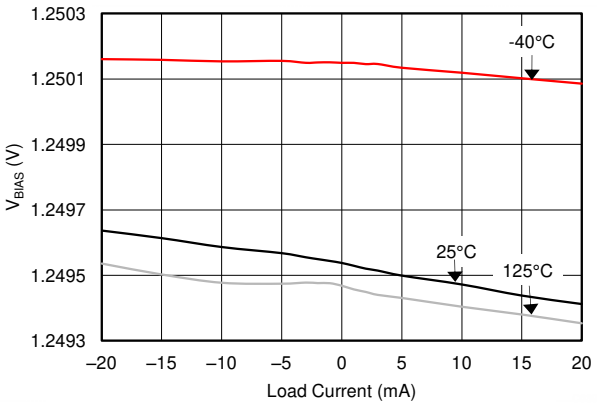


Figure 7-10. V_{REF} – 2 × V_{BIAS} Tracking vs Temperature



V_{REF} output

Figure 7-11. Output Voltage Change vs Load Current (V_{REF})



V_{BIAS} output

Figure 7-12. Output Voltage Change vs Load Current (V_{BIAS})

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7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.

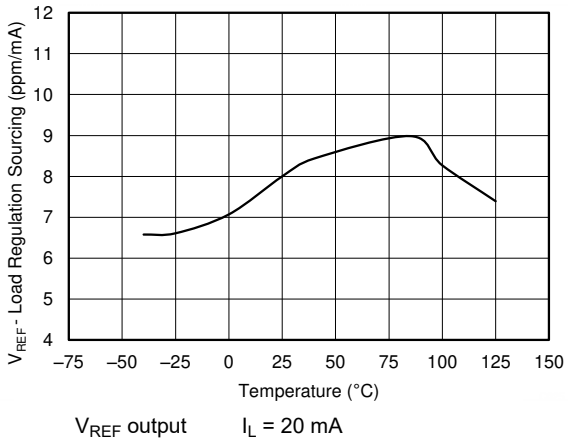

Figure 7-13. Load Regulation Sourcing vs Temperature (V_{REF})

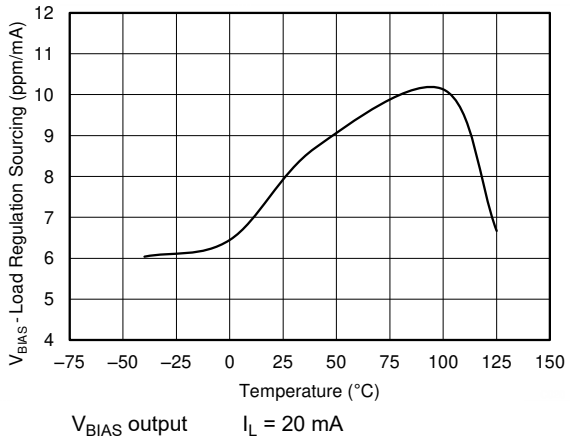

Figure 7-14. Load Regulation Sourcing vs Temperature (V_{BIAS})

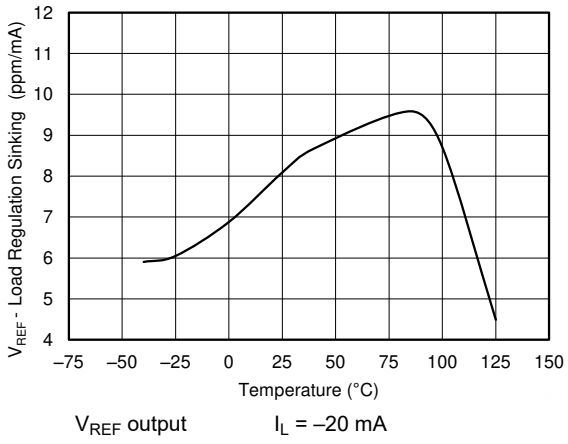

Figure 7-15. Load Regulation Sinking vs Temperature (V_{REF})

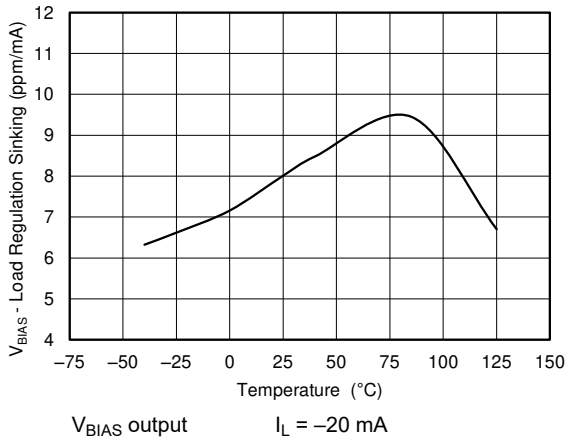

Figure 7-16. Load Regulation Sinking vs Temperature (V_{BIAS})

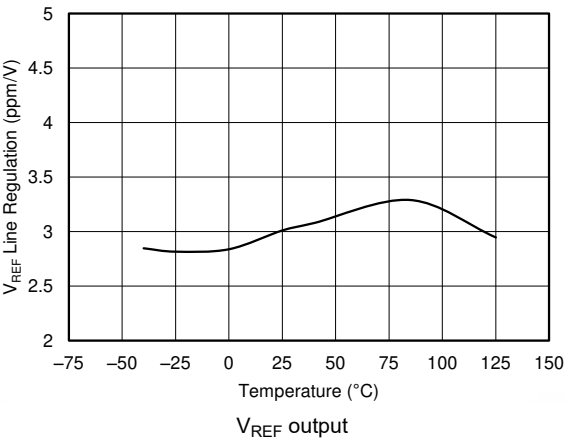

Figure 7-17. Line Regulation vs Temperature (V_{REF})

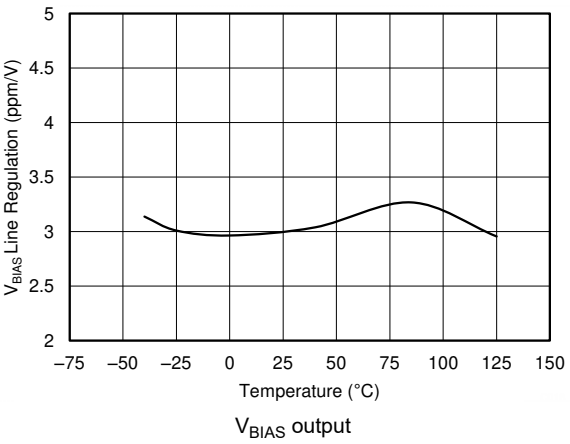

Figure 7-18. Line Regulation vs Temperature (V_{BIAS})

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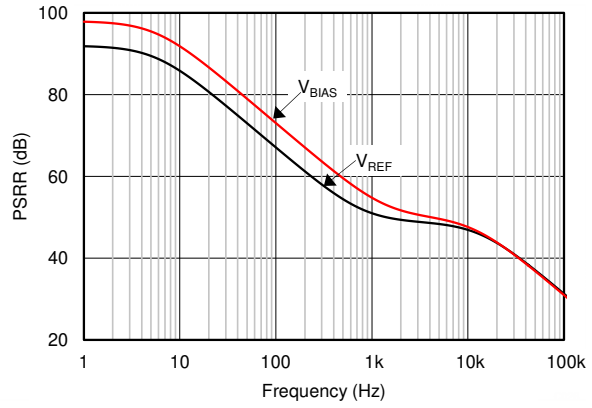
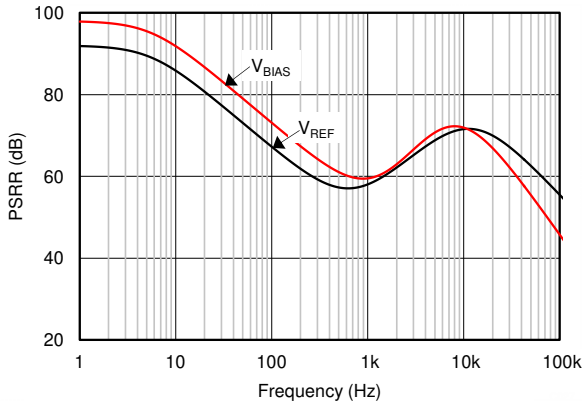
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.



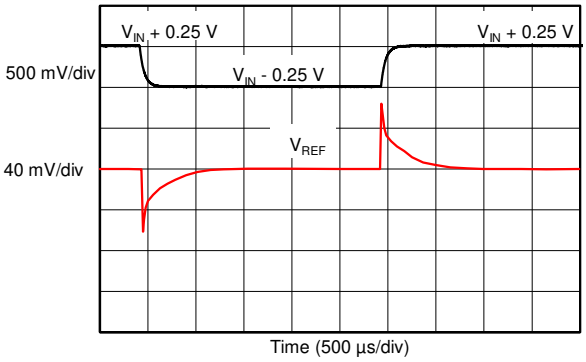
C_L = 0 µF

Figure 7-19. Power-Supply Rejection Ratio vs Frequency



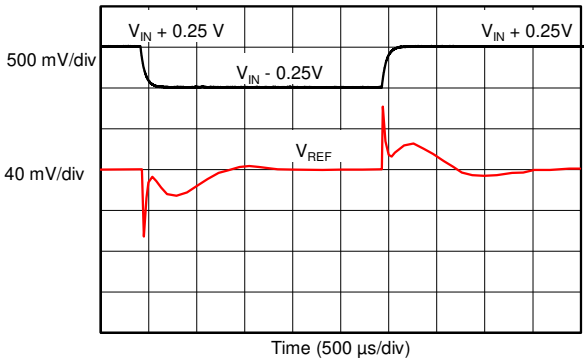
C_L = 10 µF

Figure 7-20. Power-Supply Rejection Ratio vs Frequency



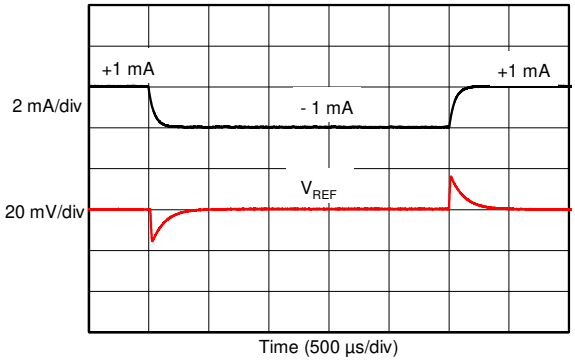
C_L = 1 µF

Figure 7-21. Line Transient Response



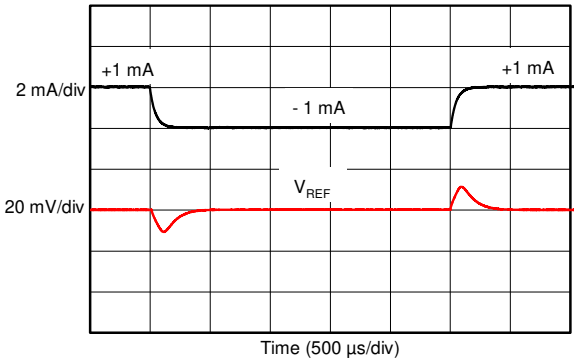
C_L = 10 µF

Figure 7-22. Line Transient Response



C_L = 1 µF I_L = ±1-mA step

Figure 7-23. Load Transient Response



C_L = 10 µF I_L = ±1-mA step

Figure 7-24. Load Transient Response

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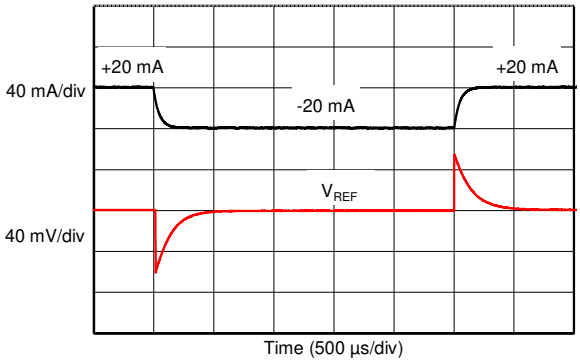
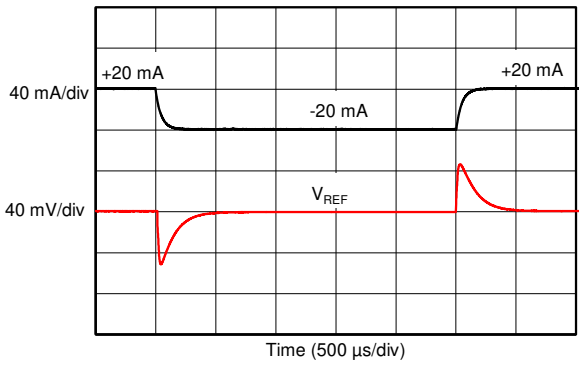
7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.



C_L = 1 µF I_L = ±20-mA step

Figure 7-25. Load Transient Response



C_L = 10 µF I_L = ±20-mA step

Figure 7-26. Load Transient Response

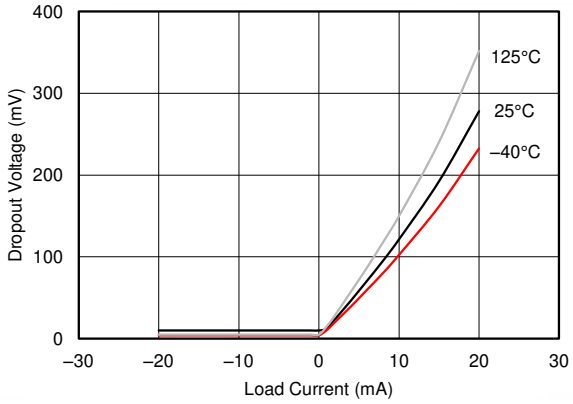
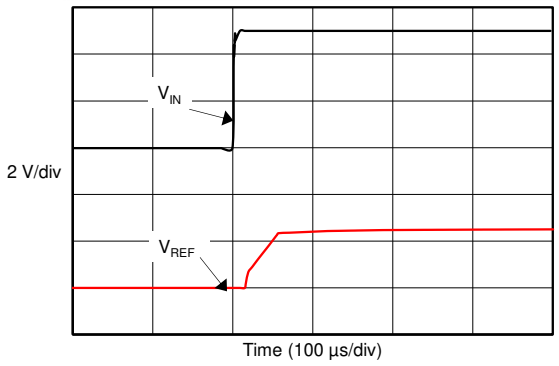
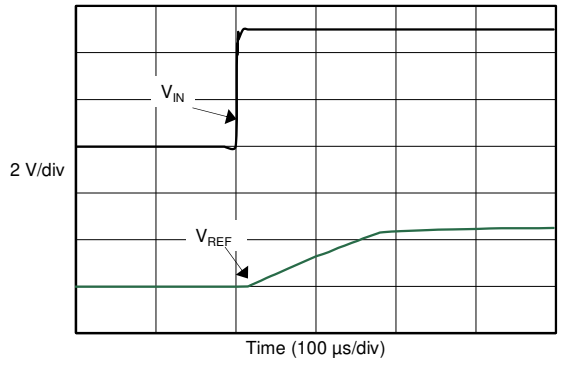


Figure 7-27. Minimum Dropout Voltage vs Load Current



C_L = 1 µF

Figure 7-28. Turn-On Settling Time



C_L = 10 µF

Figure 7-29. Turn-On Settling Time

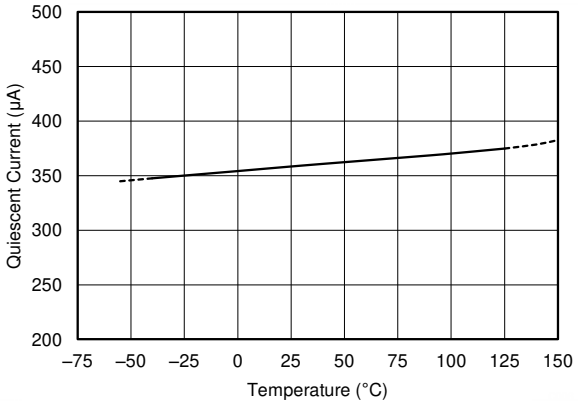


Figure 7-30. Quiescent Current vs Temperature

7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.

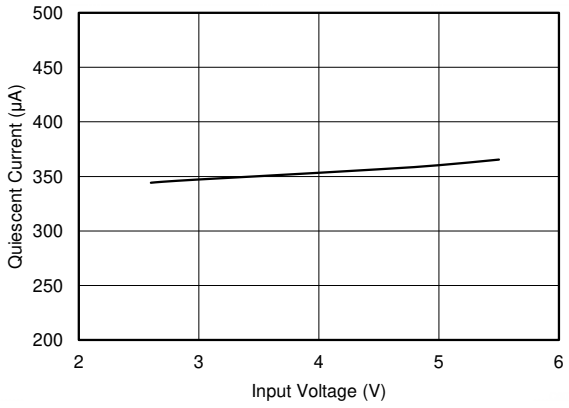
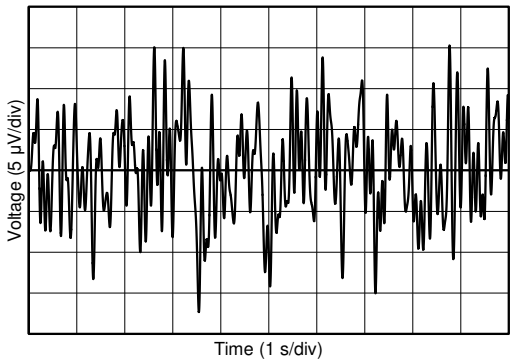
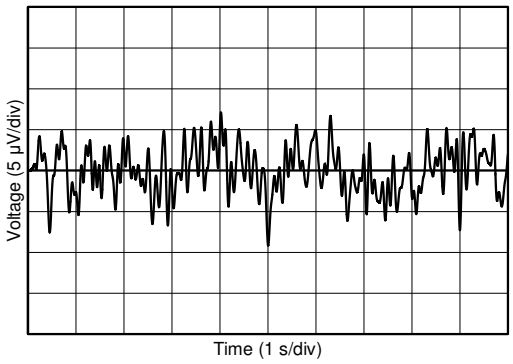


Figure 7-31. Quiescent Current vs Input Voltage



V_{REF} output

Figure 7-32. 0.1-Hz to 10-Hz Noise (V_{REF})



V_{BIAS} output

Figure 7-33. 0.1-Hz to 10-Hz Noise (V_{BIAS})

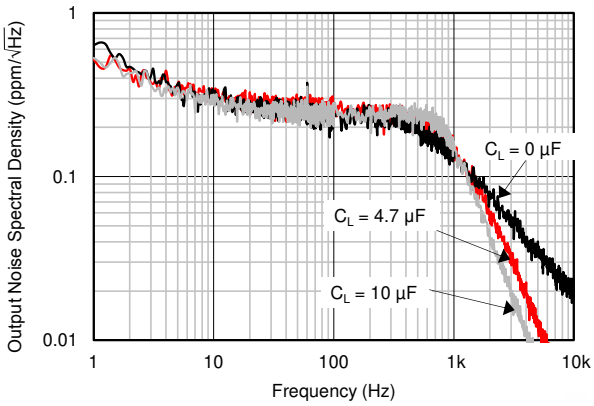
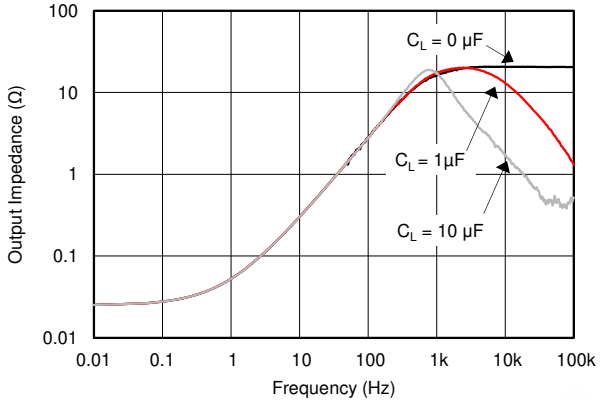
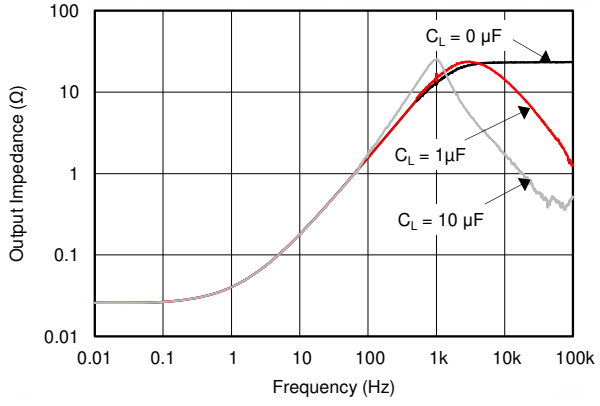


Figure 7-34. Output Voltage Noise Spectrum



V_{REF} output

Figure 7-35. Output Impedance vs Frequency (V_{REF})



V_{BIAS} output

Figure 7-36. Output Impedance vs Frequency (V_{BIAS})

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7.6 Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5 V power supply, C_L = 0 µF, and 2.5 V output, unless otherwise noted.

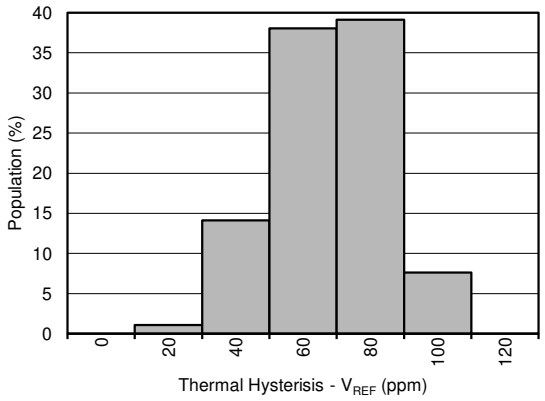

Figure 7-37. Thermal Hysteresis Distribution (V_{REF})

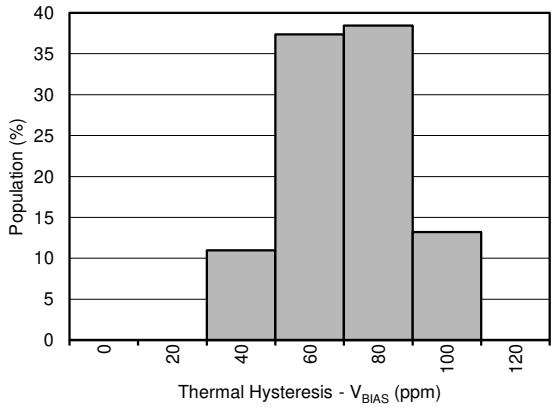

Figure 7-38. Thermal Hysteresis Distribution (V_{BIAS})

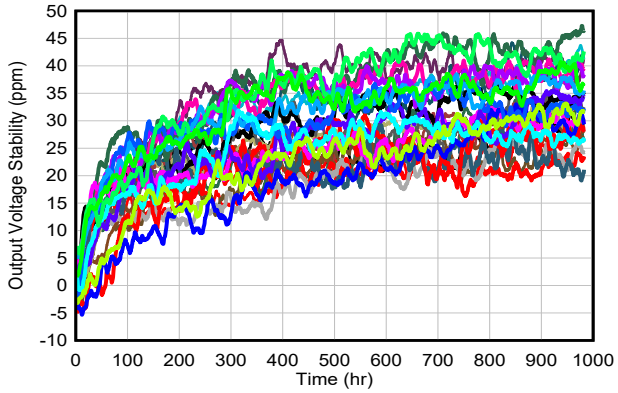

Figure 7-39. Long-Term Stability (First 1000 Hours)

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8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF20xx-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 8-1. The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 8-2 and Figure 8-3. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

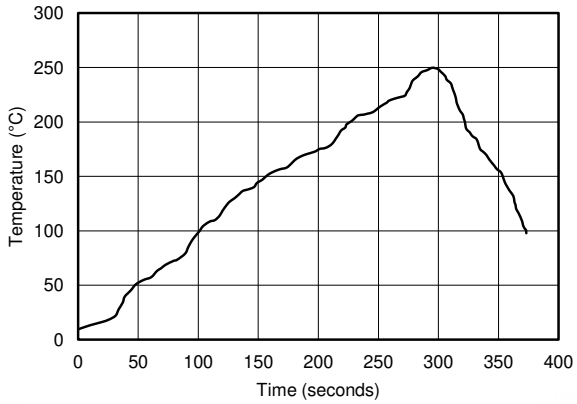

Figure 8-1. Reflow Profile

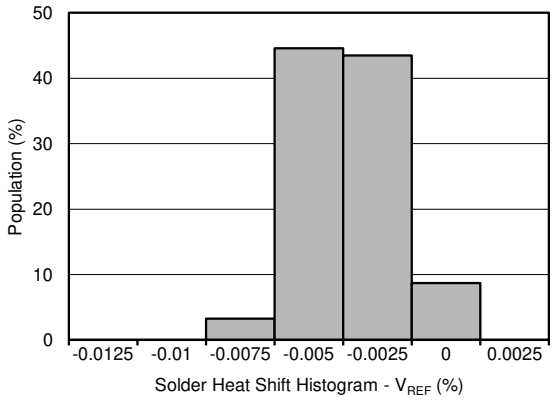

Figure 8-2. Solder Heat Shift Distribution, V_{REF} (%)

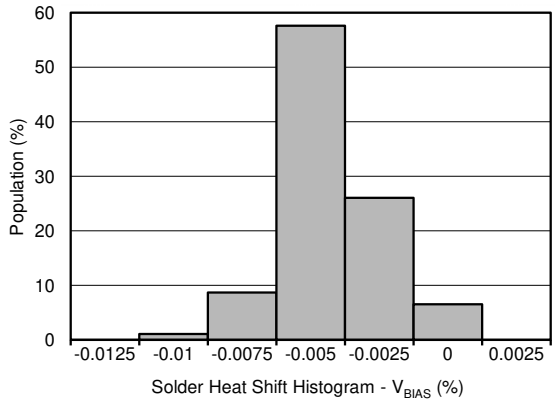

Figure 8-3. Solder Heat Shift Distribution, V_{BIAS} (%)

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8.2 Long-Term Stability

The long term stability of the REF20xx-Q1 was collected on 32 parts that were soldered onto Printed Circuit Boards without any slots or special layout considerations. The boards were then placed into an oven with air temperature maintained at T_A = 35°C. The Vref output of the 32 parts was measured regularly. Typical long term stability is as shown in Figure 8-4.

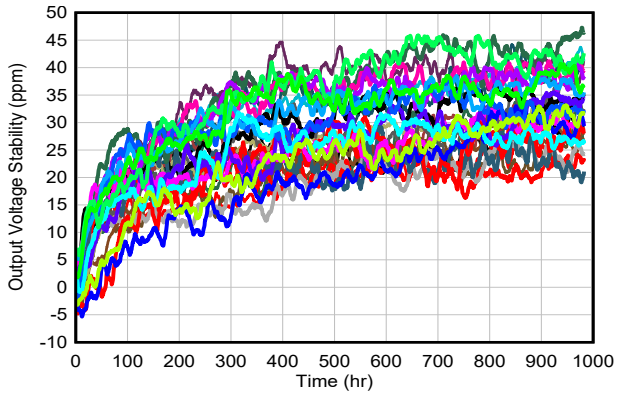

Figure 8-4. Long Term Stability – 1000 hours (V_{REF})

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8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF20xx-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{\left| V_{PRE} - V_{POST} \right|}{V_{NOM}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{1}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C

Typical thermal hysteresis distribution is as shown in Figure 8-5 and Figure 8-6.

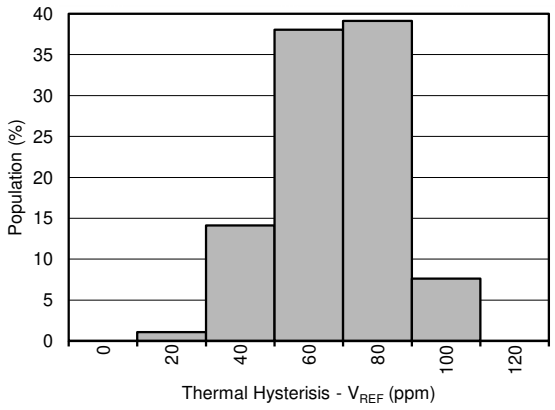

Figure 8-5. Thermal Hysteresis Distribution (V_{REF})

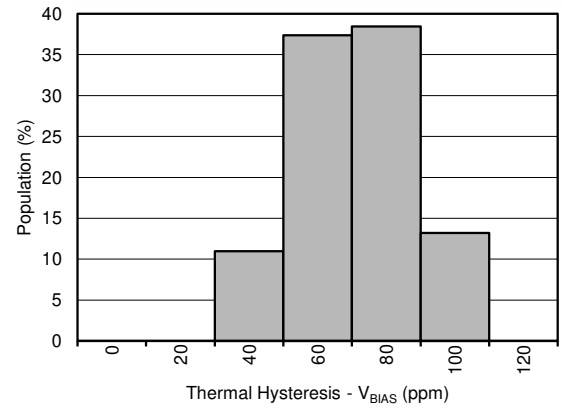

Figure 8-6. Thermal Hysteresis Distribution (V_{BIAS})

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8.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 8-7 and Figure 8-8. Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 8-9.

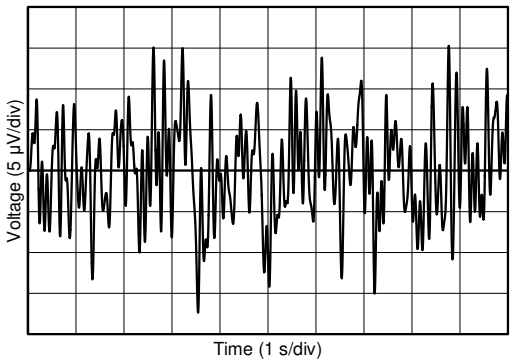


Figure 8-7. 0.1-Hz to 10-Hz Noise (V_{REF})

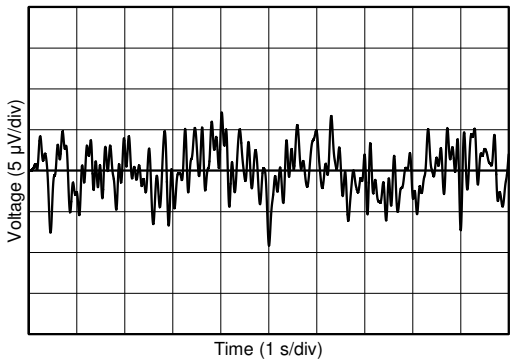


Figure 8-8. 0.1-Hz to 10-Hz Noise (V_{BIAS})

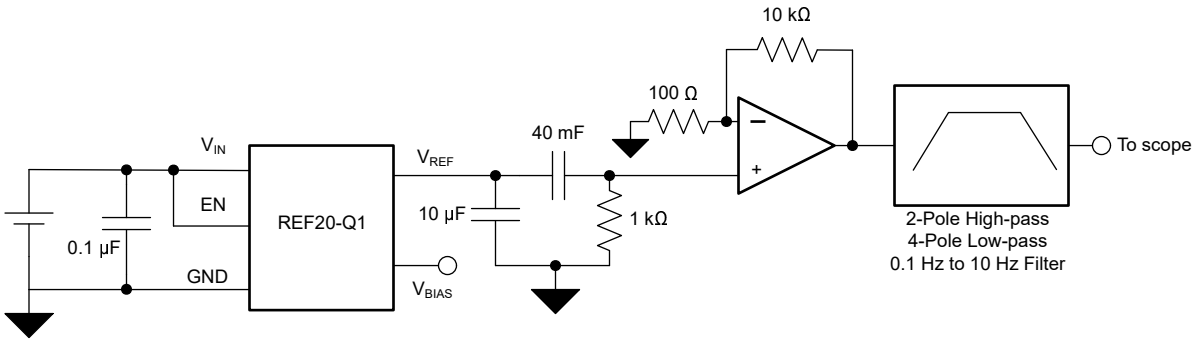


Figure 8-9. 0.1-Hz to 10-Hz Noise Measurement Setup

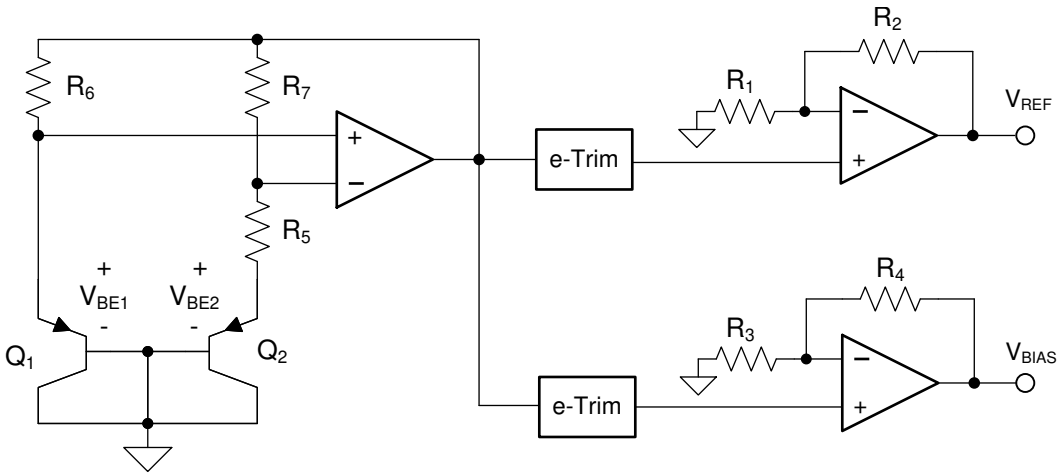
9 Detailed Description

9.1 Overview

The REF20xx-Q1 are a family of dual-output, V_{REF} and V_{BIAS} (V_{REF} / 2) band-gap voltage references. The *Section 9.1* section provides a block diagram of the basic band-gap topology and the two buffers used to derive the V_{REF} and V_{BIAS} outputs. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base emitter voltages (V_{BE1} – V_{BE2}) has a positive temperature coefficient and is forced across resistor R_5. The voltage is amplified and added to the base emitter voltage of Q_2, which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate V_{REF} and V_{BIAS} from the band-gap voltage. The resistors R_1, R_2 and R_3, R_4 are sized such that V_{BIAS} = V_{REF} / 2.

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of V_{REF} and V_{BIAS}, implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx-Q1 to minimize the temperature drift and maximize the initial accuracy of both the V_{REF} and V_{BIAS} outputs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 V_{REF} and V_{BIAS} Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The V_{REF} and V_{BIAS} outputs of the REF20xx-Q1 are generated from the same band-gap voltage as shown in the *Section 9.2*. Hence, both outputs track each other over the full temperature range of –40°C to 125°C with an accuracy of 7 ppm/°C (maximum). The tracking error is calculated using the box method, as described by Equation 2:

$$\text{Tracking Error} = \left(\frac{V_{DIFF(MAX)} - V_{DIFF\ (MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{2}$$

where

- $V_{DIFF} = V_{REF} - 2 \bullet V_{BIAS}$

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The tracking accuracy is as shown in Figure 9-1.

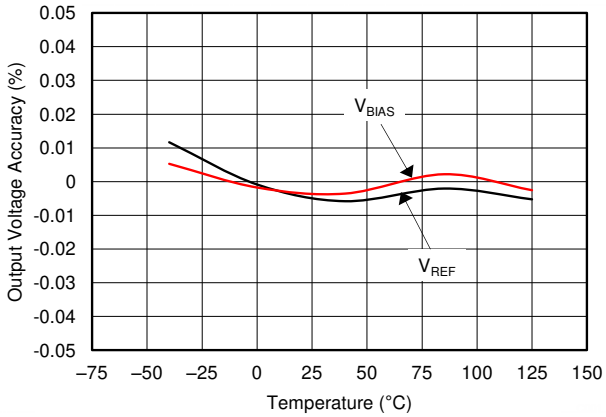

Figure 9-1. V_{REF} and V_{BIAS} Tracking vs Temperature

9.3.2 Low Temperature Drift

The REF20xx-Q1 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{3}$$

9.3.3 Load Current

The REF20xx-Q1 family is specified to deliver a current load of ±20 mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \bullet R_{\theta JA} \tag{4}$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- P_D = power dissipated (W)
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF20xx-Q1 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

When the EN pin of the REF20xx-Q1 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF20xx-Q1 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5 µA in shutdown mode. See the *Section 7.5* for logic high and logic low voltage levels.

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10 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from –2.5 A to 2.5 A. The linear range of the output is from 250 mV to 2.75 V. Positive current is represented by output voltages from 1.5 V to 2.75 V, whereas negative current is represented by output voltages from 250 mV to 1.5 V. The difference amplifier is the INA240-Q1 current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030-Q1.

10.2 Typical Application

10.2.1 Low-Side, Current-Sensing Application

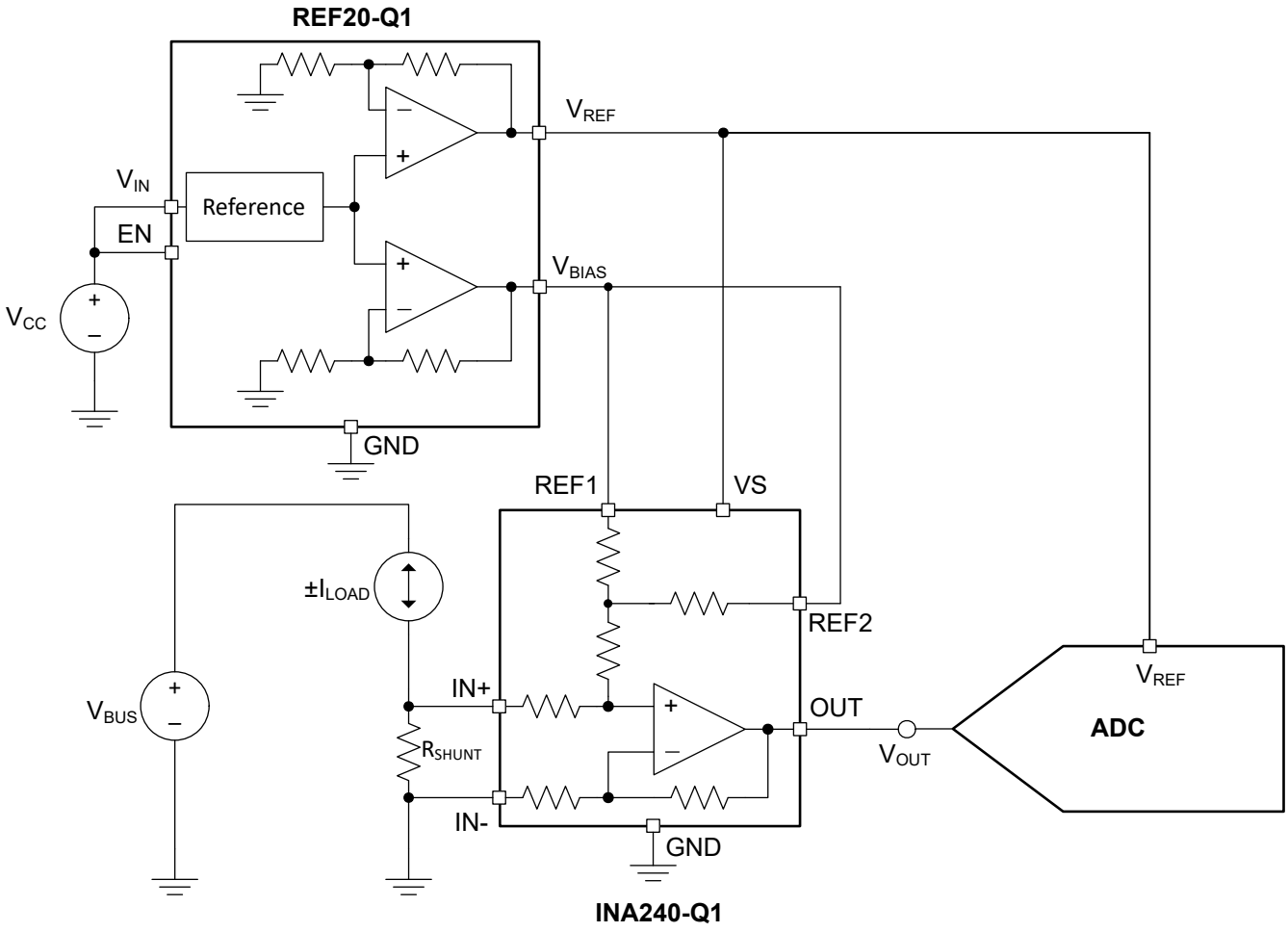

Figure 10-1. Low-Side, Current-Sensing Application

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10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current: ±2.5 A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage: ±25 mV

10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (V+) and the reference voltage (V_{REF}, or V_{BIAS}) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 10-2 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see Figure 10-1. Not only do V_{REF} and V_{BIAS} track over temperature, but their matching is much better than alternate topologies.

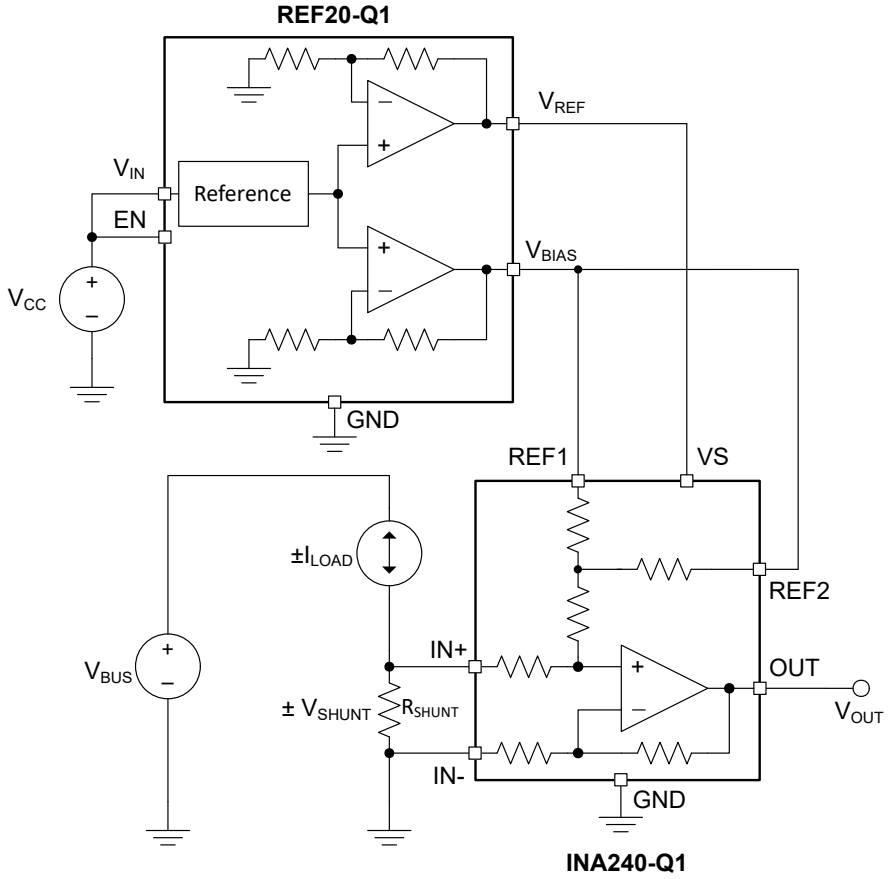

Figure 10-2. Low-Drift, Low-Side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in Figure 10-2 is as shown in Equation 5:

$$V_{OUT} = G \bullet (\pm V_{SHUNT}) + V_{BIAS}$$
$$= G \bullet (\pm I_{LOAD} \bullet R_{SHUNT}) + V_{BIAS} \quad (5)$$

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10.2.1.2.1 Shunt Resistor

As illustrated in Figure 10-2, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of V_{SHUNT} that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. Equation 6 can be used to calculate the maximum value of R_{SHUNT}.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \tag{6}$$

Given that the maximum shunt voltage is ±25 mV and the load current range is ±2.5 A, the maximum shunt resistance is calculated as shown in Equation 7.

$$R_{SHUNT\,(max)} = \frac{V_{SHUNT\,(max)}}{I_{LOAD\,(max)}} = \frac{25mV}{2.5A} = 10m\Omega \tag{7}$$

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design must have the following features:

1. Single-supply (3 V)
2. Reference voltage input
3. Low initial input offset voltage (V_{OS})
4. Low-drift
5. Fixed gain
6. Low-side sensing (input common-mode range below ground)

For this design, a current-shunt monitor (INA240-Q1) is used. The INA240-Q1 family topology is shown in Figure 10-3. The INA240-Q1 specifications can be found in the INA240-Q1 product data sheet.

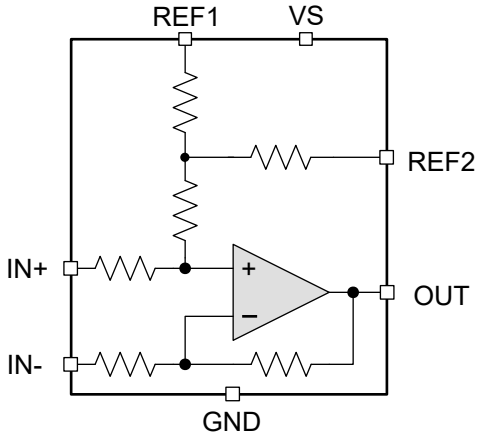

Figure 10-3. INA240-Q1 Current-Shunt Monitor Topology

The INA240-Q1 is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

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10.2.1.2.3 Voltage Reference

The voltage reference for this application must have the following features:

1. Dual output (3.0 V and 1.5 V)
2. Low drift
3. Low tracking errors between the two outputs

For this design, the REF2030-Q1 is used. The REF20xx-Q1 topology is as shown in the *Section 9.2* section.

The REF2030-Q1 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in Figure 10-4 and Figure 10-5.

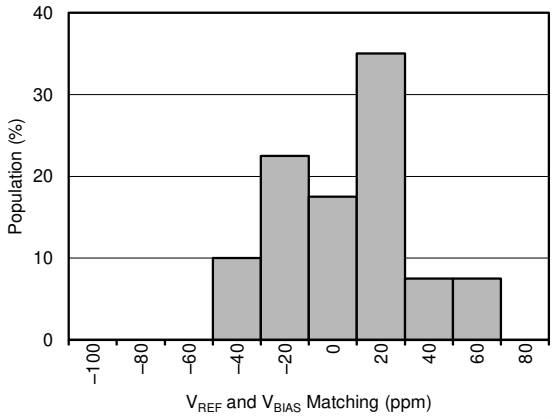

Figure 10-4. V_{REF} – 2 × V_{BIAS} Distribution (At T_A = 25°C)

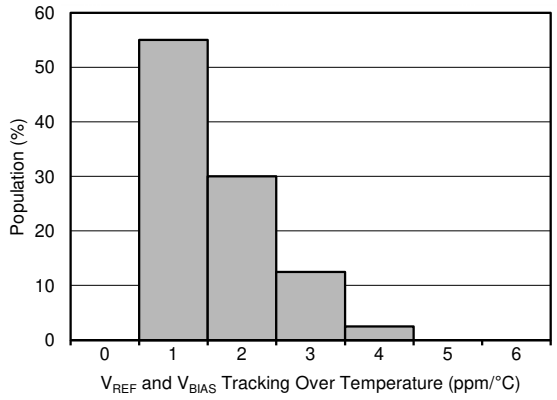

Figure 10-5. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

10.2.1.2.4 Error Calculations

Two types of errors will be discussed: initial accuracy and drift. Accuracy errors include:

- Shunt resistor tolerance: α_{shunt_tol} = 0.1% (maximum)
- INA initial input offset voltage: V_{OS_INA} = 5 µV (typical)
- INA PSRR: $V_{OS_INA_PSRR}$ = 1 µV/V (typical)
- INA CMRR: $V_{OS_INA_CMRR}$ = 132 dB (typical)
- INA gain error: α_{INA_GE} = 0.05% (typical)
- Reference output accuracy: α_{REF_output} = 0.05% (maximum)

It should be noted that these error sources can be greatly reduced at 25ºC by performing a two point system calibration. Drift errors, on the other hand, can only be reduced by performing the calibration over temperature. The drift errors include:

- Shunt resistor drift: δ_{shunt_drift} = 15 ppm/ºC (maximum)
- INA offset voltage drift: $\delta_{INA_drift_Vos}$ = 50 nV/ºC (typical)
- INA gain error drift: $\delta_{INA_drift_GE}$ = 0.5 ppm/ºC (typical)
- Reference output drift: $\delta_{REF_drift_output}$ = 3 ppm/ºC (typical)

Equation 8 can be used to convert specifications given in parts per million (ppm) to a percentage (%), and vice versa.

$$\% = (ppm/10{,}000) \tag{8}$$

Equation 9 can be used to convert specifications given in decibels (dB) to a linear representation.

$$(V / V) = (1 / 10^{(dB/20)}) \tag{9}$$

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For some error calculations a full-scale range (FSR) is required. The FSR for this design is determined by the voltage across the shunt resistor, which is ±25 mV (or 50 mV).

For drift errors, the largest change in temperature (ΔT) is 100ºC, which is the difference between the maximum specified temperature (125ºC) and room temperature (25ºC). This temperature change is used when calculating drift errors for the shunt resistor and INA240-Q1. Because the REF20-Q1 uses the box method to determine drift, the temperature range used for calculations is the entire operating range, or 150ºC.

Finally, errors due to CMRR and PSRR specifications require an adjustment depending on the difference between the system's requirements and how the devices were characterized. For example, the INA240-Q1 was characterized using a common-mode voltage of 12 V. The common-mode voltage in this design is ~0V. This discrepancy causes an input-referred offset voltage.

Below, Table 10-1 summarizes the initial accuracy calculations.

Table 10-1. Initial Accuracy Error Summary

ERROR SOURCE	DEVICE: R_{SHUNT} (PPM)	DEVICE: IN240-Q1 (PPM)	DEVICE: REF2030-Q1 (PPM)	TOTAL (PPM, RSS)
OFFSET		100 FSR	500 FSR	510 FSR
CMRR		60 FSR		60 FSR
PSRR		40 FSR		40 FSR
GAIN ERROR	1000	500		1118
TOTAL (PPM, RSS)	1000	1087.5 FSR	500 FSR	1231 FSR (0.123%)

Below, Table 10-2 summarizes the total temperature drift calculations.

Table 10-2. Temperature Drift Error Summary

ERROR SOURCE	DEVICE: R_{SHUNT} (PPM)	DEVICE: IN240-Q1 (PPM)	DEVICE: REF2030-Q1 (PPM)	TOTAL (PPM, RSS)
OFFSET DRIFT		100 FSR	495	505 FSR
GAIN ERROR DRIFT	1500	50		1501
TOTAL (PPM, RSS)	1500	111.8 FSR	495	1583.52 FSR (0.194%)

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10.2.1.2.5 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. Figure 10-6 to Figure 10-8 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to TIDU357.

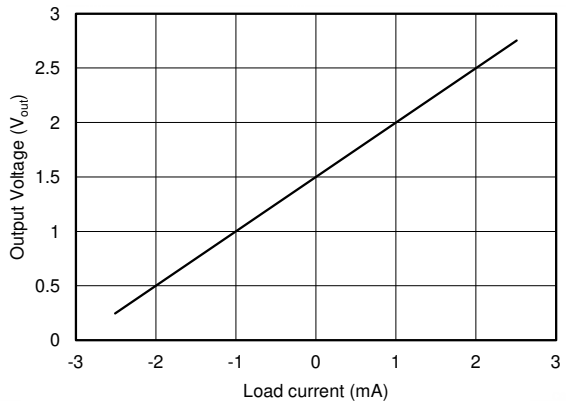

Figure 10-6. Measured Transfer Function

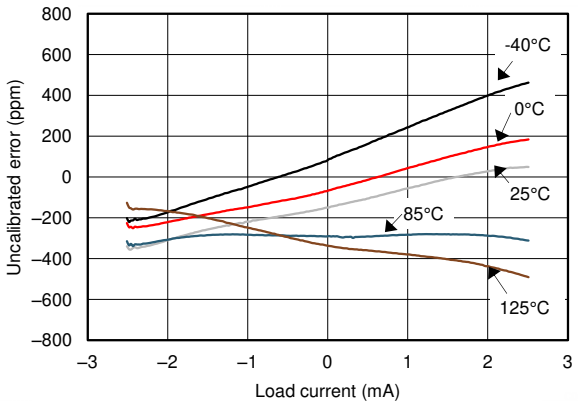

Figure 10-7. Uncalibrated Error vs Load Current

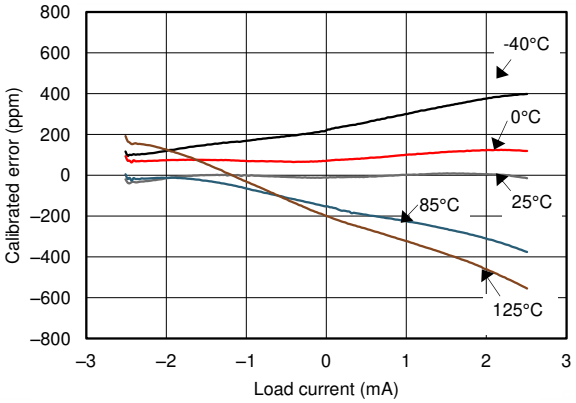

Figure 10-8. Calibrated Error vs Load Current

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11 Power-Supply Recommendations

The REF20xx-Q1 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in Figure 11-1. A supply bypass capacitor ranging between 0.1 µF to 10 µF is recommended.

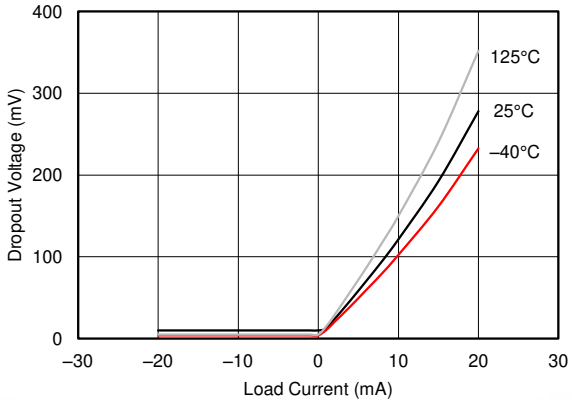

Figure 11-1. Dropout Voltage vs Load Current

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12 Layout

12.1 Layout Guidelines

Figure 12-1 shows an example of a PCB layout for a data acquisition system using the REF2030-Q1. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF}, and V_{BIAS} of the REF2030-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

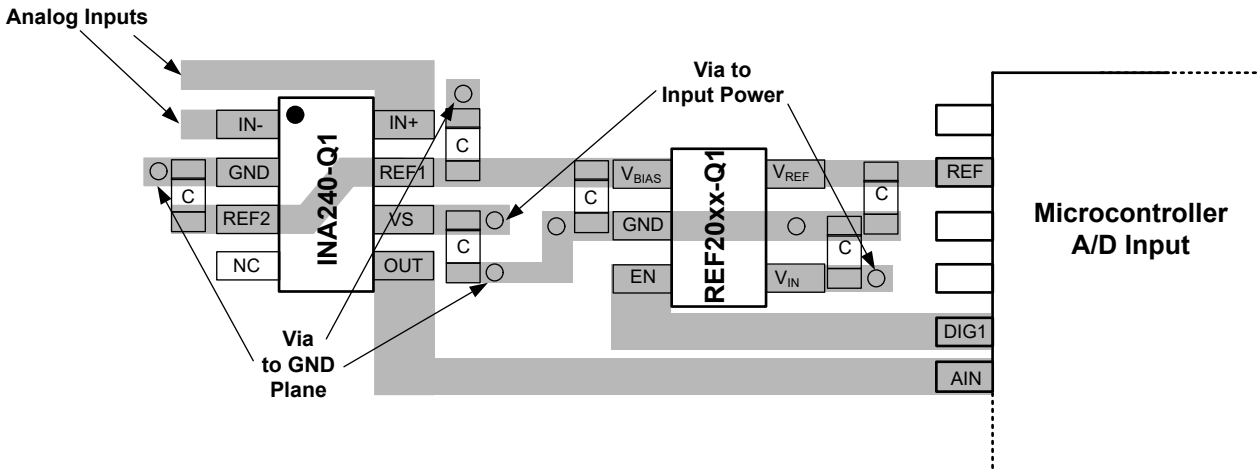

Figure 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA240-Q1 Automotive, Wide Common-Mode Range, High- and Low-Side, Bidirectional, Zero-Drift, Current-Sense Amplifier With Enhanced PWM Rejection* (SBOS808)
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design* (TIDU357)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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TI E2E™ is a trademark of Texas Instruments.
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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2025QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACQ	Samples
REF2030QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADQ	Samples
REF2033QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEQ	Samples
REF2041QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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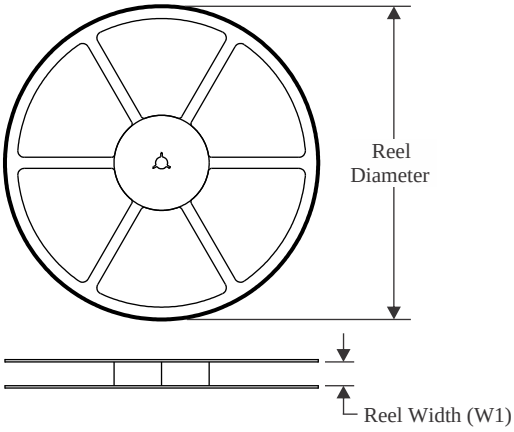
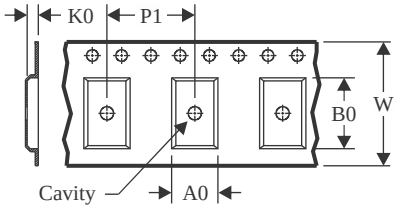
TAPE AND REEL INFORMATION

REEL DIMENSIONS

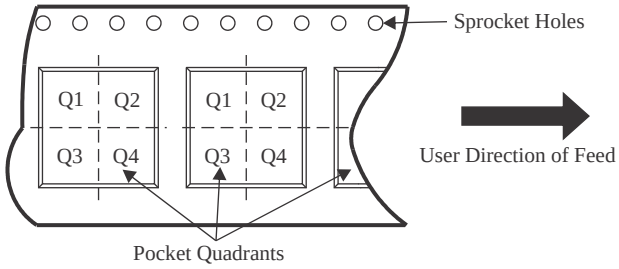


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

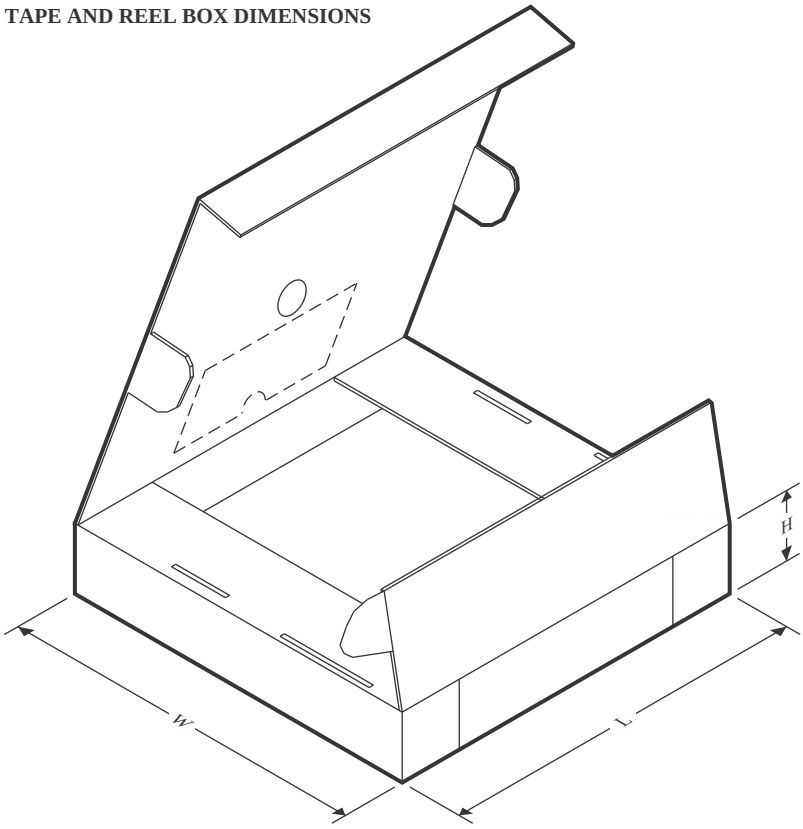
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

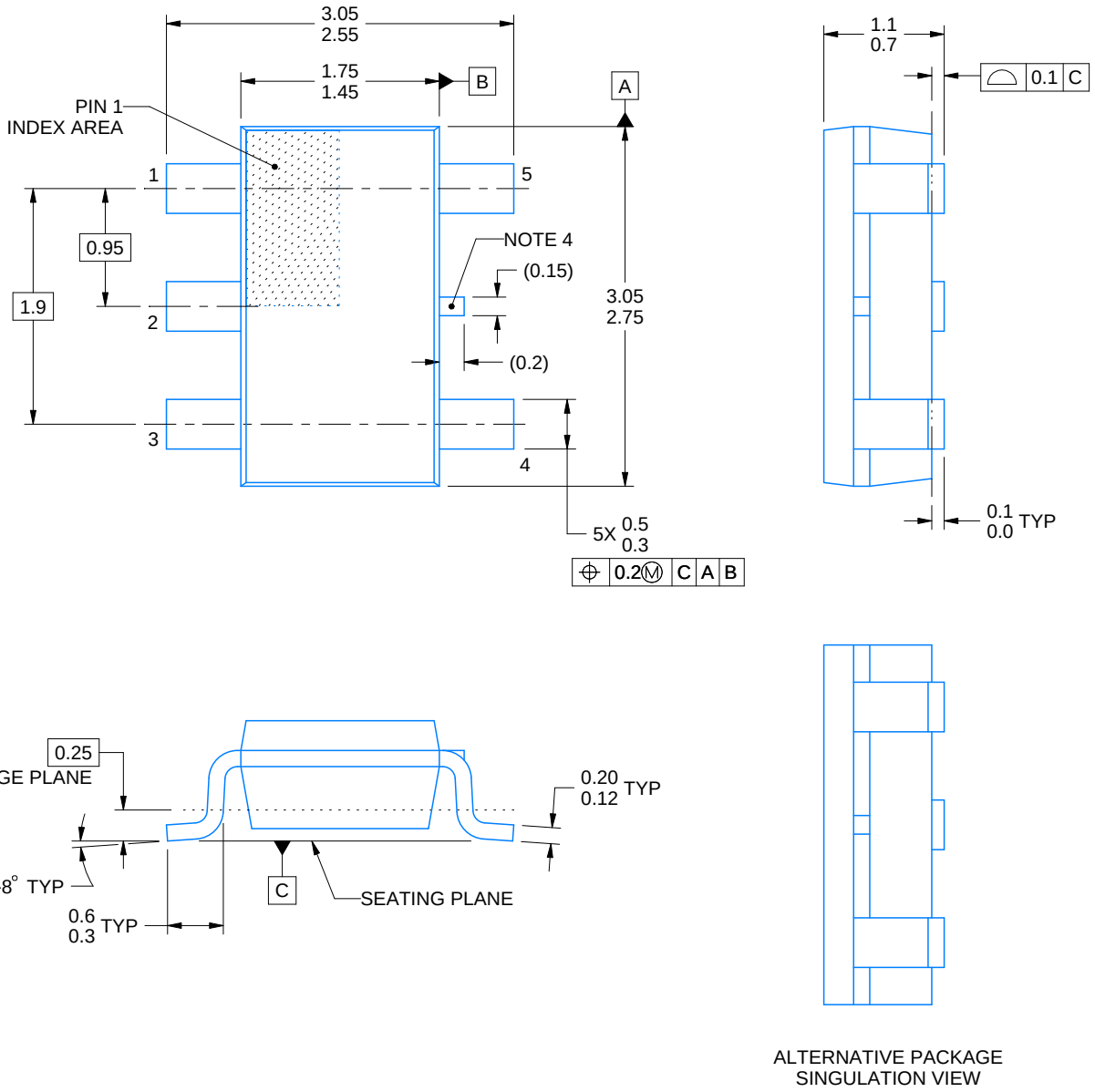
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2033QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2041QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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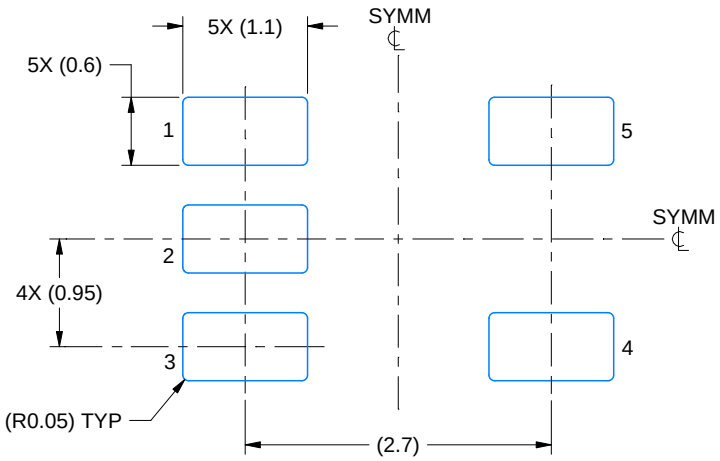
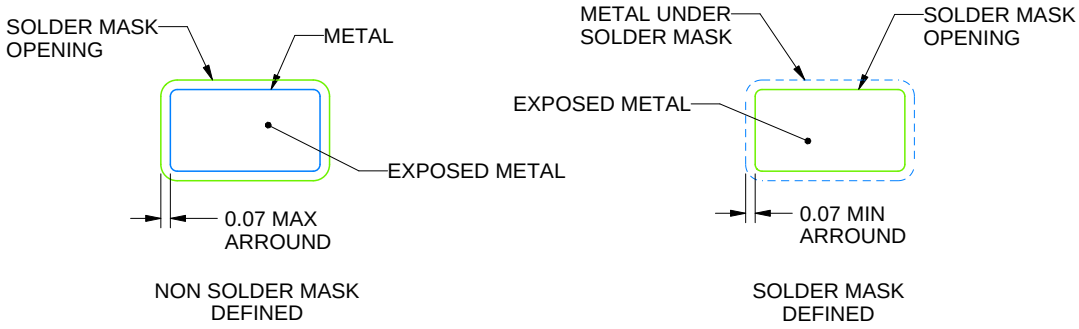
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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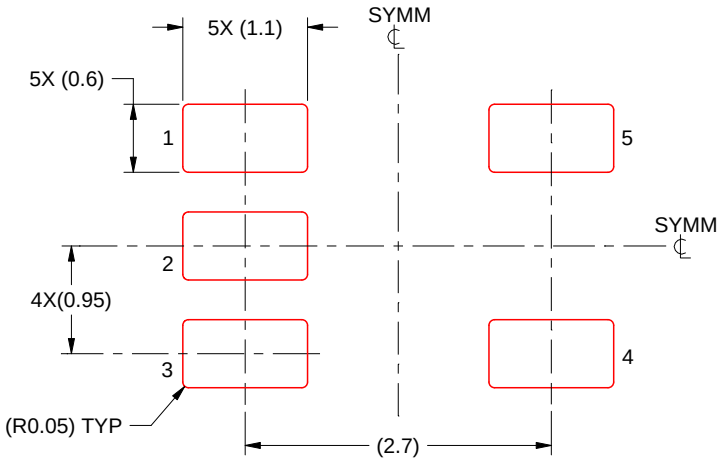
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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