



THE DATASHEET OF 74HC164BQ-Q100X





74HC164-Q100; 74HCT164-Q100

8-bit serial-in, parallel-out shift register

Rev. 3 — 28 May 2024

Product data sheet

1. General description

The 74HC164-Q100; 74HCT164-Q100 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (\overline{MR}) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

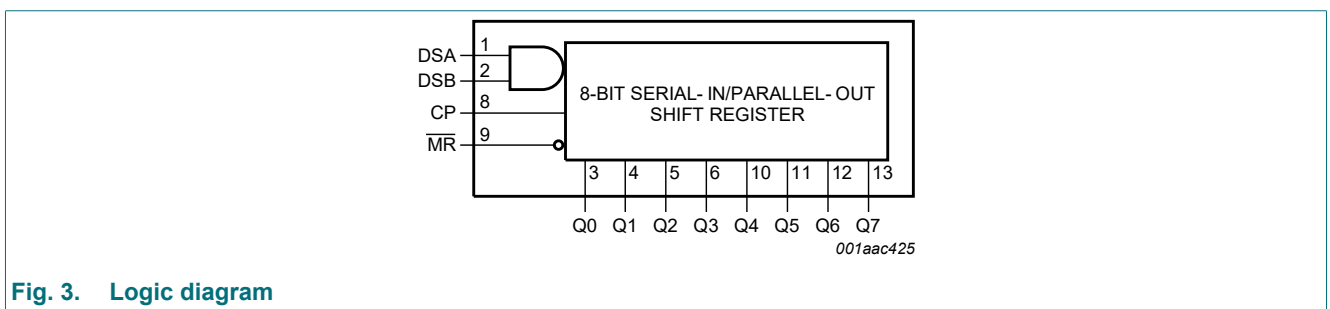
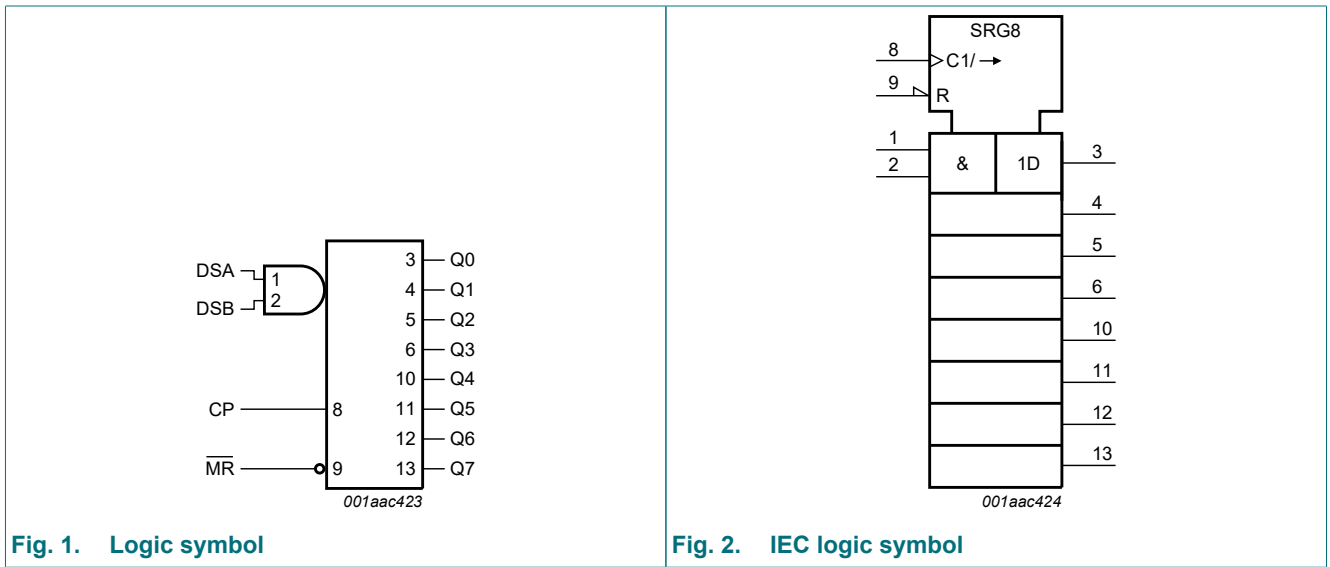
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC164-Q100: CMOS level
 - For 74HCT164-Q100: TTL level
- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC164D-Q100 74HCT164D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC164PW-Q100 74HCT164PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC164BQ-Q100 74HCT164BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram



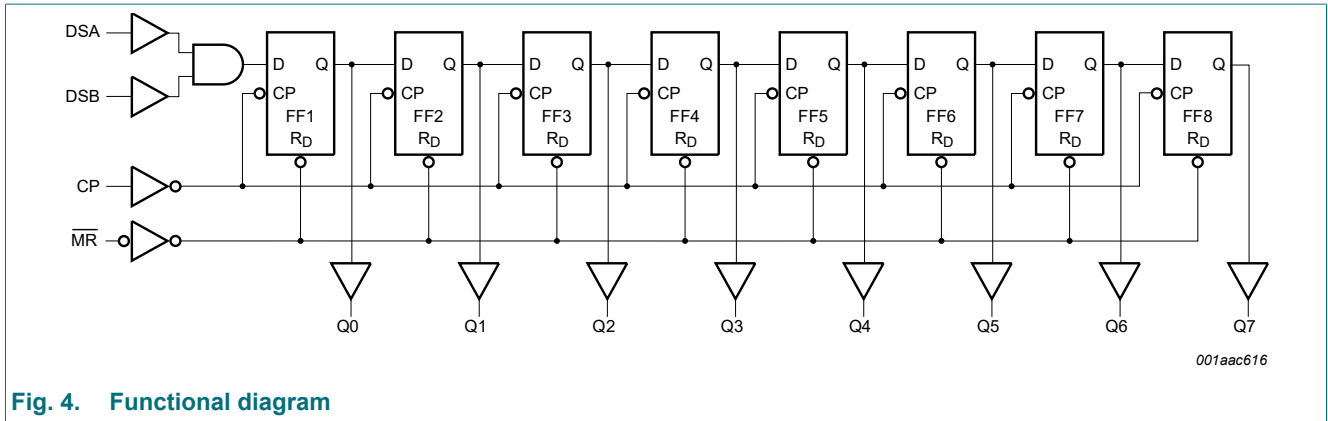
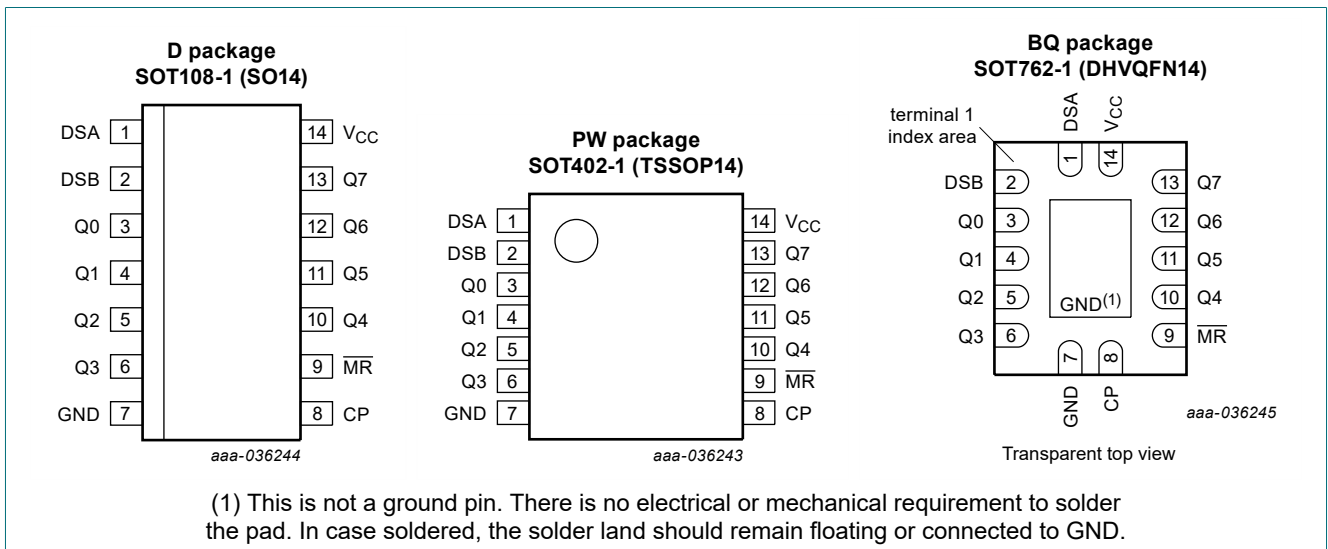


Fig. 4. Functional diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	3, 4, 5, 6, 10, 11, 12, 13	output
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
MR	9	master reset input (active LOW)
V _{CC}	14	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition; X = don't care

Operating modes	Input				Output	
	MR	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	L	q0 to q6
	H	↑	h	h	H	q0 to q6

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC164-Q100			74HCT164-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC164-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT164-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; test circuit see Fig. 8; unless otherwise specified

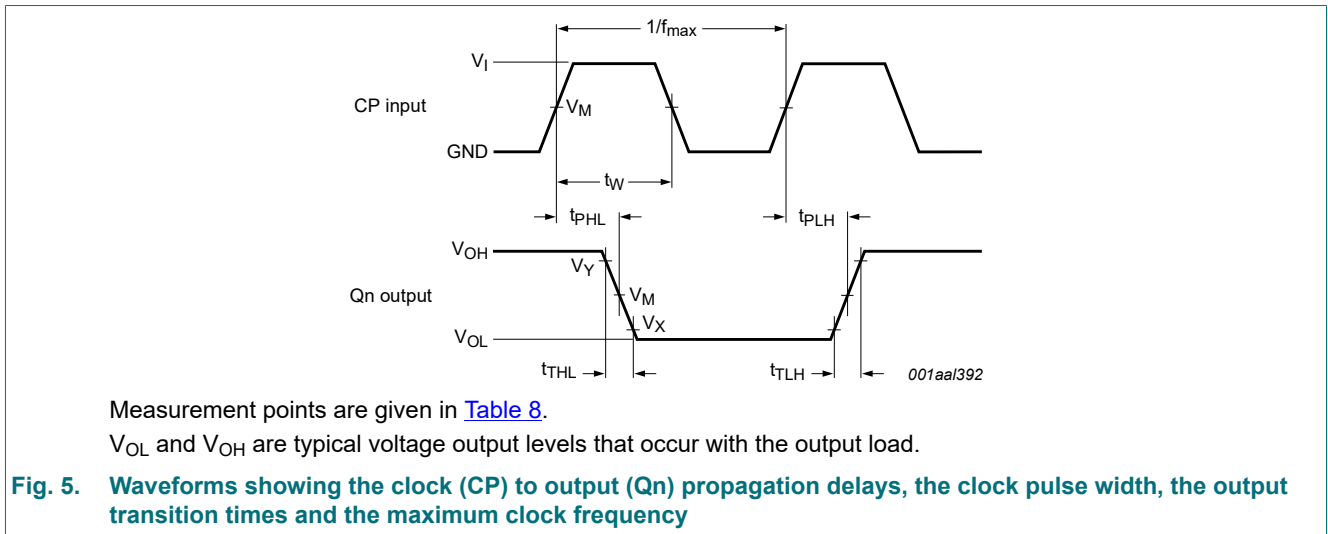
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC164-Q100										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	41	170	-	215	-	255	ns
		V _{CC} = 4.5 V	-	15	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	29	-	37	-	43	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V _{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V _{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t _t	transition time	see Fig. 5 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	CP HIGH or LOW; see Fig. 5								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR LOW; see Fig. 6								
		V _{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	5	-	13	-	15	-	ns

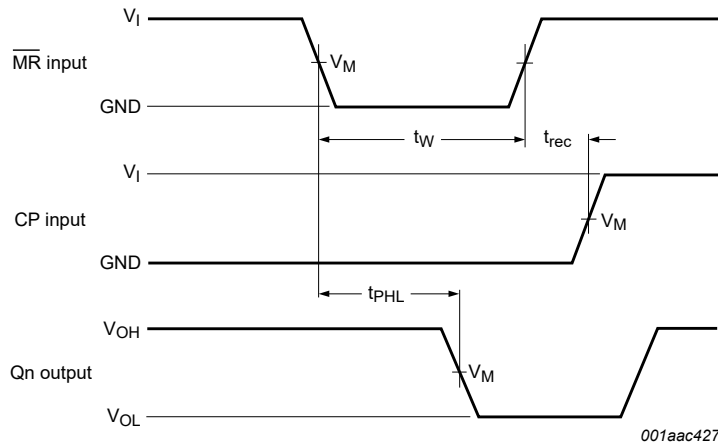
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{rec}	recovery time	MR to CP; see Fig. 6								
		V _{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t _{su}	set-up time	DSA, and DSB to CP; see Fig. 7								
		V _{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	2	-	13	-	15	-	ns
t _h	hold time	DSA, and DSB to CP; see Fig. 7								
		V _{CC} = 2.0 V	+4	-6	-	4	-	4	-	ns
		V _{CC} = 4.5 V	+4	-2	-	4	-	4	-	ns
		V _{CC} = 6.0 V	+4	-2	-	4	-	4	-	ns
f _{max}	maximum frequency	for Cp, see Fig. 5								
		V _{CC} = 2.0 V	6	23	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	71	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	78	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	85	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	40	-	-	-	-	-	pF
74HCT164-Q100										
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	17	36	-	45	-	54	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V _{CC} = 4.5 V	-	19	38	-	48	-	57	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
t _t	transition time	see Fig. 5 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _w	pulse width	CP HIGH or LOW; see Fig. 5								
		V _{CC} = 4.5 V	18	7	-	23	-	27	-	ns
		MR LOW; see Fig. 6								
t _{rec}	recovery time	V _{CC} = 4.5 V	18	10	-	23	-	27	-	ns
		MR to CP; see Fig. 6								
t _{su}	set-up time	V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		DSA, and DSB to CP; see Fig. 7								
t _h	hold time	V _{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		DSA, and DSB to CP; see Fig. 7								
		V _{CC} = 4.5 V	+4	-2	-	4	-	4	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	for C _p , see Fig. 5								
		V _{CC} = 4.5 V	27	55	-	22	-	18	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	61	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V [3]	-	40	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

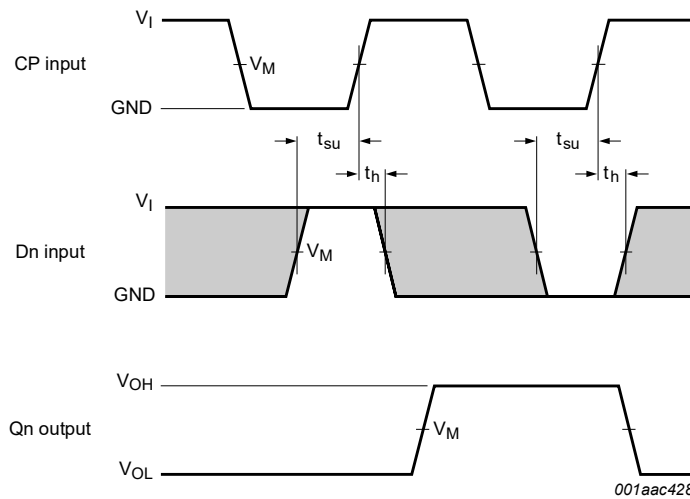




Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time



Measurement points are given in [Table 8](#).

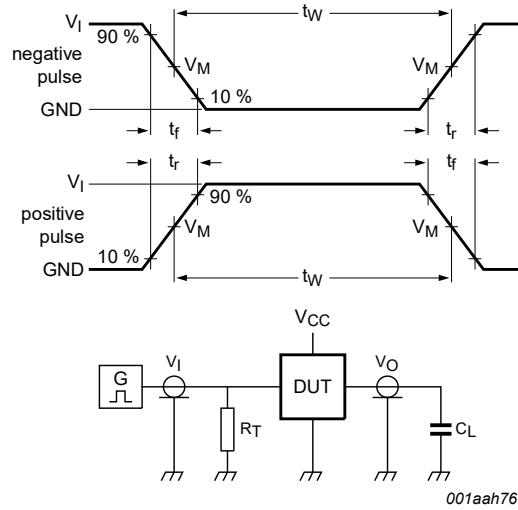
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Waveforms showing the data set-up and hold times for D_n inputs

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC164-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT164-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



001aah768

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = load capacitance including jig and probe capacitance

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC164-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT164-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT164_Q100 v.3	20240528	Product data sheet	-	74HC_HCT164_Q100 v.2
Modifications:	<ul style="list-style-type: none"> Fig. 9, Fig. 10: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT164_Q100 v.2	20200611	Product data sheet	-	74HC_HCT164_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 11: Package outline drawing SOT762-1 (DHVQFN14) updated. 			
74HC_HCT164_Q100 v.1	20130816	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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